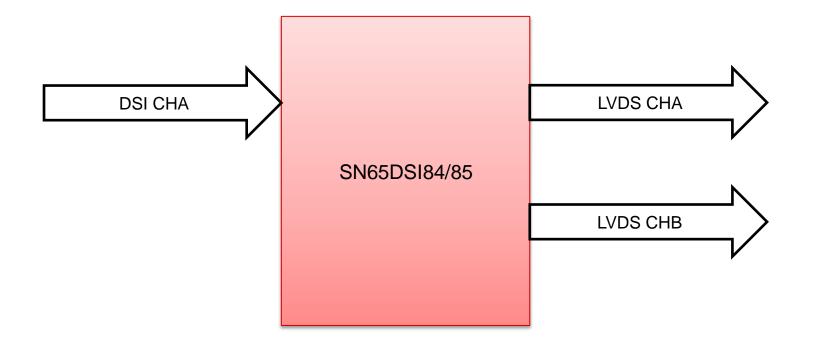
SN65DSI83/84/85- Single DSI Input to **Dual-Link LVDS**

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- Please watch the "Dual DSI Input to Dual-Link LVDS" video before watching this video
- The SN65DSI84 or SN65DSI85 can be used for this demo





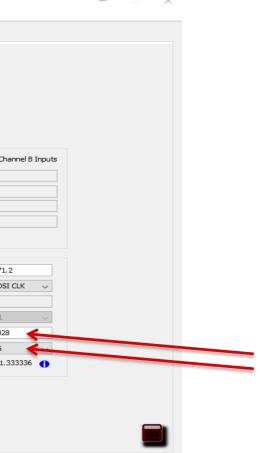
- The same display and settings used for the display in the "Dual DSI Input to Dual-Link LVDS" will be used here
- Change the "DSI Ch Mode" to "Single" in the "DSI_Inputs" window

🐑 DSI83/84/85/86 Tuner - SN65DSI85 📰 🗱 🔟 🕜	-	ED DSI83/84/85/86 Tuner - SN65DSI85 —
Panel Inputs DSI_Inputs Outputs		Panel Inputs DSI_Inputs Outputs
Panel Info Channel A Panel Vendor Panel Model Resolution 1920 pixels x 1080 lines LVDS Mode Dual Test Pattern	TEXAS INSTRUMENTS	DSI Info DSI Channel A DSI Channel A DSI Channel A DSI Channel B Panel Resolution 1920x1080 LP All All DSI Ch Mode Single V Burst Mode Burst V Left right or even odd LR CROP Enable OE Sync Mode Event Event
Pixels LVDS Channel A LVDS Channel B LVDS_HPW 30 30 LVDS_HBP 30 30 LVDS_HFP 30 30 LVDS_HFP 30 30 LVDS_HActive 960 960 Htotal 1050 1050 Additional Panel Info Channel A Channel B FORMAT Format 2 Format 2 Data Enable Polarity Positive Horizontal Sync Polarity Negative Vertical Sync Polarity Negative Bits Per Pixel 24bpp 24bpp		Pixels DSI Channel A Inputs DSI Channel B Inputs DSI_HPW 30



 Double all of the horizontal parameters (HPW, HBP, HFP, HActive) and the DSI CLK frequency from what they were before in the "Dual DSI Input to Dual-Link" LVDS"

Panel Info		Panel Inputs DSI_Inputs Outputs	
Channel A		DSI Info DSI Channel A DSI Channel A DSI Channel A	DSI Channel B
Panel Vendor	TEXAS INSTRUMENTS	Panel Resolution 1920x1080 LP All	V All V
Panel Model		DSI Ch Mode Single V Burst Mode Burst	🗸 Burst 🗸
Resolution 1920 pixels x 1080 lines			🗸 Event 🗸
LVDS Mode Dual 🗸		LR CROP Enable	
Test Pattern			
Pixels	Lines	Pixels Lines DSI Channel A Inputs DSI Channel B Inputs	DSI Channel A Inputs DSI Ch
LVDS Channel A LVDS Channel B	LVDS Channel A	DSI_HPW 60 DSI_W	PW 17
LVDS_HPW 30 30	LVDS_VPW 17 17	DSI_HBP 60 DSI_VI	
LVDS_HBP 30 30	LVDS_VBP 17 17	DSI_HFP 60 DSI_VI	
LVDS_HFP 30 30 LVDS_HActive 960 960	LVDS_VFP 16 16 LVDS_VActive 1080 1080	DSI_HActive 1920 DSI_V.	Active 1080
Htotal 1050 1050	Vtotal 1130 1130	DSI_Htotal 2100 0 DSI_V	total 1130 0
Additional Panel Info Additional Panel Info Channel A Channel B FORMAT Format 2 V Data Enable Polarity Positive V Horizontal Sync Polarity Negative V Vertical Sync Polarity Negative V Bits Per Pixel 24bpp V 24bpp V		Additional Channel info DSI Channel A input DSI Channel B Input DSI DDR 428 214 DSI # of lanes 4 ~ 4 ~ DSI Video Mode RGB888 RGB888 LEFT_CROP RIGHT_CROP	CLK LVDS CLK(MHz) - nominal 71 LVDS CLK source DS Ref CLK(MHz) 1 Multiplier(1-4) 1 DSI Ch A CLK 42 Divisor(1-25) 6 LVDS CLK(MHz) - Actual 71

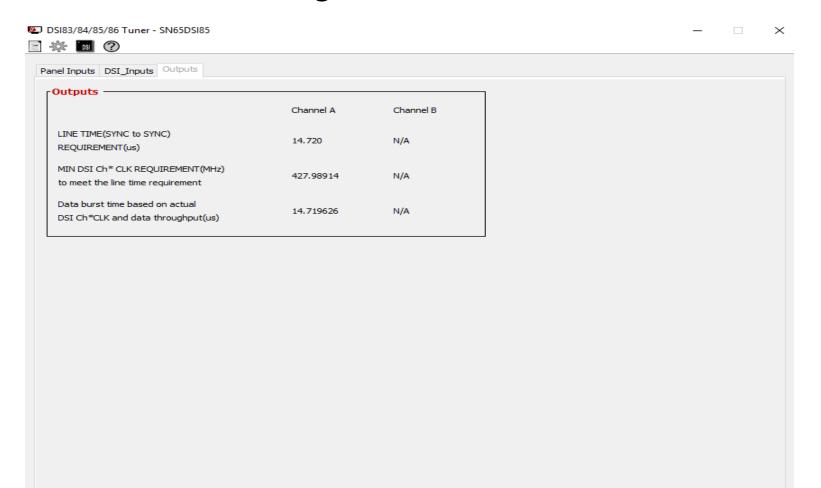




- To calculate the minimum required DSI CLK frequency, use the below equation:
- *Minimum DSICLK frequency* = $\frac{Throughput}{2 \times \# of DSI Lanes} = \frac{LVDS CLK \times bpp}{2 \times \# of DSI Lanes}$
- For this example:
- Minimum DSICLK frequency $= \frac{2 \times 71.2 \text{ MHz} \times 24 \text{ bpp}}{2 \times 4} = \frac{1708.8 \text{ Mbps}}{2 \times 4} = 428 \text{ MHz}$



• Observe the "Outputs" window, and follow the same procedure as in the previous videos to generate the CSR settings







Thanks for your time!



