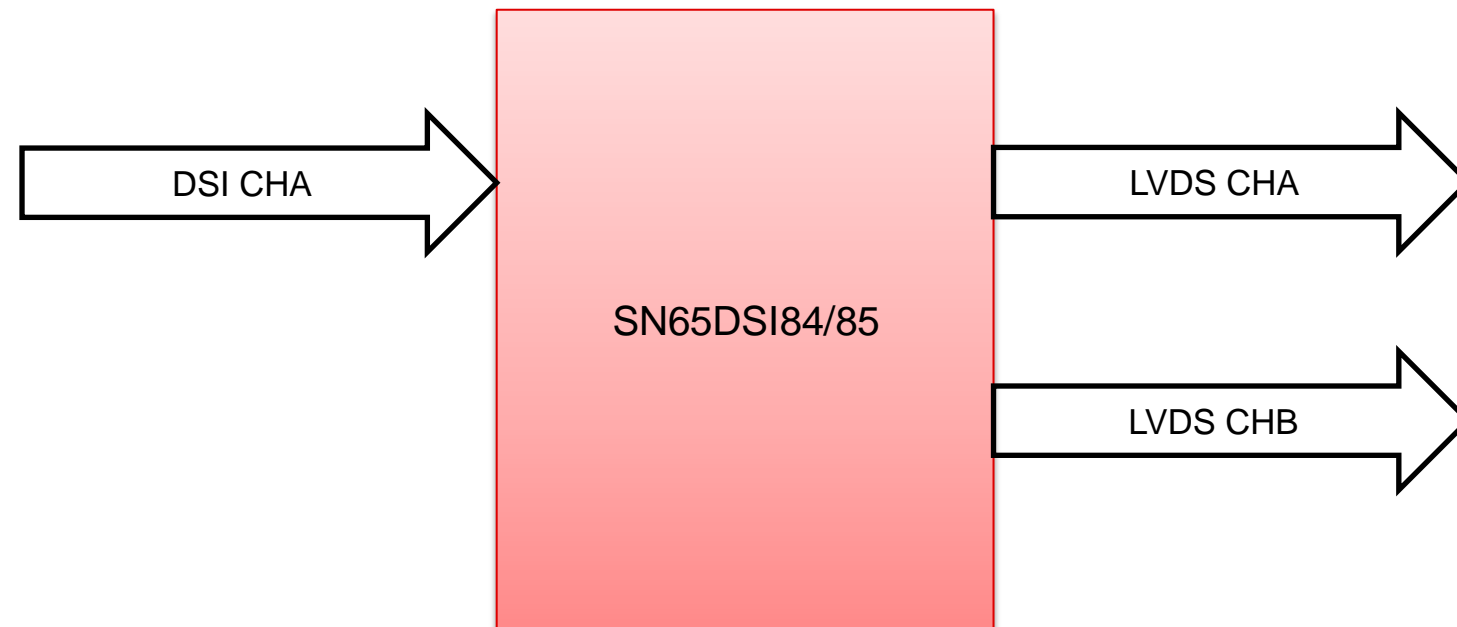


SN65DSI83/84/85- Single DSI Input to Dual-Link LVDS

Ikechukwu (I.K.) Anyiam

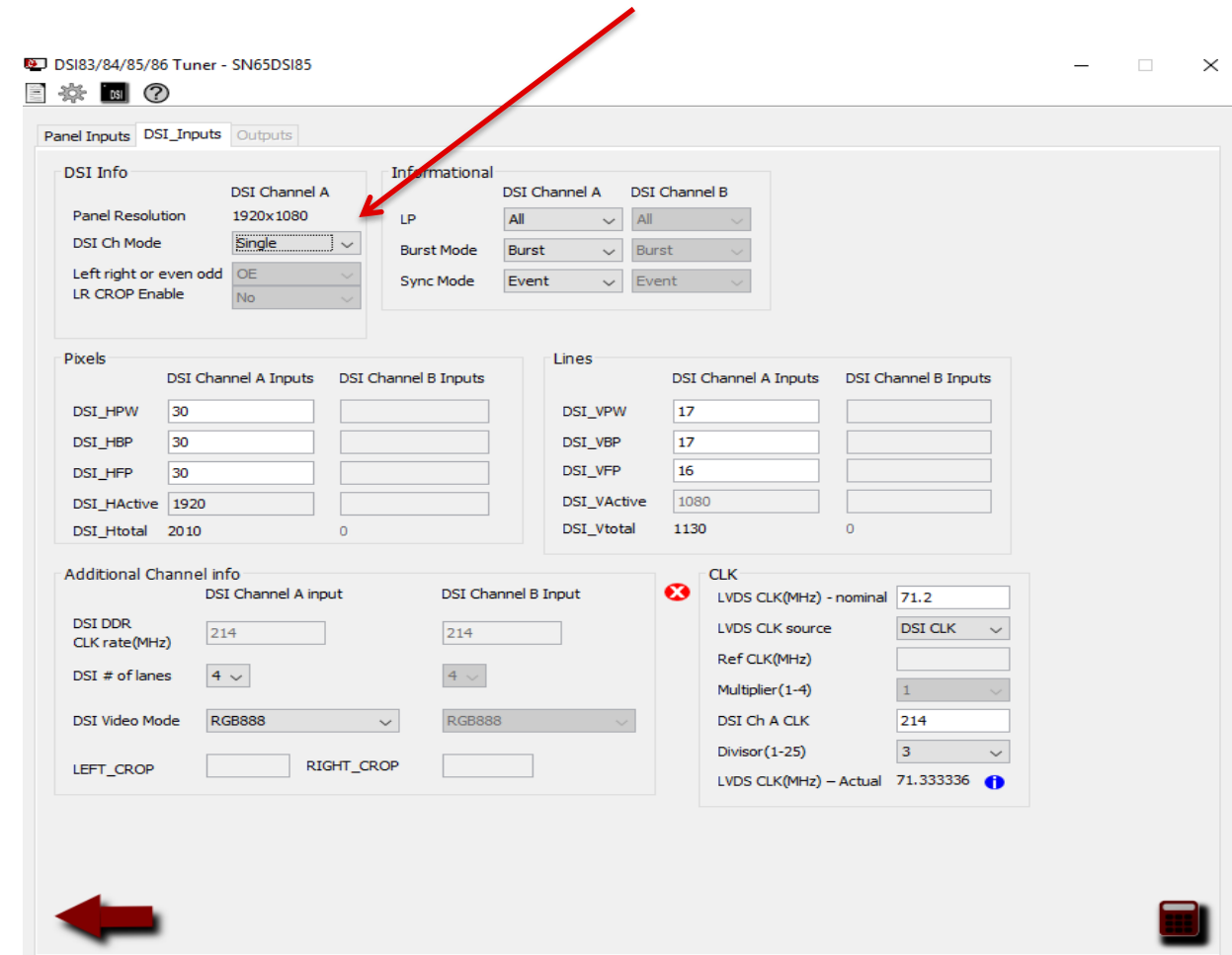
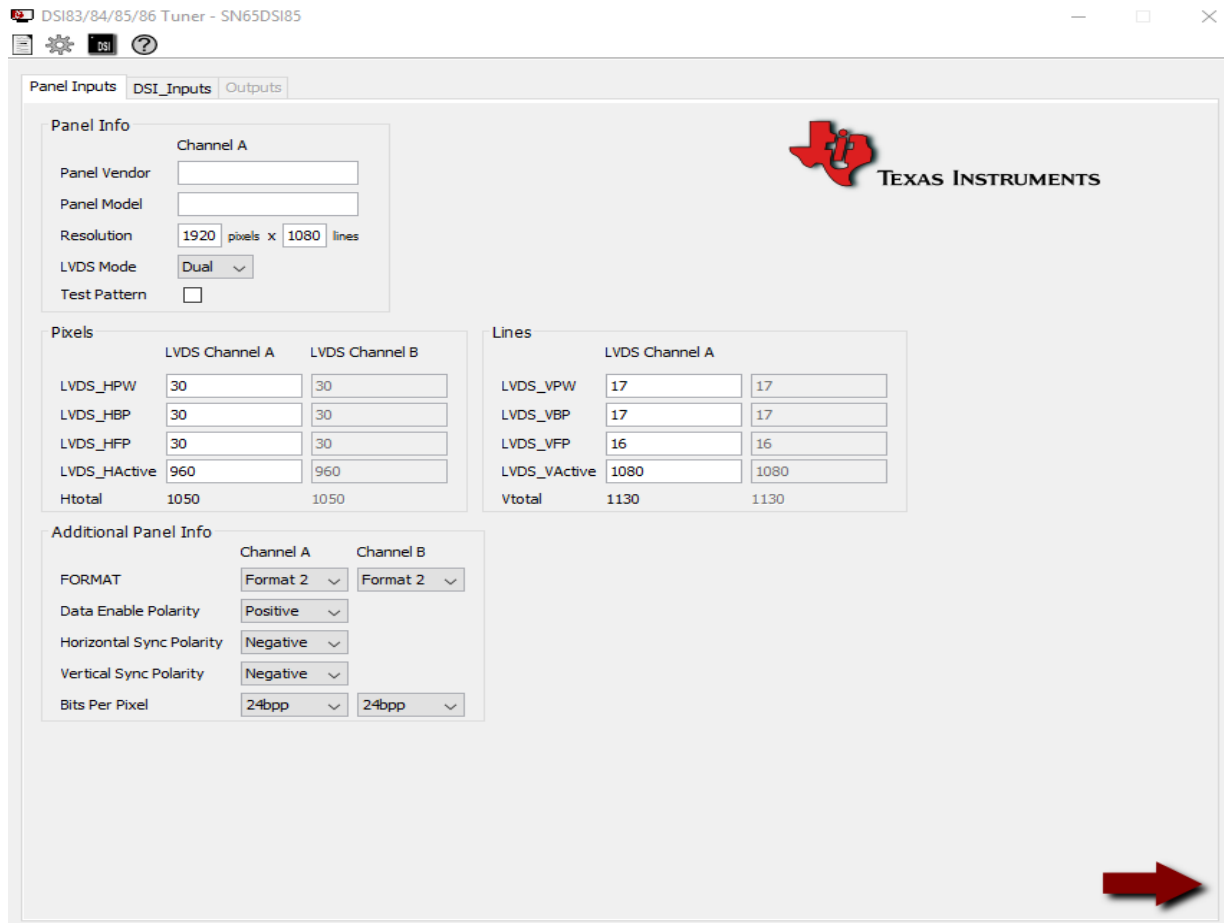
Single to dual

- Please watch the “Dual DSI Input to Dual-Link LVDS” video before watching this video
- The SN65DSI84 or SN65DSI85 can be used for this demo



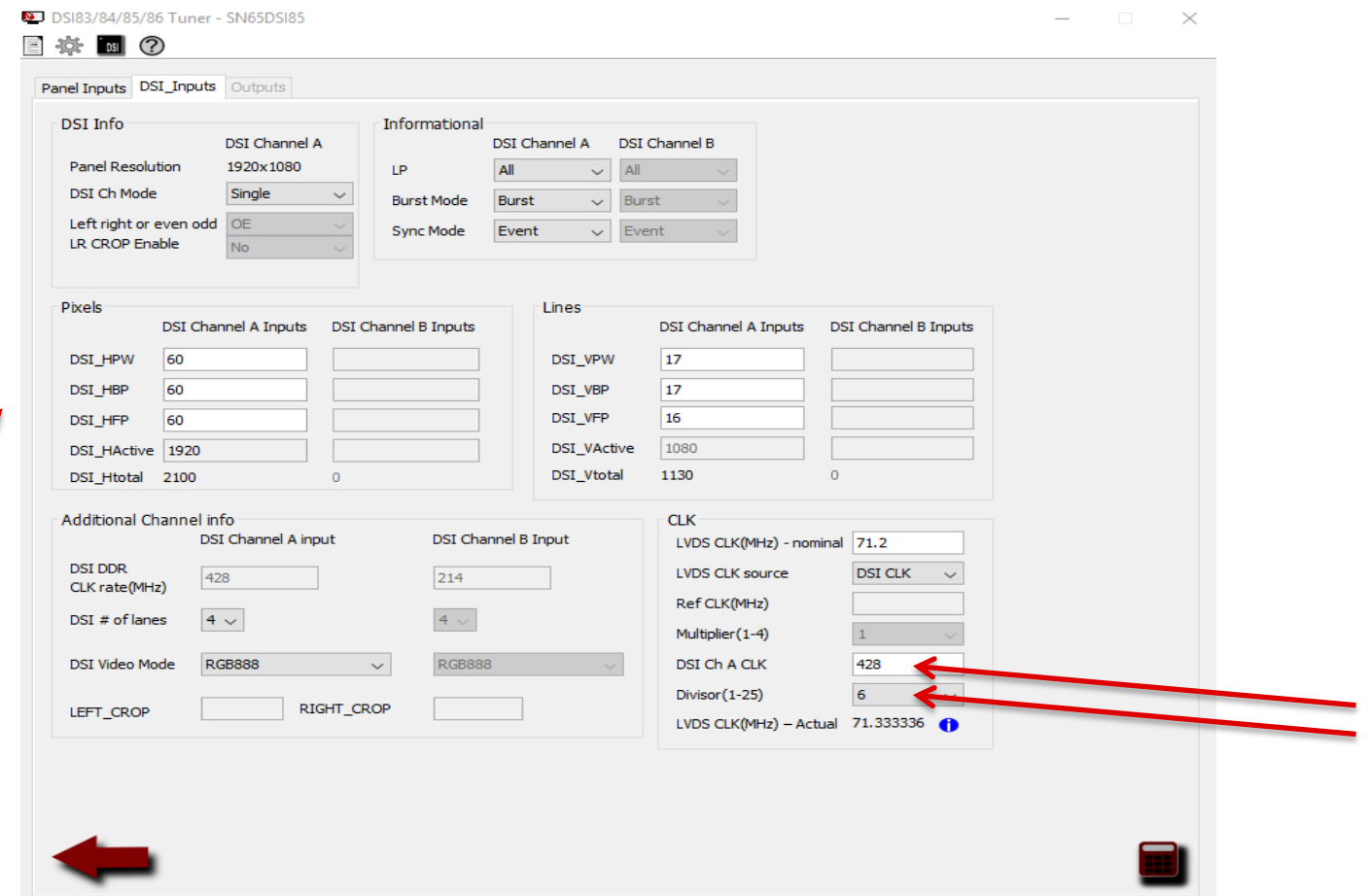
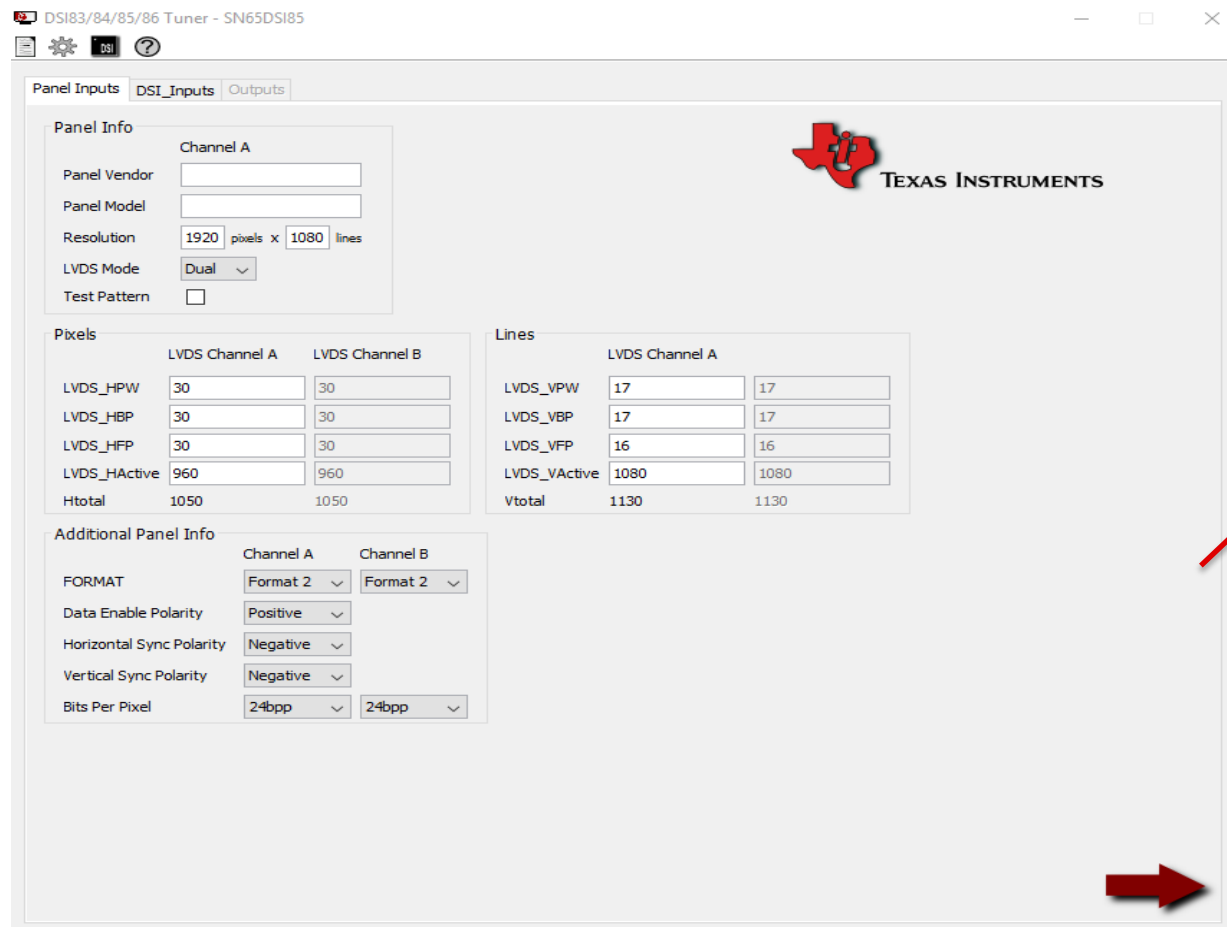
Single to dual

- The same display and settings used for the display in the “Dual DSI Input to Dual-Link LVDS” will be used here
- Change the “DSI Ch Mode” to “Single” in the “DSI_Inputs” window



Single to dual

- Double all of the horizontal parameters (HPW, HBP, HFP, HActive) and the DSI CLK frequency from what they were before in the “Dual DSI Input to Dual-Link LVDS”



Single to dual

- To calculate the minimum required DSI CLK frequency, use the below equation:

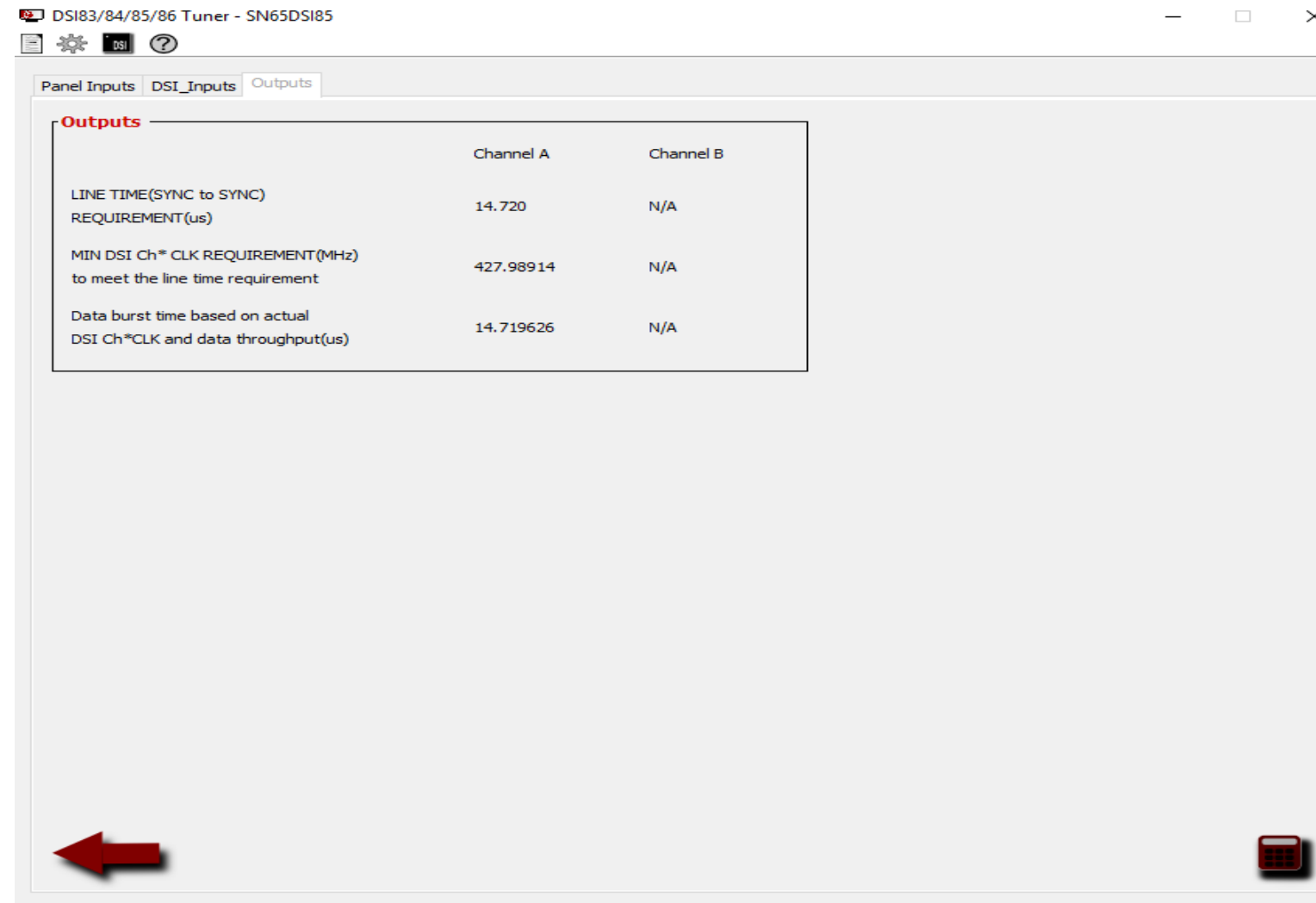
- $$\text{Minimum DSICLK frequency} = \frac{\text{Throughput}}{2 \times \# \text{ of DSI Lanes}} = \frac{\text{LVDS CLK} \times \text{bpp}}{2 \times \# \text{ of DSI Lanes}}$$

- For this example:

- $$\text{Minimum DSICLK frequency} = \frac{2 \times 71.2 \text{ MHz} \times 24 \text{ bpp}}{2 \times 4} = \frac{1708.8 \text{ Mbps}}{2 \times 4} = 428 \text{ MHz}$$

Single to dual

- Observe the “Outputs” window, and follow the same procedure as in the previous videos to generate the CSR settings



The screenshot shows the 'Outputs' window of the DSI83/84/85/86 Tuner - SN65DSI85 software. The window has three tabs: 'Panel Inputs', 'DSI_Inputs', and 'Outputs'. The 'Outputs' tab is active and displays a table with the following data:

	Channel A	Channel B
LINE TIME(SYNC to SYNC) REQUIREMENT(us)	14.720	N/A
MIN DSI Ch* CLK REQUIREMENT(MHz) to meet the line time requirement	427.98914	N/A
Data burst time based on actual DSI Ch*CLK and data throughput(us)	14.719626	N/A

A red arrow points to the bottom-left corner of the window, and a calculator icon is visible in the bottom-right corner.

Thanks for your time!