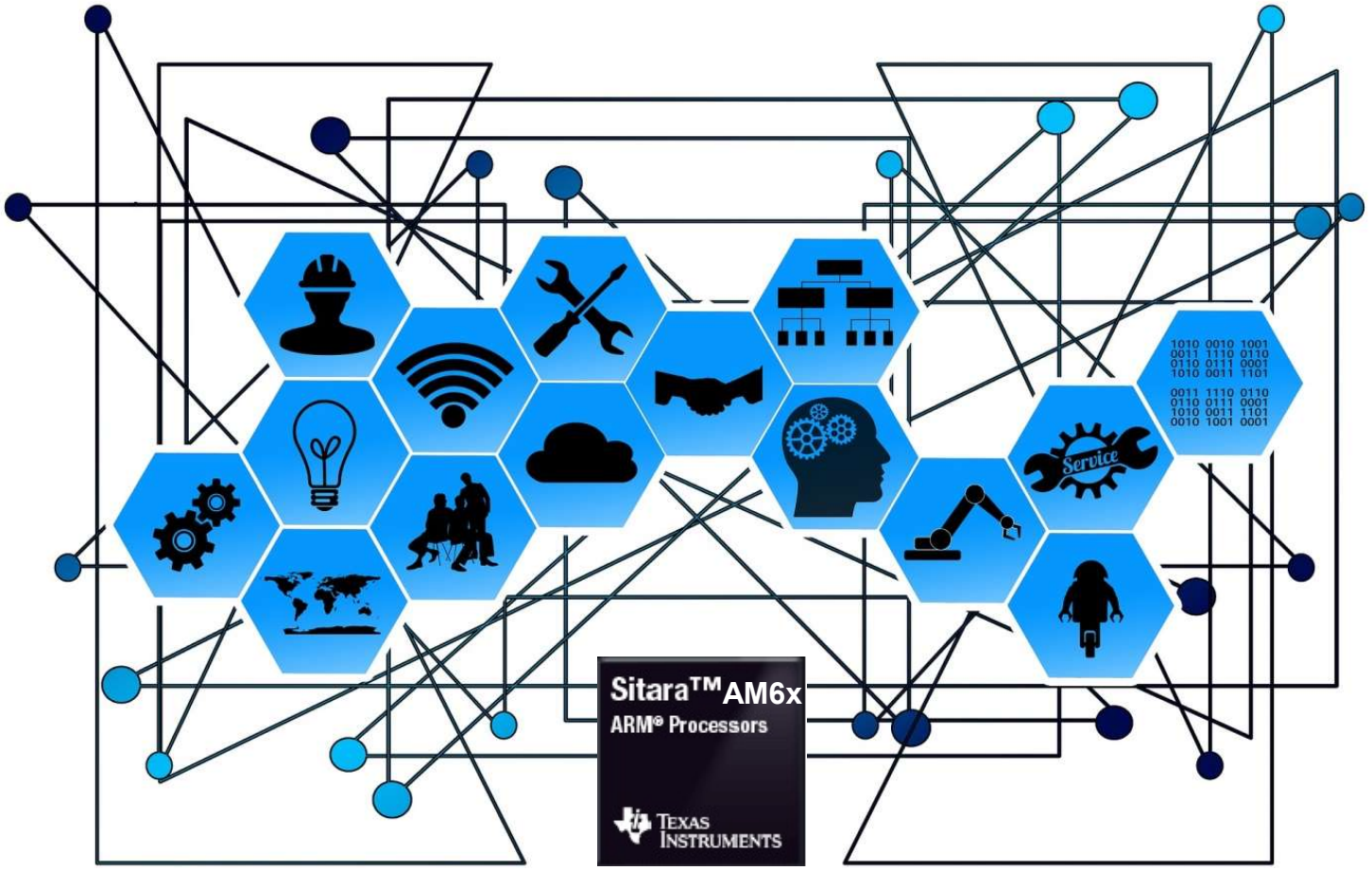
AM6x Architecture Overview

Fulfilling Industry 4.0 Requirements with AM6x

Mike Hannah, Processors, Catalog Business Unit


Sitara™ AM6x
ARM® Processors
Texas Instruments
Service
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0011 1110 0110
0110 0111 0001
1010 0011 1101
0011 1110 0110
0110 0111 0001
1010 0011 1101
0010 1001 0001

AM6x for Industry 4.0

AM6x processor family was designed to address the requirements and goals of Industry 4.0 for factories of the future:

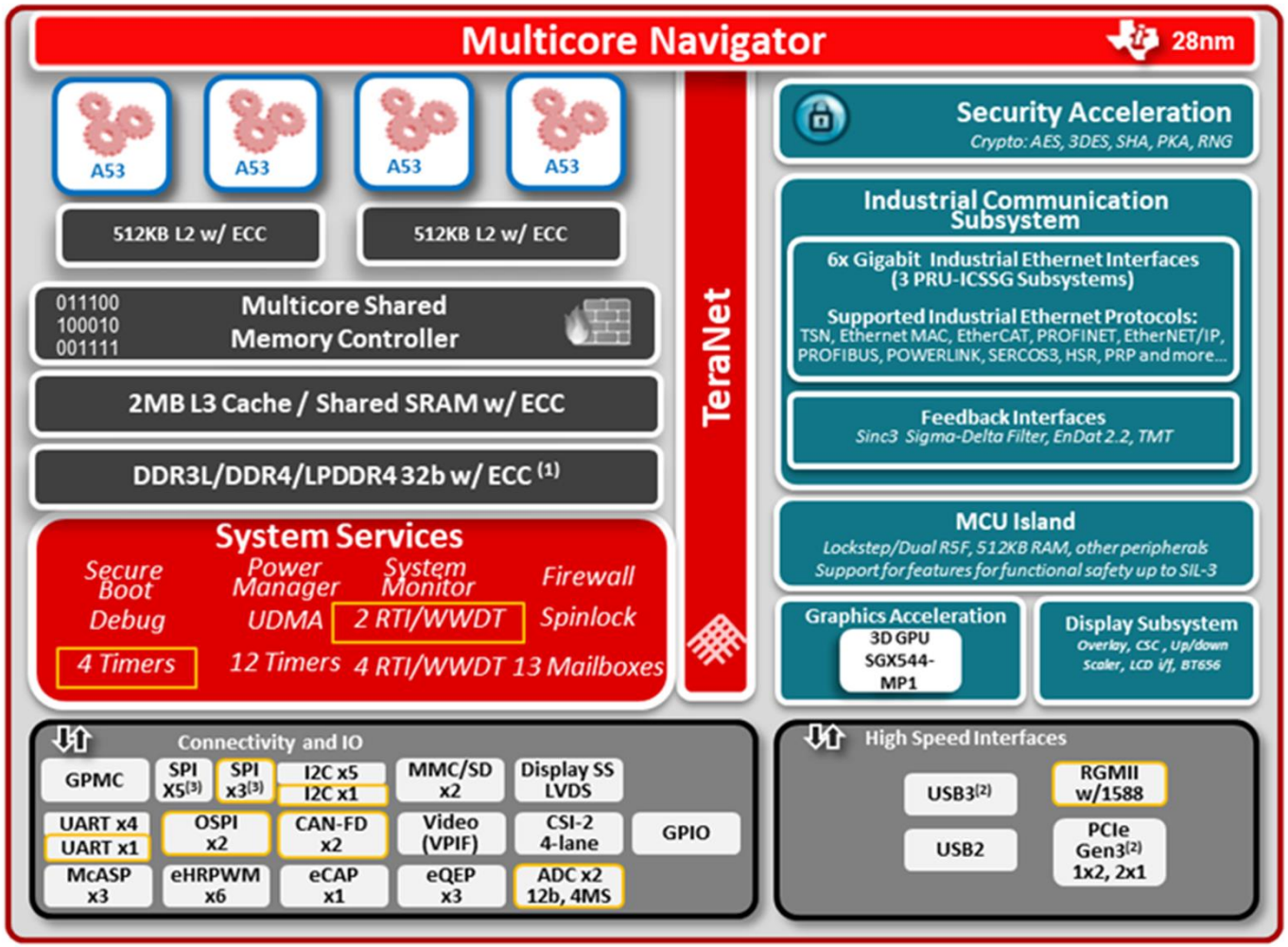
- Scalability
- Next-generation industrial networking
- Secure processing
- Functional safety
- Enhanced reliability

Highlights

Efficient 64-bit Arm® cores:
- Cortex®-A53 cores up to 1.1GHz
- Quad- and dual-core pin-to-pin compatible devices
- ECC on most on-chip memories

Security features:
- Secure boot support with customer-programmable keys
- Runtime security & crypto acceleration
- Secure storage

Device Management Security Controller (DMSC) provides secure device services:
- Power control, reset control
- Isolation control (on-chip firewalls)
- Authentication requests



(1) Data rate: 1600 MT/s
(2) SGMII, USB3 and PCIe3 share two SerDes
(3) One port is internally connected only; not connected to any pins

Located in MCU Island

Highlights

PRU_ICSSG:

- Gb-speed industrial protocol support, including TSN
- Three PRU instances support six (6) lanes of real-time Ethernet, such as EtherCAT, PROFINET, and more

MCU Island:

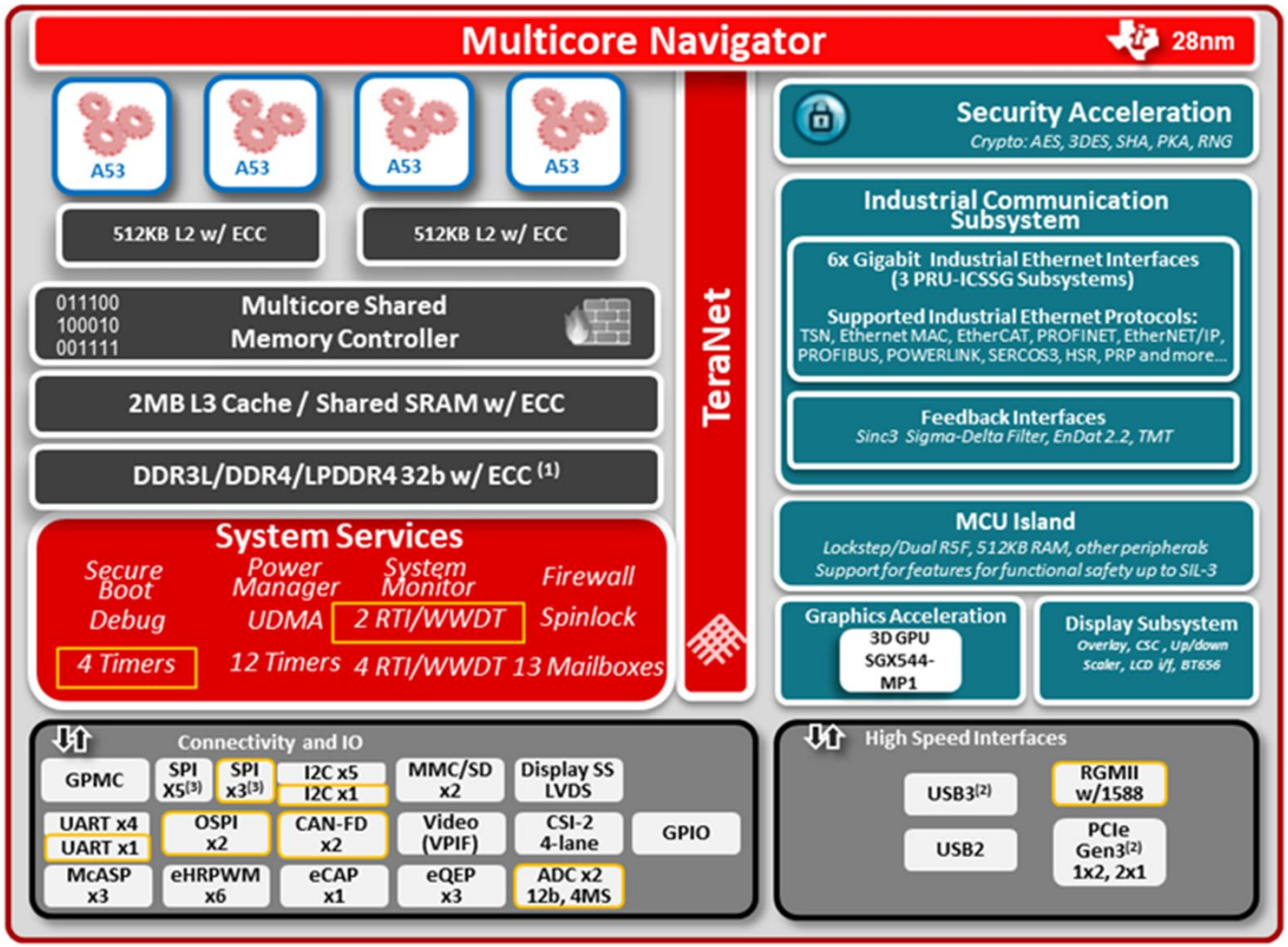
- Features help enable SIL3 systems
- 2x Lock-Step Arm Cortex-R5F
- Memory, serial comms, ADCs

New levels of power integration:

- Simplified power sequencing
- Integrated power-on-reset generation and voltage supervisors
- Integrated LDOs, reducing complexity of external supply solution

Updated peripherals:

- PCIe Gen 3
- CAN-FD
- Octal SPI



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AM65x core components

Cores

- Dual/Quad Arm® Cortex®-A53 up to 1.1 GHz (800 MHz nominal):
  - 32KB L1P
  - 32KB L1D
- Dual-Arm Cortex-R5F up to 400 MHz:
  - 32KB L1
  - 64KB L2 RAM
- 3x PRU_ICSSG up to 250 MHz:
  - Two support 2x RGMII or MII_RT
  - One supports 2x R/SGMII or MII_RT

Memory/Memory Interface

- 2MB on-chip L3 cache/SRAM (A53)
- 512KB on-chip SRAM (R5F)
- Support for NOR and NAND (w/ 16-bit ECC)
- 32-bit EMIF supporting (LP-)DDR3/3L/4 up to 1600 data rate plus ECC
- Octal/Quad SPI/HyperBus

Serial Peripherals

- 5x UART:
  - 3 additional UARTs possible with PRU_ICSSG (one from each)
  - 1 w/ IrDA
- 8x SPI
- 6x I2C

Media Connectivity

- 2x USB:
  - USB3.0 w/ integrated PHY
  - USB2.0 w/ integrated PHY
- 2x HS-MMC/SD/SDIO
  - Configurations vary

Network Connectivity

- 1x GbE port (RGMII)
- 3x 2-port GbE switches (one each per PRU_ICSSG):
  - MII_RT (up to 6x)
  - RGMII (up to 6x)
  - SGMII (up to 2x)
- 2x CAN controllers (CAN FD capable)
- 2x PCI Express (PCIe):
  - Gen 3 compliant
  - 1x2 or 2x1 lane support
  - Root complex/endpoint

System Peripherals

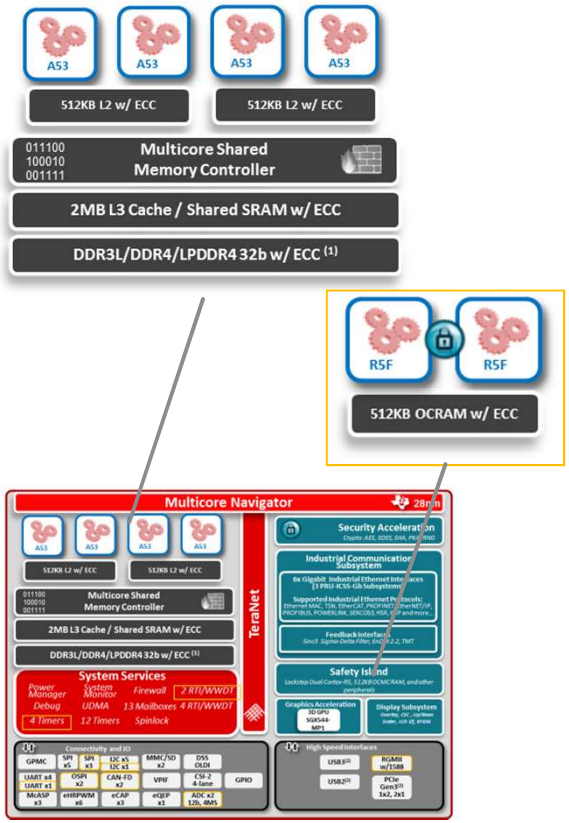
- 16x 32-bit timers
- 1x Watch-Dog Timer (WDT) per core
- 32 kHz sync timer
- 13x mailboxes
- Spinlock
- 6x PWM, 3x eCAP, 1x eQEP
- GPIO
- Keyboard

Audio

- 3x Multi-Channel Audio Serial Ports (MCASP):
  - 2x 16-channel
  - 6x 4-channels

Not all features available on all devices
Not all features shown

Processor and memory



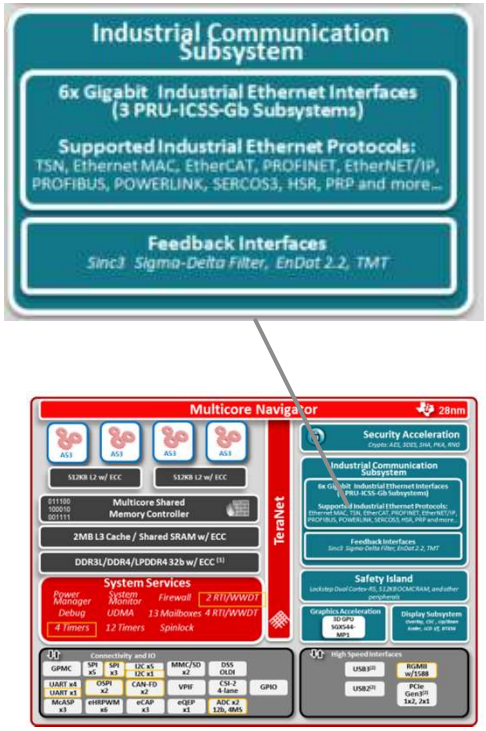
AM6548 diagram shown

- Quad (AM654x) / Dual (AM652x) Arm Cortex-A53:
  - Up to 1.1 GHz (800 MHz nominal), r0p4 revision core(s), ARMv8-A instruction set
  - AArch64 for 64b support and new architecture features
  - Backward compatible with code for previous Arm processors (AArch32)
  - Out-of-order instruction dispatch and completion
  - Integrated NEON™ media processing engine and VFPv4-compatible hardware
  - Hardware virtualization support
  - Five execution units handle simple instructions, branch instructions, NEON and floating-point instructions, multiply instructions, and load & store instructions

- Dual-Arm Cortex-R5F:
  - Up to 400MHz, ARMv7-R
  - Optional Lock-Step operation (SafeTI devices only)
  - Integrated NEON processing engine and VFPv3-compatible hardware
  - Vectored Interrupt Manager (VIM)

PRU_ICSSG

Programmable Real-Time Unit Industrial Communication Subsystem Gb

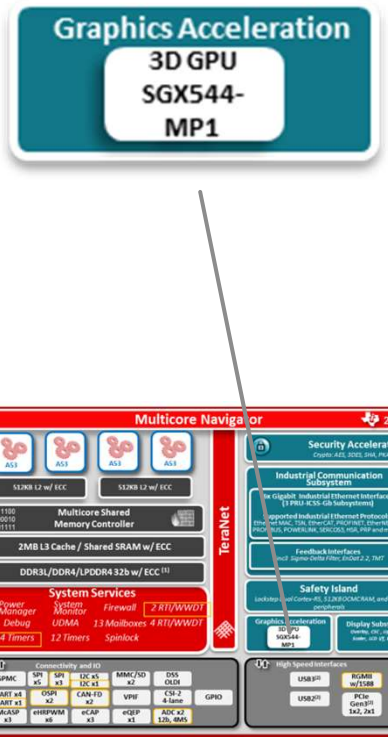


AM6548 diagram shown

3x PRU_ICSSG, with each subsystem consisting of quad 32-bit RISC cores (PRUs) and containing shared data and instruction memories, internal peripheral modules, and interrupt controllers

- 2x general-purpose PRU cores:
  - 12KB program RAM per CPU
  - 8 KB data RAM per CPU
- 64KB shared RAM
- 2x MDIO ports:
  - Two PRU_ICSSG each support 2x RGMII or MII_RT
  - One PRU_ICSSG supports 2x SGMII, RGMII, or MII_RT
- Two Industrial Ethernet Peripheral (IEP) and Industrial Ethernet timers
- 1x 16550-compatible UART
- Capable of supporting master and/or slave modes of protocols such as TSN, PROFINET IRT, Ethernet/IP with DLR, PROFIBUS, EtherCAT, POWERLINK, SERCOS III, HIPERFACE DSL, BiSS C, EnDat 2.2, HSR/PRP, and more
- Capable of supporting operation as standard Gb Ethernet

Graphics acceleration

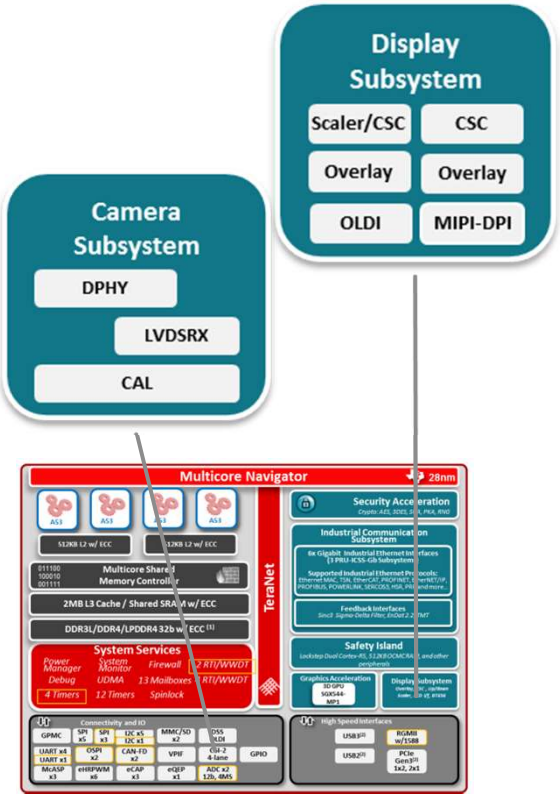


AM6548 diagram shown
Not available in AM65x6

1x Imagination PowerVR SGX544 3D graphics engine:

- Up to 450MHz
- Tile-based architecture reduces access to external memory
- API support for OpenGL® ES1.1 & 2.0

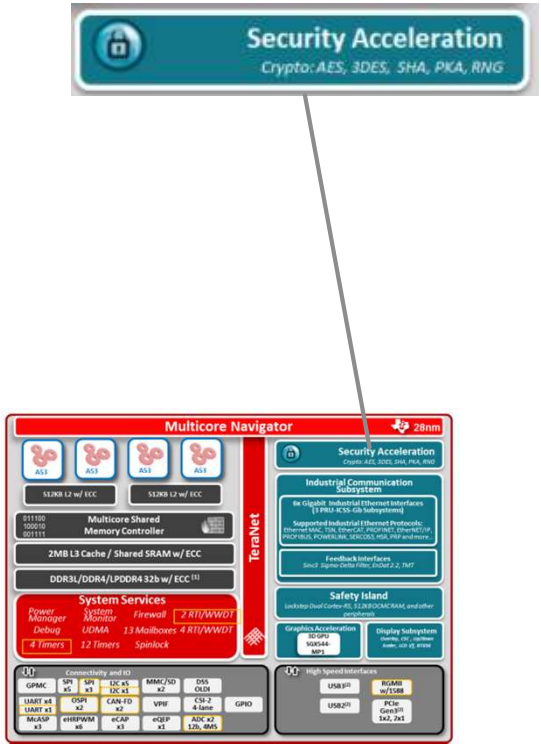
Display subsystem and camera/video input



AM6548 diagram shown

- **Display subsystem:**
  - 1x video pipe with built-in scaler and color space converters
  - 1x graphics pipe with YUV support (no scaler)
  - 2x input-mapped overlay managers
  - 2x video output ports up to 1080p60 resolution
    - One MIPI-DPI parallel interface (7MHz – 165MHz pixel clock)
    - One LVDS Link/OpenLDI-4L (up to 165MHz pixel clock)
  - Frame freeze detection
- **Camera subsystem:**
  - 1x Camera Adaption Layer (CAL) controller with option for:
    - MIPI CSI-2 4-Lane camera interface
    - LVDSRX support for generic/non-MIPI parallel protocol
    - 16-bit parallel video capture interface

Cryptographic accelerators

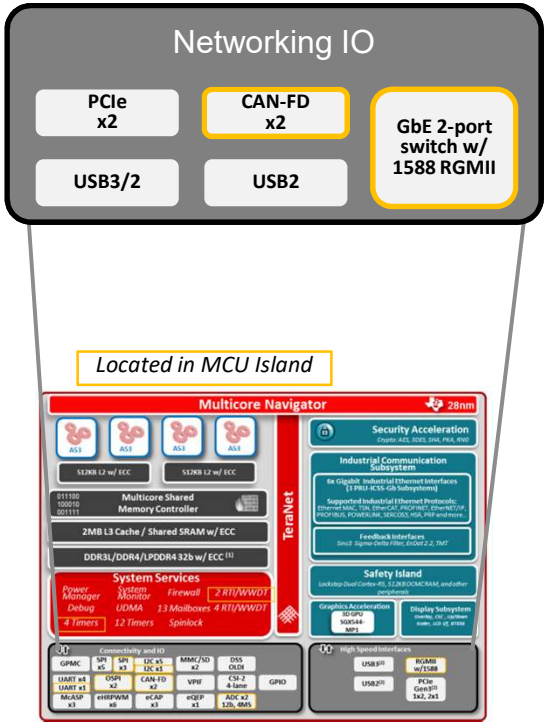


AM6548 diagram shown

Cryptographic hardware accelerators:

- 2x Advanced Encryption Standard (AES):
  - Symmetrical modules supporting 128-bit, 192-bit, or 256-bit key
- Data Encryption Standard (DES3DES) supports three modes of operation:
  - Electronic Codebook (ECB)
  - Cipher Block Chaining (CBC)
  - Cipher Feedback (CFB)
  - Does not support Output Feedback (OFB) mode
- Fast Public Key Authentication (FPKA)
- 2x Secure Hash Algorithm and Message Digest Algorithm (SHA2MD5)
- Random Number Generator (RNG)

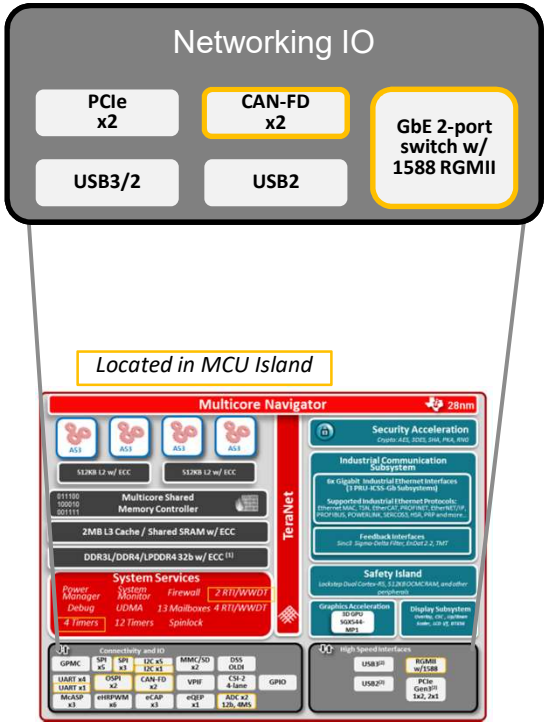
Industrial and programmable IO



AM6548 diagram shown

- **2x CAN(-FD):**
  - –Support bit rates up to 1Mbit/s and are compliant to CAN2.0B protocol specification
  - –Conforms w/ CAN Protocol 2.0 A, B and ISO 11898-1
  - –CAN-FD protocol supported on select part numbers
  - –AUTOSAR and J1939 support
- **2x PCIe:**
  - –Support for PCIe Gen3 modes:
    - One controller by-two lane configuration
    - Two controller by-one lane configuration
  - –Root Complex and Endpoint support
  - –Use of second lane is mutually exclusive with USB3.0
  - –Use of PCIe is mutually exclusive with PRU_ICSSG SGMII configuration

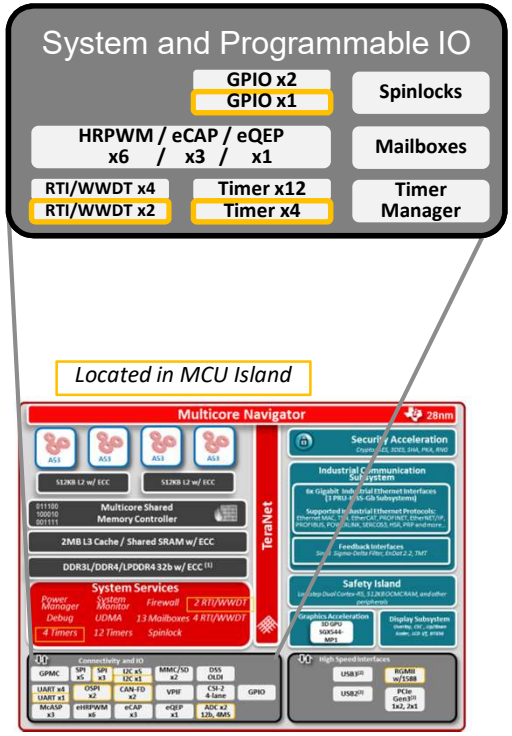
Industrial and programmable IO



AM6548 diagram shown

- **1x USB 3.0/2.0; 1x USB 2.0:**
  - –SuperSpeed Universal Serial Bus (USB) Dual-Role-Device (DRD) subsystem with embedded HS and SS PHYs, compliant with the USB2.0 (up to 480 Mbps) and USB3.0 (5 Gbps) standards
  - –HS USB dynamic OTG 2.0 subsystem with embedded HS PHY, supporting up to 480 Mbps
  - –Use of USB3.0 is mutually exclusive with second lane of PCIe and with PRU_ICSSG SGMII
- **Gigabit Ethernet:**
  - –Provides one external Ethernet port with AVB/Industrial Ethernet and 802.1AS support.
  - –Included support for 3.3-V RMII/MII and 1.8- or 3.3-V RGMII

System and programmable IO

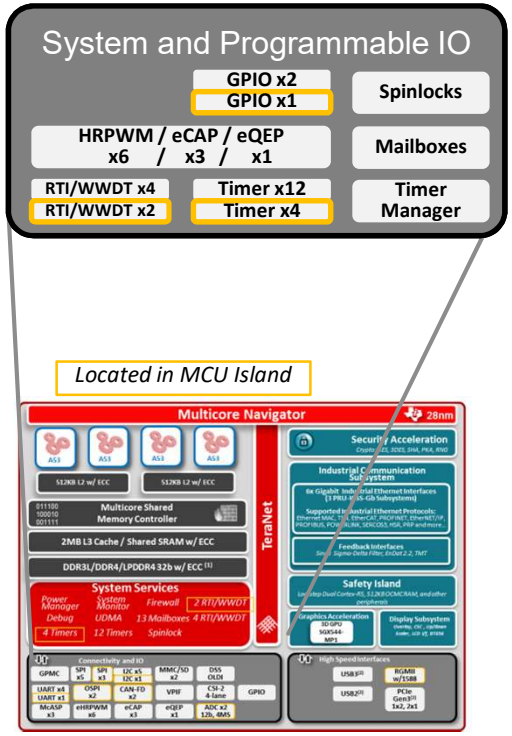


AM6548 diagram shown

PWM/CAP/QEP:

- **6x Enhanced High-Resolution Pulse-Width Modulator (eHRPWM):**
  - 16-bit time based with period/frequency control
  - Supports two (2) independent PWM outputs with single-edge operation or dual-edge symmetric operation
  - Supports one (1) independent PWM output with dual-edge asymmetric operation
- **3x Enhanced Capture (eCAP) modules:**
  - Dedicated input capture pin
  - 32-bit time based
  - 4 x 32-bit time-stamp capture registers
- **1x Enhanced Quadrature Encoder Pulse (eQEP) module:**
  - Input synchronization
  - Three-stage/six-stage digital noise filter
  - Quadrature decoder unit

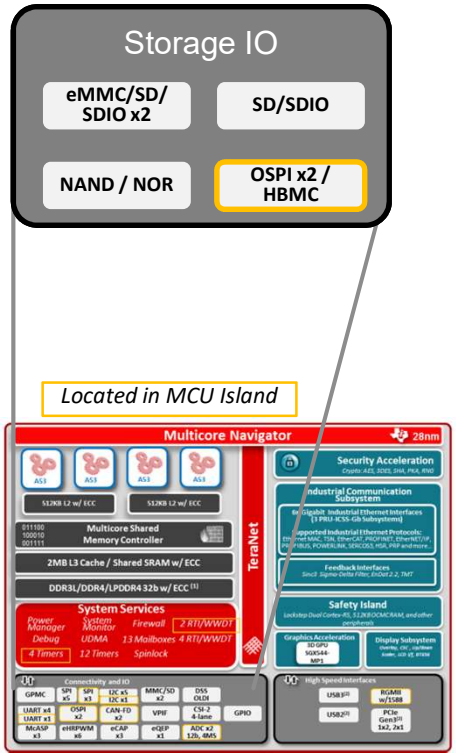
System and programmable IO



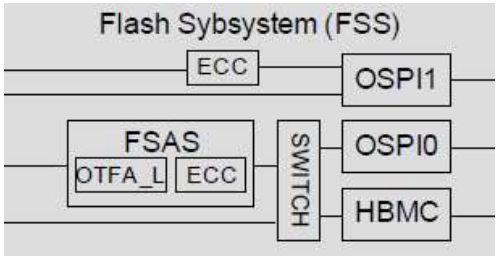
AM6548 diagram shown

- **22x Timers:**
  - Six RTI/WWDT (one per core)
    - Two RTI/WWDT in MCU Island
    - Four RTI/WWDT in Main_SOC
  - Sixteen 32b timers that can be hardware cascaded as 64b timers
    - Four timers in MCU Island
    - Twelve timers in Main_SOC GPIO
  - Timer manager
    - 2x 1024 IO monitor timer bank
- **3x GPIO controllers:**
  - Each supporting 8-64 general purpose IO
  - Count is dependent on multiplexing with functional interfaces
- **256 Spinlocks:**
  - Inter-processor arbitration
- **12x Mailboxes:**
  - 16 HW FIFOs & 4 users per mailbox

Storage IO



AM6548 diagram shown

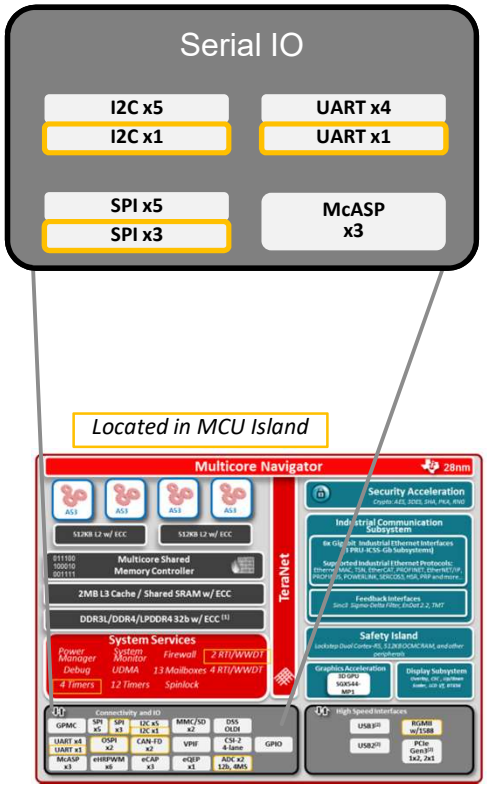


- **2x eMMC/SD/SDIO:**
  - 1x 4-bit
  - 1x 8-bit
  - JESD84-B51 (eMMC 5.01)
  - SD Card: 4.10 (limited to SD 3.0 by PHY speed)
  - SDIO Version 3.0

- **NAND/NOR, General Purpose Memory Controller (GPMC):**
  - Supports asynchhronous SRAM-like memories; async, sync, & page-mode burst NOR flash devices; NAND Flash; and pseudo SRAM devices
  - 8 and 16 bit modes
  - Up to 100MHz synchronous, 133MHz asynchronous

- **OSPI/HBMC:**
  - 2x Octal-SPI (2x Quad-SPI optional)
  - One of the Octal-SPI is multiplexed with HyperBus
    - On-the-fly encryption/decryption/authentication optional
  - Quad-SPI mode up to 133MHz SDR; Octal-SPI up to 166MHz DDR

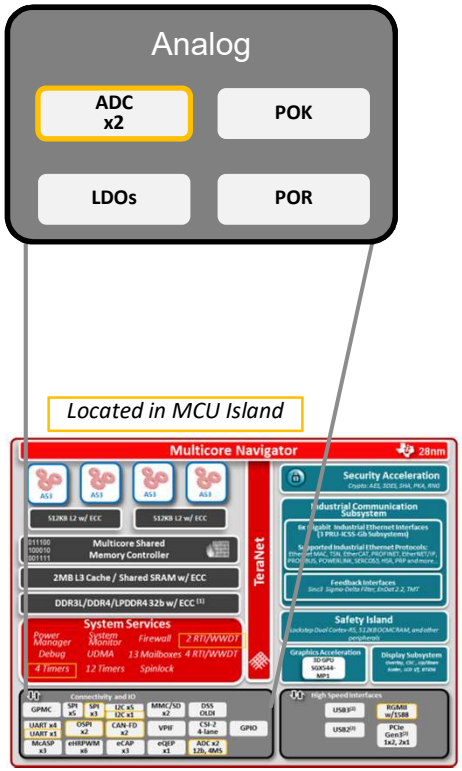
Serial IO



AM6548 diagram shown

- **6x I2C**
  - Slave or master configurable
  - Fast mode (up to 400 Kbps)
  - 7-bit/10-bit address field
  - Supports EEPROM size of 4 Mbit
  - Two ports are connected internally only; not connected to any pins
- **5x UART:**
  - Selectable UART / IrDA / CIR / ISO 7816 modes
  - Support RS485
  - Baud-rate from 300 bits/s up to 3.6864 Mbits/s
  - One instance in Wakeup domain
  - One instance in MCU Safety Island
- **8x SPI:**
  - Function as master or slave
  - Up to 50MHz
  - Each supports up to four external devices (four chip selects)
- **3x McASP:**
  - Support up to 16, 10, 4 serial data pins on McASP0/1/2 ports, respectively
  - Transmit clocks up to 50MHz; Receive clocks up to 80MHz
  - Supports TDM, I2S, and similar formats

Analog integration



AM6548 diagram shown

- **2x ADC:**
  - 12-bit
  - 4-MSPS

- **Integrated Power Management:**
  - Integrated POR, voltage supervisors, LDOs, simplified power sequencing
  - Power management architecture designed to enable different low power modes
  - Companion PMIC available from TI for more advanced power management features:
    - Run-time OPP change
    - Functional safety compliance and watchdog circuitry
    - Discrete option demonstrated on AM654x Industrial Development Kit (IDK)

AM65x family device comparison

	AM6548	AM6546	AM6528	AM6527	AM6526
Arm®	Quad Cortex®-A53 (2x Dual-core cluster) 2x 512KB L2	Quad Cortex-A53 (2x Dual-core cluster) 2x 512KB L2	Dual Cortex-A53 (1x Dual-core cluster) 512KB L2	Dual Cortex-A53 (2x Single-core clusters) 2x 512KB L2	Dual Cortex-A53 (1x Dual-core cluster) 512KB L2
MCU	2x Cortex-R5F				
MSMC / OCRAM	2MB				
EMIF	32b (LP)DDR3/3L/4 (w/ ECC)				
Graphics	SGX544-MP1	-	SGX544-MP1	-	-
HW Video Acceleration	-				
Display	DSS7_UL – OLDI + MIPI-DPI				
ICSS	3x PRU_ICSSG				
PCIe	Gen3, 2x 8Gbps (2L or 2x1L)				
USB	1x USB2 + 1x USB3/2				
Data bus	GPMC (22b address + 16-bit data)				
Other Peripherals	2x CAN-FD, 5x UART, 6x I2C, 8x SPI, 2x OctalSPI, 2x eMMC/SD, VPIF, CSI-2, Security HWA, 3x McASP, GPIO				
Power (*)	< 5W		< 4W		
Package	23x23mm Flip Chip (FC)				
Temp/ Reliability	-40 to 105C, 100k POH				

(*) Power consumption will depend on utilization and temperature condition.

For more information

- Sitara AM6x Arm Cortex-A53 Processors: http://www.ti.com/am65x
- Sitara AM6x Training Series: http://training.ti.com/am6x
- Processor SDK for Sitara AM6x: http://www.ti.com/processors/sitara-arm/am6x-cortex-a53-r5/overview.html
- AM65x General Purpose EVM http://www.ti.com/tool/TMDX654GPEVM
- AM65x IDK: http://www.ti.com/tool/TMDX654IDKEVM
- For questions about this training, refer to the E2E Community Forums at http://e2e.ti.com