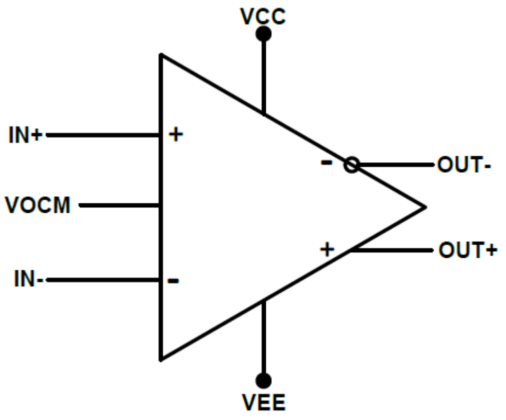
Using fully differential amplifiers to optimize high speed signal chain interfaces

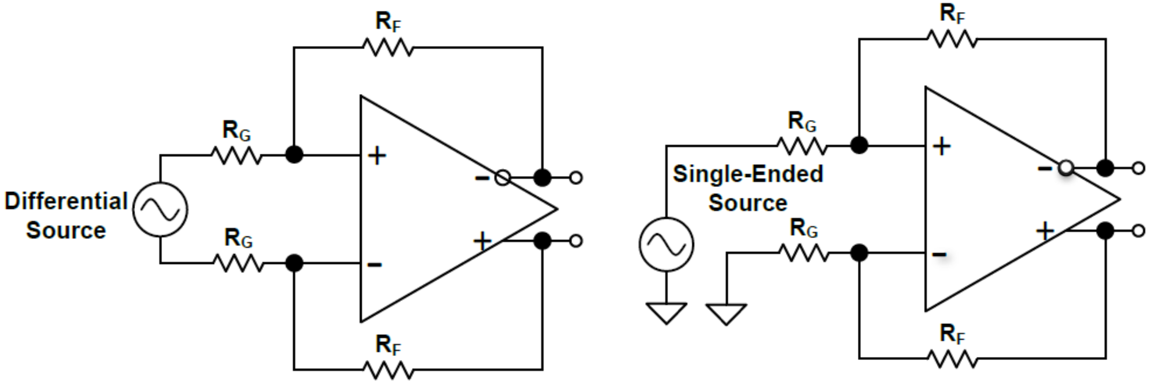
Agenda

- **What is a fully differential amplifier (FDA)?**
- **Solving interface challenges using an FDA**
  - Overcoming challenges of balun
  - Level shifting using the FDA
  - Optimizing stability of FDA for low gain
  - Buffering a clock source using FDA
  - DAC buffering to drive single-ended load
- **Summary**
- **Q/A (15min)**

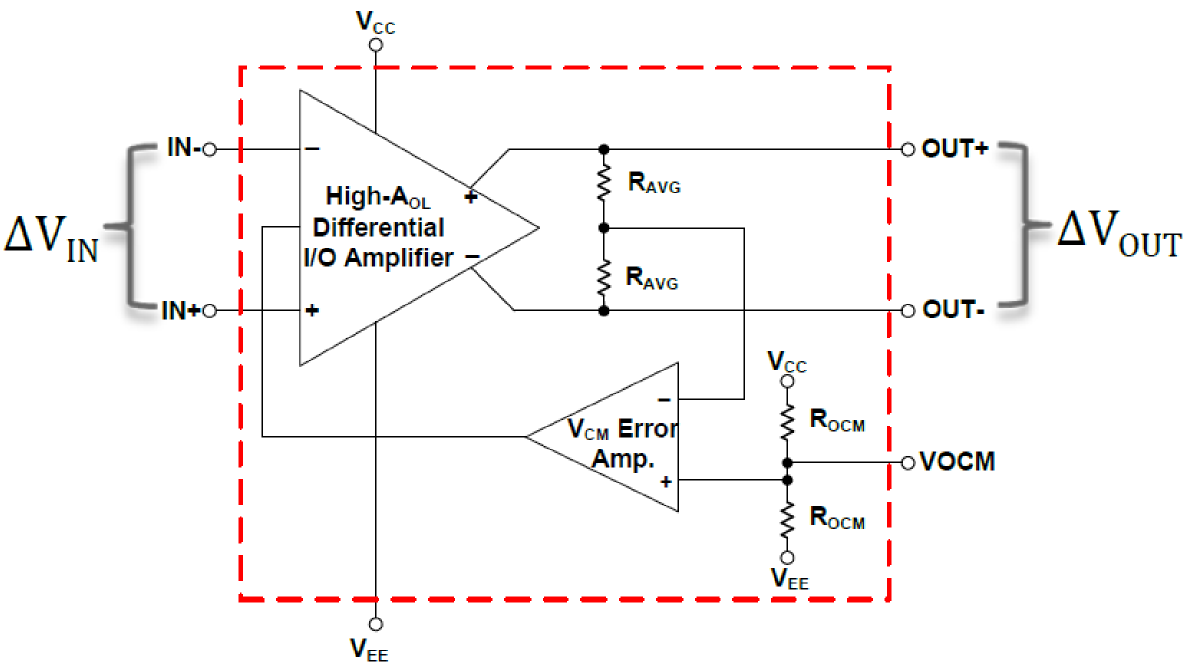
What is a fully differential amplifier (FDA)?

- **Processes the difference voltage between its two inputs converting differential input to differential output**
- **Converts single-ended input to differential output**
- **FDA's output common mode voltage can be controlled independently of the differential voltage via the VOCM pin**





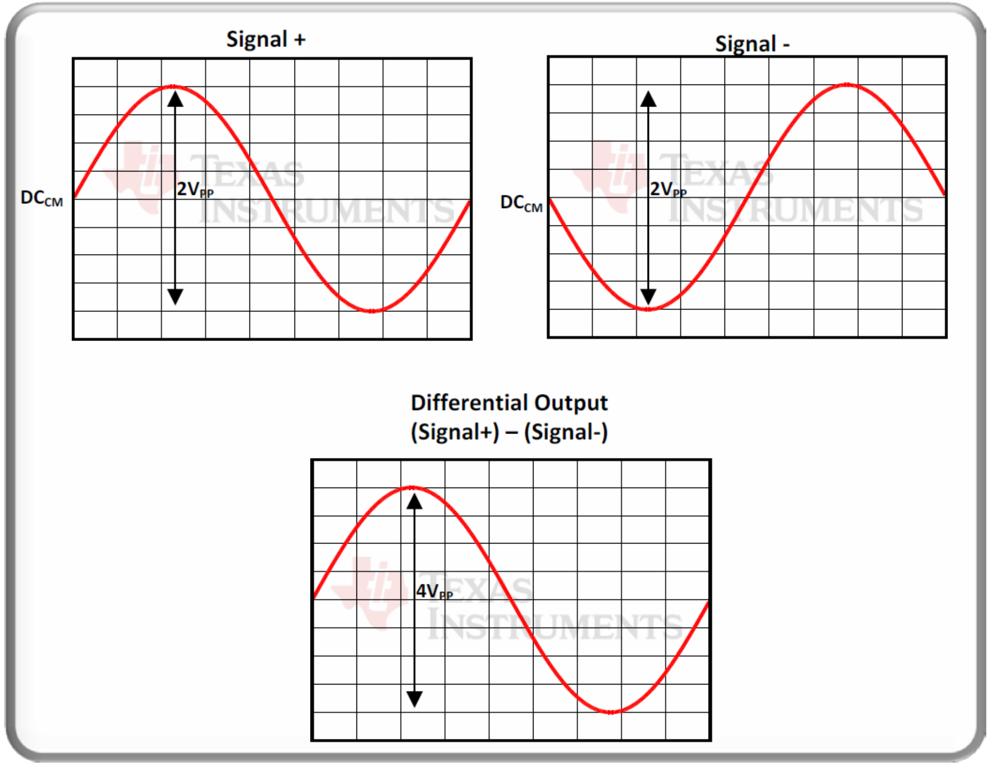
Inside a typical FDA



- Integrated fully-differential high AOL amplifier
- Integrated wide-bandwidth, common-mode feedback, error amplifier
- Integrated resistors to detect the average output common-mode voltage
- Integrated mid-supply, common mode set resistors

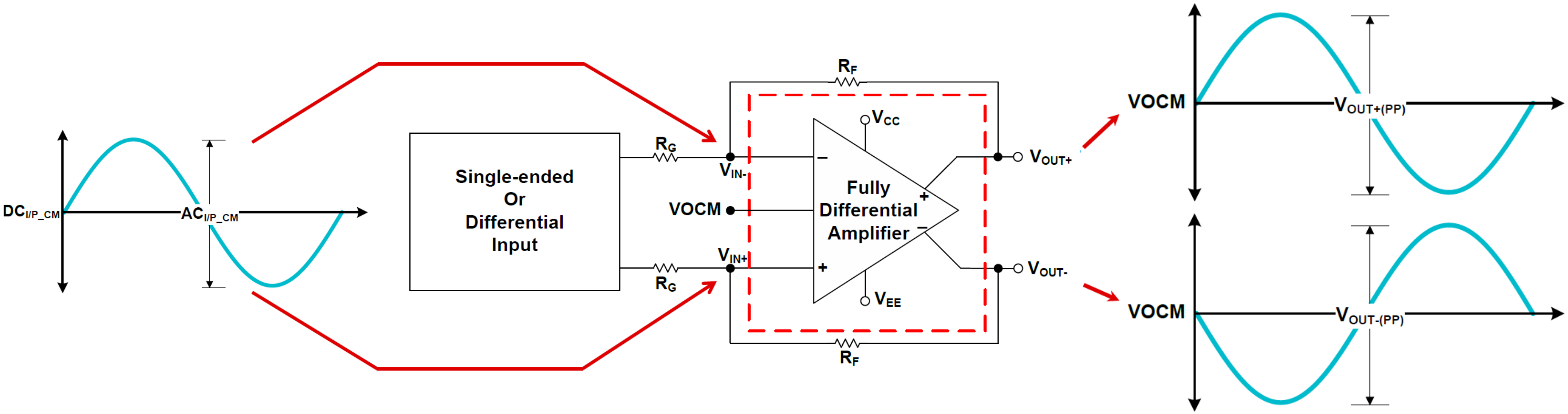
Differential signaling benefits

- **Higher output voltage swing for a given power rail**
- **Increased immunity to noise as any signal common to both inputs is cancelled**
- **Lower even-order harmonics with differential signaling**



Three rules governing FDA operation

1. The voltage at the input nodes to the amplifier track each other exactly (virtual short across inputs)
2. The two outputs are 180° out of phase
3. The two outputs have the same DC offset voltage equal to VOCM



$$V_{OUT+}(t) - VOCM = -\left(V_{OUT-}(t) - VOCM\right)$$

$$VOCM = \frac{V_{OUT+}(t) + V_{OUT-}(t)}{2}$$

FDA common mode voltages

1 **At the FDA Input, use KCL**

$$\frac{(V_{ID\mp\_CM} - V_{IN\_CM})}{R_G} = \frac{(V_{IN\_CM} - V_{OUT\pm\_CM})}{R_F}$$

$$V_{IN\_CM} = 2.5V \cdot \frac{100\Omega}{(400\Omega + 100\Omega)} = 0.5V$$

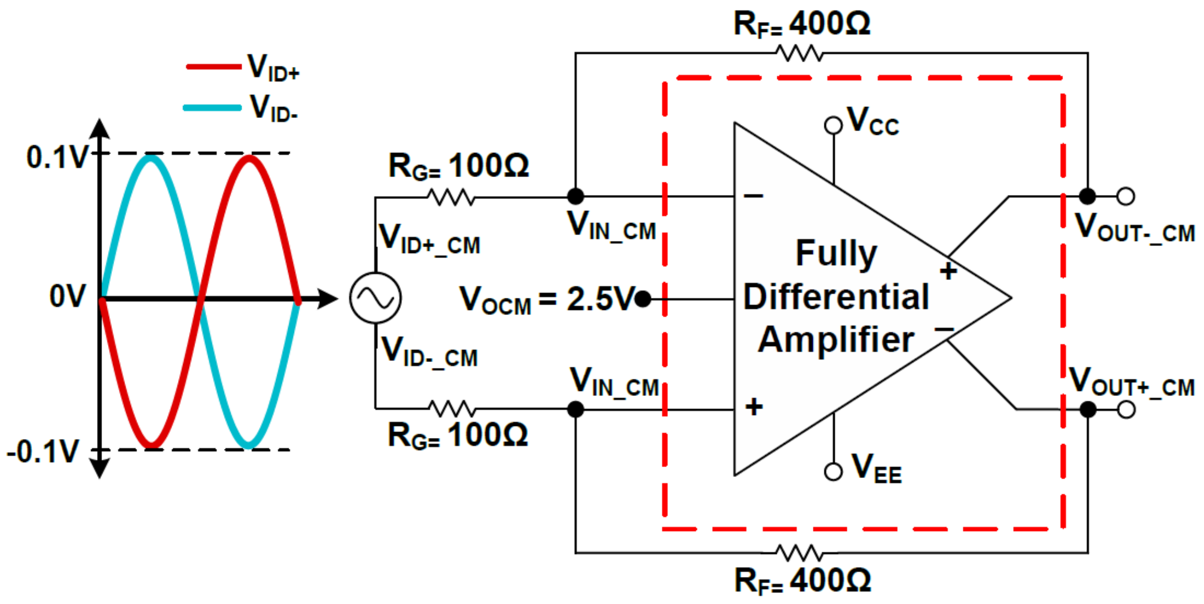
2 **At the FDA Output**

$$V_{OUT+\_CM} = V_{OUT-\_CM} = V_{OCM} = 2.5V$$

$V_{ID-} = -V_{ID+} = 0.2\ V_{PP}$

$V_{ID\pm\_CM} = 0\ V$

$V_{OCM} = 2.5\ V$

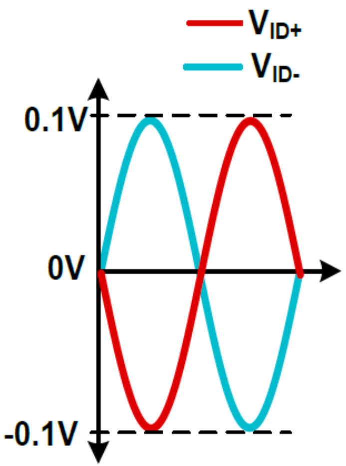


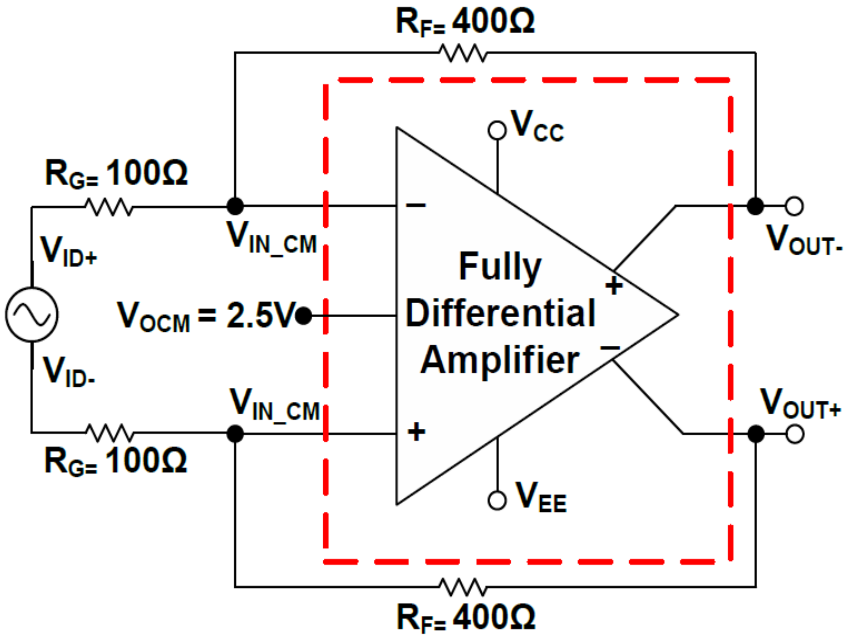
FDA differential voltages

$V_{ID-} = -V_{ID+} = 0.2\ V_{PP}$

$V_{ID\pm\_CM} = 0\ V$

$V_{OCM} = 2.5\ V$





Taking each half of the FDA separately and applying KCL,

$$V_{IN\_CM} = \frac{V_{OUT-} + V_{ID+}\left(\frac{R_F}{R_G}\right)}{\left(1+\frac{R_F}{R_G}\right)}, and \quad (3)$$

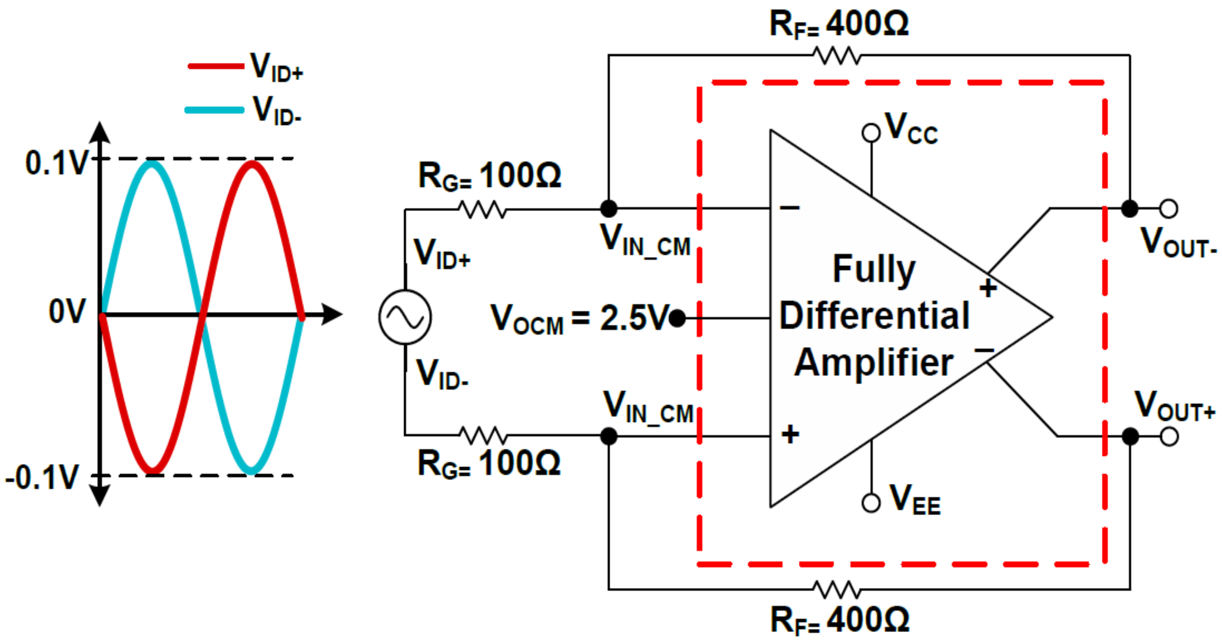
$$V_{IN\_CM} = \frac{V_{OUT+} + V_{ID-}\left(\frac{R_F}{R_G}\right)}{\left(1+\frac{R_F}{R_G}\right)} \quad (4)$$

Equating (1) & (2)

$$\left(V_{OUT-} - V_{OUT+}\right) = -\left(\frac{R_F}{R_G}\right).\left(V_{ID+} - V_{ID-}\right) \quad (5)$$

$$\frac{\Delta V_{OUT}}{\Delta V_{ID}} = -\left(\frac{R_F}{R_G}\right) = G_V \quad (6)$$

FDA output signal



Differential V_{OUT},

$$V_{OUT-} = -V_{OUT+} = 4 \times 0.2V_{PP} = 0.8V_{PP}$$

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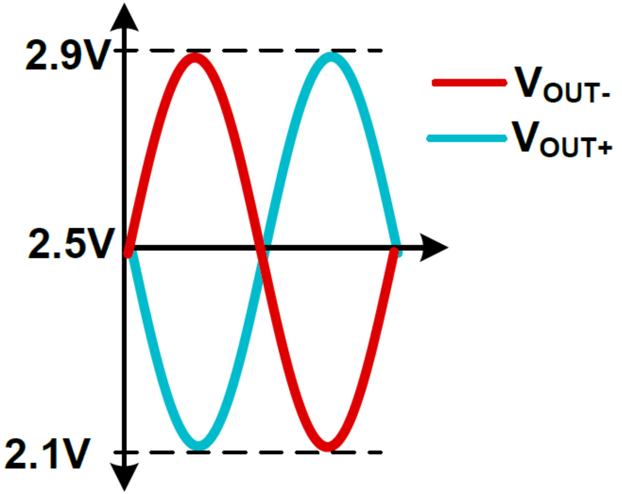

(*Differential* + CM) V_{OUT},

$$V_{OUT-} = 2.5V \pm 0.8V, \text{ and, } V_{OUT+} = 2.5V \mp 0.8V$$

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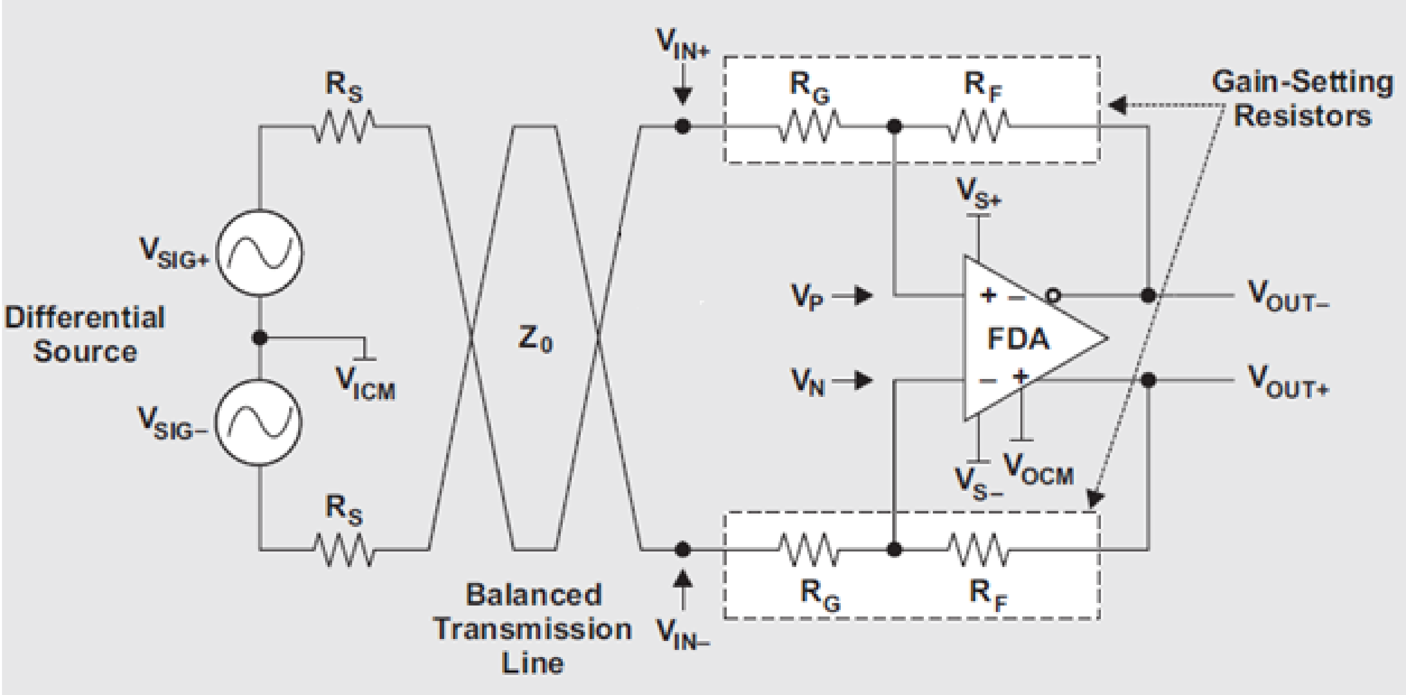
Impedance matching differential input of FDA



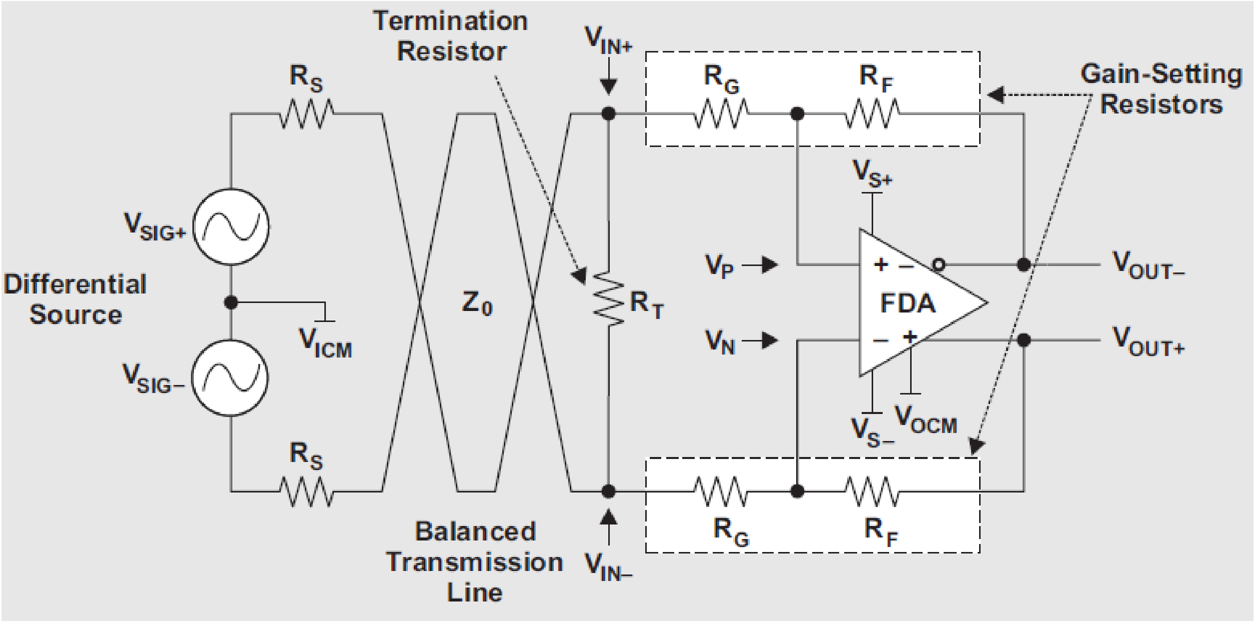
- **Signal gain of amplifier, G_V, is conventionally defined from V_{IN} signal at R_G resistor to V_{OUT} signal of FDA**
- **G_V is independent of source and load**

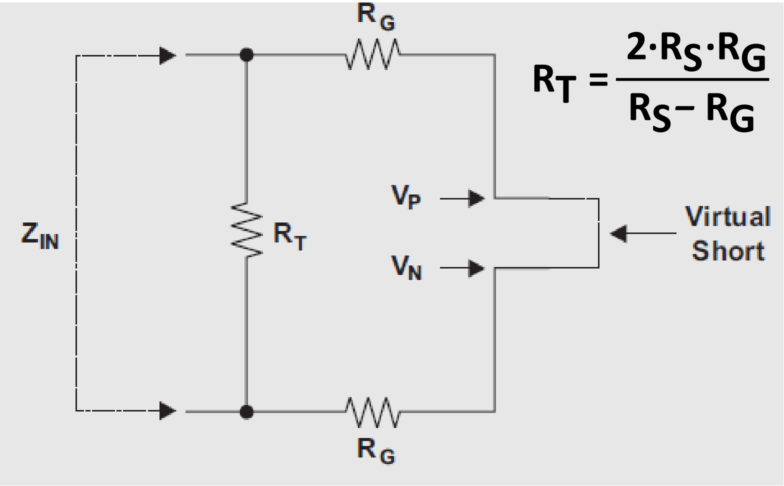
Example 1: Impedance match amplifier to R_S = 50 ohms with G_V = 1 V/V

R_G = 50 ohms, R_F = 50 ohms (R_F is too low!!)

Impedance matching differential input of FDA

- R_T is used when R_G must be set greater than the input impedance, R_S, in order to achieve the desired gain target





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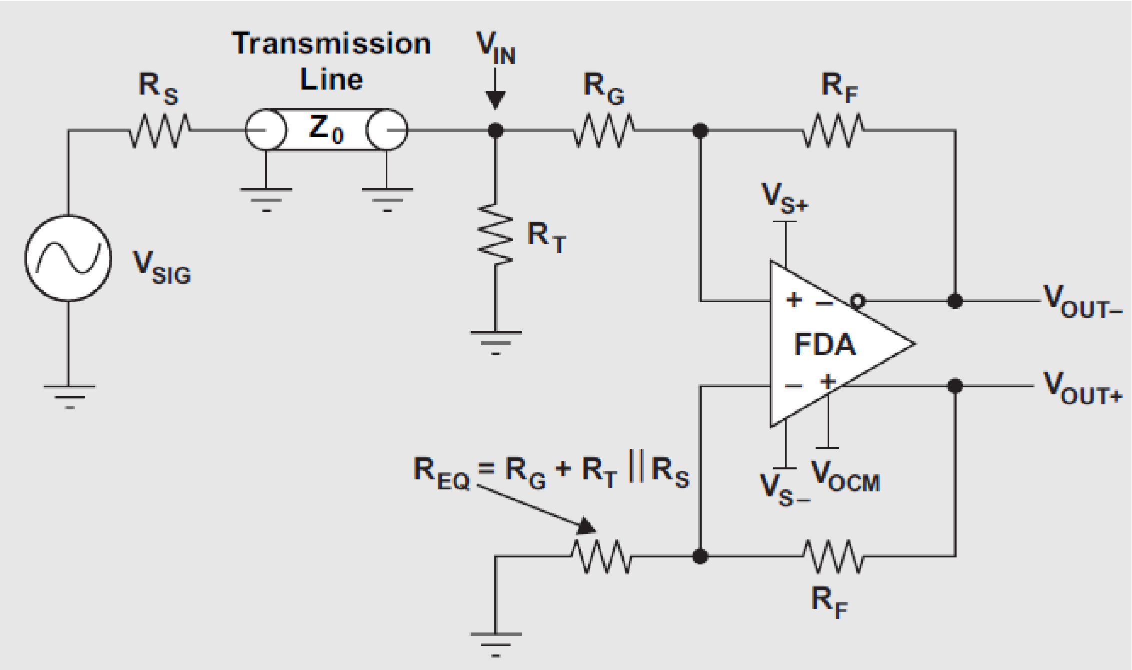
Example2: Impedance match amp to R_S = 50 ohms with G_V = 1V/V

- **R_G = 200 ohms, R_F = 200 ohms, R_T =133 ohms**

Impedance matching single-ended input of FDA



- **With only one side driven, input pins of amplifier are no longer a fixed DC voltage - there is a AC component**

- **Common mode compliance on the input nodes to amplifier becomes more of a concern as inputs move with AC signal**

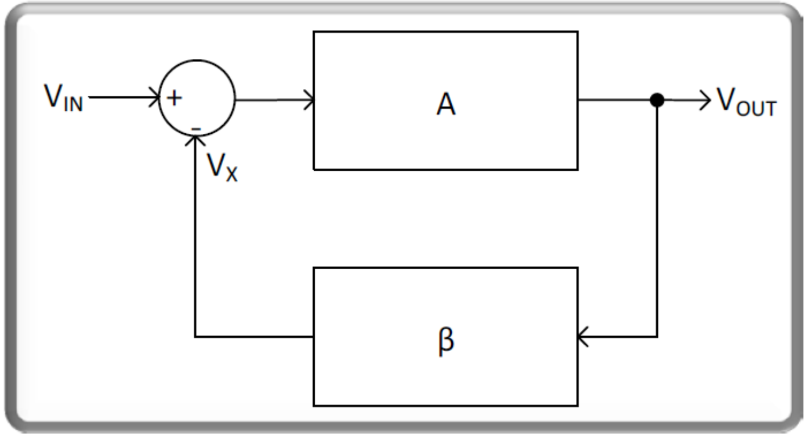
LMH5401-SP

7.5 Electrical Characteristics: V_S = 5 V

TEXAS INSTRUMENTS

PARAMETER		TEST CONDITIONS	SUBGROUP[3]	MIN	TYP	MAX	UNIT
V_{ICH}	Input common-mode high voltage		[1, 2, 3]	(VS+) – 1.41	(VS+) – 1.2		V
V_{ICL}	Input common-mode low voltage		[1, 2, 3]		VS–	(VS–) + 0.41	V

FDA: Generalized transfer function



A ⇒ Forward open-loop gain of system

β ⇒ Reverse transfer function of feedback path

V_X ⇒ Fraction of system output fed back to input

$$V_{OUT} = A(V_{IN} - V_X) \quad (1)$$

$$V_X = \beta \cdot V_{OUT} \quad (2)$$

$$V_{OUT} = A(V_{IN} - \beta \cdot V_{OUT}) \quad (3)$$

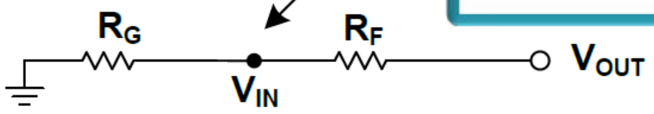
$$V_{OUT}(1 + A \cdot \beta) = V_{IN} \quad (4)$$

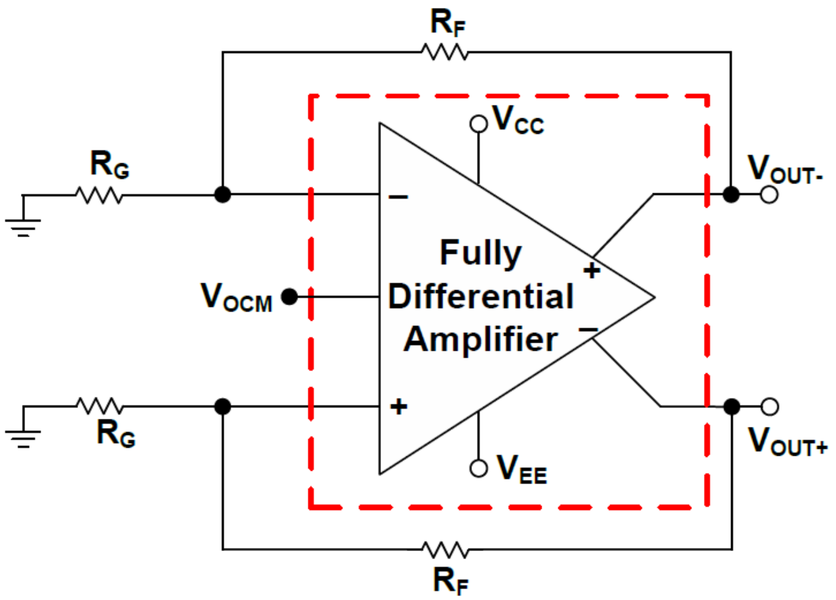
$$Gain = \frac{V_{OUT}}{V_{IN}} = \frac{A}{(1 + A \cdot \beta)} \quad (5)$$

FDA: Generalized transfer function

$$\text{Signal Gain} = -\frac{R_F}{R_G}$$ 6

$\beta = R_G/(R_F+R_G)$ 7





$$\text{Noise Gain} = \frac{1}{\text{Feedback Factor}}$$

$$\text{Noise Gain} = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$$ 8

$$\text{Signal Gain} \neq \text{Noise Gain}$$

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta}, \text{ As } A_{OL} \to \infty, \quad A_{CL} = \frac{1}{\beta}.$$ 9

$A_{OL}\beta \to$ Loop Gain.

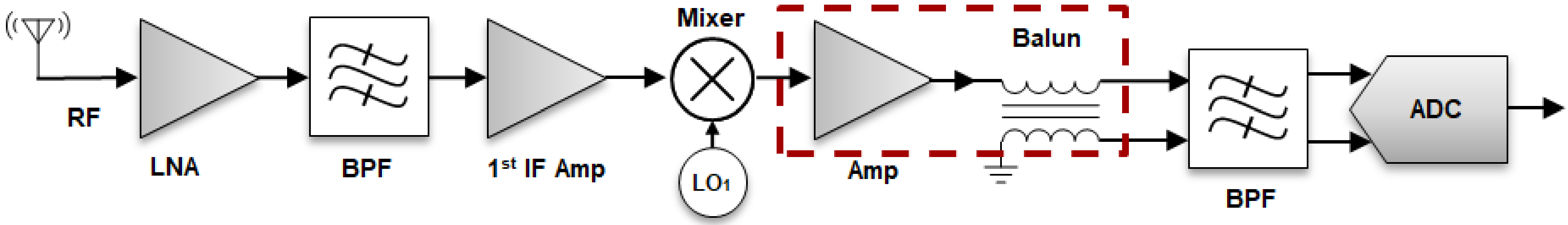
Frequency @ which $|A_{OL}\beta| = 1$, is the (A_{CL}) -3dB BW

FDA solving signal chain challenges

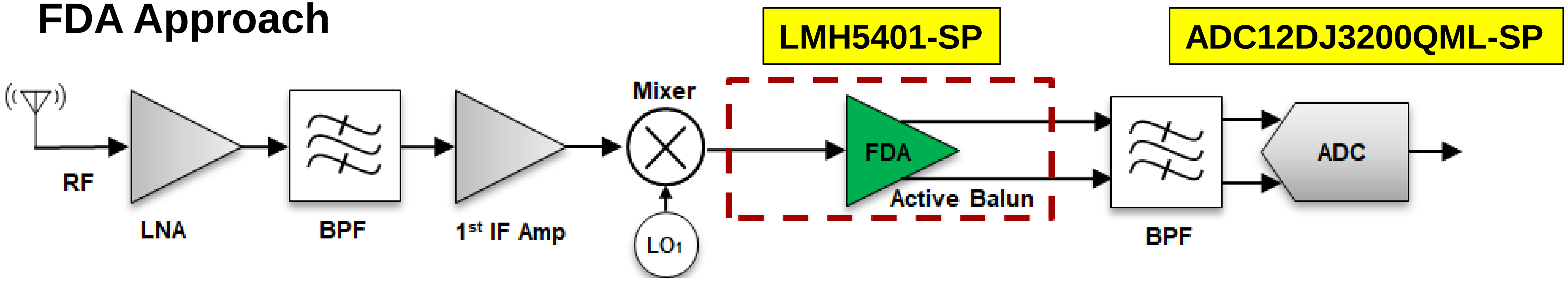
- **Solving interface challenges using an FDA**
  - Overcoming challenges of balun
  - DC level shifting
  - Optimizing stability of FDA for low gain
  - Clock buffer using FDA
  - DAC output buffering

FDA replacing balun to drive high speed ADC

Conventional Balun Approach



FDA Approach



FDA compared to balun

Parameter	Balun	FDA
Size	**Larger** size (66 **mm²**)	**Smaller** size (**LMH5401-SP: 33mm²**)
DC coupled	**Not suitable** for DC coupled application	**Suitable** for DC coupled applications
Frequency response	**Not suitable** for wide bandwidth: **Large** insertion loss and **varies** with frequency	**Suitable** for wide bandwidth: **Minimal** insertion loss and almost **constant** across frequency
Power gain	**No** power gain - Impedance matching and voltage/current gain are **dependent**	**Supports** power gain - Impedance matching and gain are **independent**
Buffering	**No** buffering - Requirement on **previous stage to drive** filter and ADC input load - **No reverse isolation**	**Buffered** - **Previous stage is isolated** from filter and ADC input load - **Reverse isolation:** Avoids ADC switching components going back to previous stages (ex: antenna)
Distortion	**Worse** distortion due to phase unbalance	**Better** distortion with wideband amplifiers
Noise	**Less noise** (dependent on insertion loss)	**Adds noise**
Temperature range	**Limited** temp range (ex: -20 to 85C) **Large gain variation** across temperature	**Wide** temp range (ex: -55°C to +125°C for LMH5401-SP) **Small gain variation** across temperature
Reliability	**Less reliable** due to mechanical construction (ex: vibration during flight)	**Reliable** due to monolithic implementation

FDA excel calculator tool

https://e2e.ti.com/support/amplifiers/f/14/t/771636

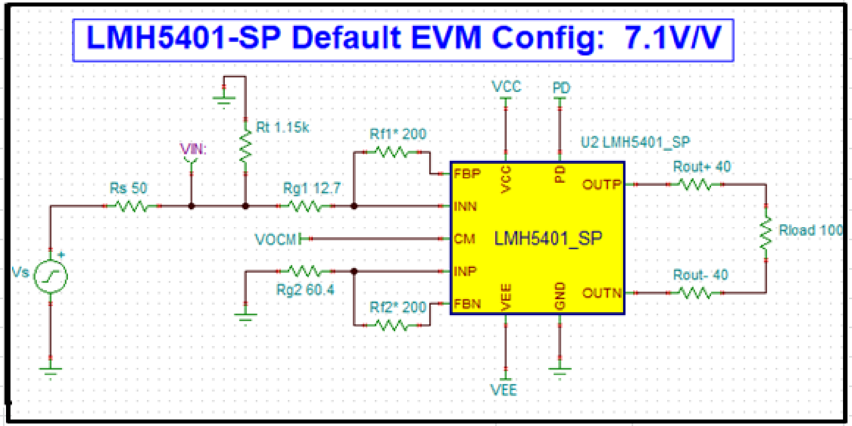
LMH5401-SP SE-DIFF CALCULATOR

Given Gv, Rs, and Rf, solve for Rf*, Rt, Rg1, and Rg2 such that input impedance is matched in single-ended input to differential output configuration.

INPUT Parameter	Value	Units
Enter Target Voltage Gain, Gv (at AMPOUT)	7.100	V/V
Enter Source Impedance, Rs	50	ohms
Enter Target Feedback Resistance, Rf	225	ohms

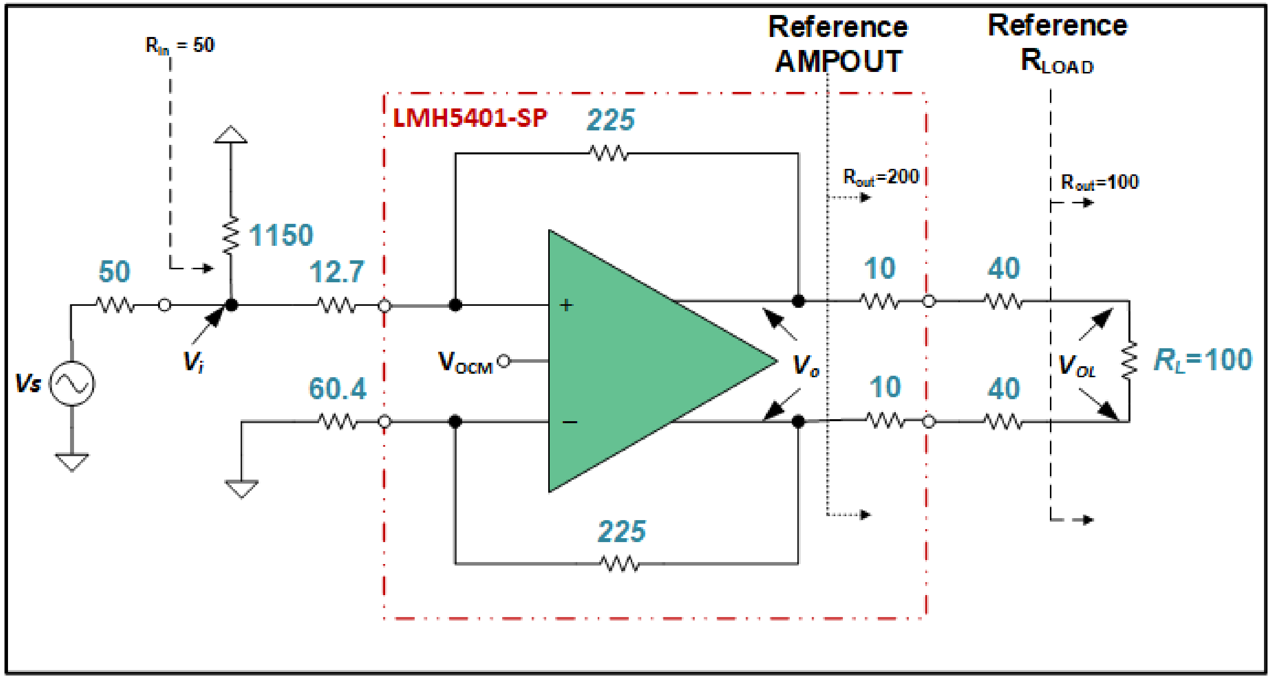
CALCULATED Solution	Value	Units
Voltage Gain, Gv (V/V)	7.114	V/V
Voltage Gain, Gv (dB)	17.043	dB
Realizable Rf*	200.0	ohms
Realizable Rt	1150.0	ohms
Realizable Rg1	12.7	ohms
Realizable Rg2	60.4	ohms
Zin (looking into Rt)	49.8	ohms
Noise Gain, G_N	4.725	V/V

Example Circuit showing naming Convention



- **Calculator solves for voltage gain at AMPOUT node, node internal to device inside series 10 ohms on each output. Aligns with datasheet specifications.**

Power gain, voltage gain and reference plane



Reference AMPOUT

$$G_V = V_o/V_i = 7.1\ \mathrm{V/V} = 17dB \quad (1)$$

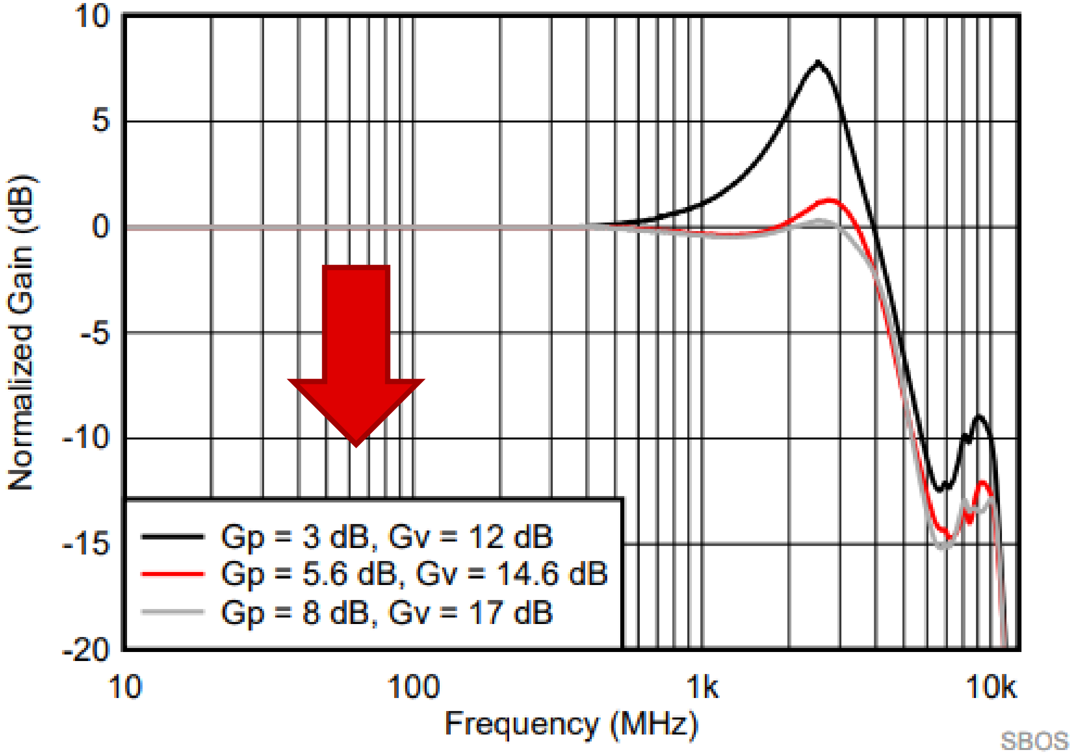
$$G_P = \frac{P_o}{P_i} = G_V + 10\log\left(\frac{\mathrm{R_{in}}}{\mathrm{R_{out}}}\right) = 11dB \quad (2)$$

Reference R_{LOAD}

$$G_V = \frac{V_{OL}}{V_i} = \frac{V_O}{2 * V_i} = 3.55\ \mathrm{V/V} = 11dB \quad (3)$$

$$G_P = \frac{P_{OL}}{P_i} = G_V + 10\log\left(\frac{\mathrm{R_{in}}}{\mathrm{R_{LOAD}}}\right) = 8dB \quad (4)$$

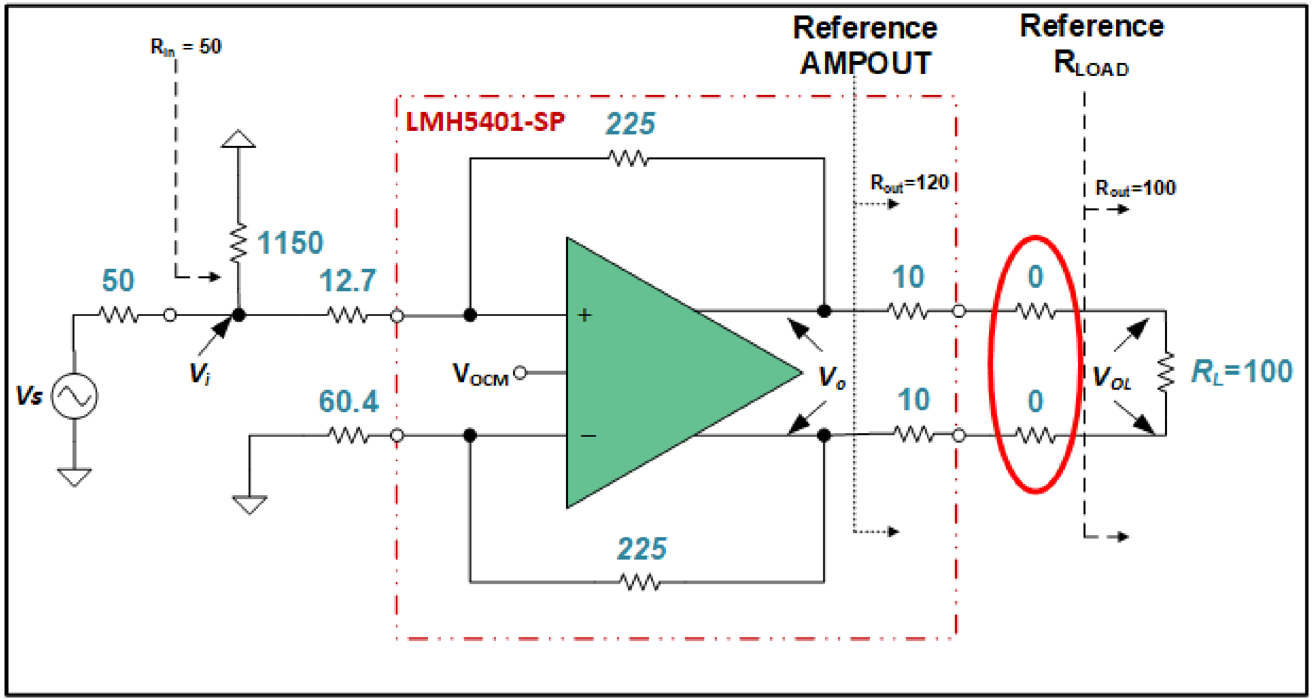
Power gain, voltage gain and reference plane



SE-DE Small Signal Frequency Response vs Gain

- **Frequency response normalized to 0dB**
- **Both power gain, G_P, and voltage gain, G_V shown in legend**
- **Power gain assumes matched input and output impedance.**

Unmatched load impedance

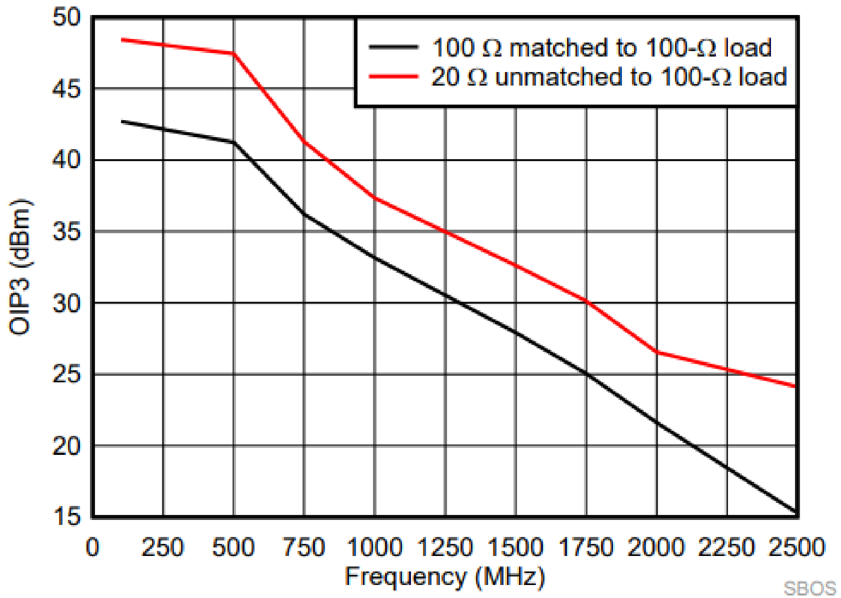


Unmatched output increases 'voltage' efficiency

Matched Load: $V_{OL} = \left(\frac{100}{200}\right) \cdot V_O$ » $V_O = 2 \cdot V_{OL}$ 5

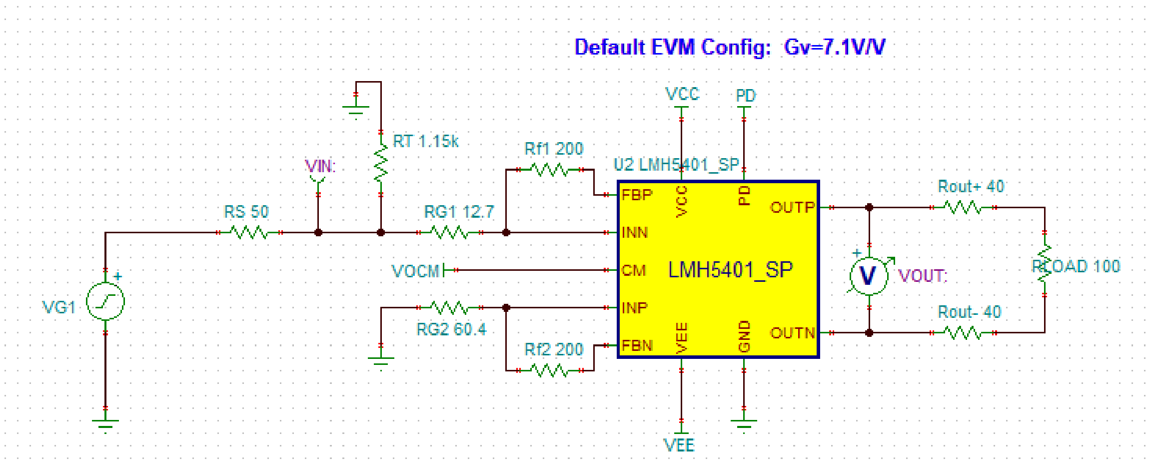
Unmatched Load: $V_{OL} = \left(\frac{100}{120}\right) \cdot V_O$ » $V_O = 1.2 \cdot V_{OL}$ 6

- **5dB improvement in OIP3 for same signal at load**

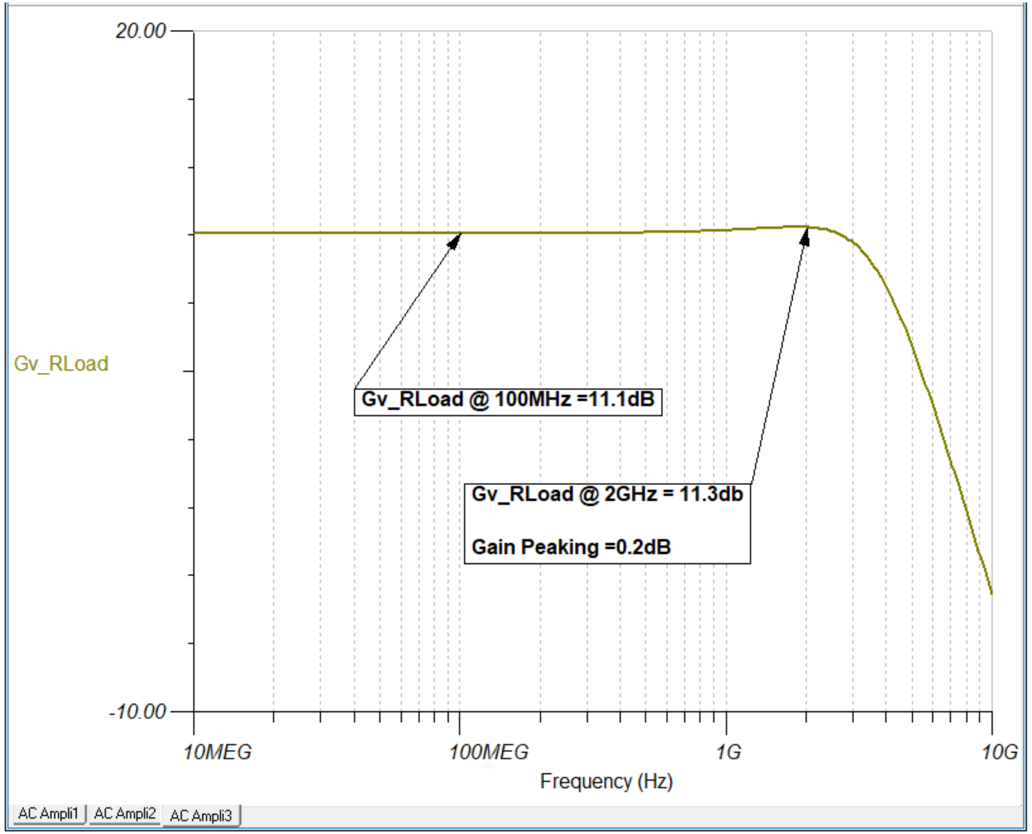


SE-DE Output 3rd Order Intercept Point

TINA simulation single-ended in to differential out



19	Realizable Rg2	60.4	ohms
20	Zin (looking into Rt)	49.8	ohms
21	Noise Gain, G_N	4.725	V/V



Low gain single-ended to differential input

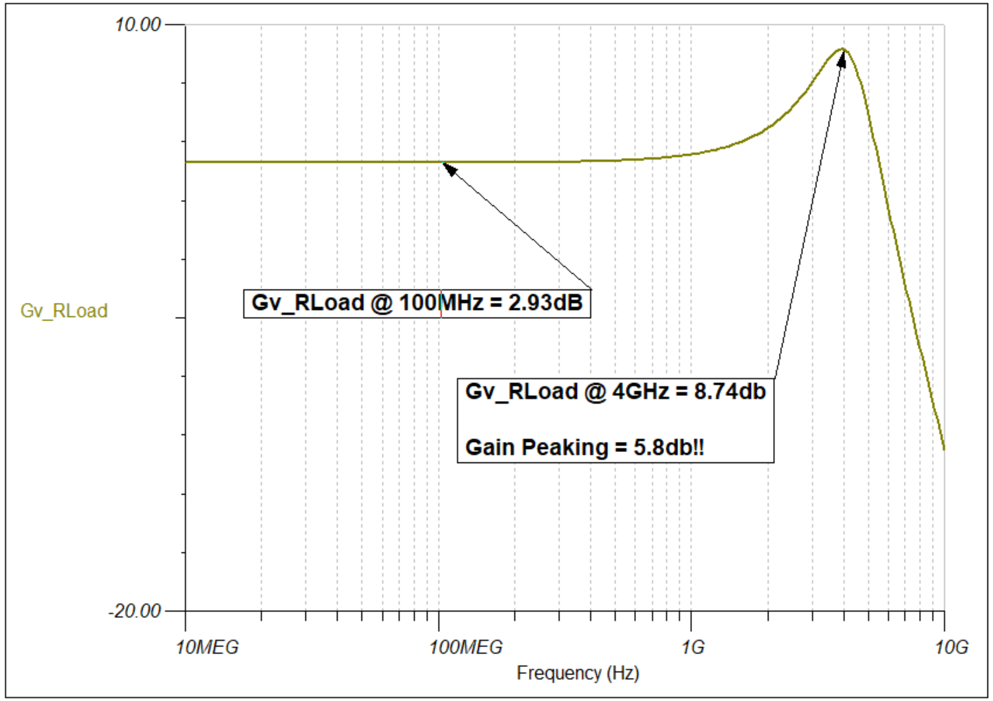
LMH5401-SP SE-DIFF CALCULATOR

Given Gv, Rs, and Rf, solve for Rt, Rg1, and Rg2 such that input impedance is matched in single-ended input to differential output configuration.

INPUT Parameter	Value	Units
Enter Target Voltage Gain, Gv (at AMPOUT	2.810	V/V
Enter Source Impedance, Rs	50	ohms
Enter Target Feedback Resistance, Rf	225	ohms

CALCULATED Solution	Value	Units
Voltage Gain, Gv (V/V)	2.793	V/V
Voltage Gain, Gv (dB)	8.922	dB
Realizable Rf*	200.0	ohms
Realizable Rt	84.5	ohms
Realizable Rg1	69.8	ohms
Realizable Rg2	100.0	ohms
Zin (looking into Rt)	50.0	ohms
Noise Gain, G_N	3.250	V/V

- **Design for 0dB power gain from source to load. (Gv_load = 3 dB, Gv_AMPOUT = 2.8 V/V = 9dB)**



FDA Stability

Barkhausen Stability Criterion

$$A_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta},$$ 1

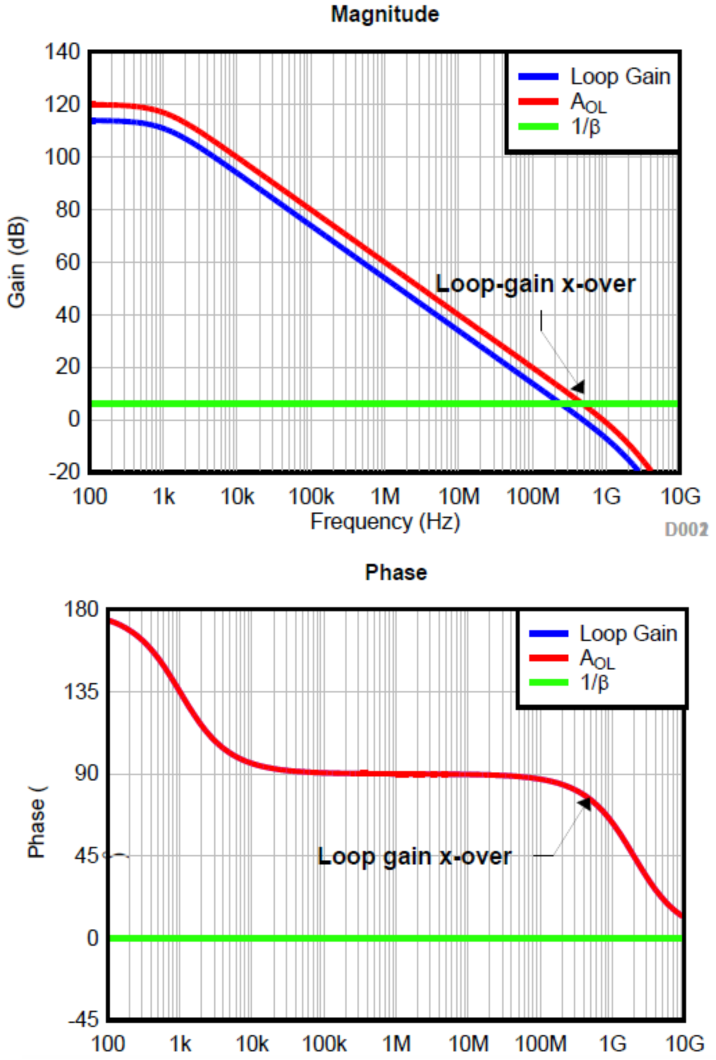
When $|A_{OL}\beta| = 1$, and phase shift around the loop is 180°,

$$A_{CL} = \frac{A_{OL}}{1-1} = \infty$$ 2

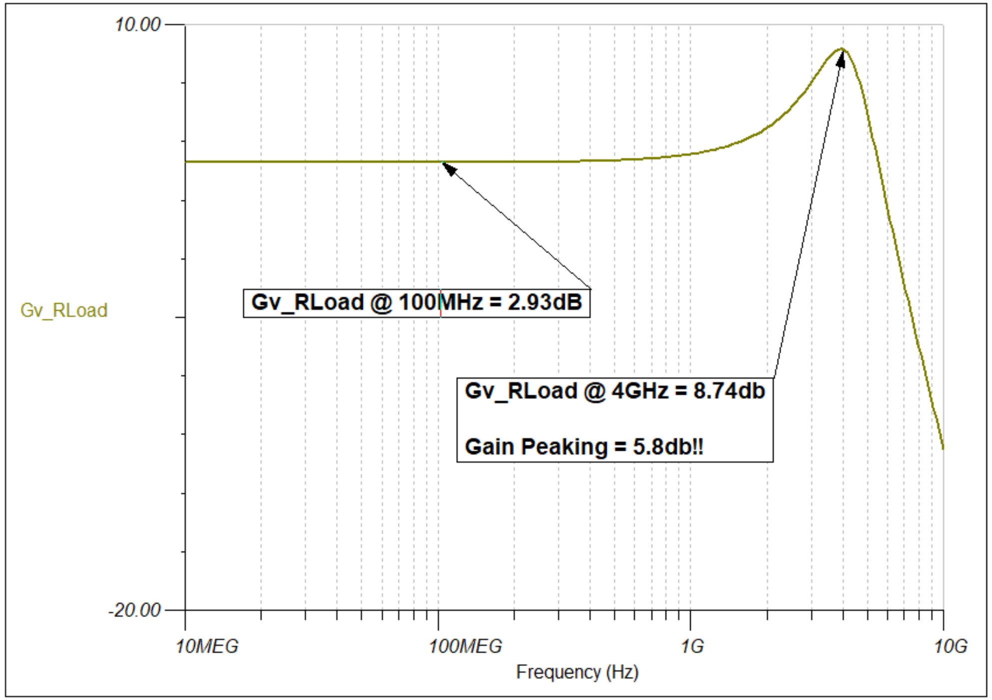
the denominator is unbounded and the system is unstable.

$$\text{Loop Gain} = A_{OL}\beta = \frac{A_{OL}}{\left(\frac{1}{\beta}\right)} = \left((A_{OL}) - \left(\frac{1}{\beta}\right)\right)_{dB}$$ 3

Loop Gain crossover occurs when $|A_{OL}\beta| = 1, \Rightarrow |A_{OL}| = \left|\frac{1}{\beta}\right|$ 4



Low gain single-ended to differential input

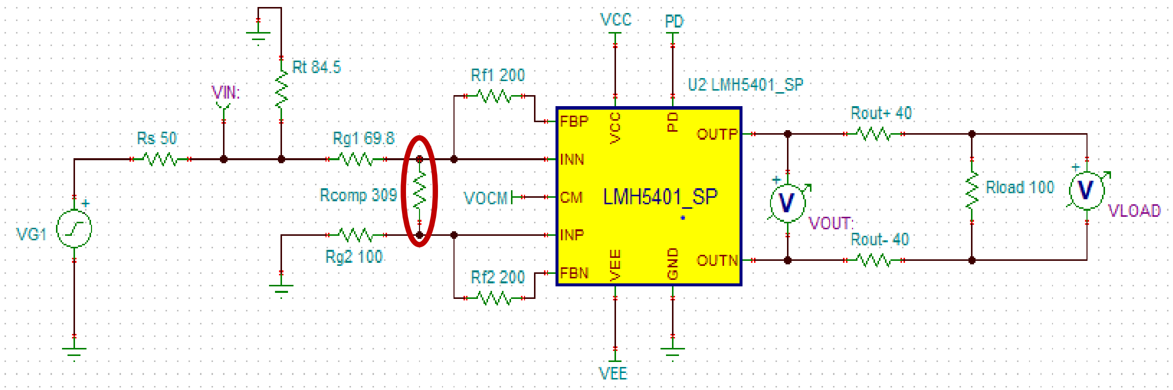


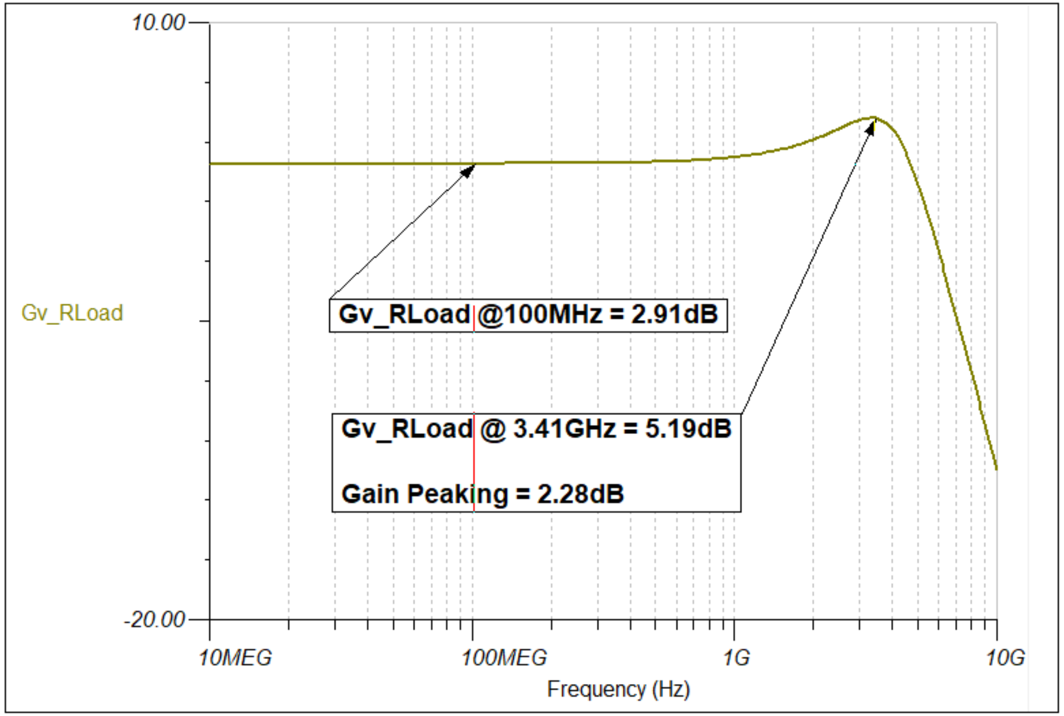
- **Design Targets:**
  - **Gp = 0dB**
  - **Gv_load = 3 dB**
  - **Gv_AMPOUT = 9.0 dB**
  - **Gv_AMPOUT = 2.8 V/V**
- **Simulated Results:**
  - **Gp = -0.07dB**
  - **Gv_load = 2.93 dB**
  - **Gv_AMPOUT = 8.3dB**
  - **Gv_AMPOUT = 2.6 V/V**
  - **AC Peaking = 5.8 dB**

Noise gain compensation for low signal gains

72	Noise Gain, G_N	3.250	V/V	
73				
74				
75	Target Noise Gain, G_N	4.725	V/V	<=
76	Rcomp_calculated	305.085	ohms	301
77	Rcomp_actual (closest 1% value)	309	ohms	309

$$G_N = 1 + \frac{R_f}{R_{g2} \,||\, \frac{R_{comp}}{2}}$$





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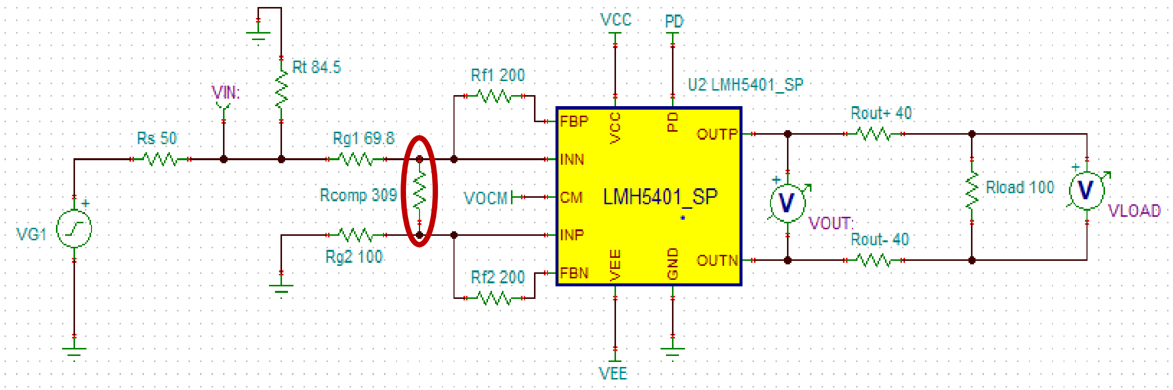
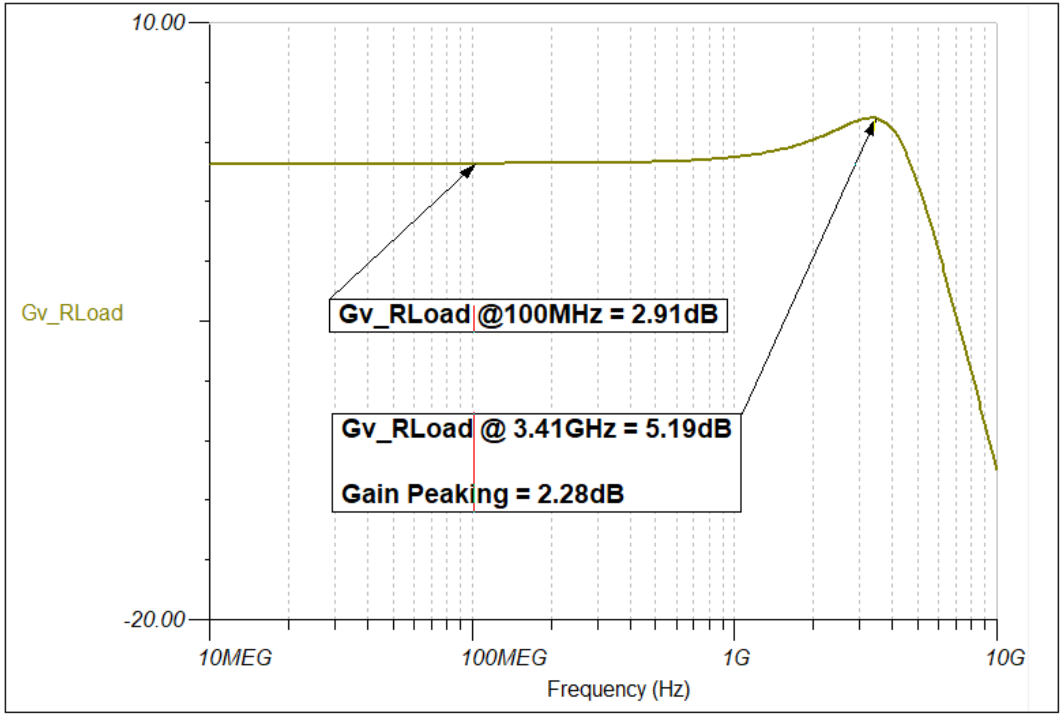
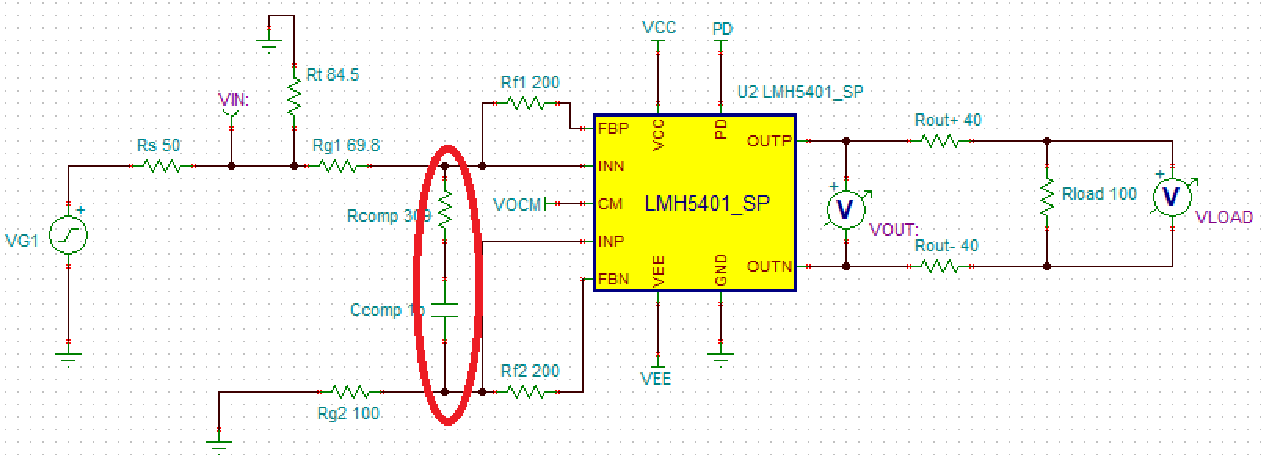


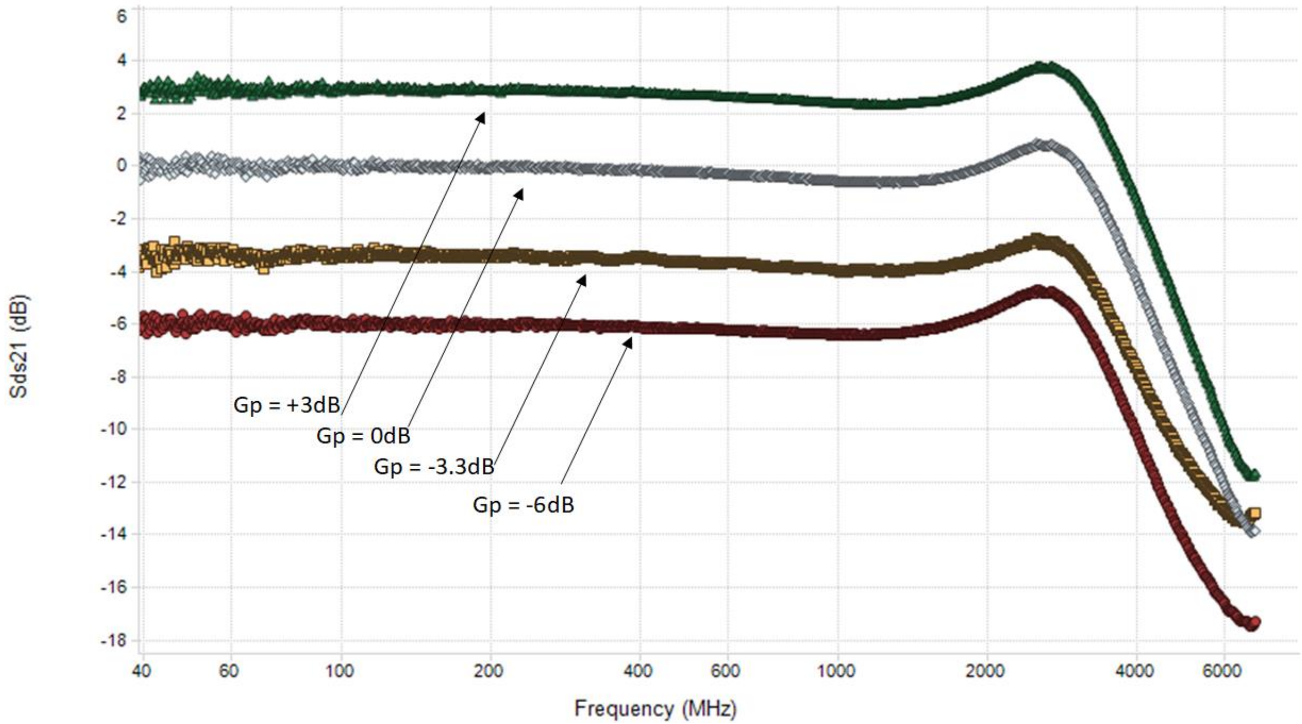


Noise shaping for improved stability



- **Shunt C can be added in series with resistor to shape noise**
- **At low frequencies capacitor is open, noise gain is unaffected (remains low) where stability is not a problem**
- **At higher frequencies, capacitor shorts presenting shunt path to circuit and increasing noise gain, thus, decreasing AC gain peaking.**

Low gain single-ended to differential freq. response



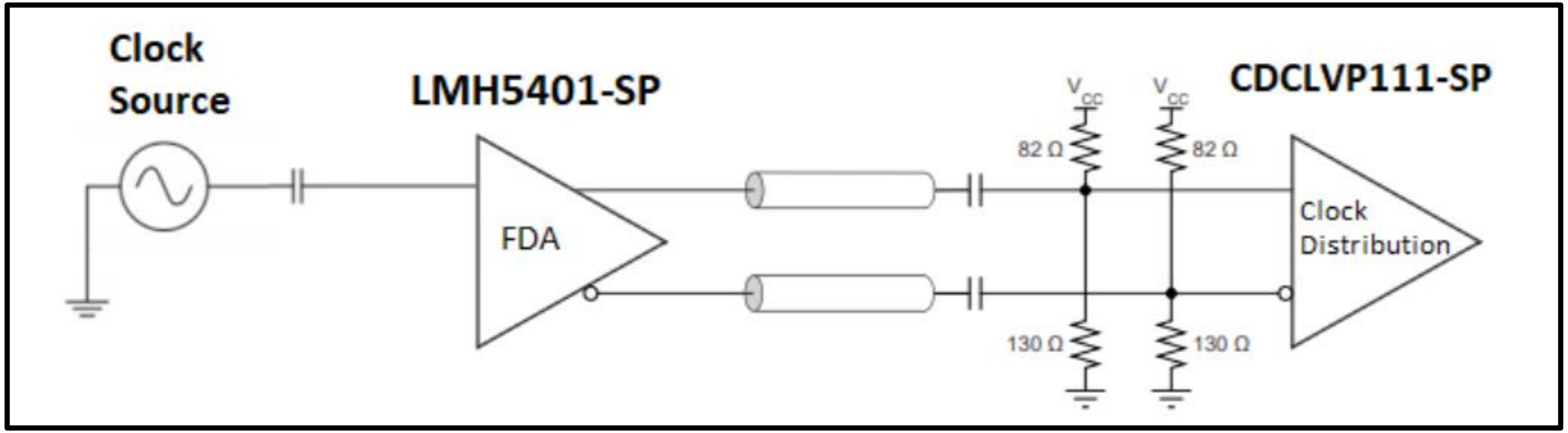
- **Sds21 is:**
  - **S-parameter measurement using vector network analyzer instrument**
  - **Power gain**

- **Optimal noise gain compensation resistor determined for each signal gain curve**

G_P (dB)	$G_{VAMPOUT}$ (dB)	AC Peaking (dB)	3DB_BW (MHz)	G_N (V/V)
3.0	12.0	0.84	3742	4.77
0.0	9.0	0.84	3706	4.76
-3.3	5.7	0.65	3670	5.07
-6.0	3.0	1.40	3670	4.74

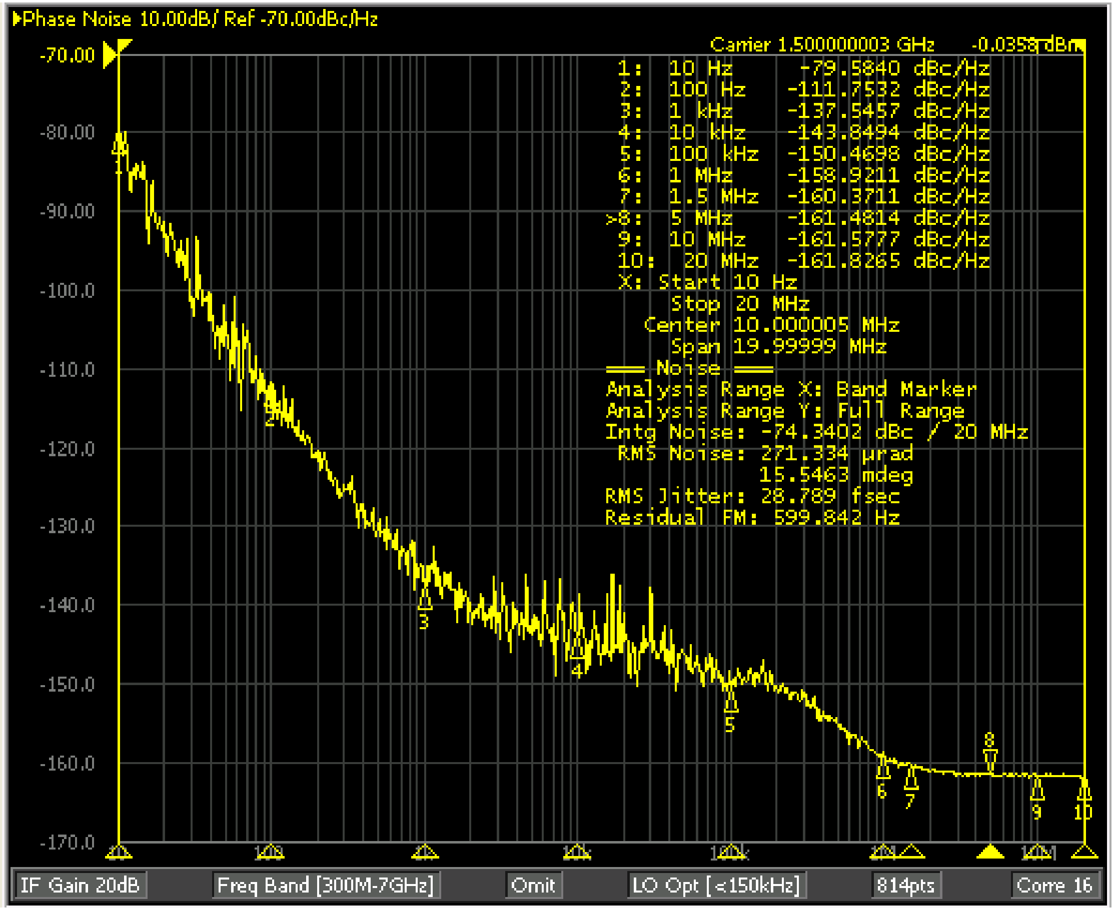
FDA used as a clock buffer

- FDA replaces balun where single ended clock source drives differential input of clock distributor
- Gain of FDA overcomes the challenge of balun insertion loss and transmission line losses where clock source and clock distribution device are not in close proximity
- Additive jitter of FDA minimal

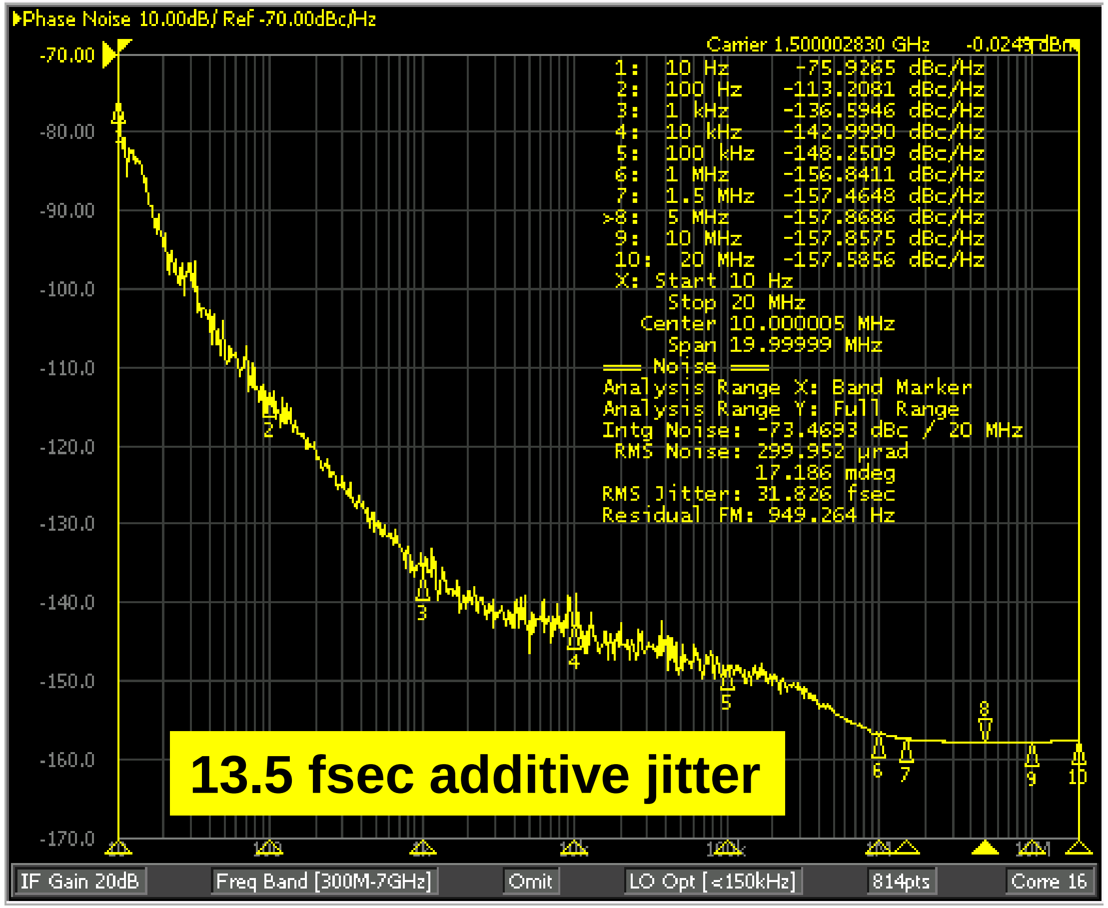


FDA used as a clock buffer

- **R&S SMA100B Signal Generator Phase Noise**
- **Integrated RMS jitter = 28.789 fsec at 1.5GHz**

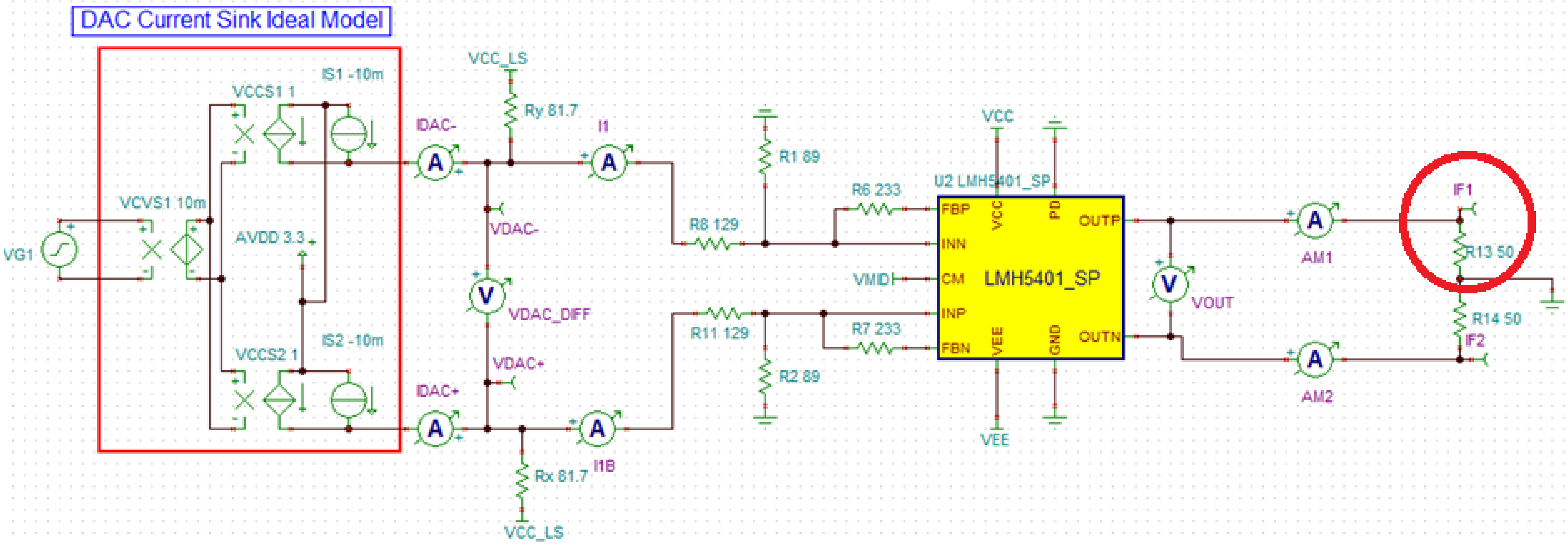


- **SMA100B + LMH5401-SP Phase Noise**
- **Integrated RMS jitter = 31.826 fsec at 1.5GHz**



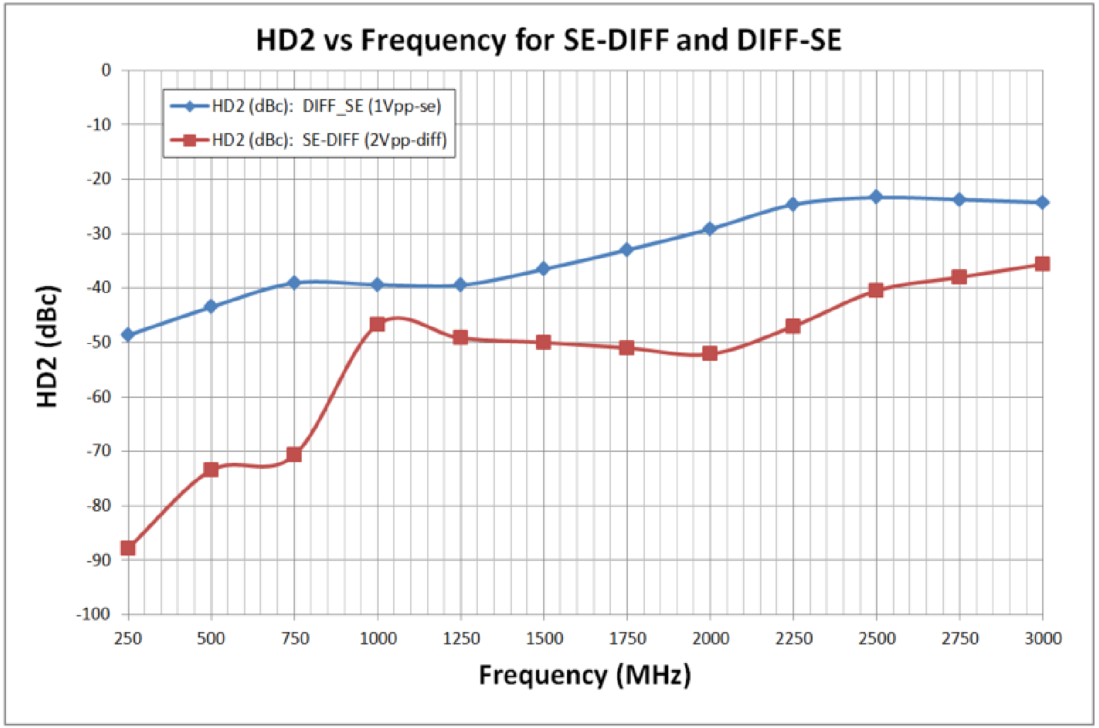
FDA used as a DAC buffer

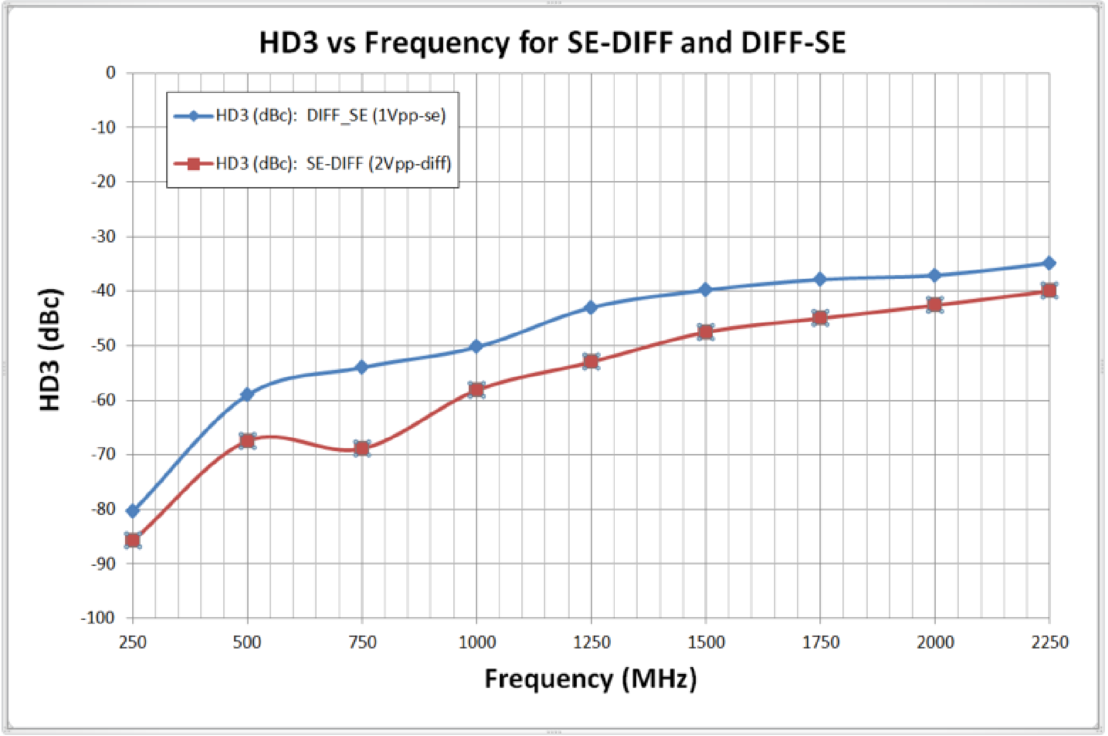
- **Spice model available to evaluate current sink DAC model (DAC5675A) driving LMH5401-SP**



FDA differential input to single-ended output

- **Using one output of FDA is feasible if HD2 and HD3 requirements are relaxed**



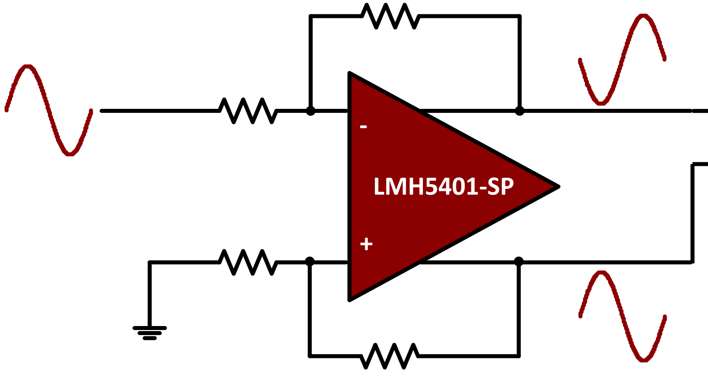


FDA used to level shift common mode

- [insert content]

TI devices referenced in this presentation

LMH5401-SP: 6.5GHz fully diff amp

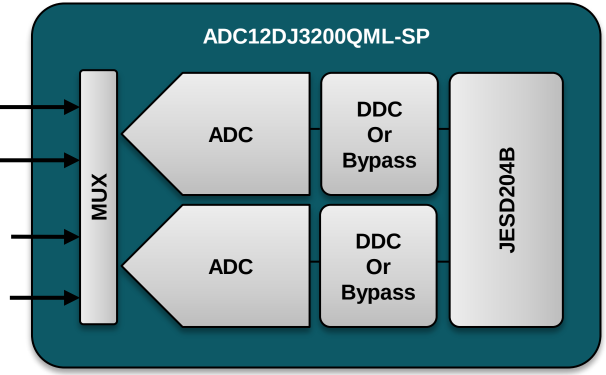


Key features

- TID: 100 krad SEL: 85 MeV-cm²/mg
- Gain-bandwidth: 6.5 GHz
- Balun upgrade for high speed ADC/DAC interface
- Suitable for signal gain, level shifting, clock buffer
- 14-pin leadless Ceramic (5.5mm x 6mm)

In production

ADC12DJ3200QML-SP: 3.2GSPS dual ADC

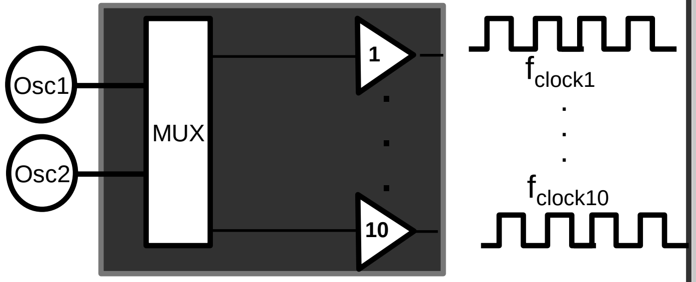


Key features

- TID: 300 krad SEL: 120 MeV-cm²/mg
- 12-bit, >7-GHz input bandwidth
- Dual 3.2-GSPS or single 6.4-GSPS
- Up to 12.8-Gbps JESD204B serdes
- Optional DDC in dual mode
- Ceramic LGA package (15mm x 15mm)

In production

CDCLVP111-SP: 1:10 Clock Distributor



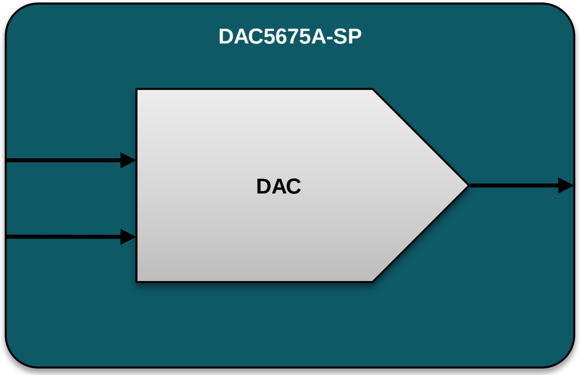
Key features

- TID: 75 krad SEL: 120 MeV-cm²/mg
- DC to 3 GHz output
- Selectable Input Clock
- Additive RMS jitter: 125 fsec typical @ 200MHz (10 kHz to 20 MHz)
- 36 pins CCFP (9mm x 9mm)

In production

TI devices referenced in this presentation

DAC5675A-SP: 14-bit, 400MSPS DAC



Key features

- SEL: 109 MeV-cm^2/mg
- 14-bit, 400 MSPS single DAC
- Ceramic QFP package (19mm x 10mm)

In production

Summary

- **Fully differential amplifiers are extremely flexible in their use case configurations**

- **A single FDA part number, such as the LMH5401-SP, that offers wideband operation and is space qualified with TID and SEE reports published, alleviates the challenge of procuring several unique devices for different signal chain needs.**

- **TI support is available to help you meet your design requirements. Please ask.**
  - **https://e2e.ti.com/support**

Resources

- TI Space Products Guide – Updated September, 2018
- New TI Aerospace & Defense Portal
- Radiation Handbook: Comprehensive radiation guide built using decades of knowledge from across TI's expert teams
- LMH5401-SP Tools
  - LMH5401-SP Spice Model
  - LMH5401-SP: Single-ended to Differential Circuit Design Calculator
- Content References
  - TI Precision Labs Training – FDAs
  - Analysis of fully differential amplifiers, Application note
  - Fully differential amplifiers, Application note
  - Input impedance matching with fully differential amplifiers, Application note
  - Output impedance matching with fully differential amplifiers, Application note
  - Using fully differential op amps as attenuators, Part 1, Application note
  - Using fully differential op amps as attenuators, Part 2, Application note
  - Using fully differential op amps as attenuators, Part 3, Application note
  - Stabilizing Differential Amplifiers as Attenuators, TI Design
  - How to use a fully differential amplifier as a level shifter, TI Blog

Online technical training from Texas Instruments

Coming up: Implementing high current applications using POL devices – March 20th, 2018
Learn about how to parallel Point of Load (POL) LDOs and DC-DC converters to help meet high current requirements. Register

Coming up: Understanding cosmic radiation effects on electronics – March 27th, 2018
During this webinar we will cover different radiation effects, how it impacts electronic circuits and compare space rated and commercial off the shelf (COTS) devices. Register

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Additional information

- ti.com/product/LMH5401-SP
- ti.com/product/THS4511-SP
- ti.com/product/THS4513-SP