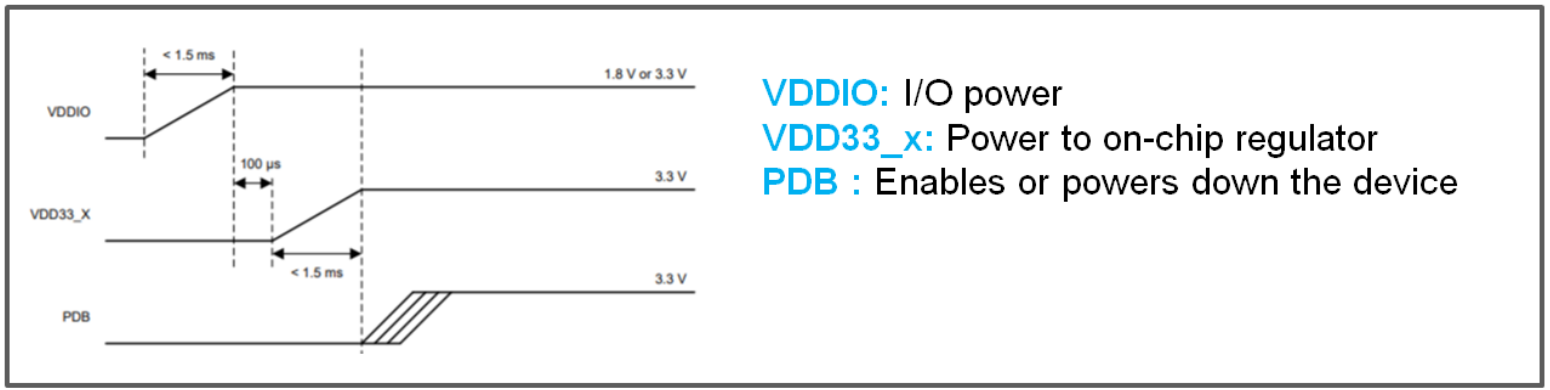
Power-up sequence for FPD-Link devices

- **All FPD-Link data sheets include a recommended power-up sequence.**
  - Power-up sequence ensures the circuit blocks are enabled in the expected sequence.
- **TI characterizes FPD-Link devices with the data sheet defined power-up sequence:**
  - This ensures proper operation.
  - Random behavior results when a device is operated beyond the data sheet spec, which can differ from device to device.



VDDIO: I/O power
VDD33_x: Power to on-chip regulator
PDB : Enables or powers down the device

Example of possible system/device-level issues:

If the device is powered up using the incorrect power-up sequence that is not defined in the data sheet, the following issues may occur:

- Blank or flickering screen
- I^2C communication issue
- Device is in incorrect mode
- Data-bit errors
- PLL locks to the incorrect frequency
- Device starts in a random state for each PDB or power cycle
- Other system/device-level issues may also occur

The system-/device-level issues stated above can lead to the following:

- May not be able to replicate on TI bench when device is powered in the correct power-up sequence.
- Can lead to unstable device behavior, which may vary from device to device.
- Can permanently damage the device.

Example of power-up sequence: DS90UB926

Table of Contents

Example of power-up sequence: DS90UB926

10.1 Power Up Requirements and PDB Pin

When VDDIO and VDD33_X are powered separately, the VDDIO supply (1.8 V or 3.3 V) must ramp 100 µs before the other supply (VDD33_X) begins to ramp. If VDDIO is tied with VDD33_X, both supplies may ramp at the same time. The VDDs (VDD33_X and VDDIO) supply ramp must be faster than 1.5 ms with a monotonic rise. A large capacitor on the PDB pin is required to ensure PDB arrives after all the VDDs have settled to the recommended operating voltage. When PDB pin is pulled to VDDIO = 3 V to 3.6 V or VDD33_X, TI recommends using a 10-kΩ pullup and a > 10-µF capacitor to GND to delay the PDB input signal.

All inputs must not be driven until VDD33_X and VDDIO has reached its steady-state value.

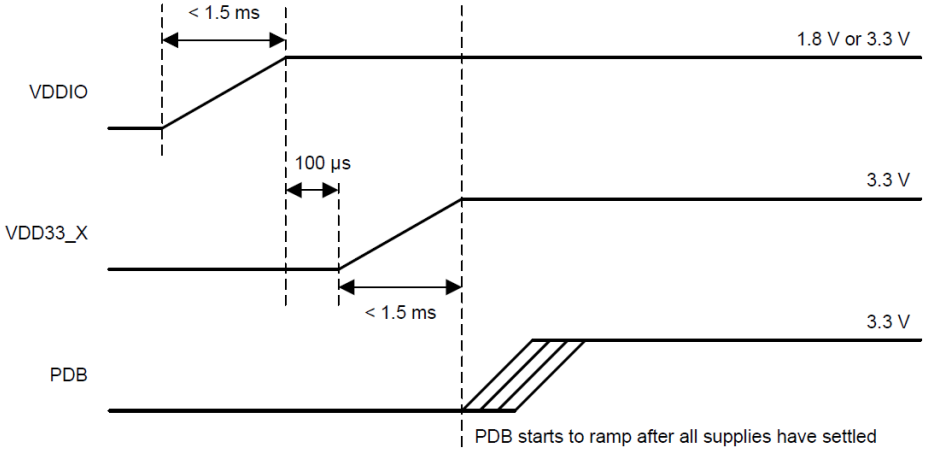


Figure 28. Power-Up Sequence of DS90UB926Q-Q1

Recommended equipment

Measurement example:

- Oscilloscope to measure the power-up sequence
- Need to probe the following signals to make sure the power-up sequence follow the data sheet power-up sequence

For the DS90UB926, the following can be checked:

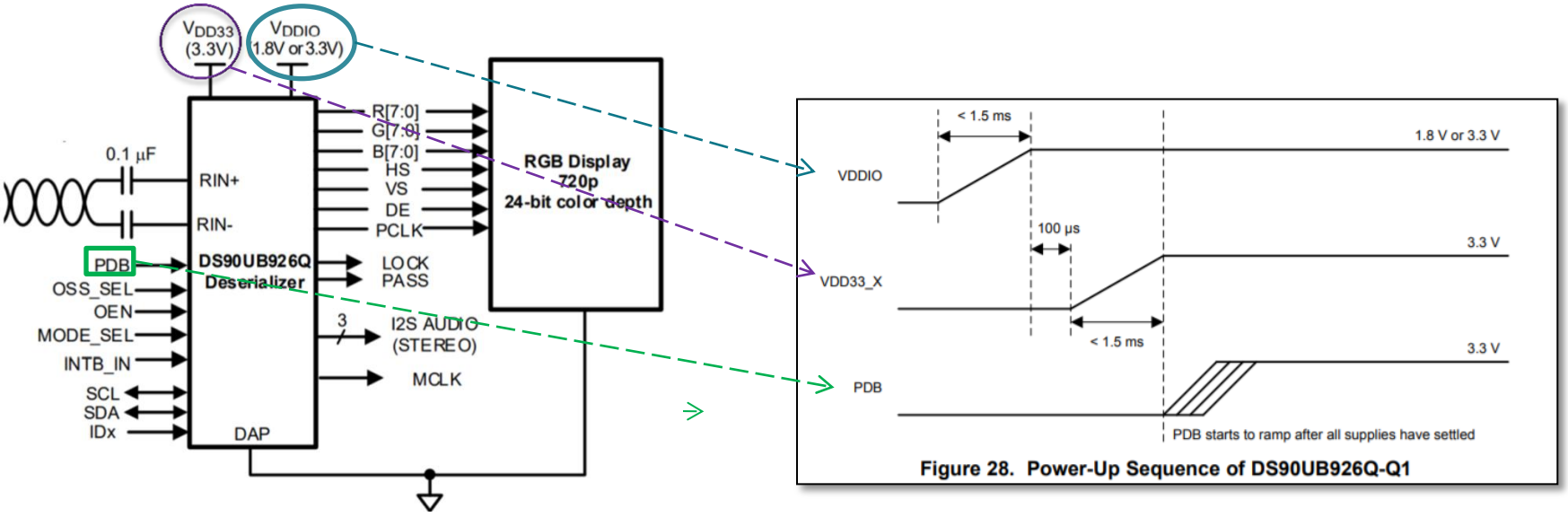
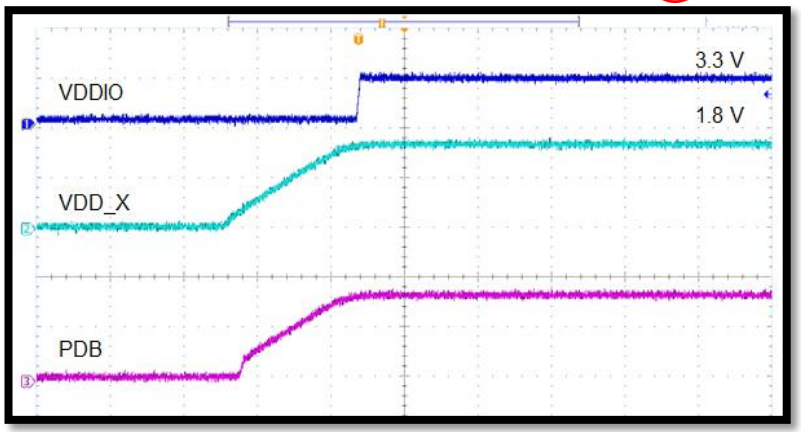


Figure 28. Power-Up Sequence of DS90UB926Q-Q1

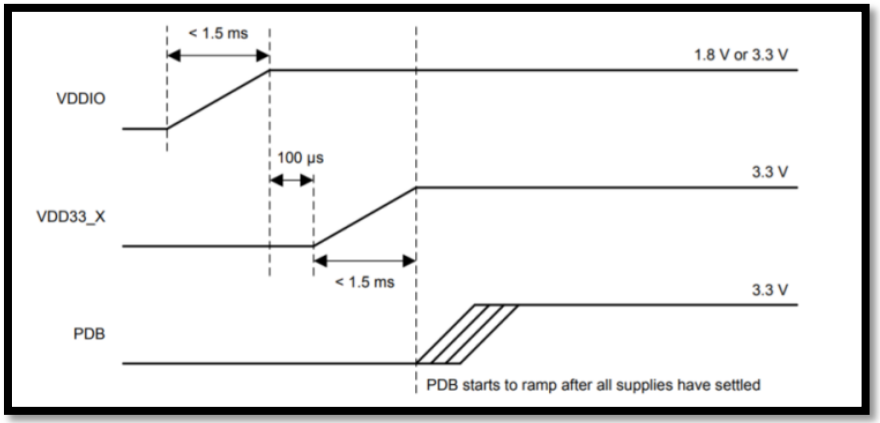
Example of incorrect power sequence

- When VDDs & PDB are powered separately:
  - The VDDIO supply must ramp 100 µs before the other supply (VDD33) begins to ramp.
  - A large capacitor on the PDB pin is required to ensure PDB arrives after all the VDDs have settled to the recommended operating voltage.
- When PDB pin is pulled to VDDIO or VDD33, TI recommends using a 10-kΩ pullup resistor and a > 10-µF capacitor to GND to delay the PDB input signal.

Incorrect power-up sequence



Data sheet power-up sequence



Example of incorrect power sequence

- If VDDIO is tied with VDD33_X, both supplies may ramp at the same time:
  - The VDDs (VDD33_X and VDDIO) supply ramp must be faster than **1.5 mS** with a monotonic rise.
- In the example below, the VDDs are tied together and ramp time is **62 mS**
  - This power sequence can lead to system/device level issues because it's not defined in the data sheet

Incorrect power-up sequence ✖