

Valley Switching Boost Power Factor Correction (PFC) Reference Design

C2000 Systems Solution: Digital Power

TIDM-1022: <http://www.ti.com/tool/TIDM-1022>

Detailed agenda

- Background:
 - Reference design feature
 - Valley switching application
 - Type-4 PWM-based valley switching control
- System configuration
 - Hardware modification
 - Peripheral usages
 - Control diagram
 - Software structure
- Technical challenges
- Waveforms and test results

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TIDM-1022: Valley switching boost PFC

Features

- Interleaved, 750W, two-phase boost PFC stage
- Full range parameter: 95~260 Vrms, 47~63Hz, 750W
- 200kHz switching frequency under normal condition (load > 10%)
- 150~330kHz variable Pulse Width Modulation (PWM) switching under light load (<10%)
- Programmable output voltage, 380-V DC output nominal
- Low Total Harmonic Distortion (THD): Close to 5% at 5% load
- High efficiency > 92% at 5% load
- powerSUITE™ support for easy adaptation of design for user requirement
- Software Frequency Response Analyzer (SFRA) for quick measurement of open loop gain
- Full digital control using TI's Piccolo F280049 controller
- Protects for output overcurrent and overvoltage conditions
- Programmable valley switching and valley skipping

Applications

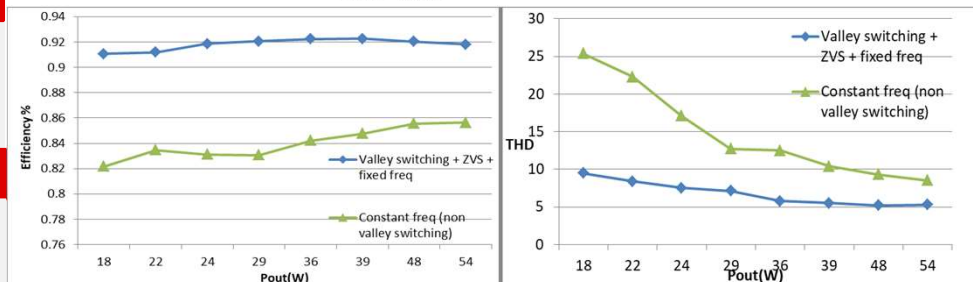
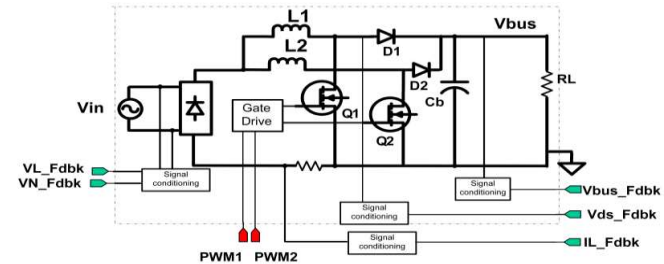
- Onboard chargers for Electronic Vehicles (EVs)
- Server and network power supplies
- Telecom rectifiers
- Industrial power supplies

Tools & Resources

- Key TI devices: TMS320F280049, OPA365, SN74LVC1G3157, TPS795, UCC27524

Benefits

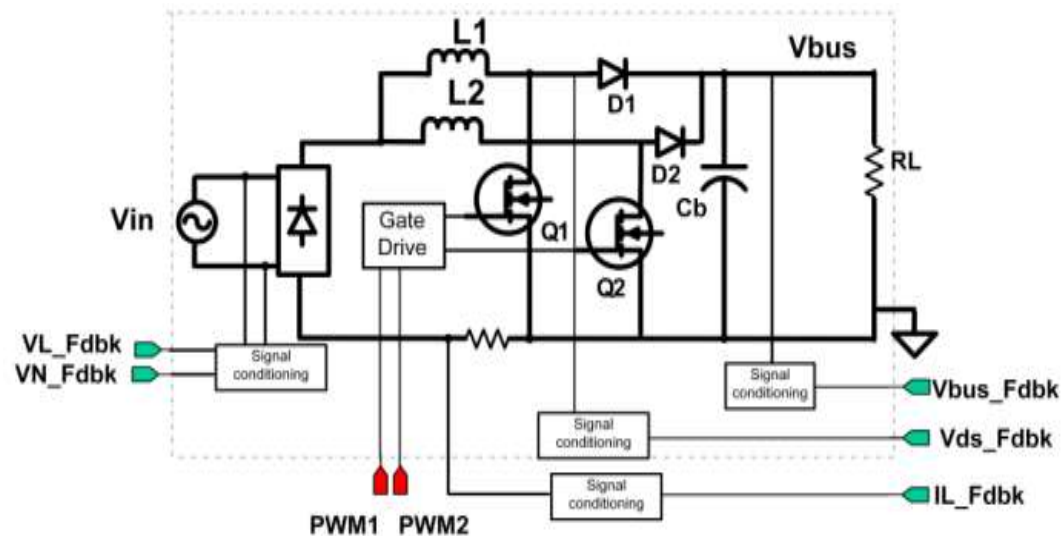
- High efficiency and low THD enabled under light load condition.
- Using latest type-4 PWM offers flexibility to implement valley switching and valley skipping.
- High-performance C2000 controller enables superior control and enables advanced control scheme to be implemented.
- powerSUITE support enables easy adaptation of software.
- CLA support enables better integration options.



Project background

2-phase Interleaved Power Factor Correction (ILPFC) converter:

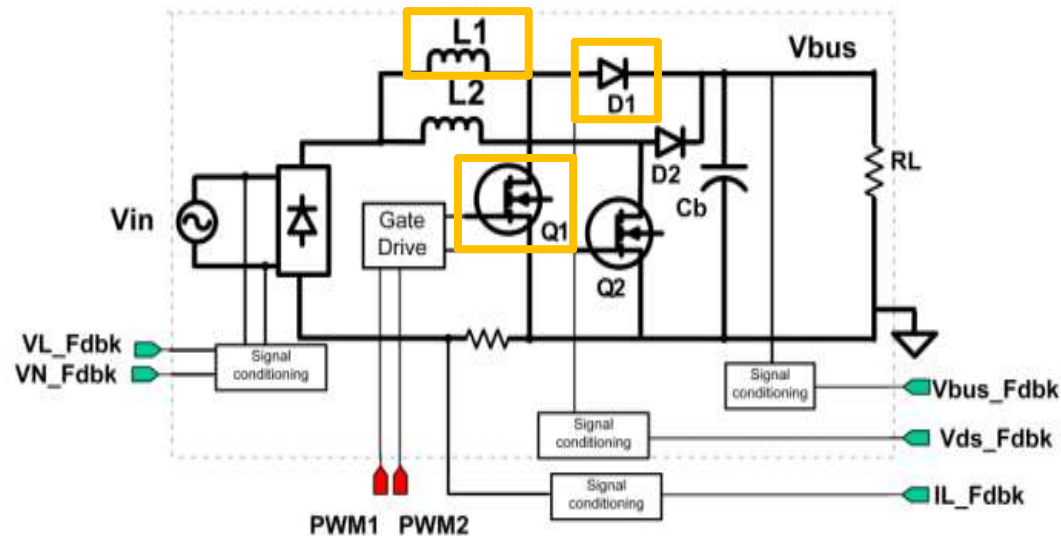
- The function of a PFC stage is to convert the AC voltage to a regulated DC bus voltage while drawing a sine wave input current in-phase with the AC input voltage.
- This is implemented using a bridge rectifier followed by a boost PFC stage.



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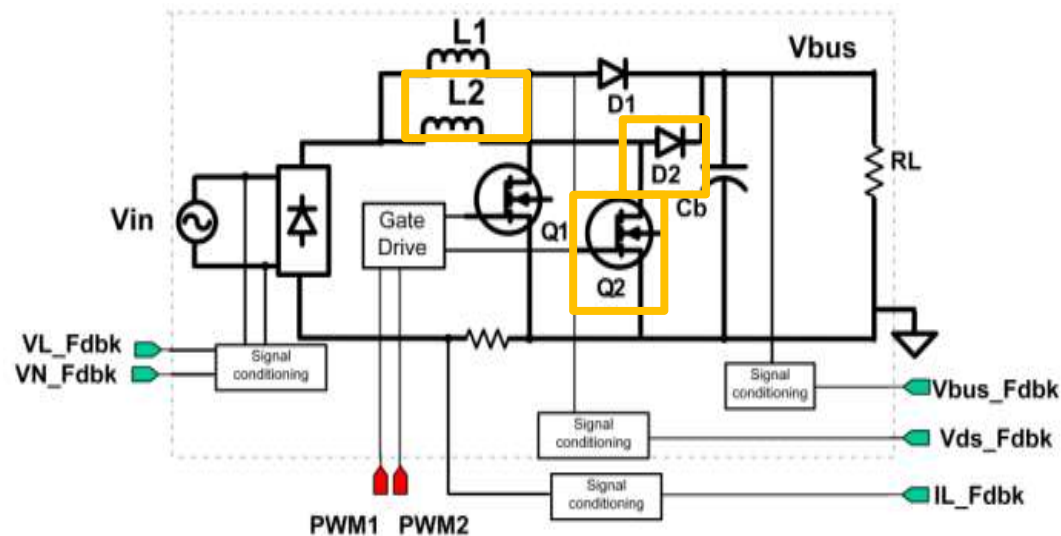
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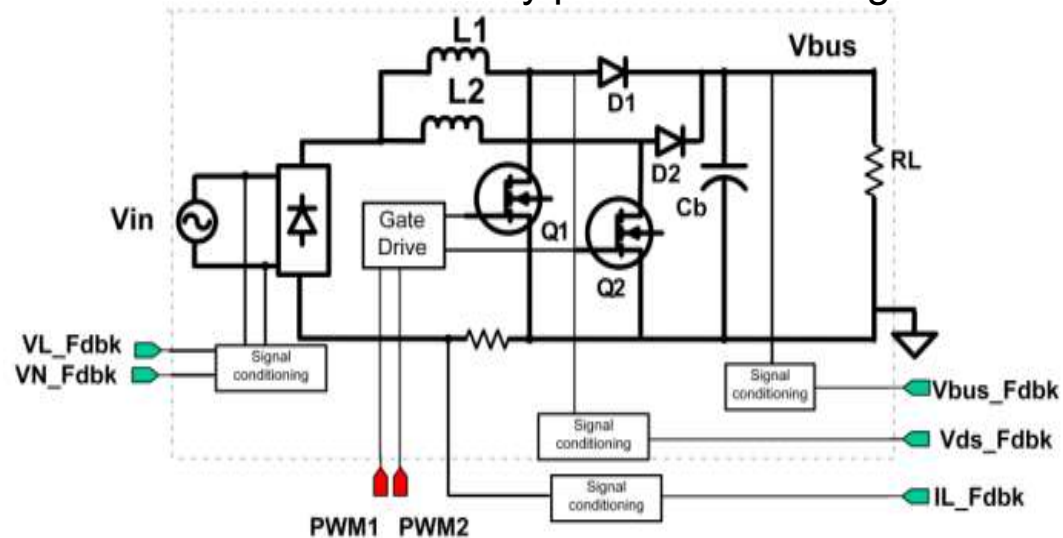
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Valley switching

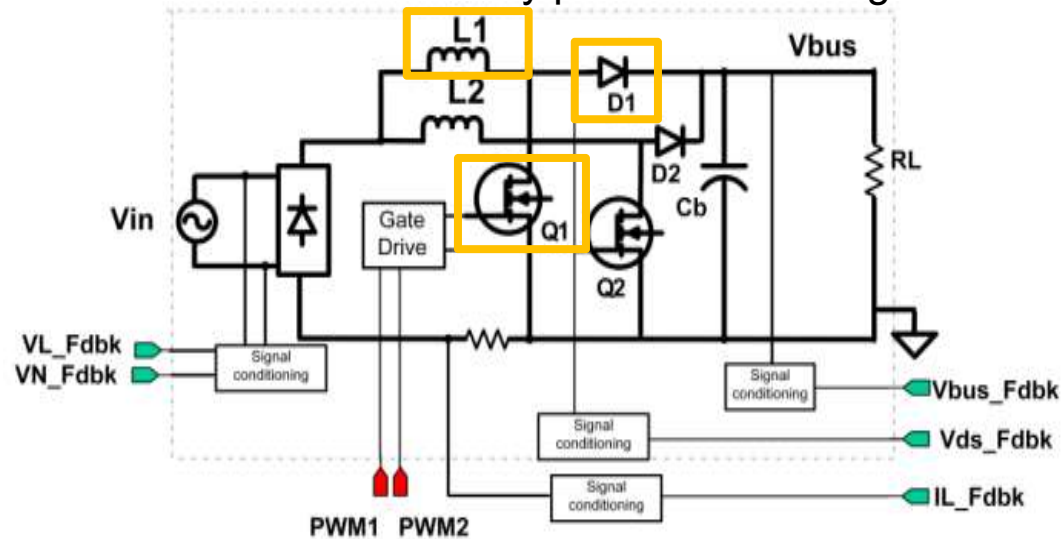
- Valley switching is a soft-switching technique, also called quasi-resonant switching.
- D1 reverse-biased, energy resonates between L1 and parasitic capacitor of Q1.
- Switch should be turned ON at the valley point of the voltage across it.



Project background

Valley switching

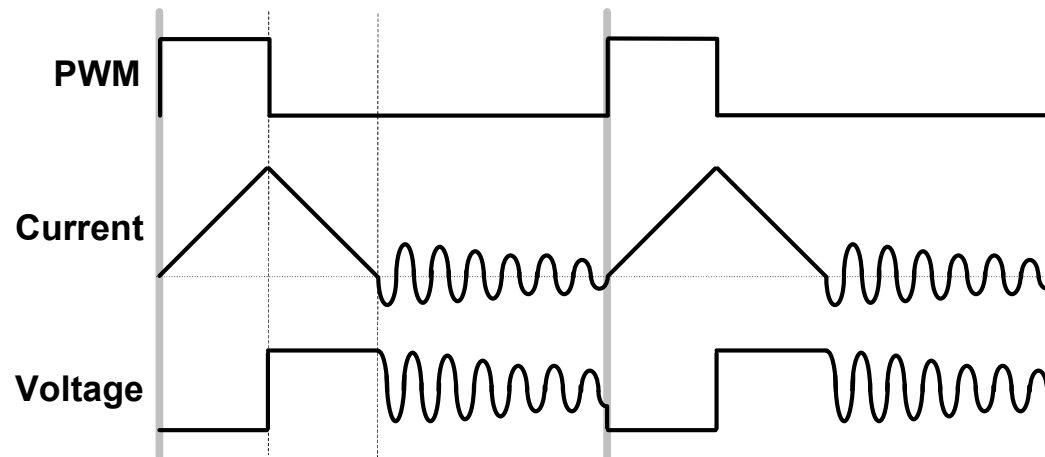
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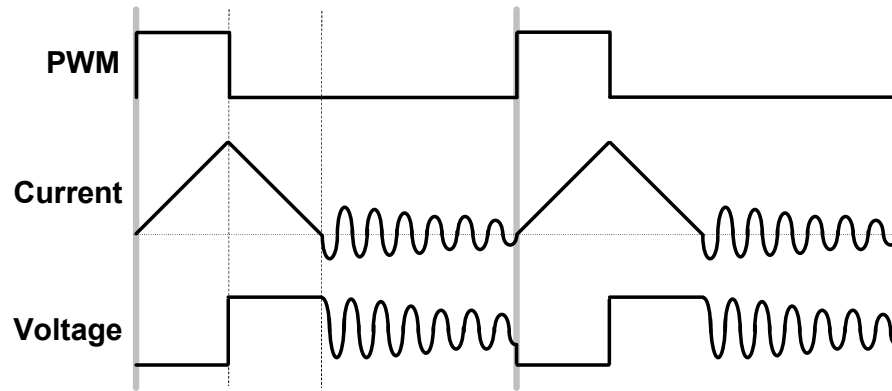
Project background

Valley-switching with Type-4 PWM allows the following:

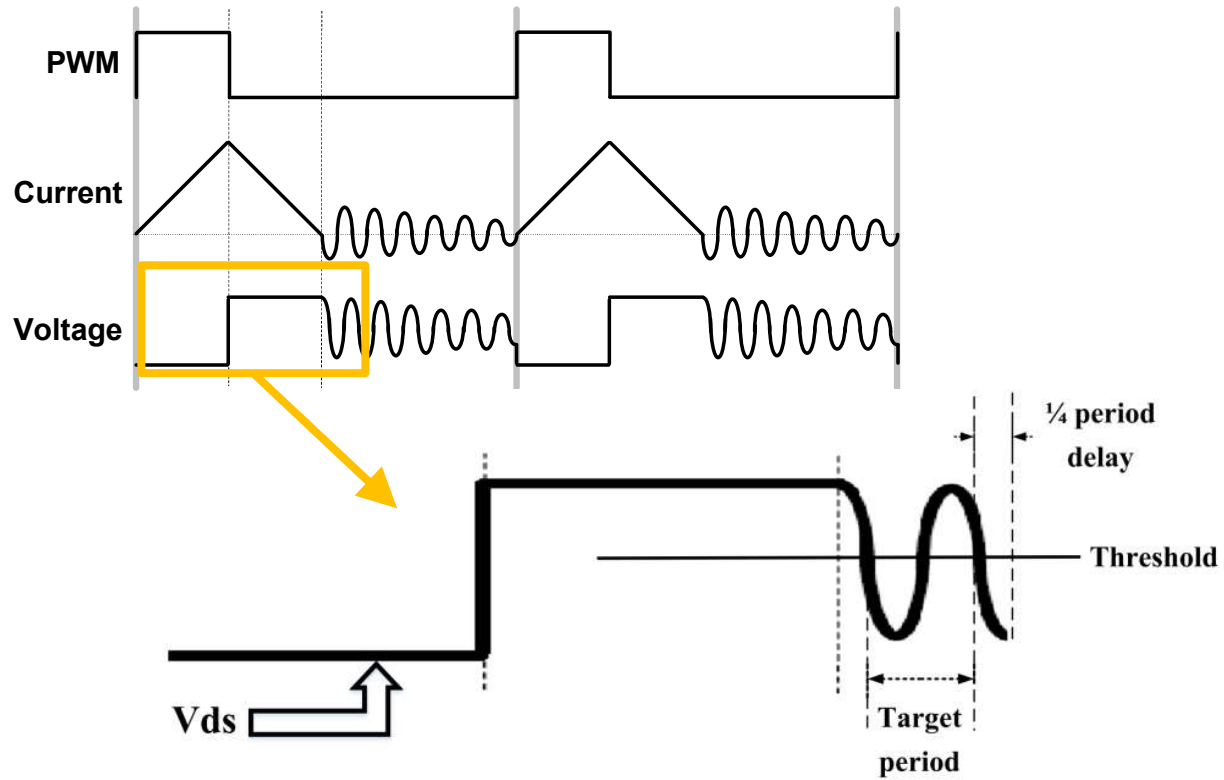
- Capture of the oscillation frequency/period
- Accurate delay of the PWM switching instant
- Programmable number of edges before the delay takes effect



Project background



Project background



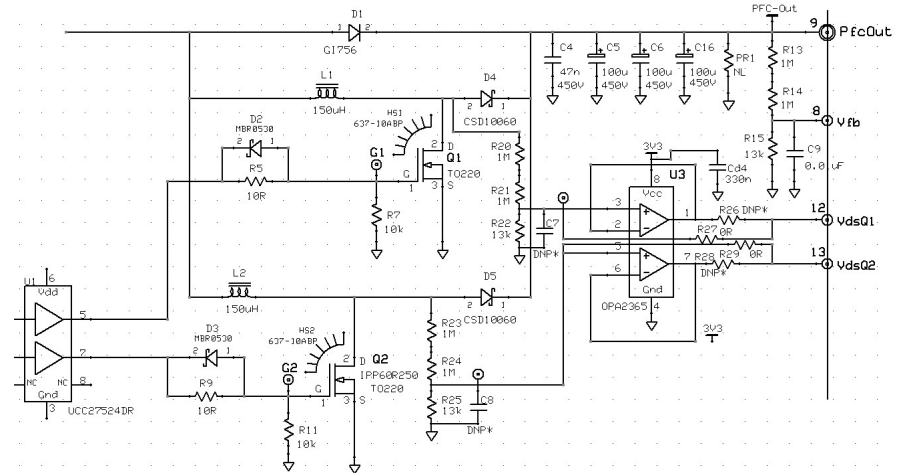
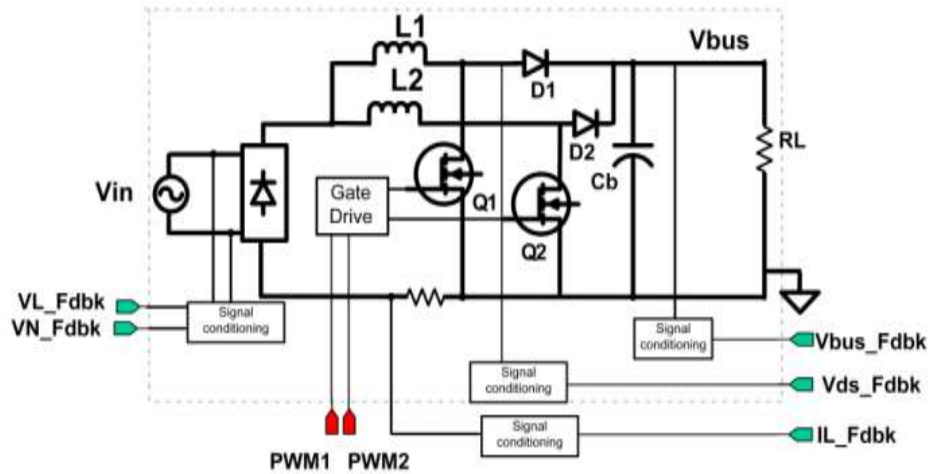
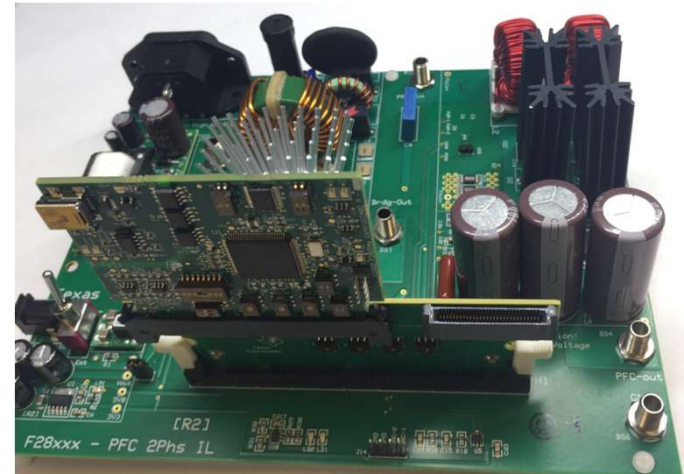
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System configuration

- Valley switching is based on a modified ILPFC board with an extra Vds sensing circuit
- Valley switching is enabled under light load condition with single phase.

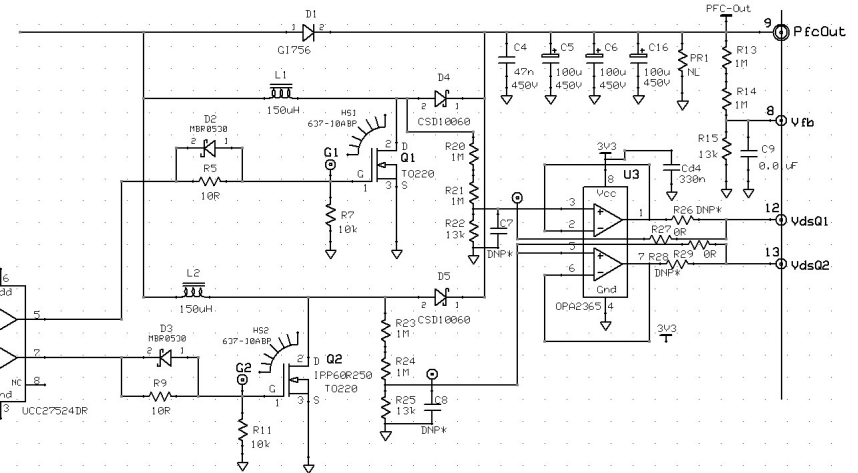
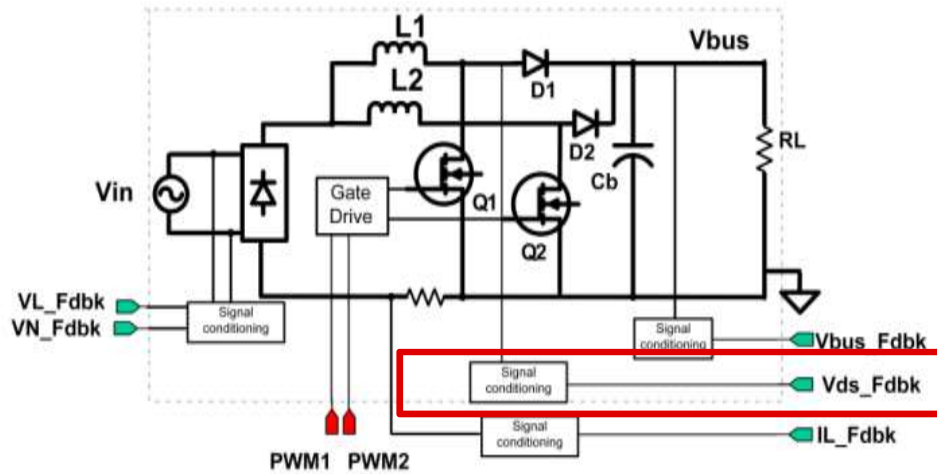
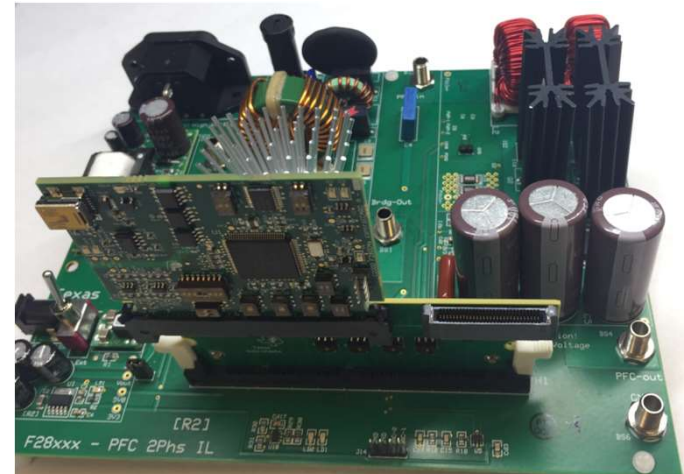
Note: Base board modifications can be found in Reference Design User Guide: <http://www.ti.com/lit/tidueg3>



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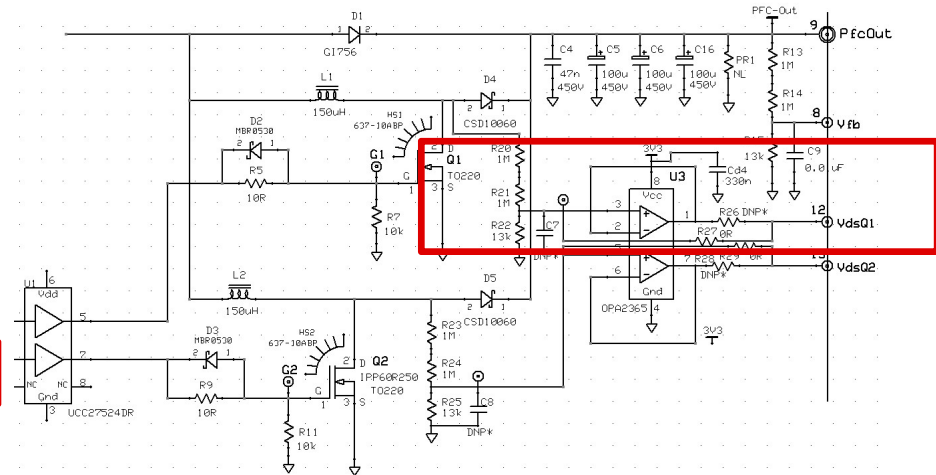
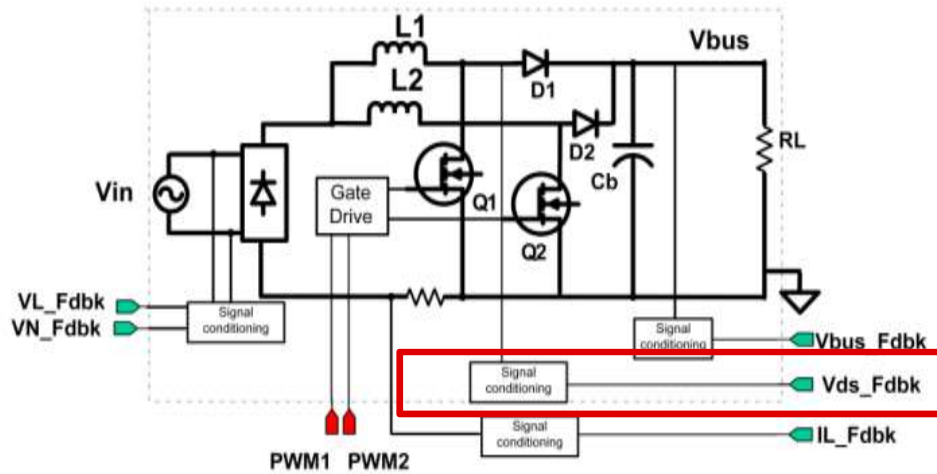
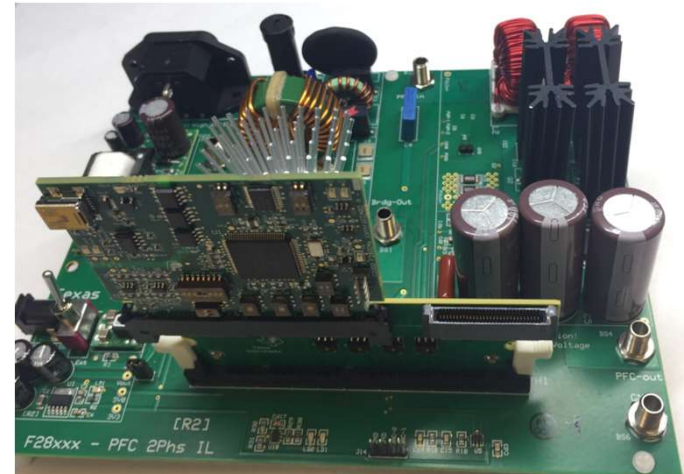
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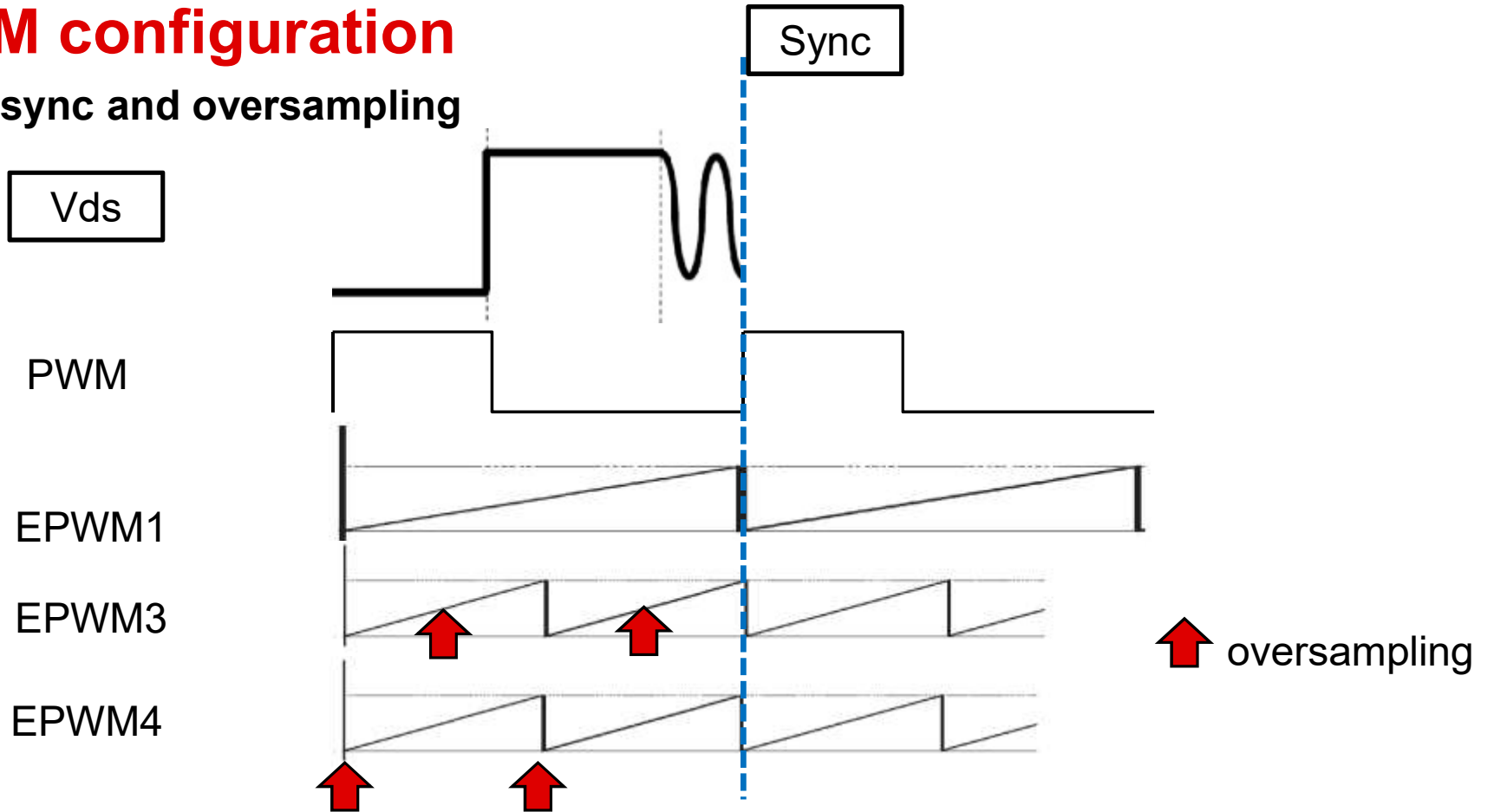


Peripheral usages



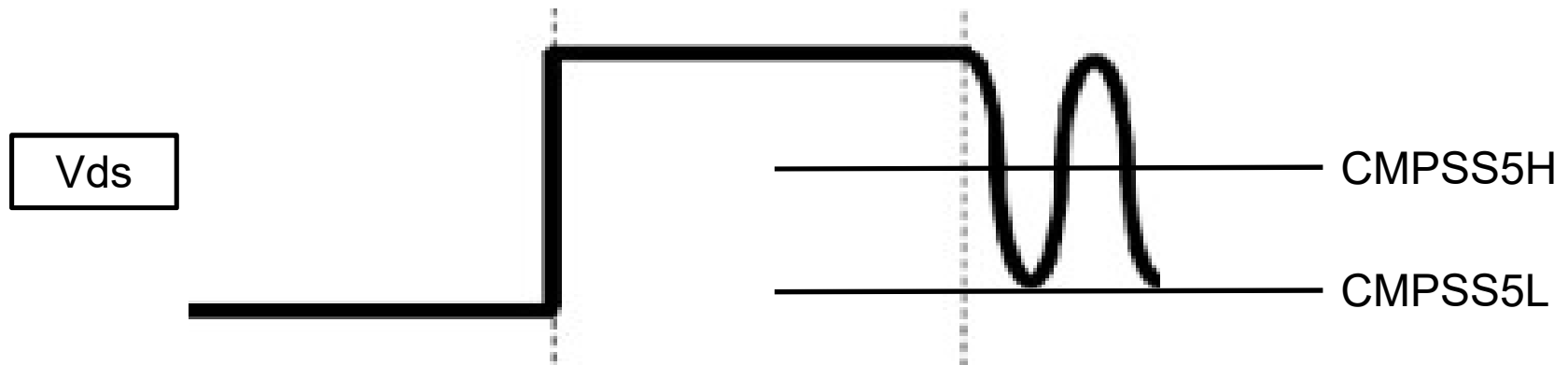
PWM configuration

PWM sync and oversampling

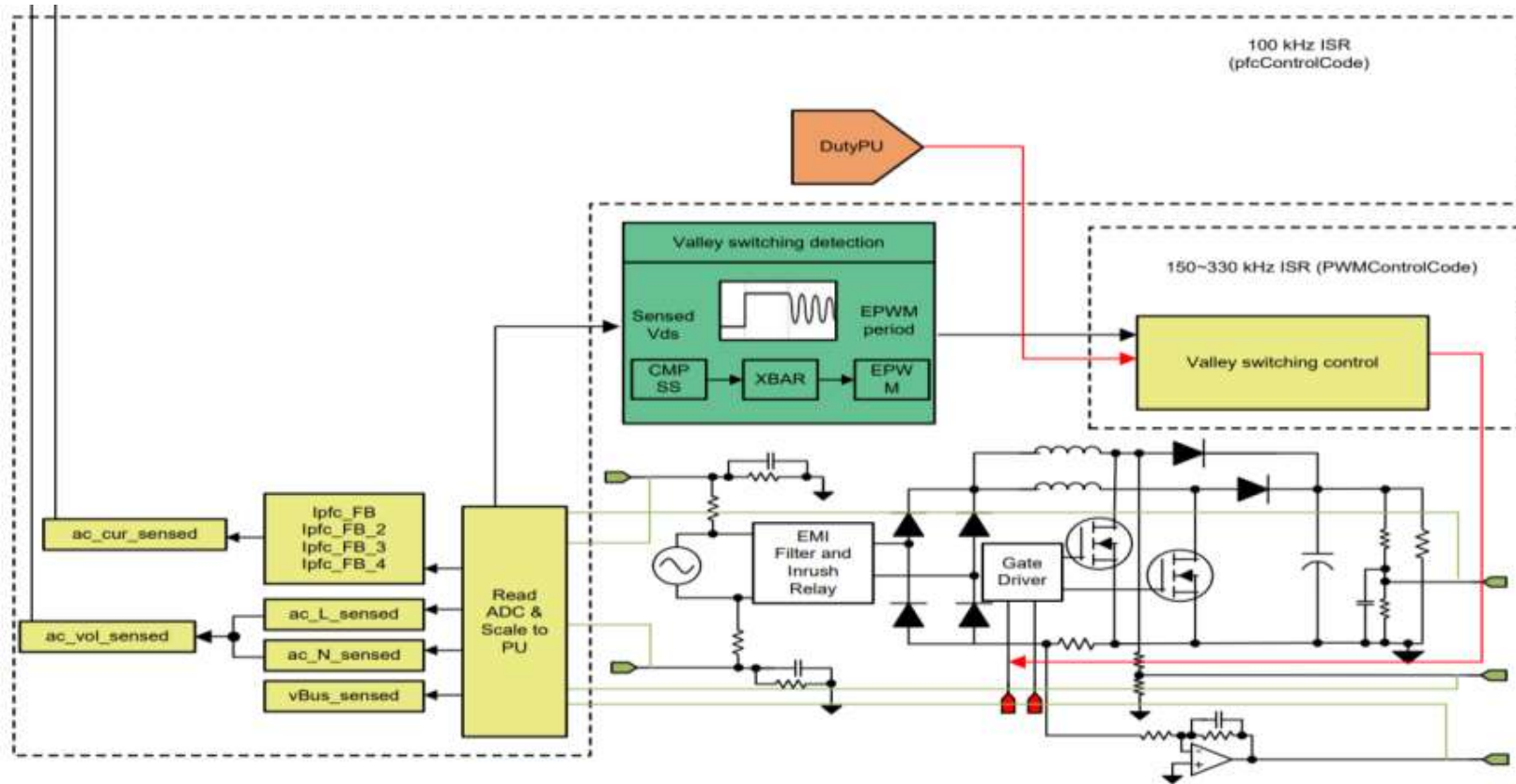


CMPSS configuration

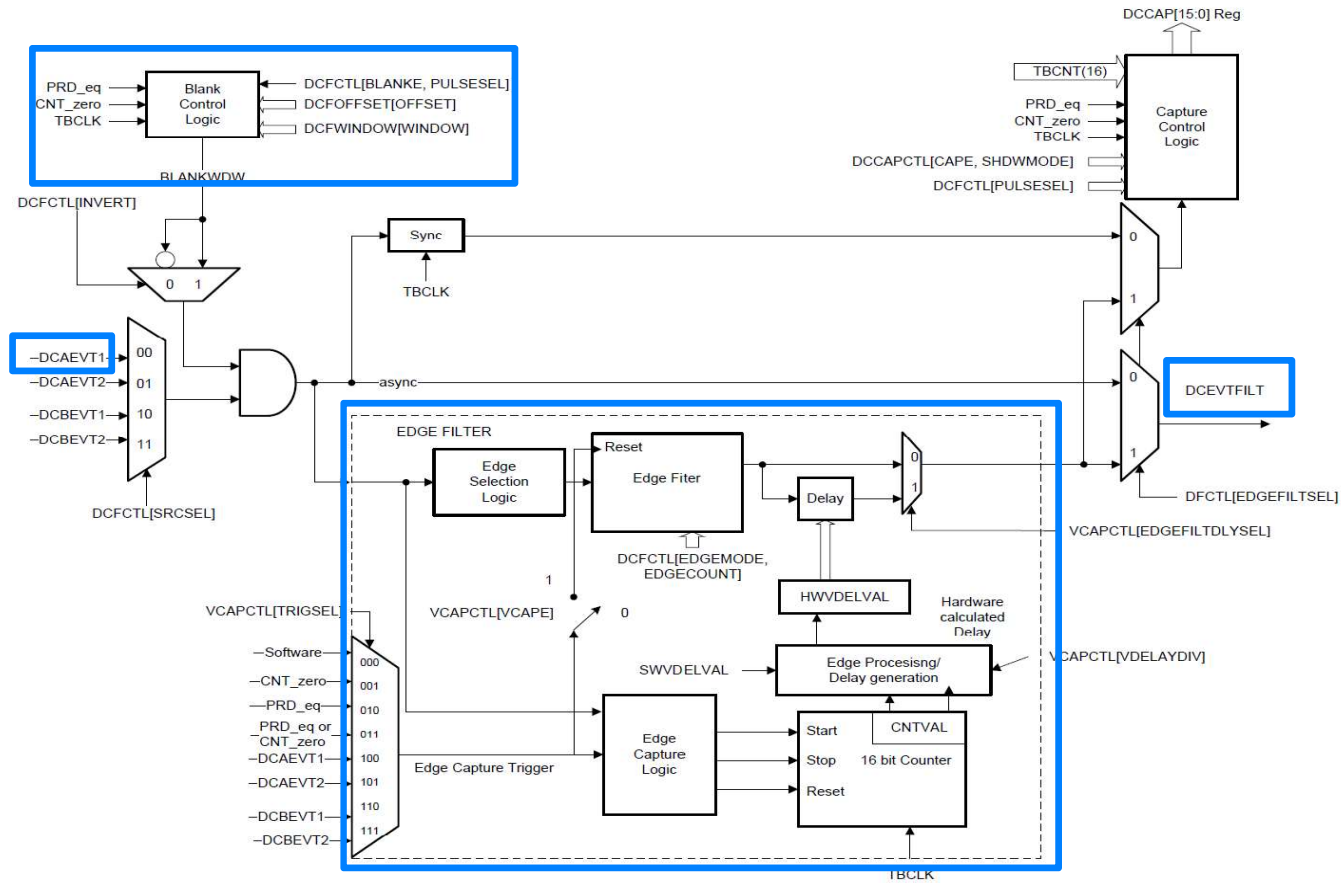
- CMPSS2H for current protection
- CMPSS5H for valley capture
- CMPSS5L ZVS or valley switching mode selection



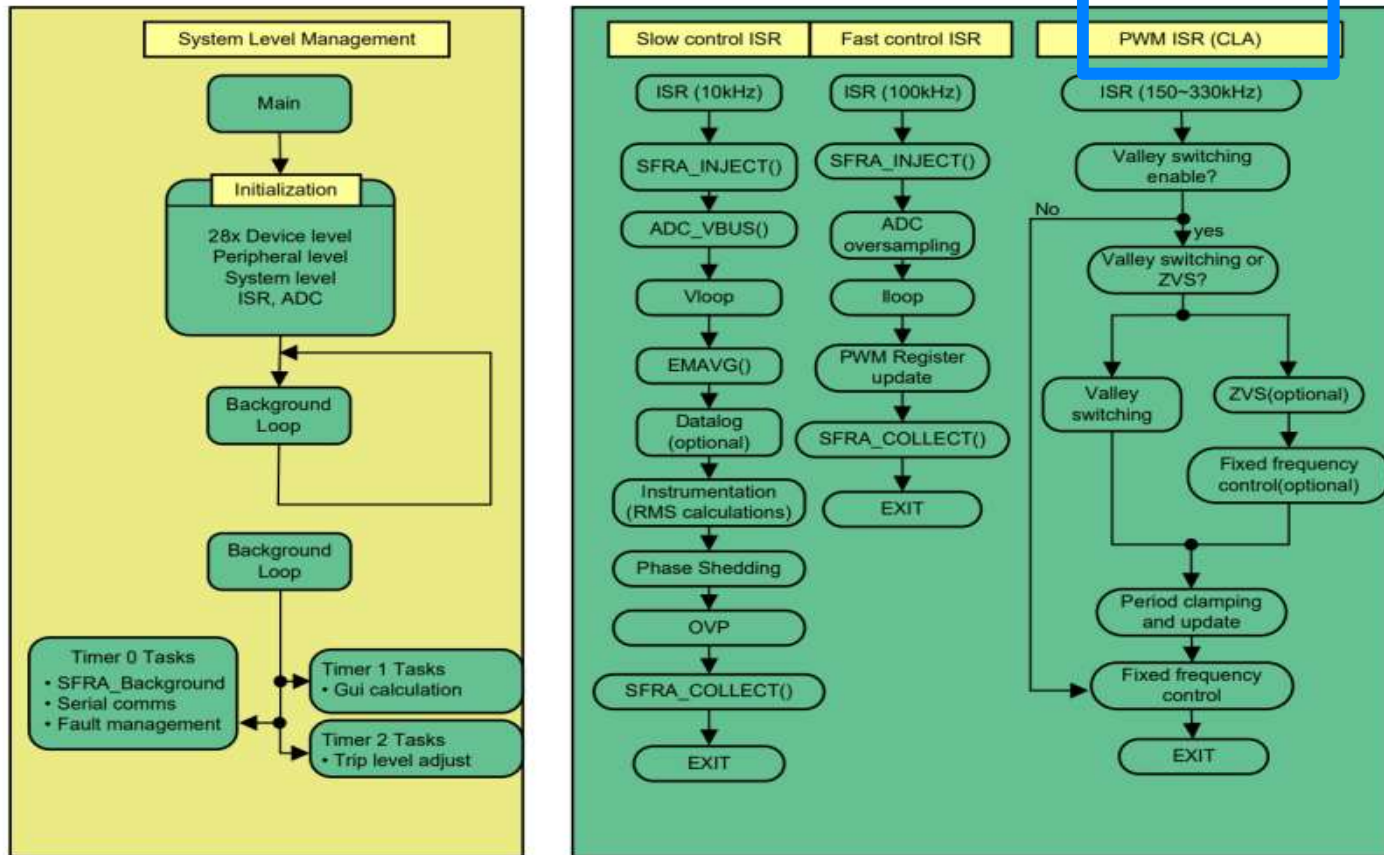
Valley switching control diagram



Valley switching block in EPWM module



Valley switching software structure



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- **Technical challenges**
- Waveforms and test results

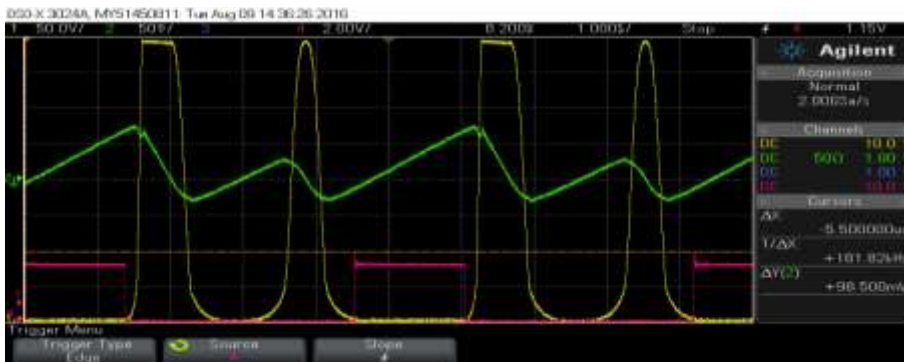
PFC with valley switching (AC input)

The V_{ds} waveform is decided by several factors: instantaneous input voltage, load, bus voltage, etc.

V_{ds}

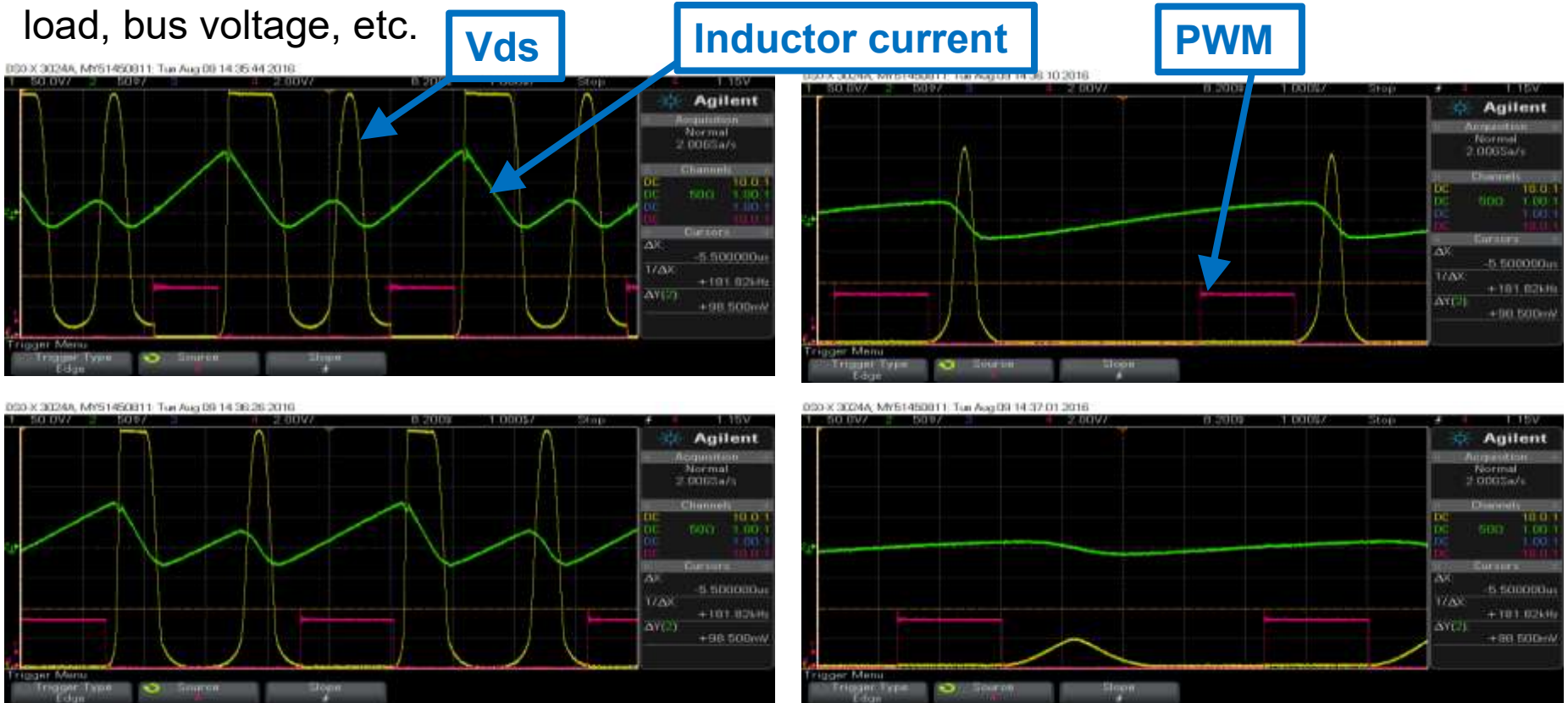
Inductor current

PWM



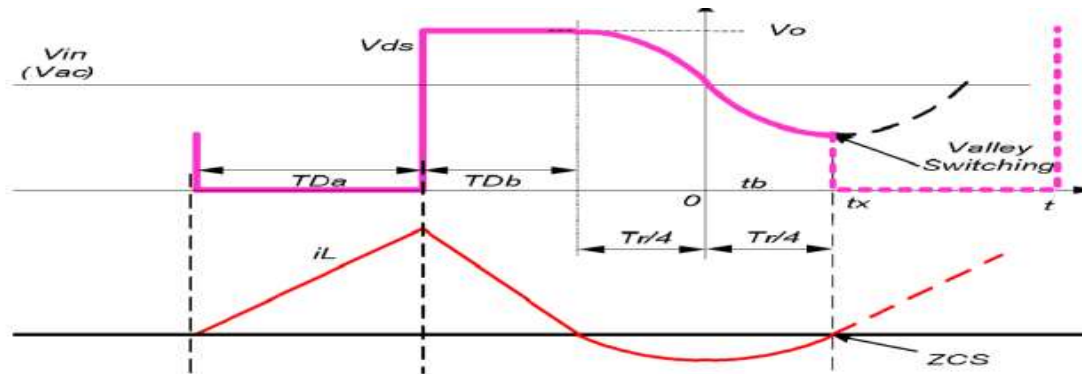
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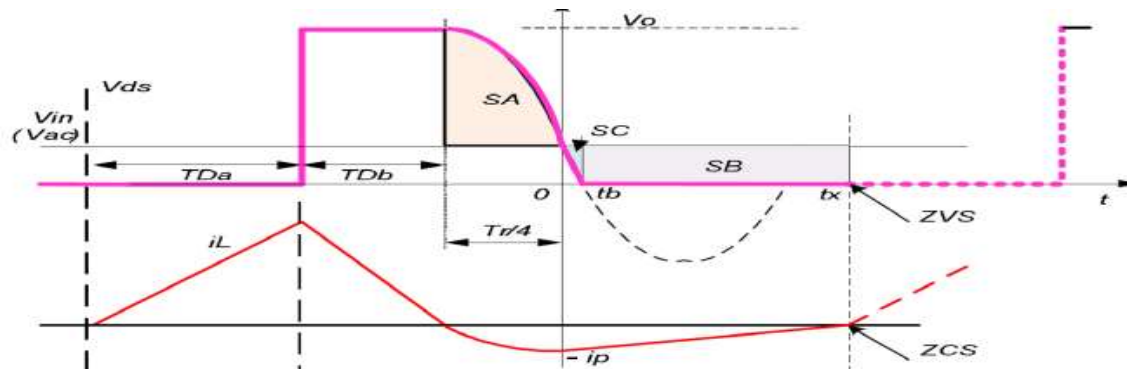


PFC with valley switching (AC input)

Valley switching and ZVS



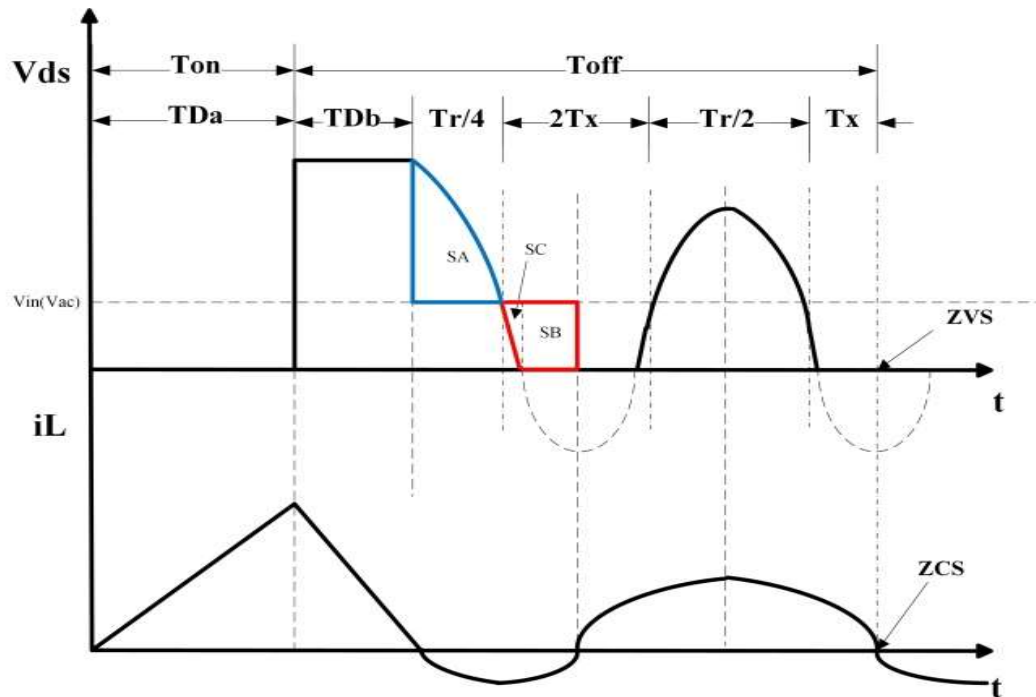
$$V_{in} > \frac{1}{2} \cdot V_{bus}$$



$$V_{in} < \frac{1}{2} \cdot V_{bus}$$

PFC with valley switching (AC input)

- ZVS – Calculation-based control
- Details are available in the application note: <http://www.ti.com/lit/sprach7>

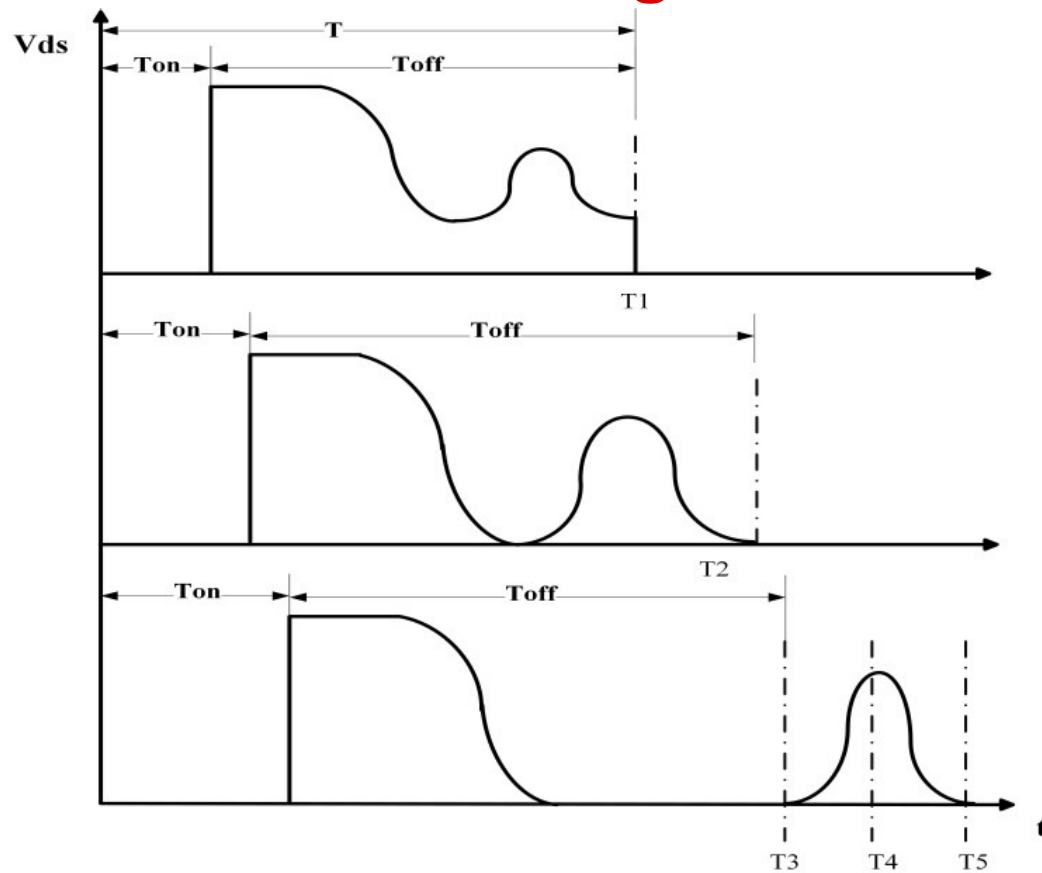


$$a. \quad T_{Db} = T_{Da} \cdot V_{in} / (V_o - V_{in})$$

$$b. \quad T_x = V_o \cdot T_r / (8 \cdot V_{in})$$

$$c. \quad T_s = T_{Da} + T_{Db} + (T_r/4 + T_x) \cdot 3$$

Technical challenges



Valley switching

ZVS/Valley switching
threshold

Fixed frequency

Technical challenges

Difficult to reduce the current distortion:

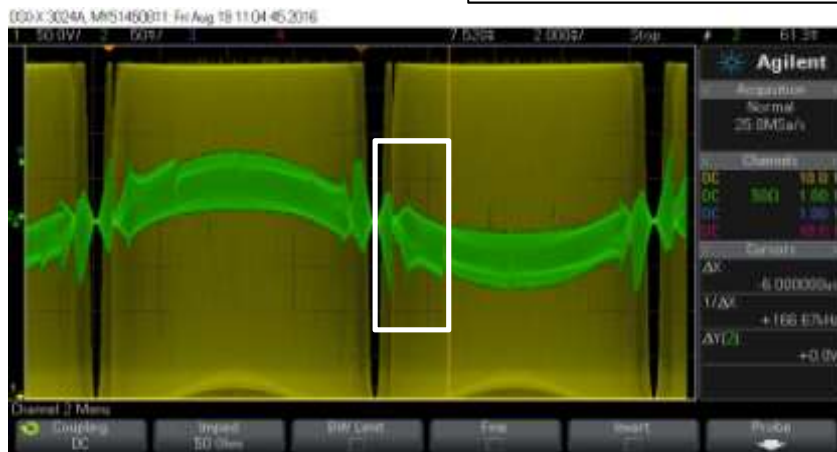
- Target: Seamless transition between valley switching, ZVS, fixed frequency operating modes
- Methods: Clamp freq during valley switching, ZVS coefficients, blanking window, CMPSS threshold, hysteresis control, etc.

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Input current distortion before implementing multi-mode control



Technical challenges

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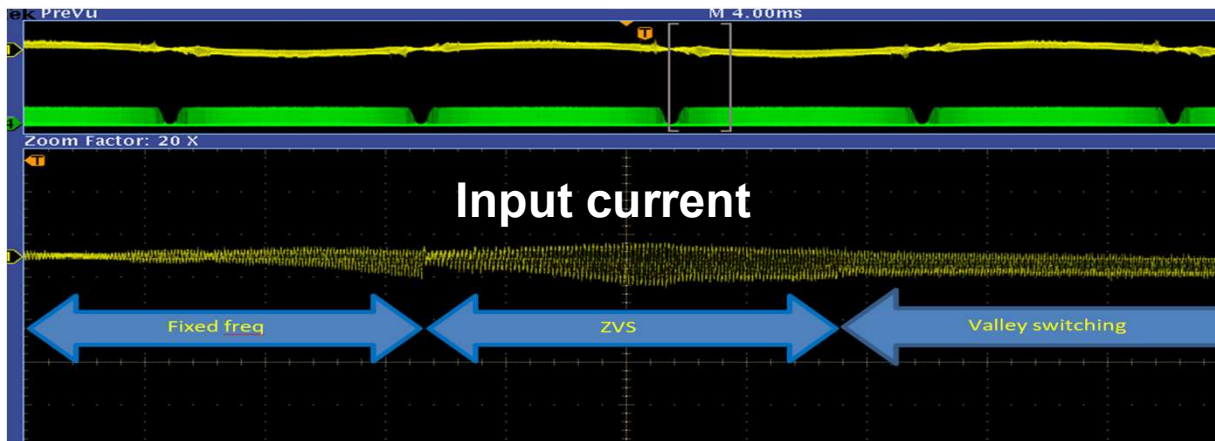
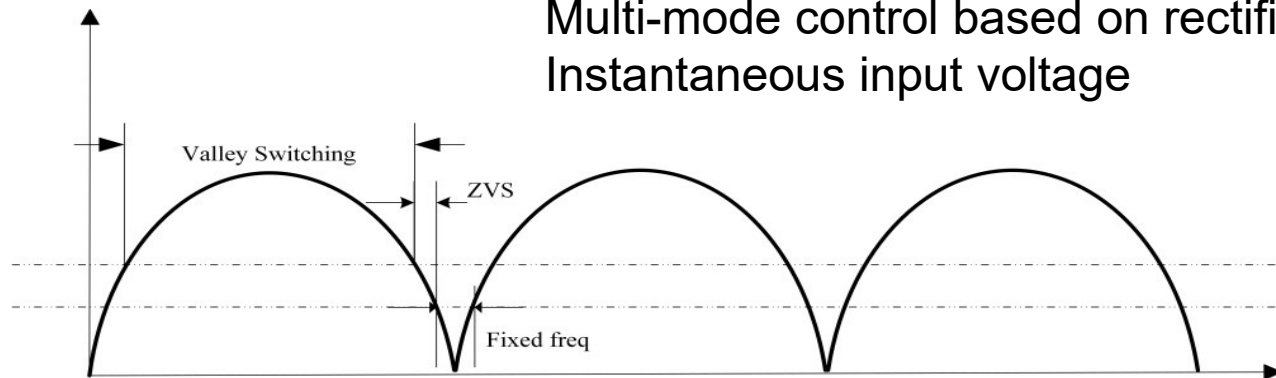
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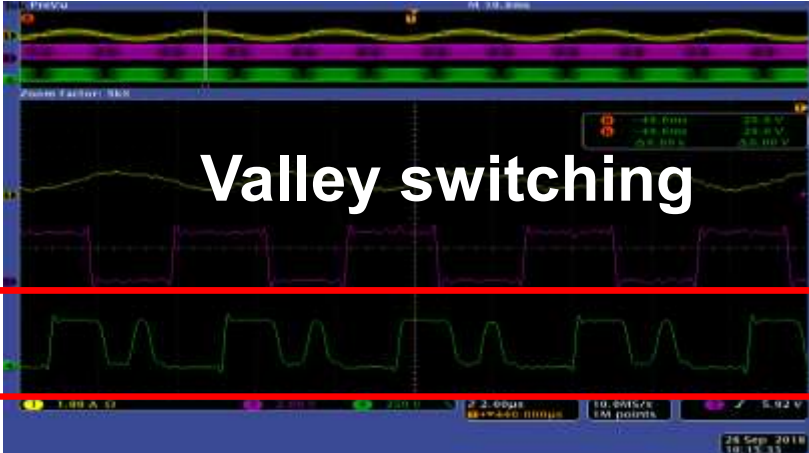


Technical challenges

Multi-mode control based on rectified
Instantaneous input voltage

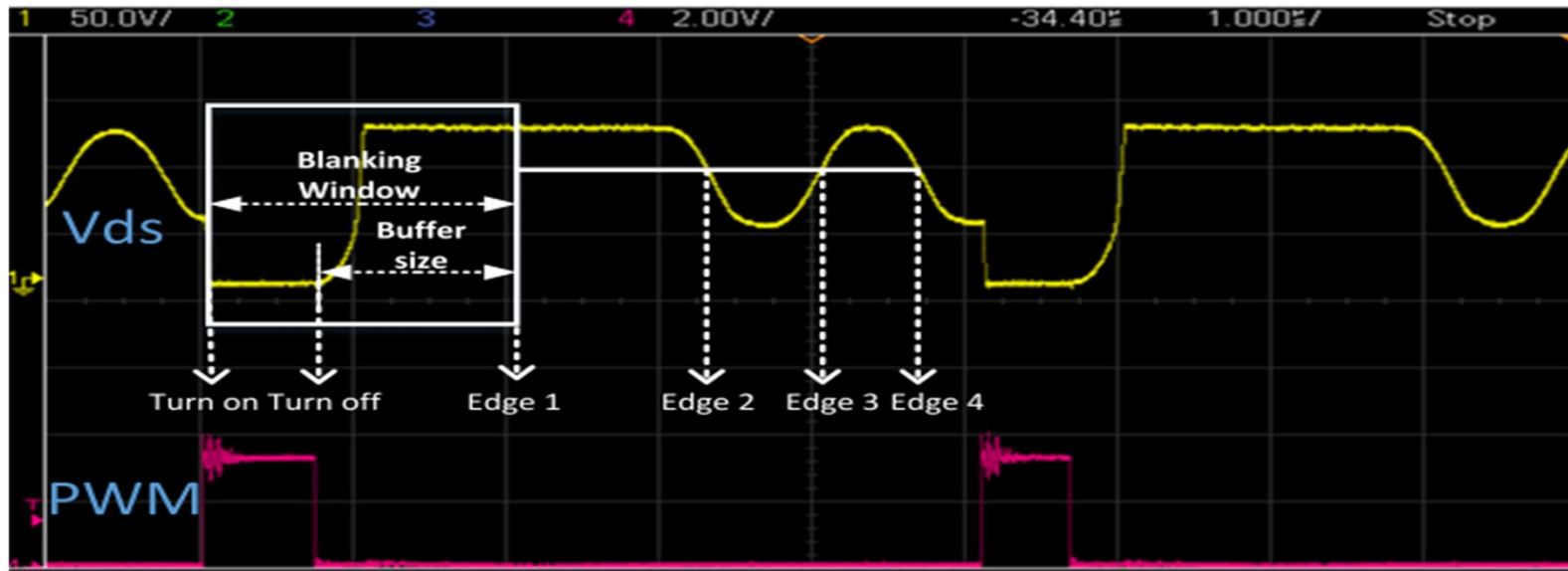


Vds waveforms under multi-mode control



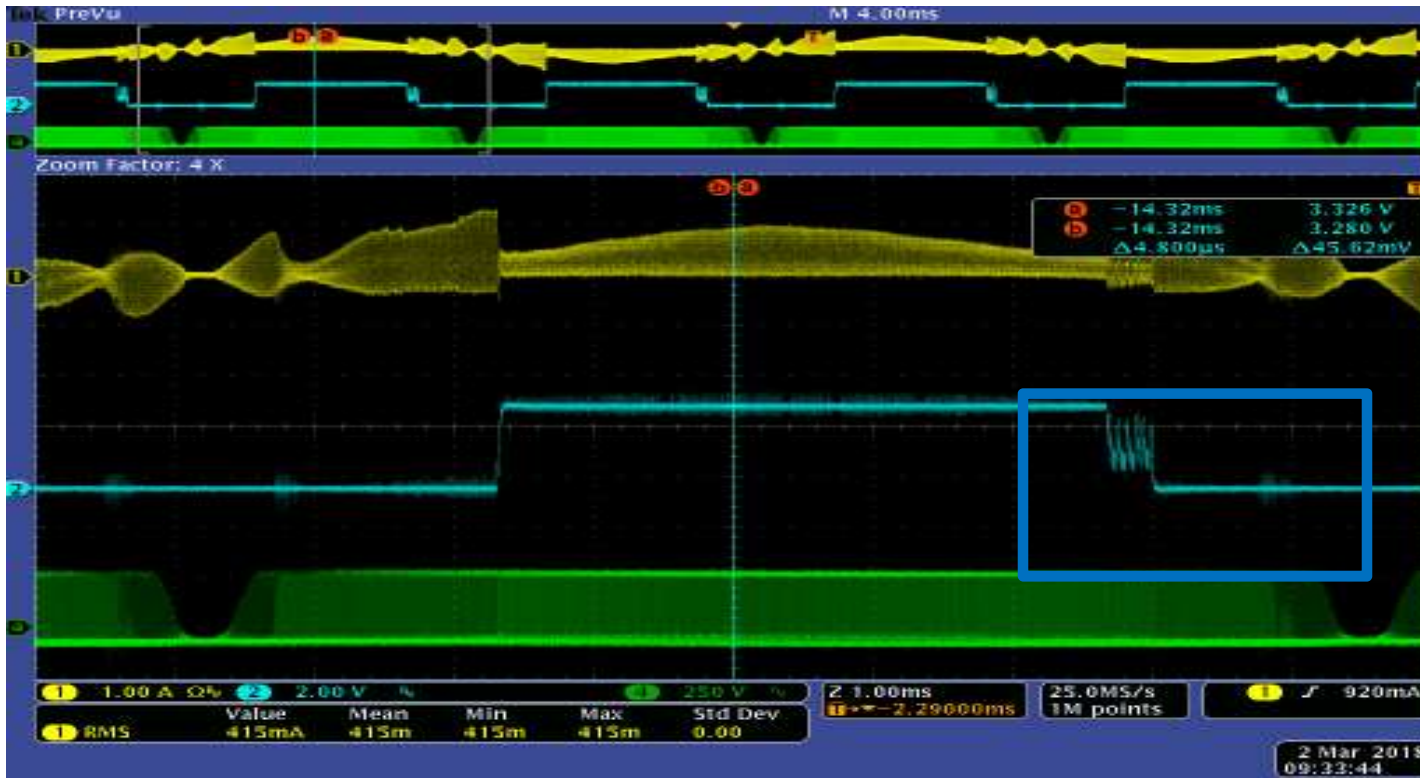
Blanking window

- Reasons for using blanking window:
 - Limit the max freq
 - Filter the noise
- Blanking window length = Duty cycle * period + Buffer size
- The high to low edge of blanking window itself will be counted as the first edge.



Hysteresis control

ZVS/valley switching transition



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Current waveforms (AC input)

- Current waveform improved with optimized valley switching control
- Low line test condition:
5% load 120V input, 380V output

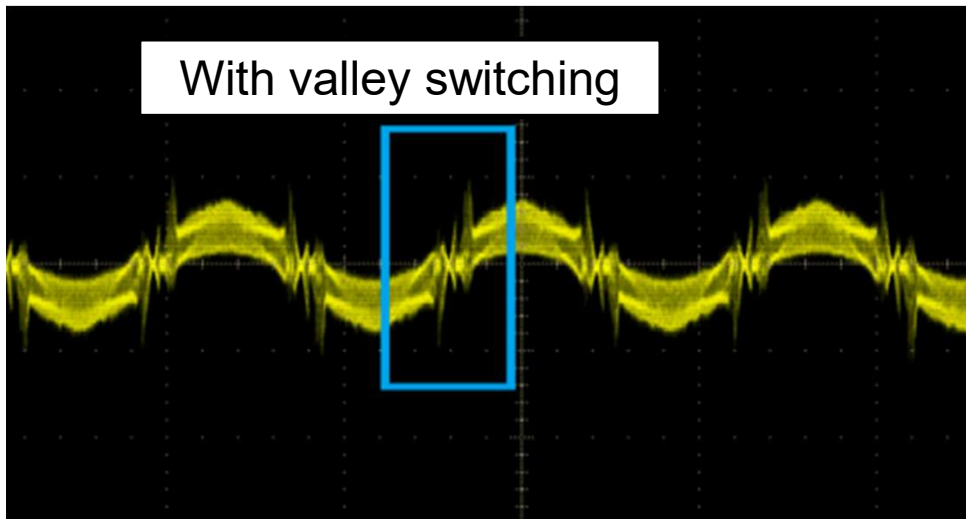
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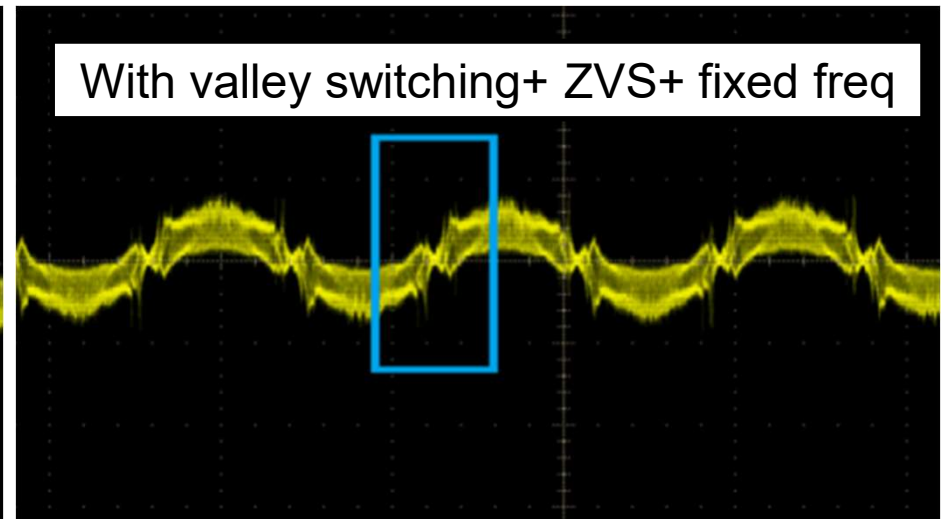
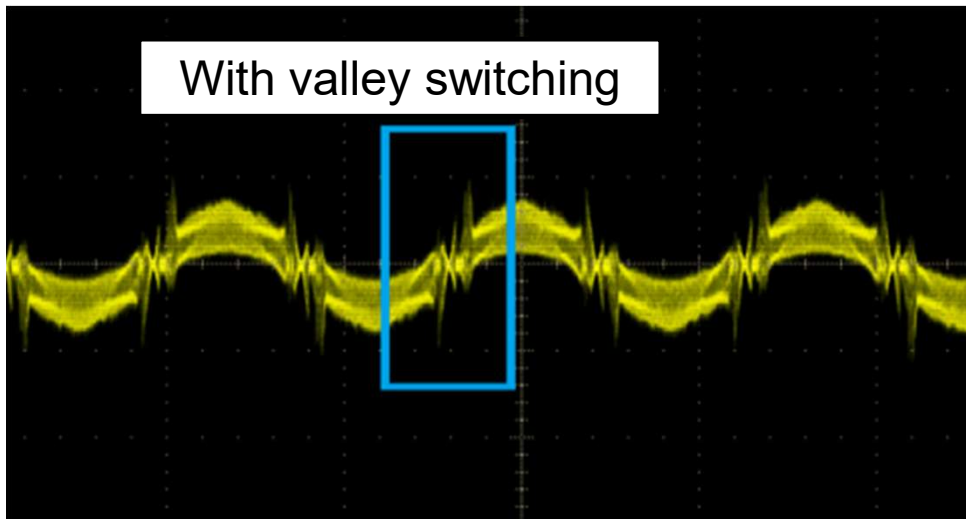
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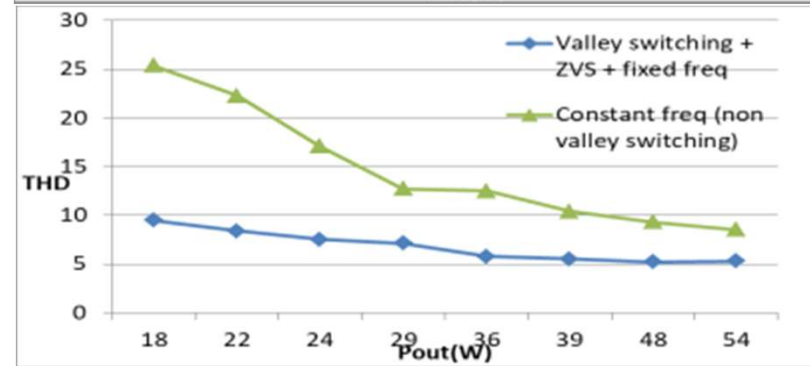
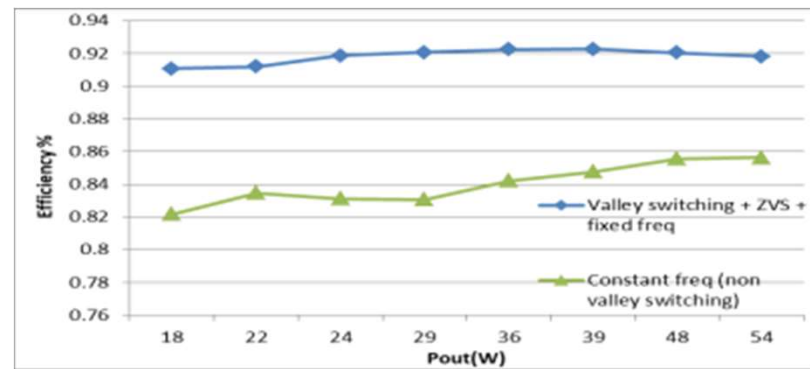
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Performance comparison

Constant freq control compared to multi-mode control

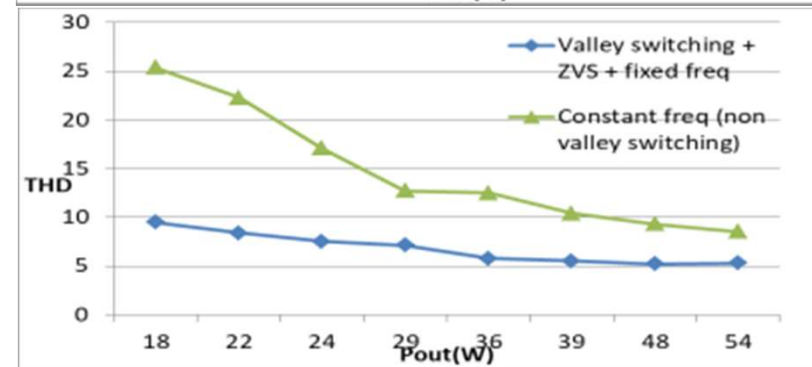
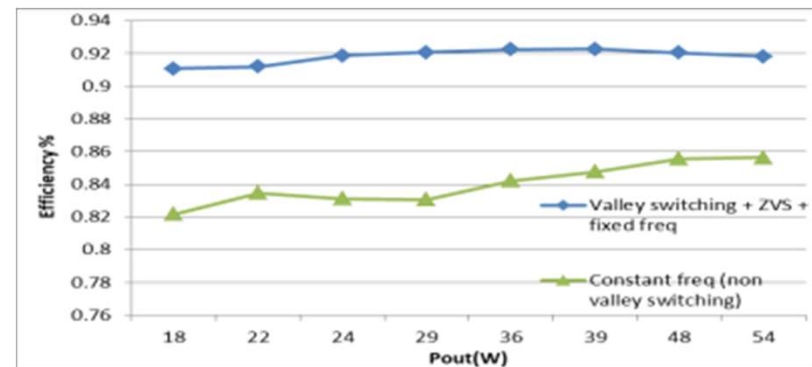
System Characteristics		
5% load Single phase	Low line (Vin = 120V)	High line (Vin = 220V)
Efficiency	84% → 92%	89% → 92%
THD	10% → 6%	22% → 7%



TIDM-1022 THD compared to spec

THD meets the requirement of the spec (Server customer)

System Characteristics		
7% load Single phase	Low line (Vin = 120V)	High line (Vin = 220V)
THD	5.3%	6.2%
Required THD based on the spec (5-10% load)		8%



For more information

- Download the valley switching Boost Power Factor Correction (PFC) reference design: <http://www.ti.com/tool/TIDM-1022>
- Learn more about the Piccolo 32-bit MCU (TMS320F280049): <http://www.ti.com/product/TMS320F280049>
- Control Law Accelerator (CLA) Usage in TIDM-1022: <http://training.ti.com/tidm1022-usage>
- For questions about this training, refer to the E2E Community Forums for C2000 Processors at <http://e2e.ti.com>