What is DisplayPort (DP)?

TI Precision Labs (TIPL) - Video interface

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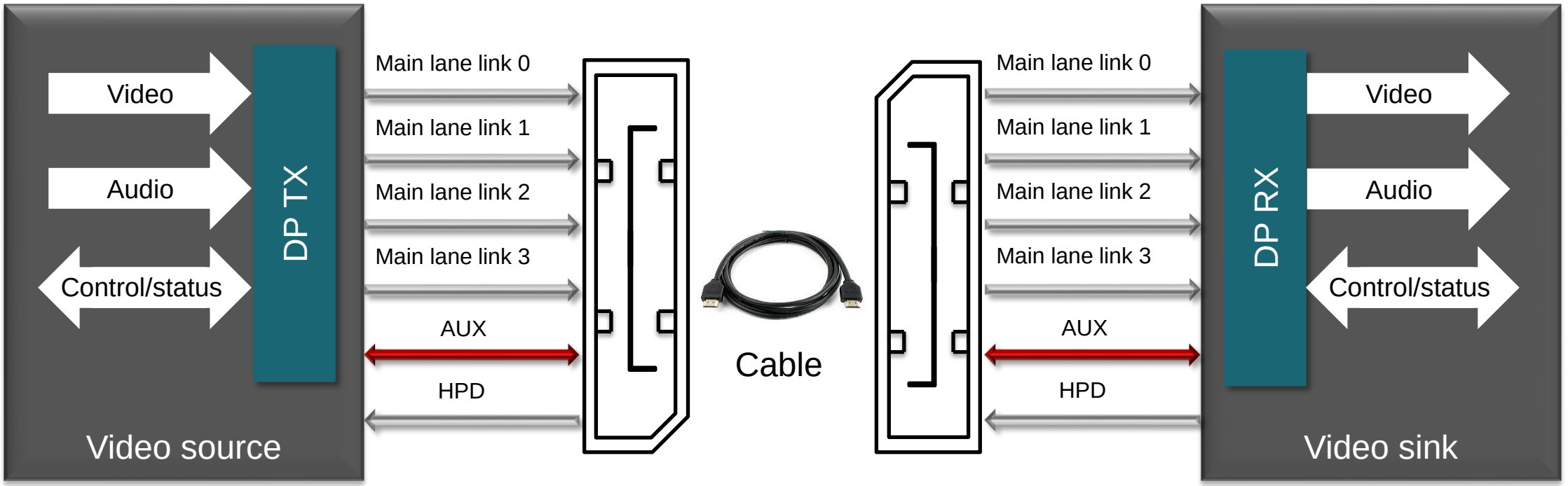
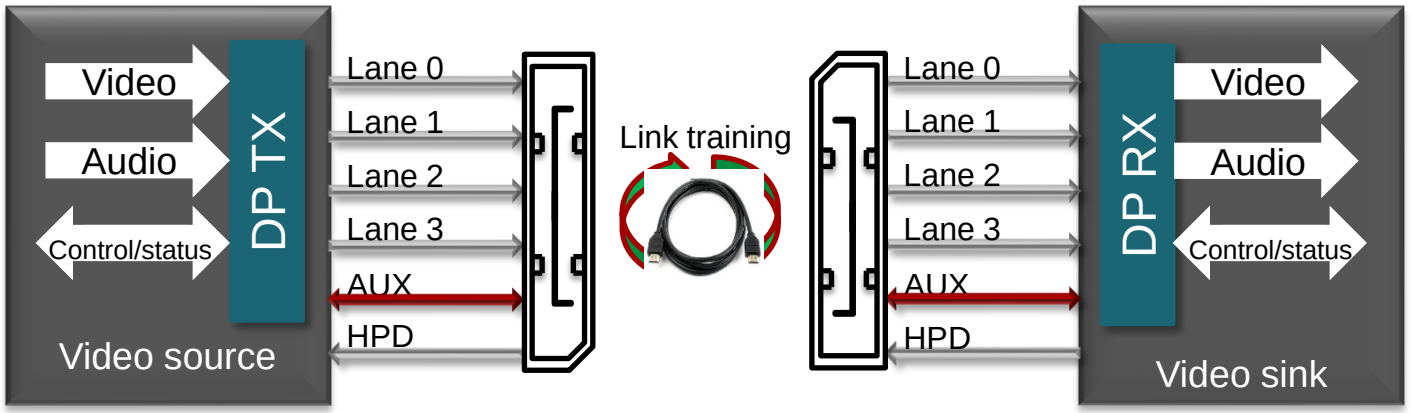
Presented by Nicholaus Malone

DisplayPort (DP) signal interface



DP Hot Plug Detect (HPD) and AUX



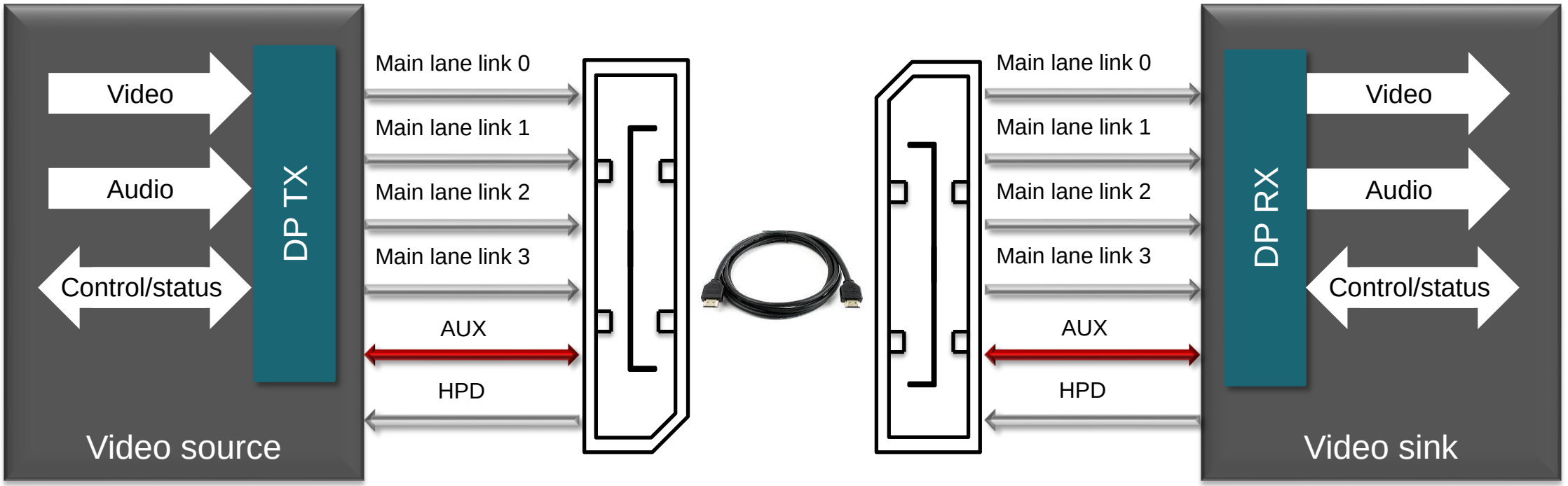
HPD

- Indicate the presence of the sink
- Serves as an interrupt from the sink to the source

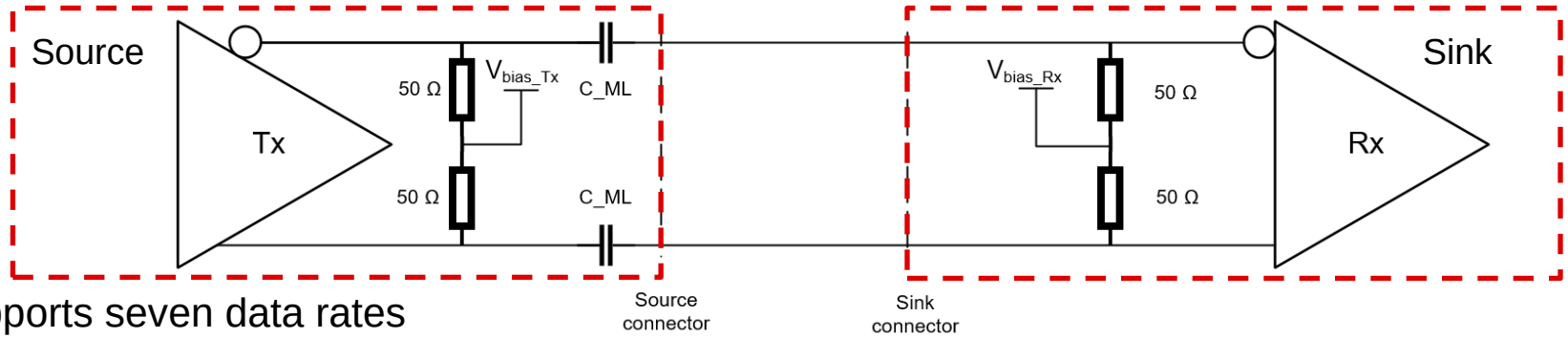
AUX

- AC coupled Bi-directional signal path
- 1 Mbps transfer rate either direction Manchester encoded

DP main link signaling characteristic



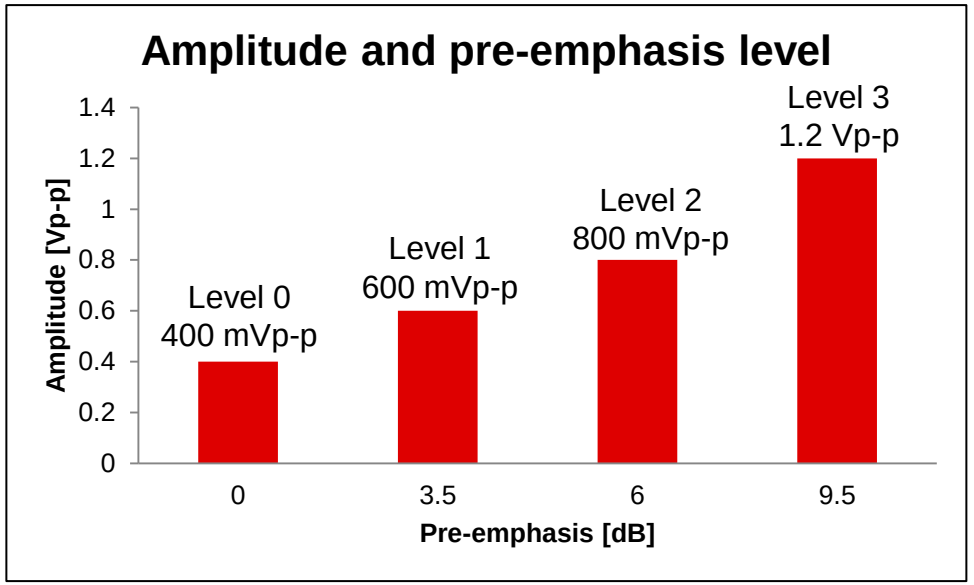
DP main link signaling characteristic



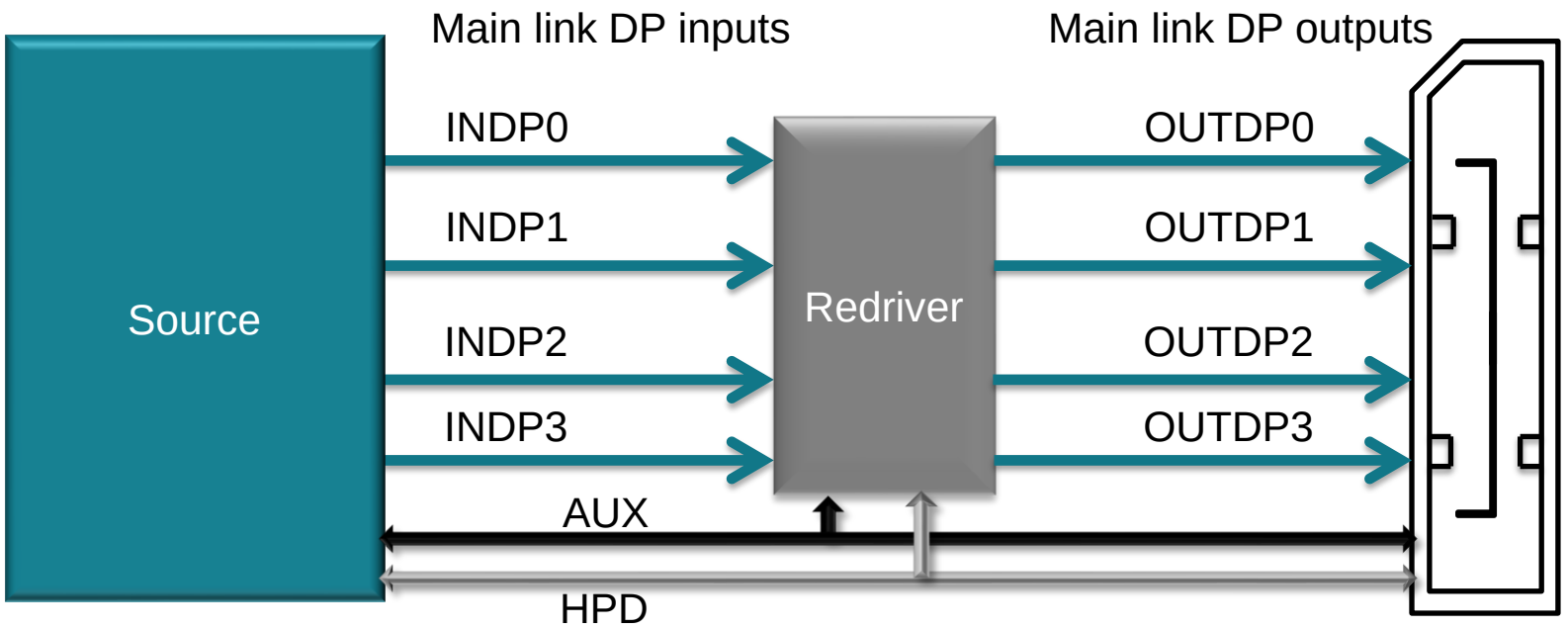
- Supports seven data rates
  - 1.62Gbps per lane (reduced bit rate (RBR))
  - 2.7Gbps per lane (high bit rate (HBR))
  - 5.4Gbps per lane (high bit rate 2 (HBR2))
  - 8.1Gbps per lane (high bit rate 3 (HBR3))
  - 10Gbps per lane (ultra high bit rate 10 (UHBR10))
  - 13.5Gbps per lane (ultra high bit rate 13.5 (UHBR13.5))
  - 20Gbps per lane (ultra high bit rate 20 (UHBR20))
- Three possible lanes configuration
  - 1 lane
  - 2 lanes
  - 4 lanes
- Data rate and supported lane configuration are communicated over AUX between the source and sink

DP main link signaling characteristic

- Amplitude and pre-emphasis defined as levels
  - Default signal amplitude at source is 400mVp-p
  - Default signal pre-emphasis at source is 0dB

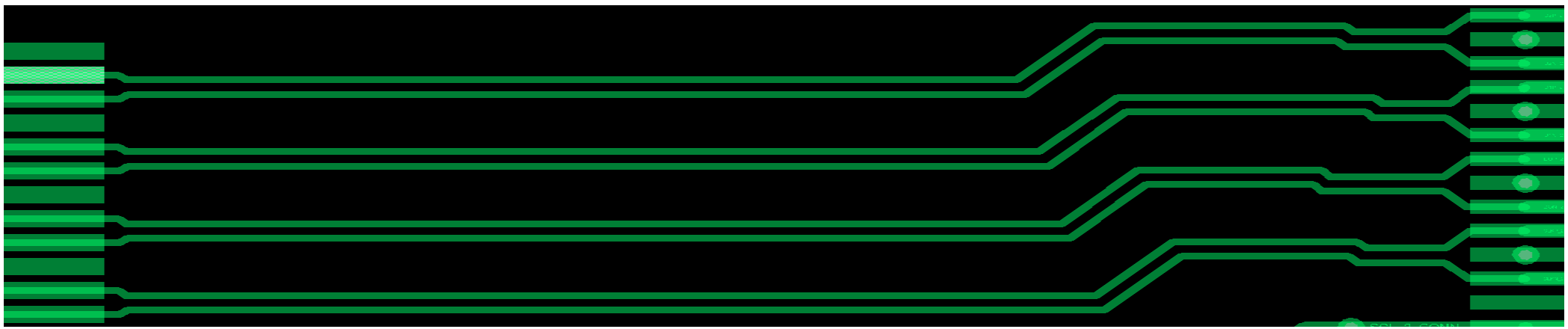


DP source TX and sink RX design challenge



Placement of the DP redriver

- Re-driver placement depends on total insertion loss of the system
- Insertion loss:
  - PCB trace
  - Via
  - Connector
  - Silicon package, etc.



Placement of the DP redriver

$$Insertion\ Loss\ \left(dB/_{in}\right) \cong \frac{f^{1/2}}{w} + 2.3 \times f \times D_f \times {D_k}^{1/2}$$

- w = trace width [mils]
- f = Nyquist frequency [GHz] → DP data rate / 2
- Df = the PCB dissipation factor
- Dk = the PCB dielectric constant

Placement of the DP redriver

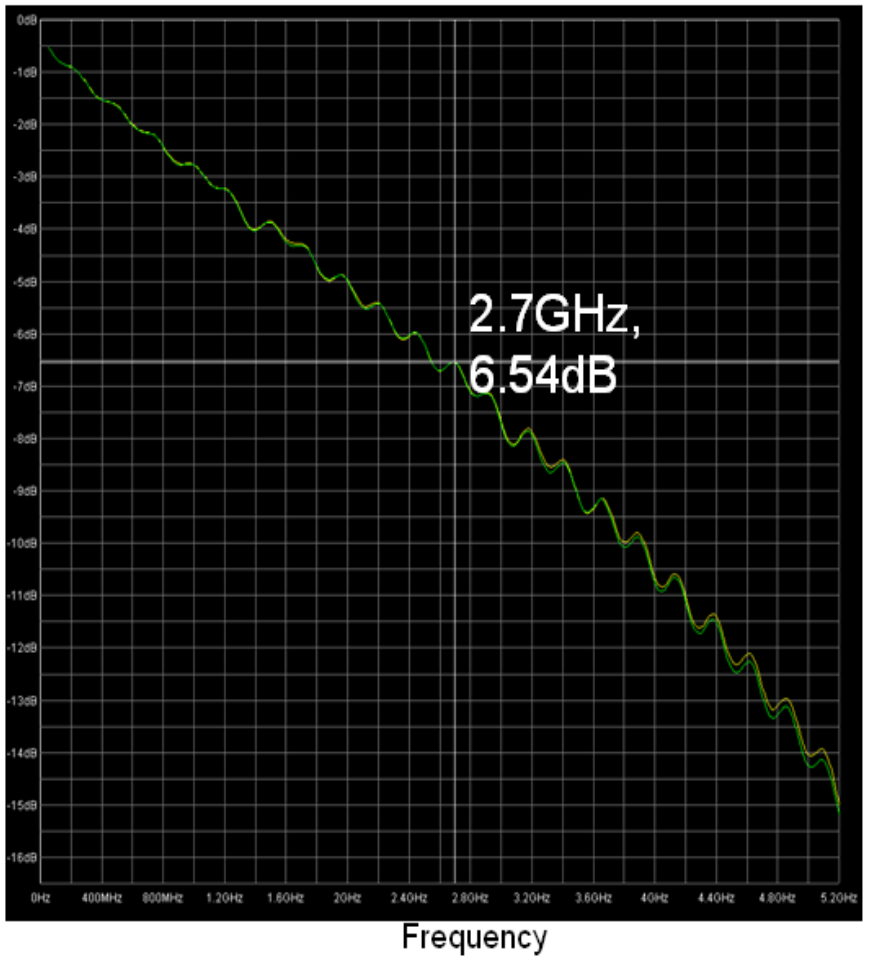
$$Insertion\ Loss\ \left(dB/_{in}\right) \cong \frac{f^{1/2}}{w} + 2.3 \times f \times D_f \times {D_k}^{1/2}$$

- f = 2.7
- w = 6
- Df = 0.02
- Dk = 4.3

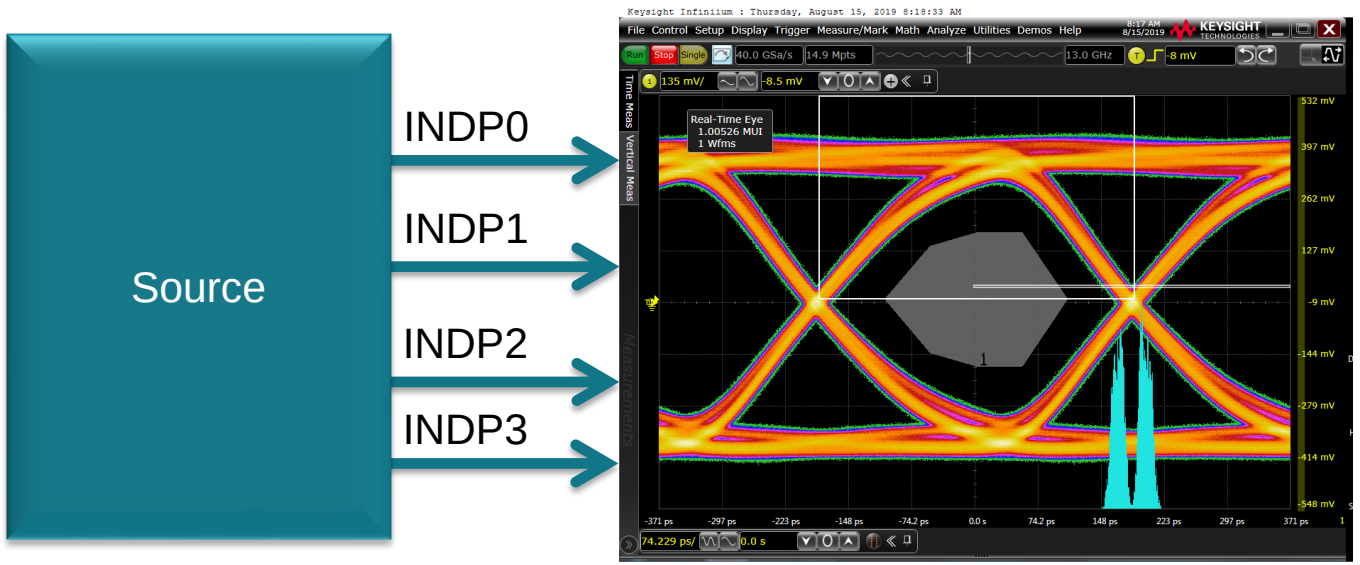
$$Insertion\ Loss\ \left(dB/_{in}\right) \cong \frac{2.7^{1/2}}{6} + 2.3 \times 2.7 \times 0.02 \times 4.3^{1/2}$$

$$\cong 0.53^{dB}/_{in}$$

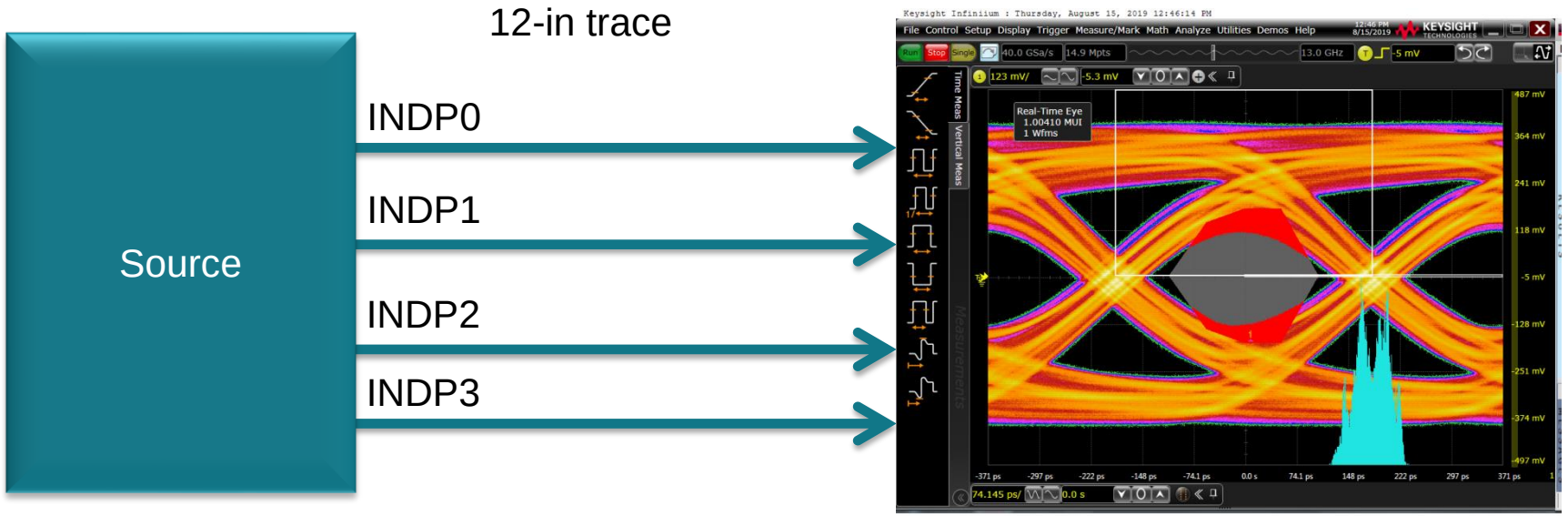
12in trace = 12 x ~0.53dB/in = ~ 6.36dB



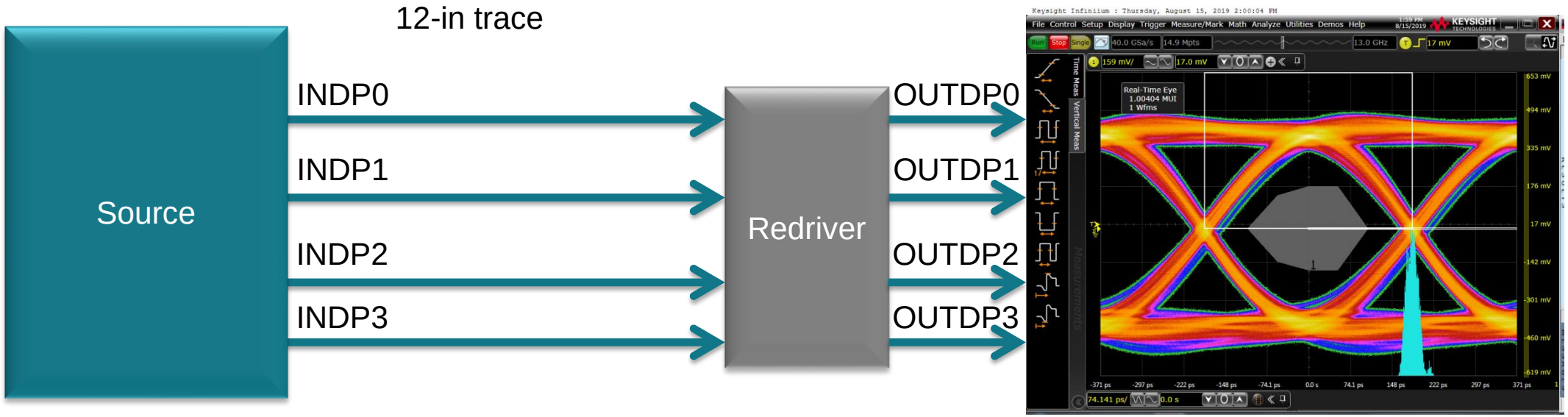
Placement of the redriver



Placement of the redriver



Placement of the redriver



Short quiz

1. True or false: DP is a DC-coupled interface FALSE
2. True or false: For data rate of 8.1Gbps and 2 lanes configuration, the total bandwidth is 16.2Gbps TRUE
3. True or false: Hot Plug Detect is used for configuring DP lanes FALSE
4. True or false: The insertion loss is the same regardless the DP data rate FALSE
5. True or false: A DP redriver can help improve the DP main link signal quality TRUE
6. True or false: The correct placement of the DP redriver is important for the design of system TRUE

Thank you

- Future video sessions
  - Details on DisplayPort 2.0 standard
  - TI's signal conditioning devices

- TI.com/e2e