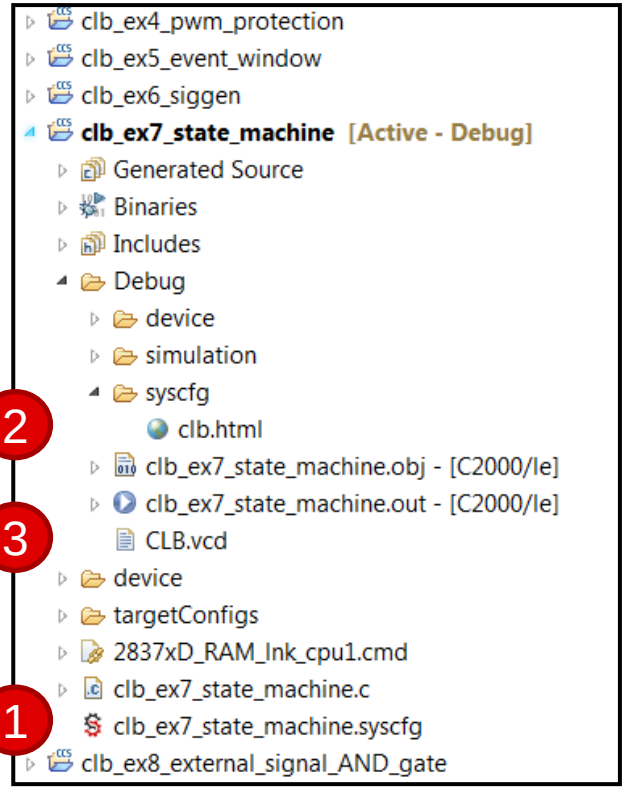
C2000™ CLB configurable logic block programming tool

CLB tool

Built into Code Composer Studio

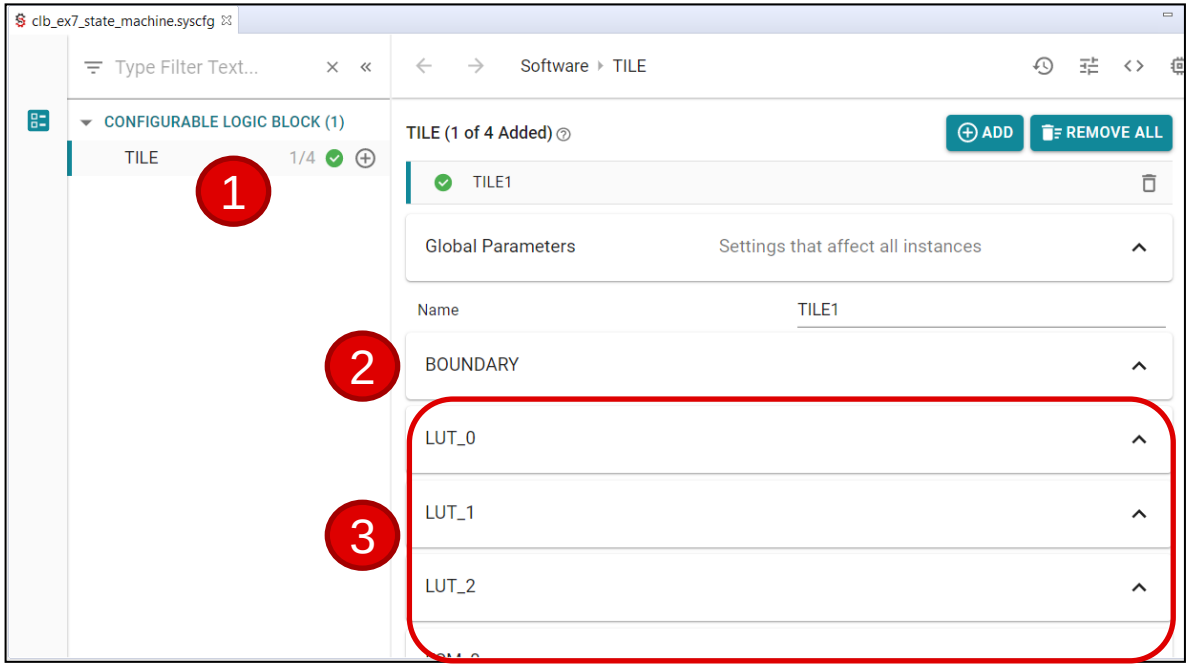
1. Simple and intuitive GUI tool to implement your hardware design for the CLB Tiles
2. Block diagram overview of the design
3. SystemC simulation for debugging

Examples available for all CLB enabled devices



CLB tool GUI

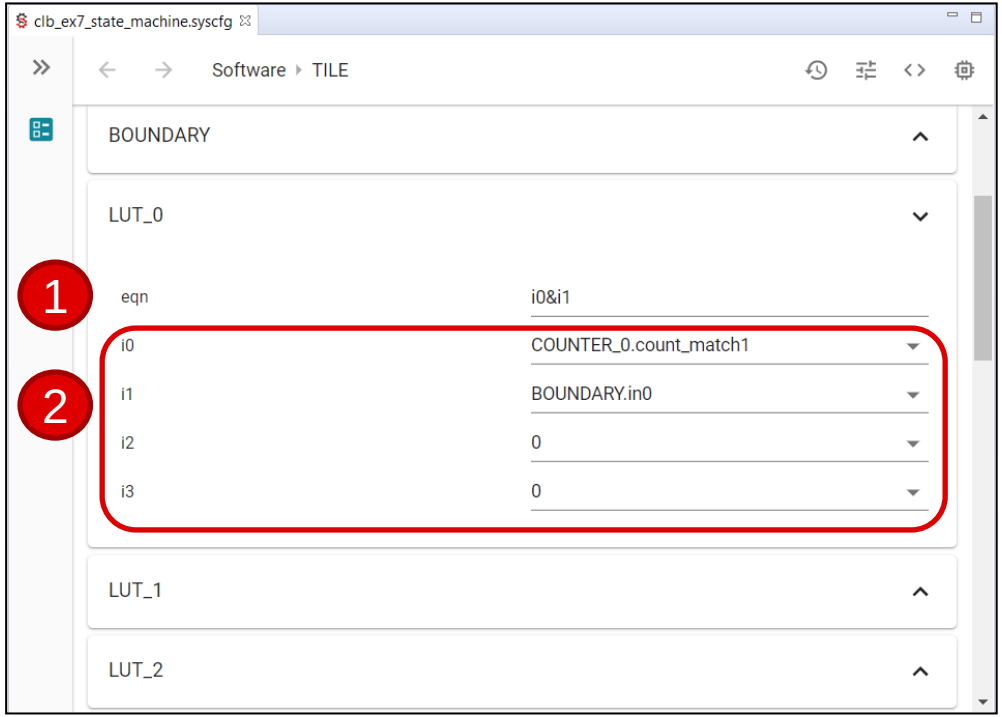
1. Keep track of available resources (number of CLB Tiles used)
2. BOUNDARY input used for simulating input signals for the TILE
3. All submodules inside the each CLB tile configurable through the tool



CLB tool – LUT configurable options

Each LUT has the following configurable options:

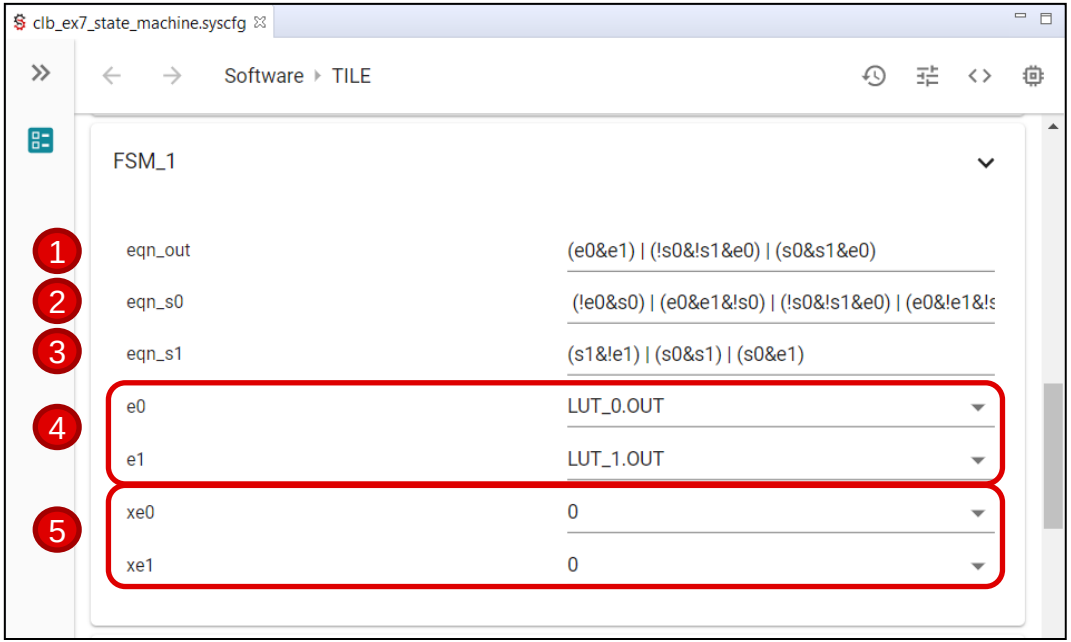
1. The logic equation for the output
2. i0 to i3 input signals



CLB tool – FSM configurable options

Each FSM has the following configurable options:

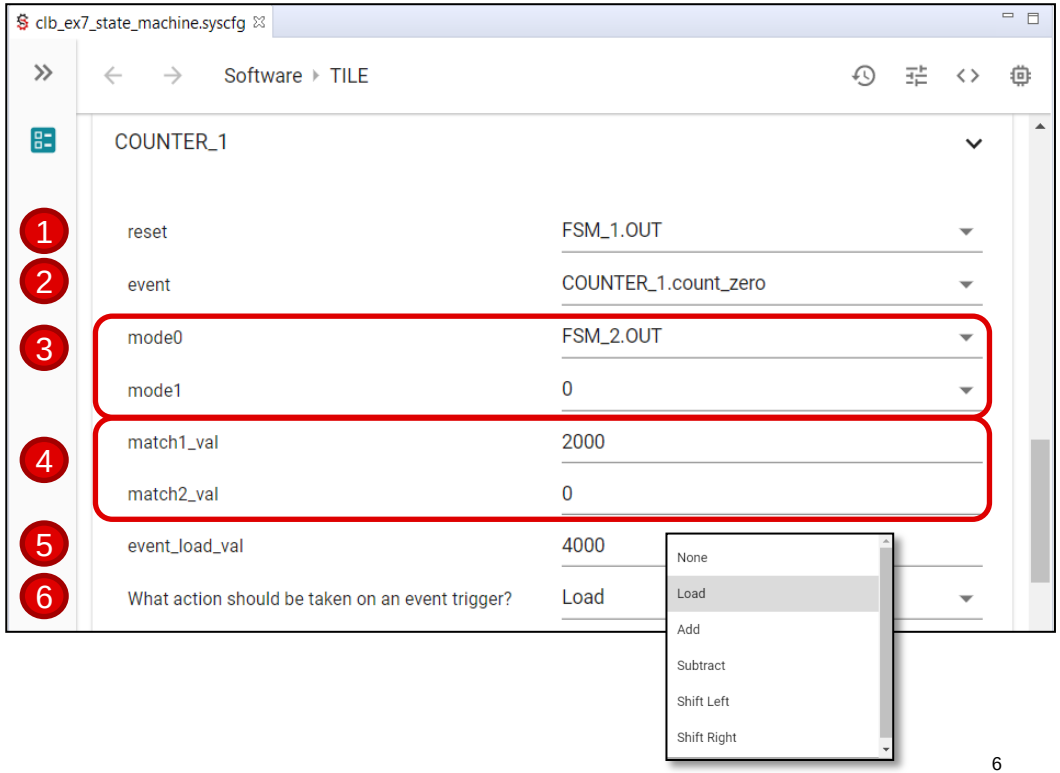
1. The logic equation for the output
2. The logic equation for the S0 NEXT state
3. The logic equation for the S1 NEXT state
4. e0 and e1 input signal
5. Extra input signal for when the FSM is used as a 2-state machine



CLB tool – COUNTER configurable options

Each COUNTER has the following configurable options:

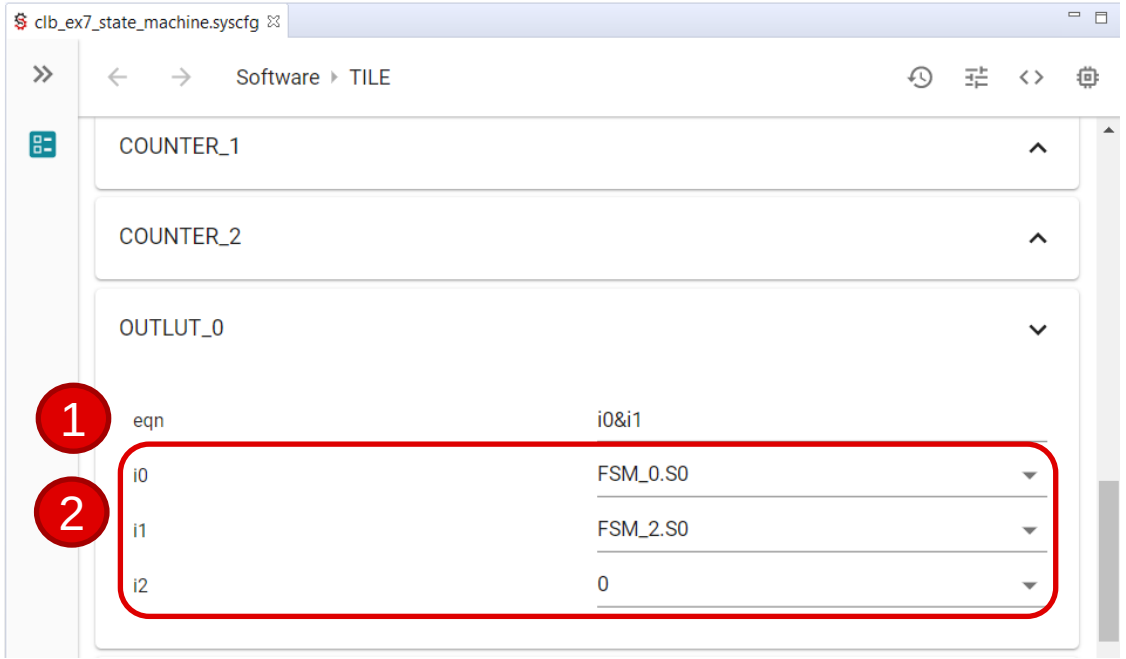
1. The reset input signal
2. The event input signal used along with the action option and the event load value option
3. mode0 and mode1input signals
4. match1 and match2 values
5. Load value
6. The action specified when the event signal is triggered
   - configure the counter as adder, x2, /2, etc.



CLB tool – OUTLUT configurable options

Each OUTLUT has the following configurable options:

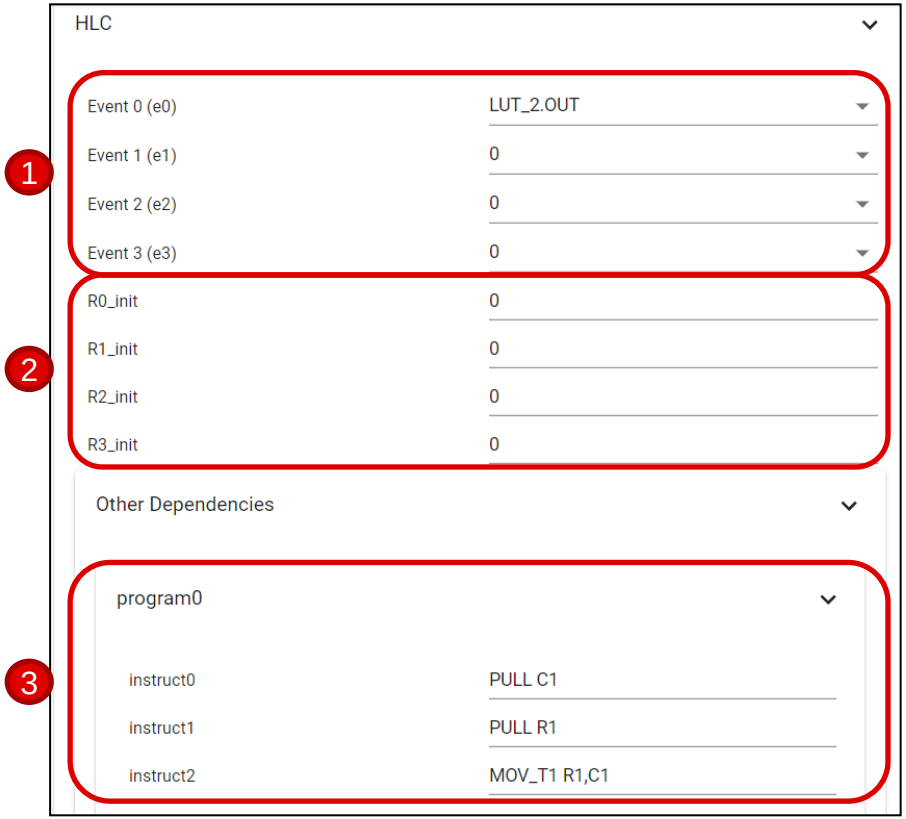
1. The logic equation for the output
2. i0 to i2 input signals



CLB tool – HLC configurable options

Each HLC has the following configurable options:

1. The event signals used to trigger the execution of up to 16 instructions
2. The general purpose registers R0-R3's initial values
3. The list instructions for each event input



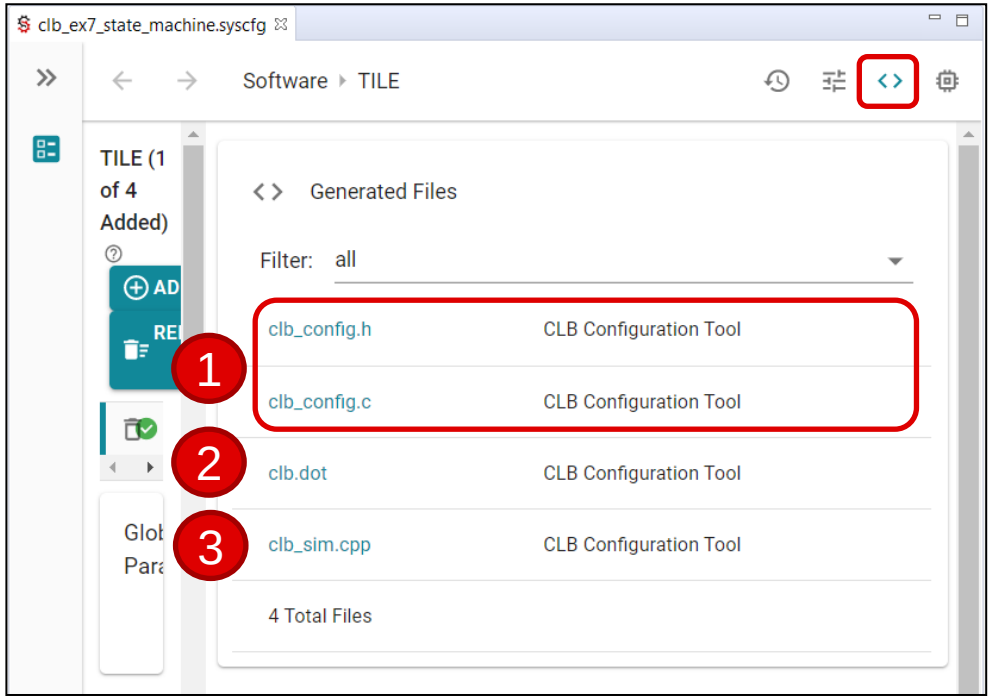
CLB tool auto-generated files

The CLB Tool will auto-generate:

1. The files needed to configure the CLB
2. The debugging simulation source file
3. The design block diagram source file

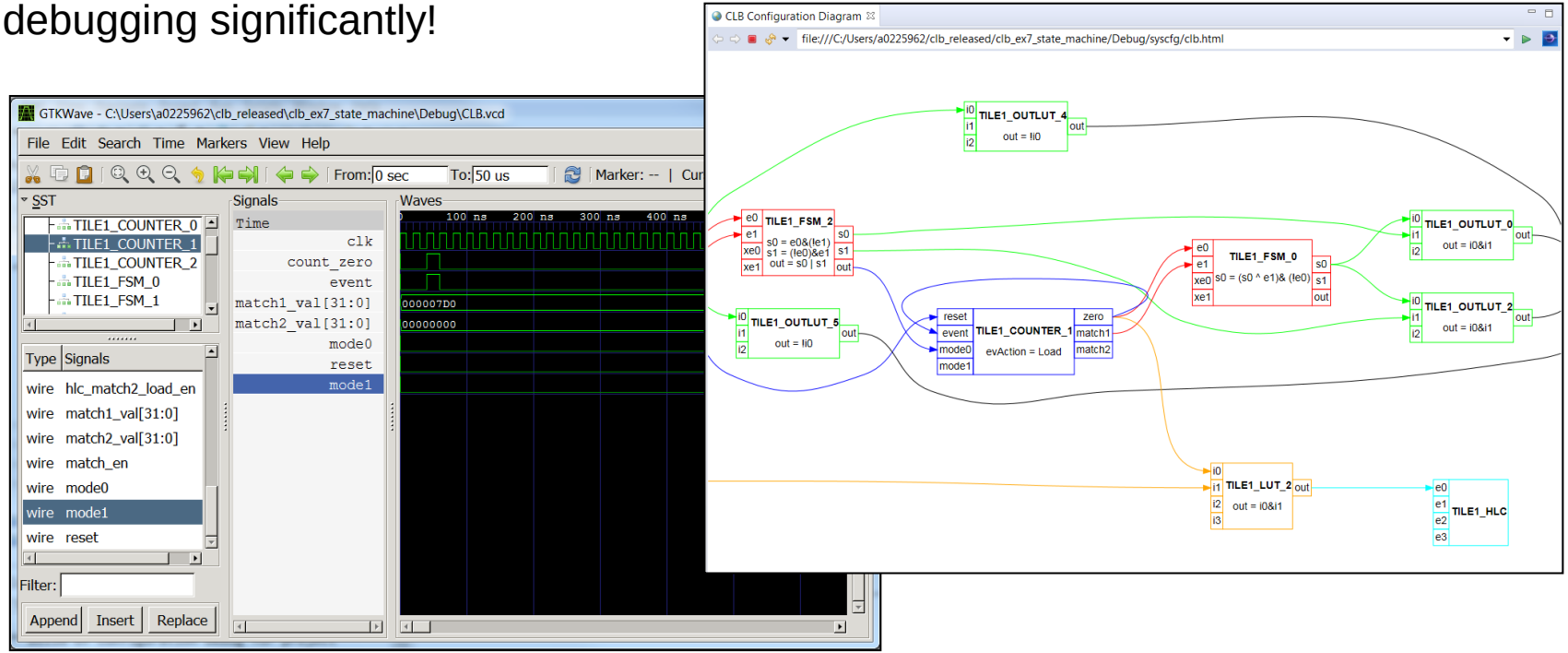
These outputs are then used by CCS to generate:

- MCU binary: .OUT file
- The simulation waveforms: .VCD file
- The CLB block diagram: .HTML file



CLB tool debugging tools

- The simulation waveform and the block diagram of the CLB design can facilitate debugging significantly!



Resources

- www.ti.com/c2000clb
- C2000Ware including the CLB Tool User's Guide [SPRUIR8]
- Application Note: How to Design with the CLB [SPRACL3]
- Application Note: How to Migrate from FPGA/CPLD to CLB [SPRACO2]

***Integrate* custom logic and *Augment* peripheral capability in your real-time MCU applications**