

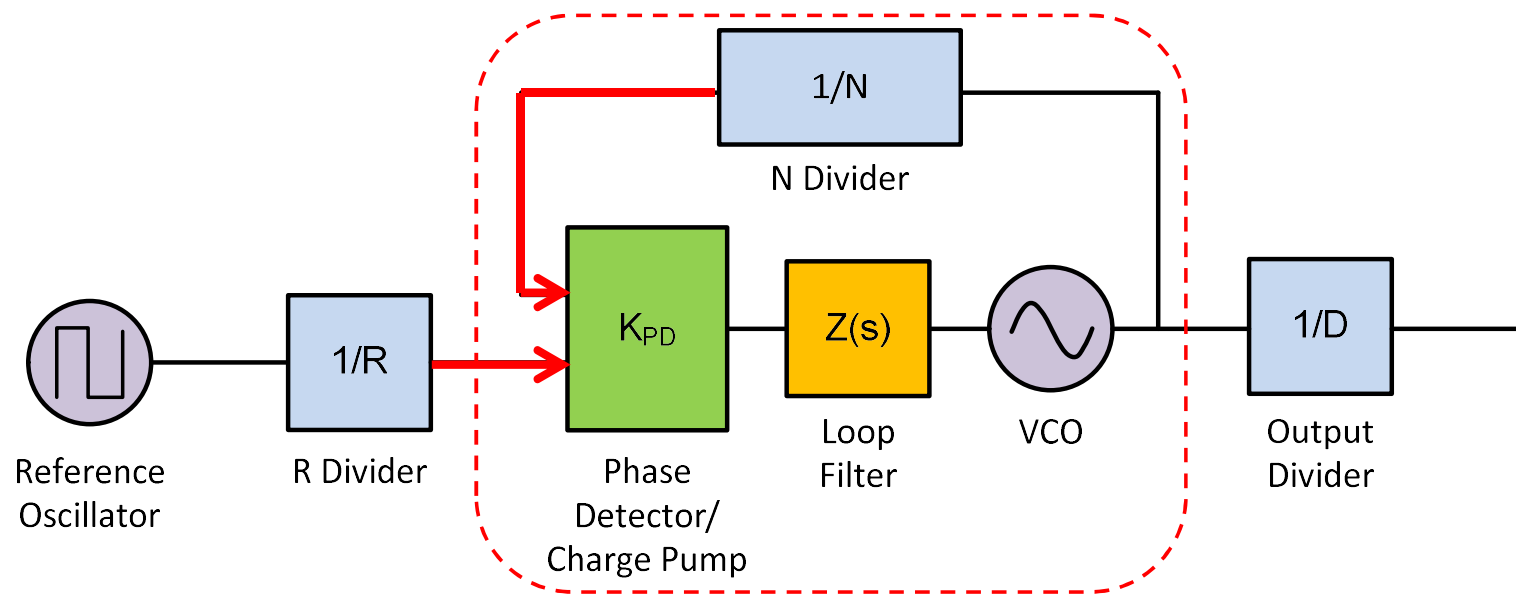
# RF PLLs and Synthesizers: Key Parameters and Specifications

TI Precision Labs – Clocks and Timing

Presented by Liam Keese

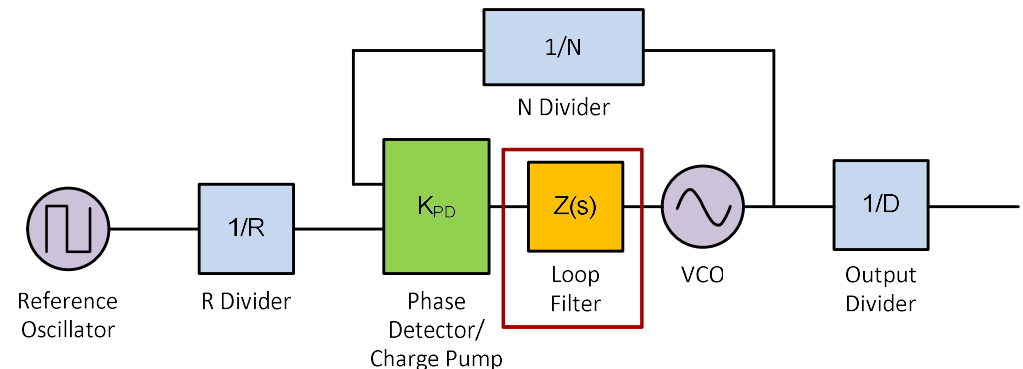
Prepared by Noel Fung

# Phase lock loop (PLL) overview



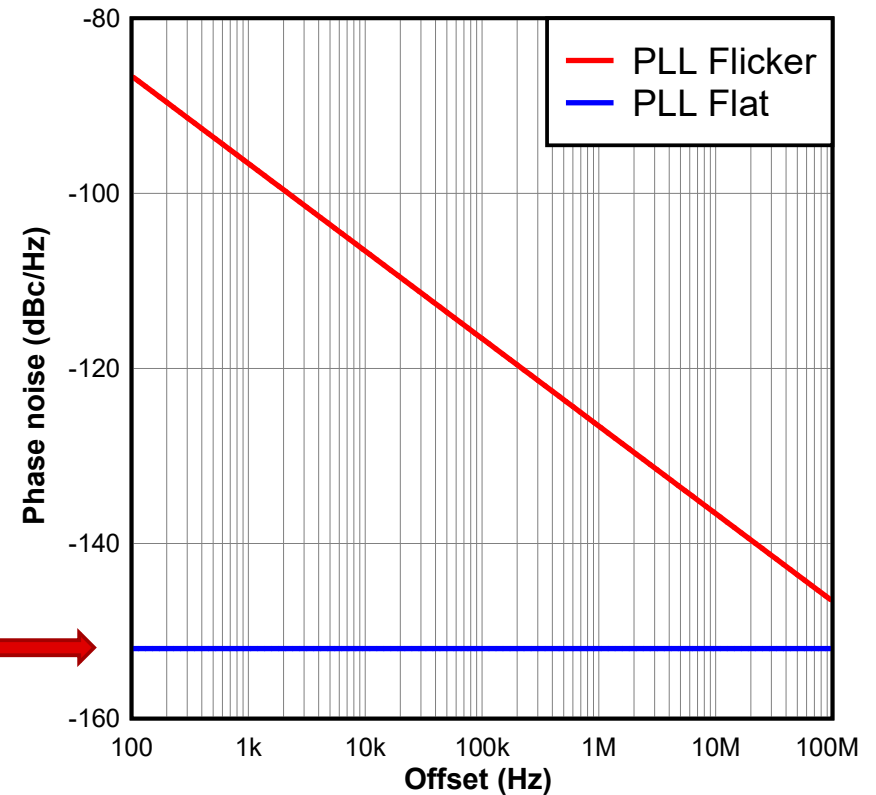
# Phase lock loop (PLL) overview

- Carefully *design loop filter* to meet phase noise, lock time and spurs requirement
- Key parameters and specifications for a design
  - Phase detector frequency
  - Charge pump current
  - VCO gain
  - PLL and VCO noise
  - Spurs
  - Lock time
- Design tools
  - Clock Architect
  - PLLatinum Sim



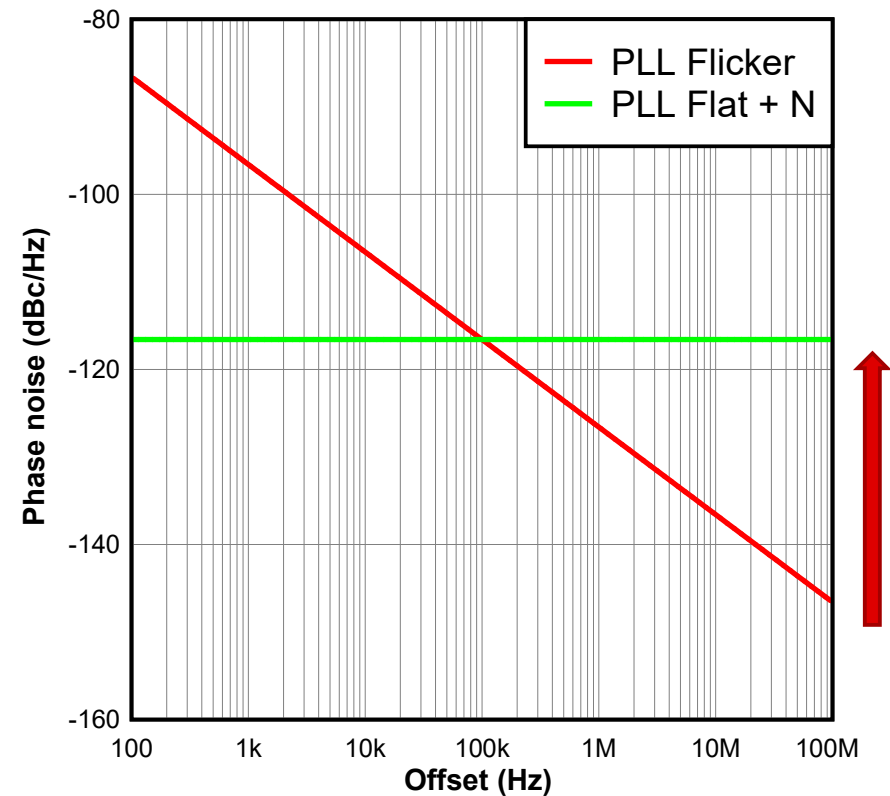
# PLL – Flicker noise and FOM

- Normalized PLL 1/f noise (Flicker noise)
  - Usually dominates at offset below 1 kHz
  - Typical value better than -120 dBc/Hz
- Normalized PLL noise floor (FOM)
  - Determines phase noise at mid-range offset
  - Typical value better than -230 dBc/Hz



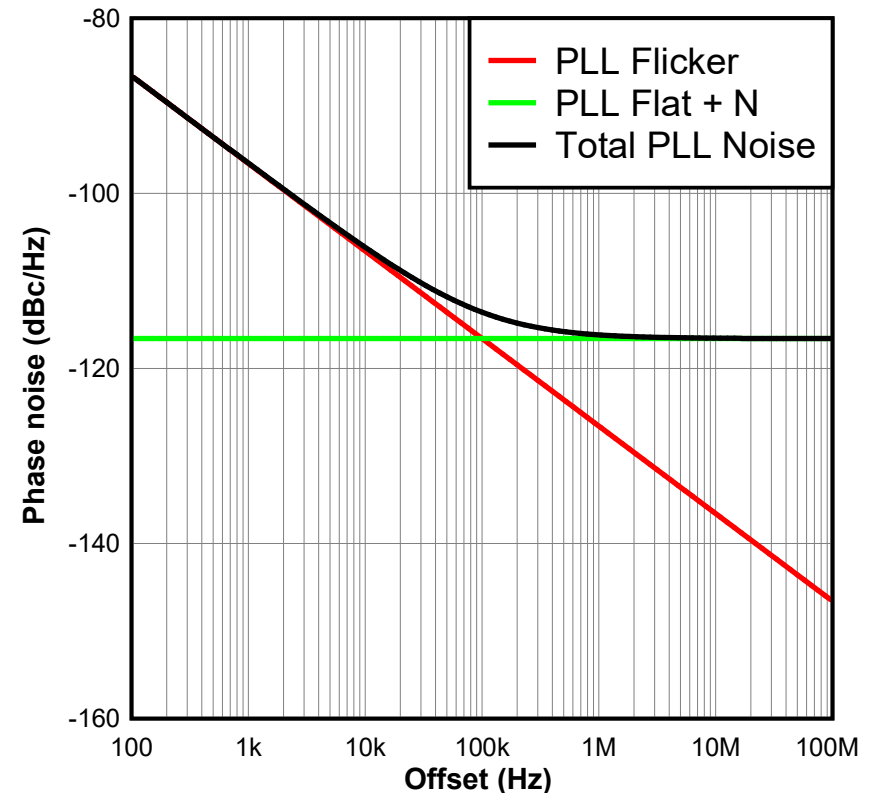
# PLL – N Divider noise

- Normalized PLL 1/f noise (Flicker noise)
  - Usually dominates at offset below 1 kHz
- Normalized PLL noise floor (FOM)
  - Determines phase noise at mid-range offset
- N-counter
  - Added noise =  $20\log(N)$
  - e.g. added noise = 40 dB for  $N = 100$

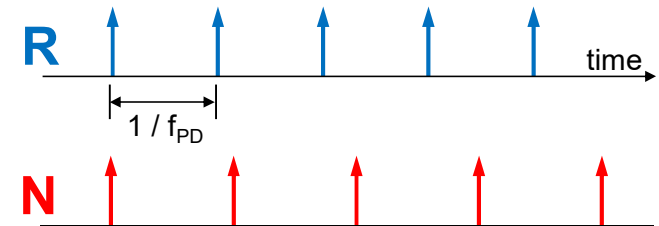
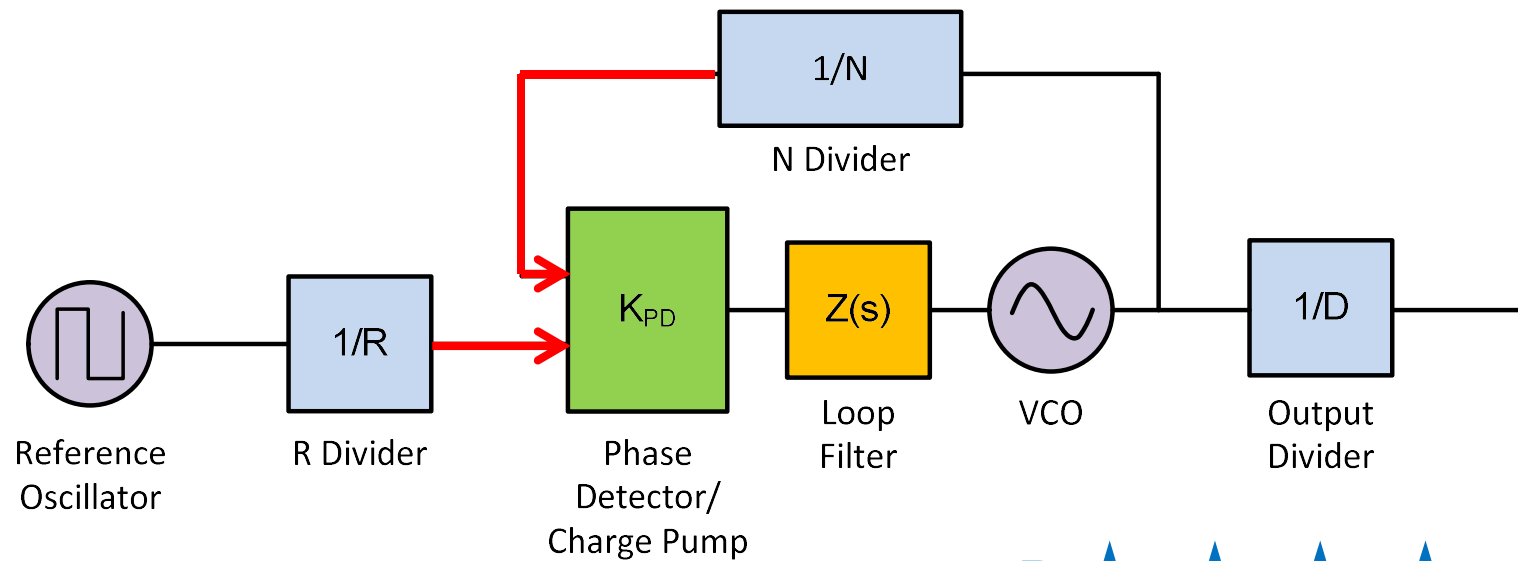


# PLL – Total PLL noise (in-band noise)

- Normalized PLL 1/f noise (Flicker noise)
  - Usually dominates at offset below 1 kHz
- Normalized PLL noise floor (FOM)
  - Determines phase noise at mid-range offset
- N-counter
  - Added noise =  $20\log(N)$
- Total noise determines PLL in-band noise

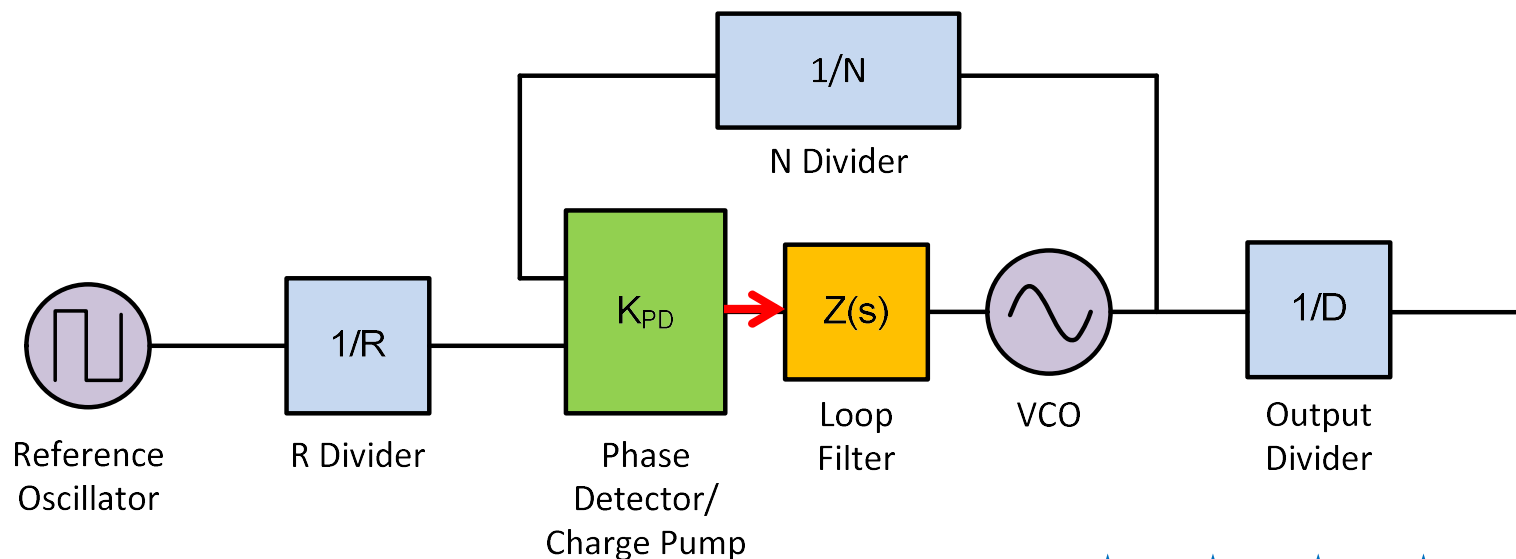


# Phase detector frequency, $f_{PD}$

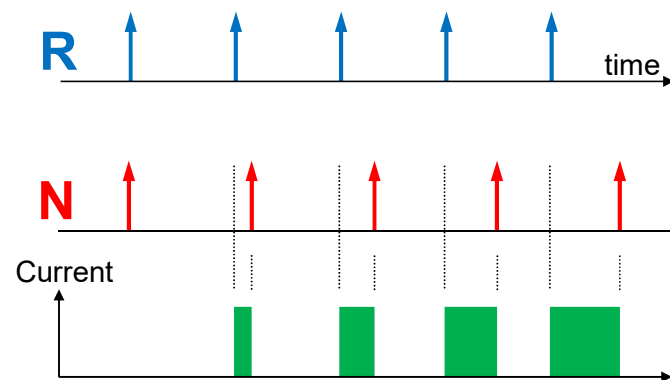


- $f_{PD} = \text{Reference clock frequency} / R$
- Rising edge of R-divider signal triggers phase comparison
- Max.  $f_{PD}$  is usually less than 300 MHz

# Charge pump current



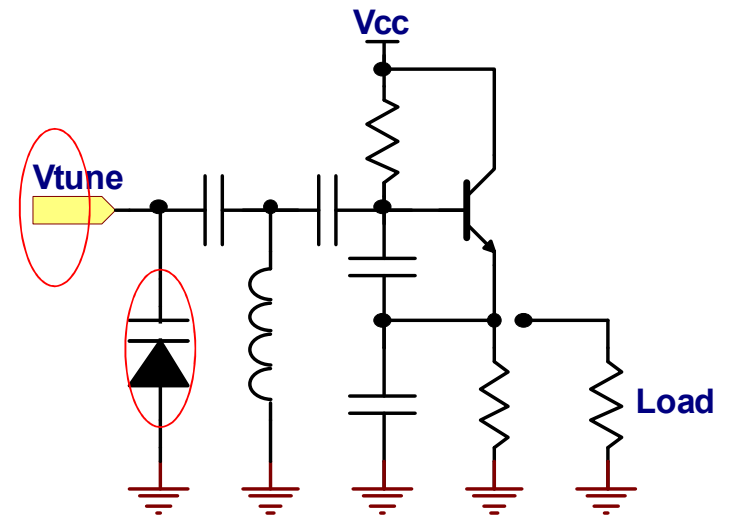
- Constant current source
- Turn-on time is variable
- Current is configurable
  - 100  $\mu$ A to a few mA per step





# VCO gain, $K_{VCO}$

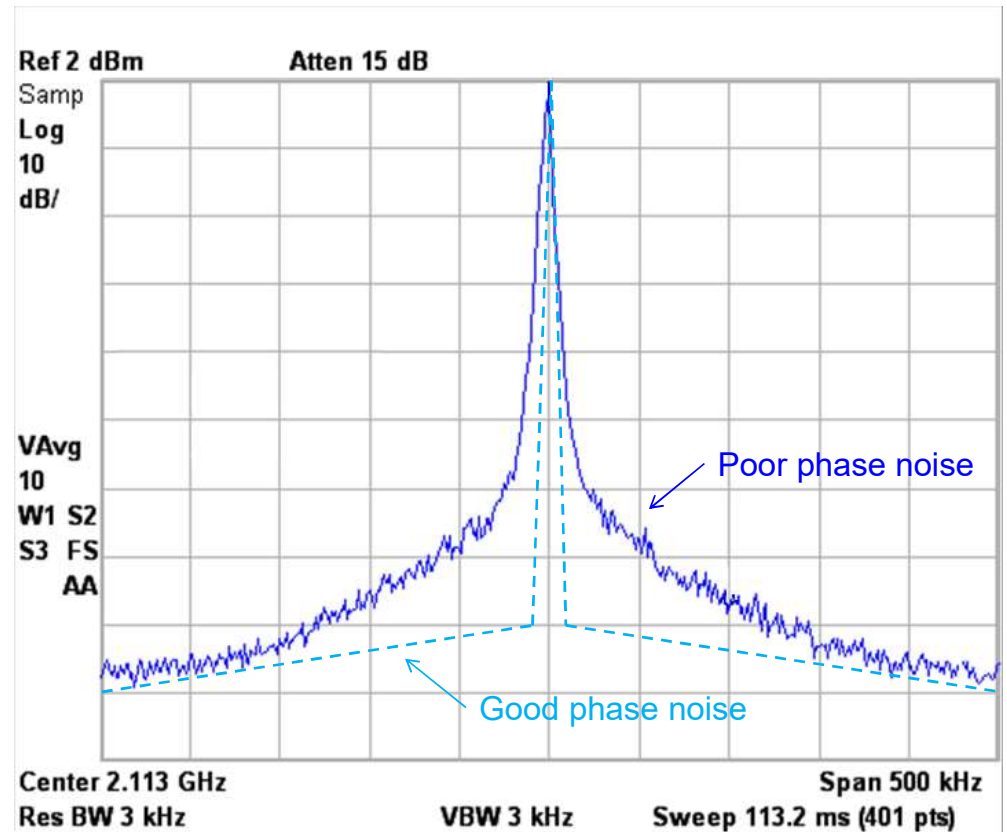
- Use a varactor diode to change the oscillator frequency
- Tuning range is limited
- $K_{VCO}$ 
  - Changes in frequency against  $V_{tune}$
  - Varies across the whole VCO tuning range
  - A few MHz/V to more than a 100 MHz/V



A typical Colpitts oscillator

# VCO phase noise

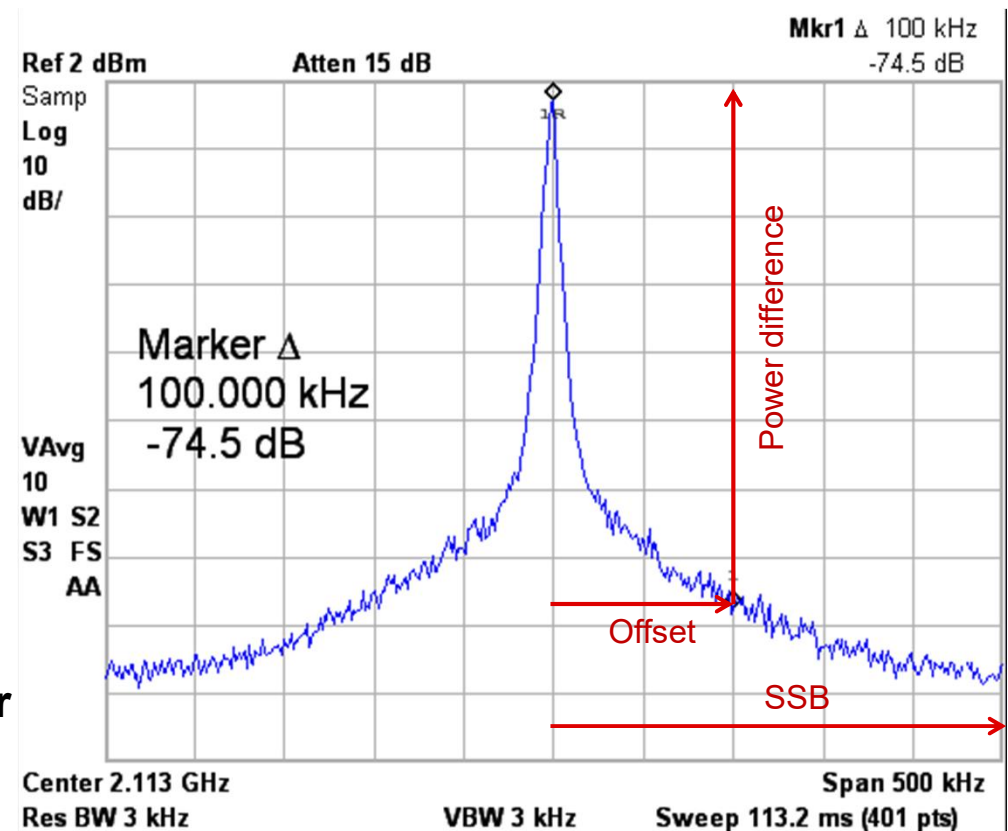
- Determines closed-loop far-out phase noise



# VCO phase noise

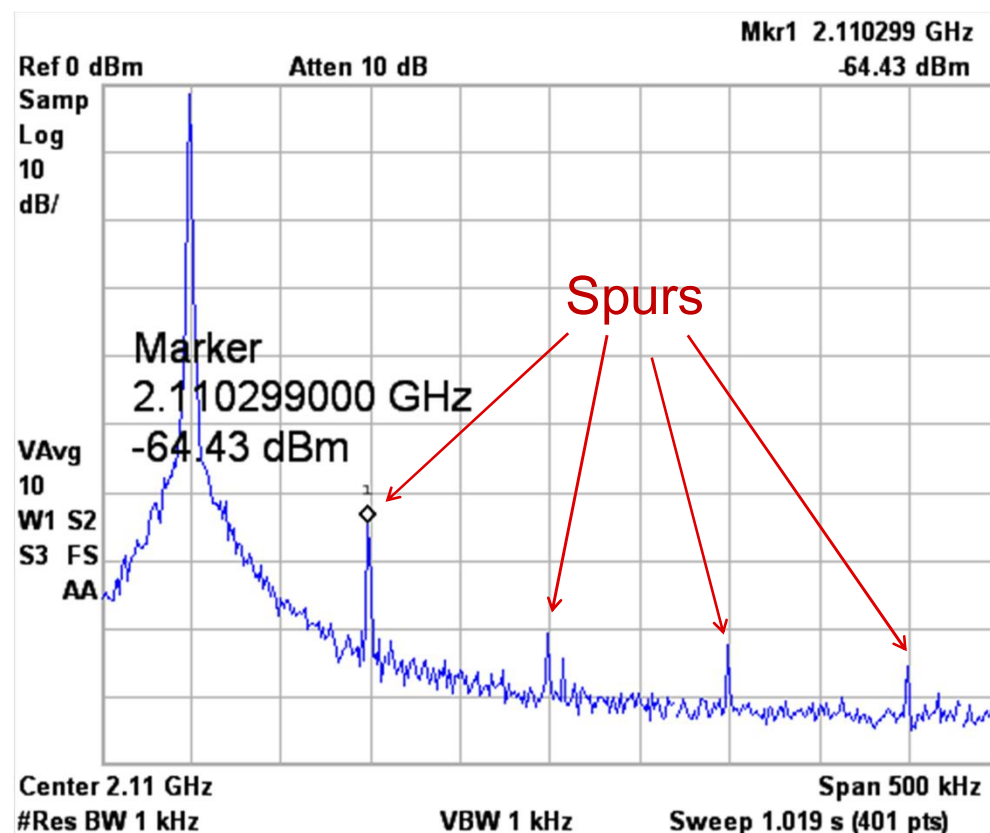
- Determines closed-loop far-out phase noise
- Phase noise
  - SSB power difference between the carrier and an offset, normalized in 1 Hz
  - Expressed in xx dBc/Hz@ yy Hz offset
  - Carrier frequency specific

**-121 dBc/Hz @ 100 kHz offset at 2.1 GHz carrier**



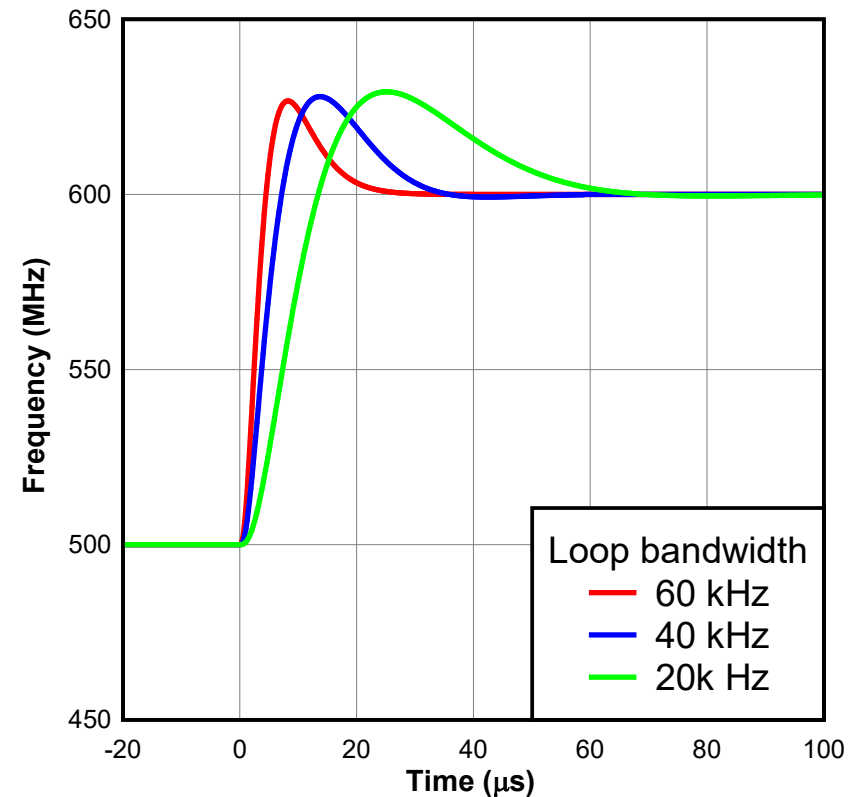
# Spurs

- Phase detector spurs
  - Offset =  $f_{PD}$
- Fractional spurs
  - Offset =  $N_{frac} \times f_{PD}$
- Sub-fractional spurs
  - $\frac{1}{2}$ ,  $\frac{1}{4}$  of fractional spurs
- Crosstalk spurs
  - Crosstalk between
    - Phase detector and VCO
      - Integer Boundary Spurs (IBS)
    - Phase detector and output
    - Reference clock and output
    - Reference clock and VCO

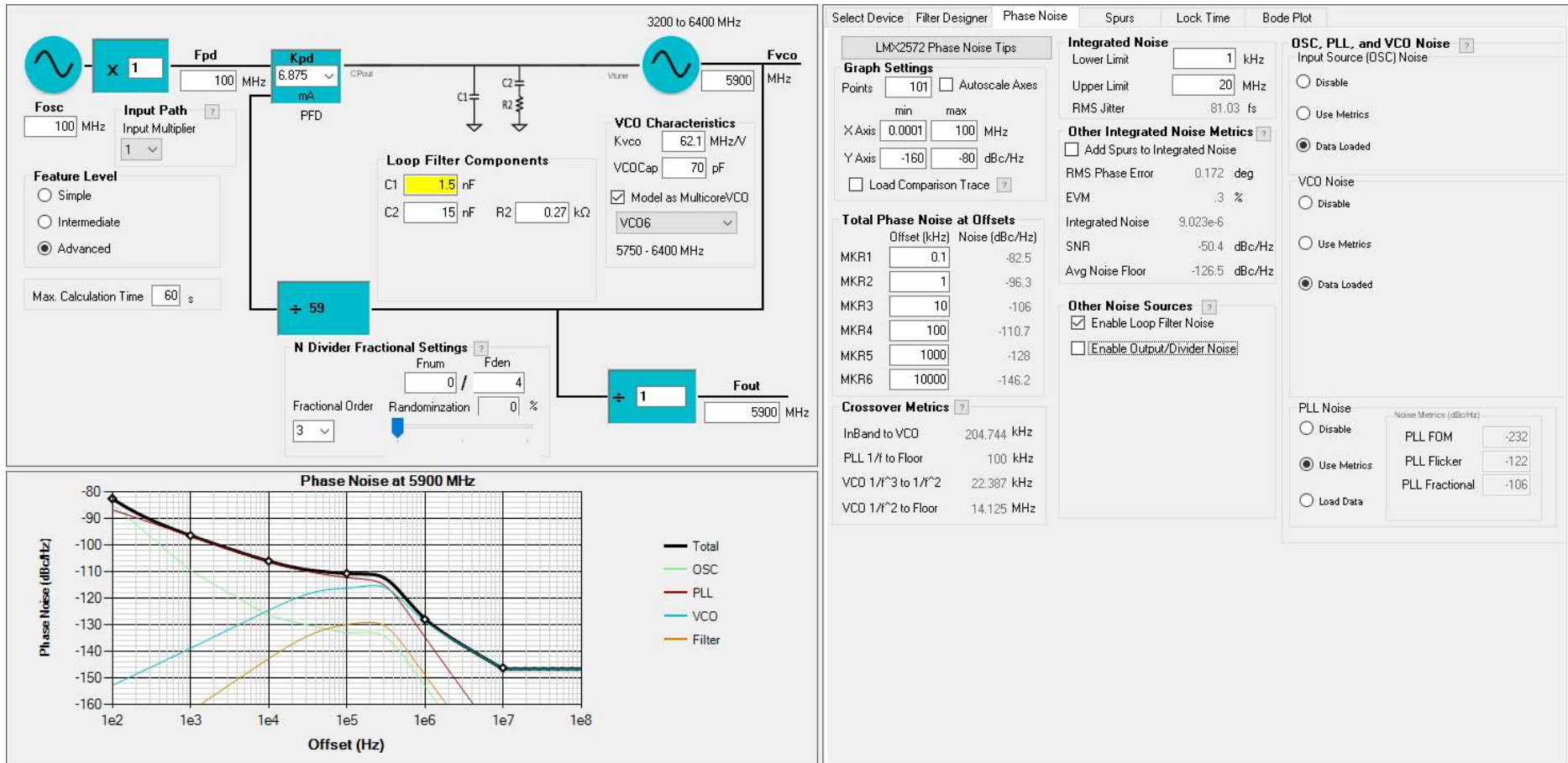


# Lock time

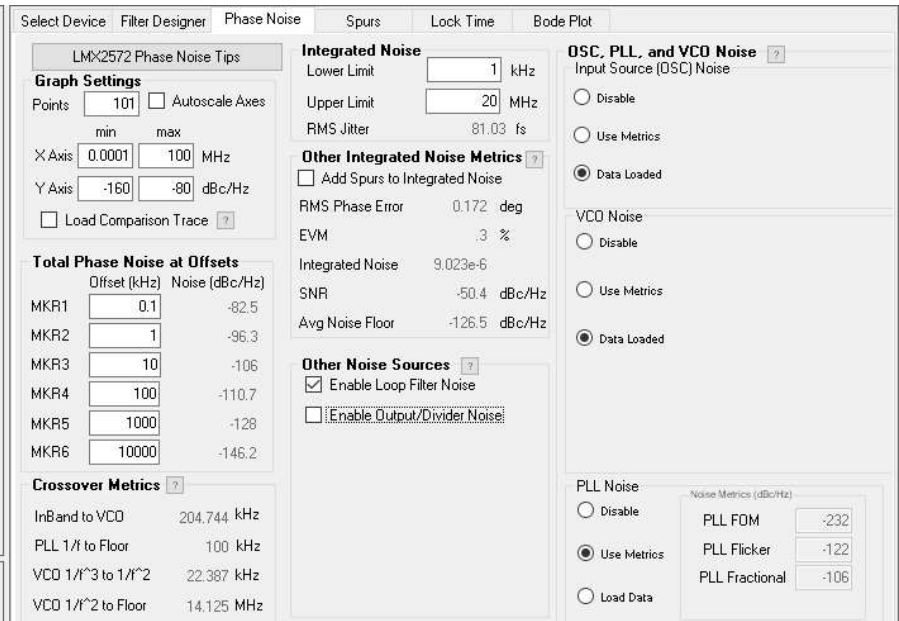
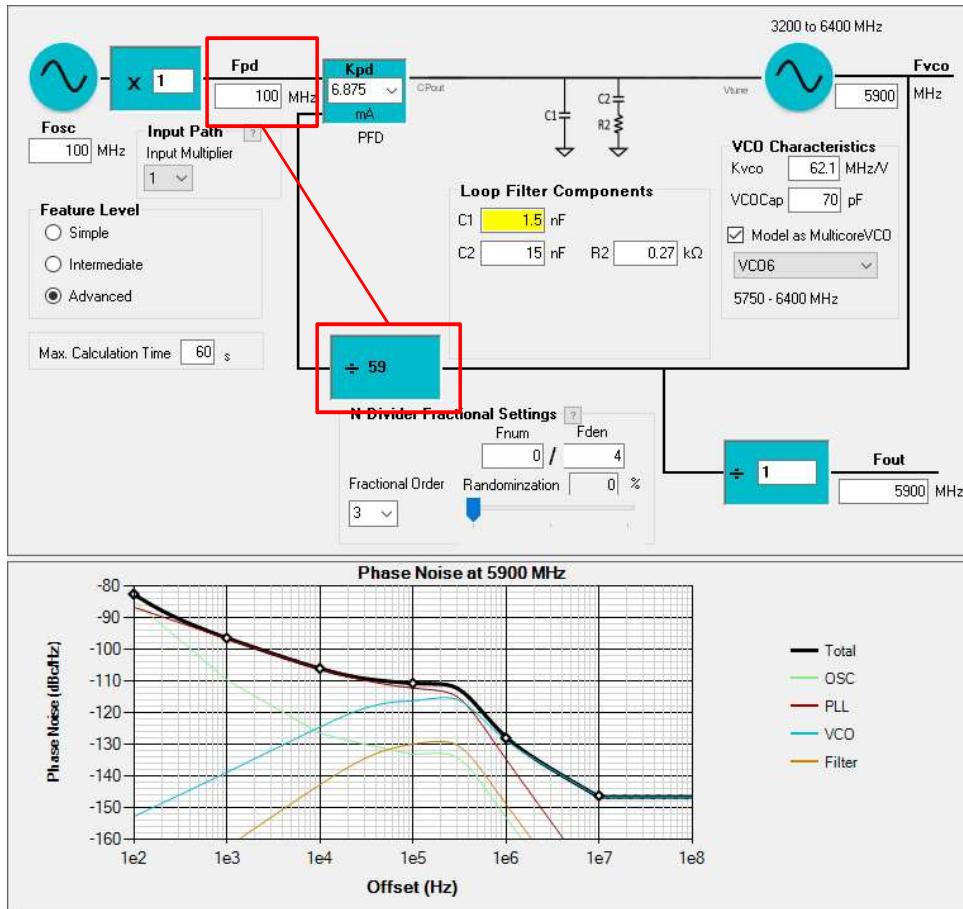
- Lock time is how long it takes to change one frequency to another and get within a certain frequency tolerance
- Wide loop bandwidth reduces lock time
- Lock time  $\cong 4 / \text{loop bandwidth}$



# Applying key parameters and specifications



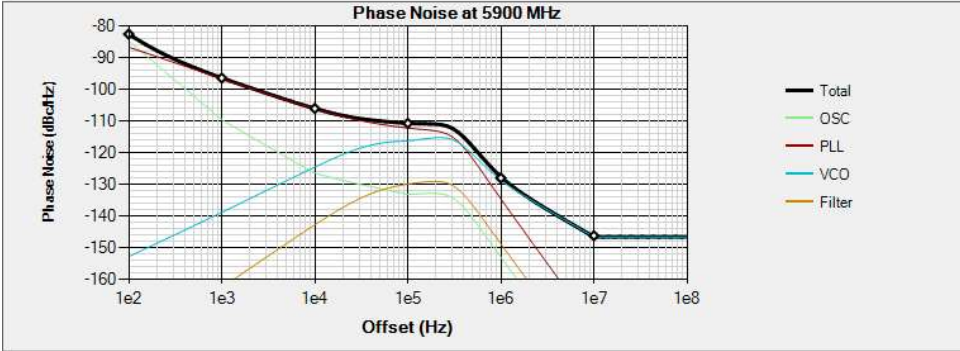
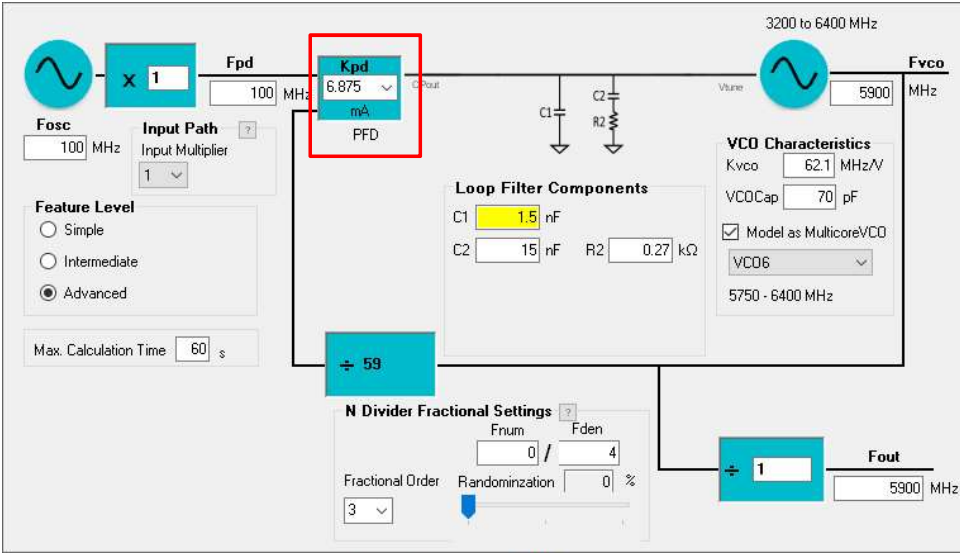
# Phase detector frequency



$f_{PD}$  determines N-divider value



# Charge pump current



The software interface displays the following analysis results for the LMx2572:

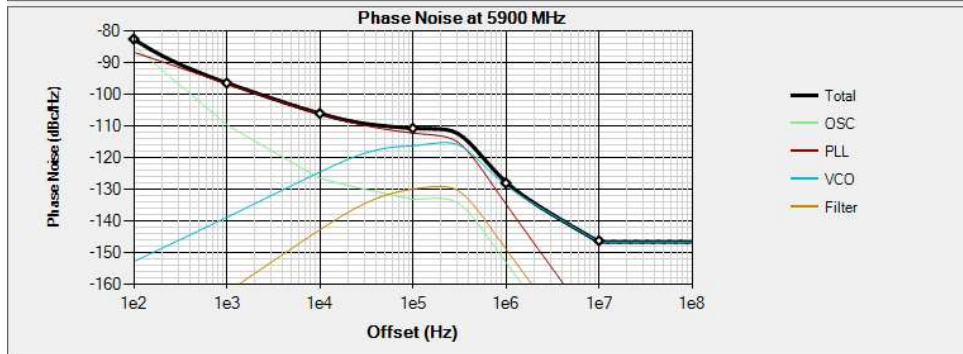
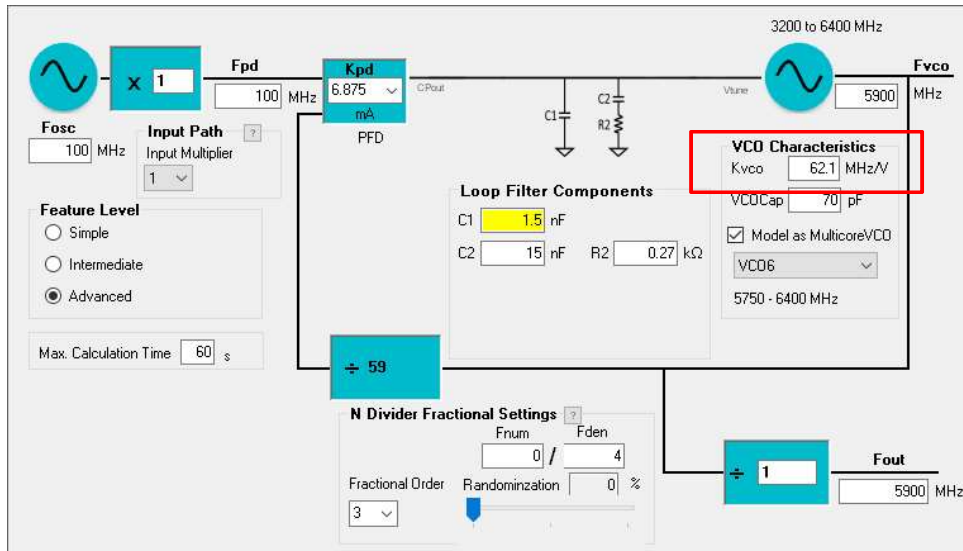
- Graph Settings:** Points = 101, X Axis = 0.0001 to 100 MHz, Y Axis = -160 to -80 dBc/Hz.
- Integrated Noise:** Lower Limit = 1 kHz, Upper Limit = 20 MHz, RMS Jitter = 81.03 fs.
- Other Integrated Noise Metrics:** RMS Phase Error = 0.172 deg, EVM = .3 %.
- Total Phase Noise at Offsets:**

Offset (kHz)	Noise (dBc/Hz)
MKR1 (0.1)	-82.5
MKR2 (1)	-96.3
MKR3 (10)	-106
MKR4 (100)	-110.7
MKR5 (1000)	-128
MKR6 (10000)	-146.2
- Crossover Metrics:**
  - InBand to VCO: 204.744 kHz
  - PLL 1/f to Floor: 100 kHz
  - VCO 1/f<sup>3</sup> to 1/f<sup>2</sup>: 22.387 kHz
  - VCO 1/f<sup>2</sup> to Floor: 14.125 MHz
- Other Noise Sources:**  Enable Loop Filter Noise,  Enable Output/Divider Noise.
- PLL Noise Metrics (dBc/Hz):**
  - PLL FOM: -232
  - PLL Flicker: -122
  - PLL Fractional: -106

# Charge pump gain



# VCO gain



Select Device Filter Designer Phase Noise Spurs Lock Time Bode Plot

LMX2572 Phase Noise Tips

**Graph Settings**  
 Points: 101 Autoscale Axes:   
 X Axis: min 0.0001 max 100 MHz  
 Y Axis: -160 -80 dBc/Hz  
 Load Comparison Trace

**Integrated Noise**  
 Lower Limit: 1 kHz  
 Upper Limit: 20 MHz  
 RMS Jitter: 81.03 fs

**Other Integrated Noise Metrics**  
 Add Spurs to Integrated Noise  
 RMS Phase Error: 0.172 deg  
 EVM: .3 %  
 Integrated Noise: 9.023e-6  
 SNR: -50.4 dBc/Hz  
 Avg Noise Floor: -126.5 dBc/Hz

**Other Noise Sources**  
 Enable Loop Filter Noise  
 Enable Output/Divider Noise

**OSC, PLL, and VCO Noise**  
 Input Source (OSC) Noise:  Disable  Use Metrics  
 VCO Noise:  Disable  Use Metrics  
 Data Loaded

**PLL Noise**  
 Disable  Use Metrics  Load Data

Noise Metrics (dBc/Hz):  
 PLL FOM: -232  
 PLL Flicker: -122  
 PLL Fractional: -106

**Total Phase Noise at Offsets**

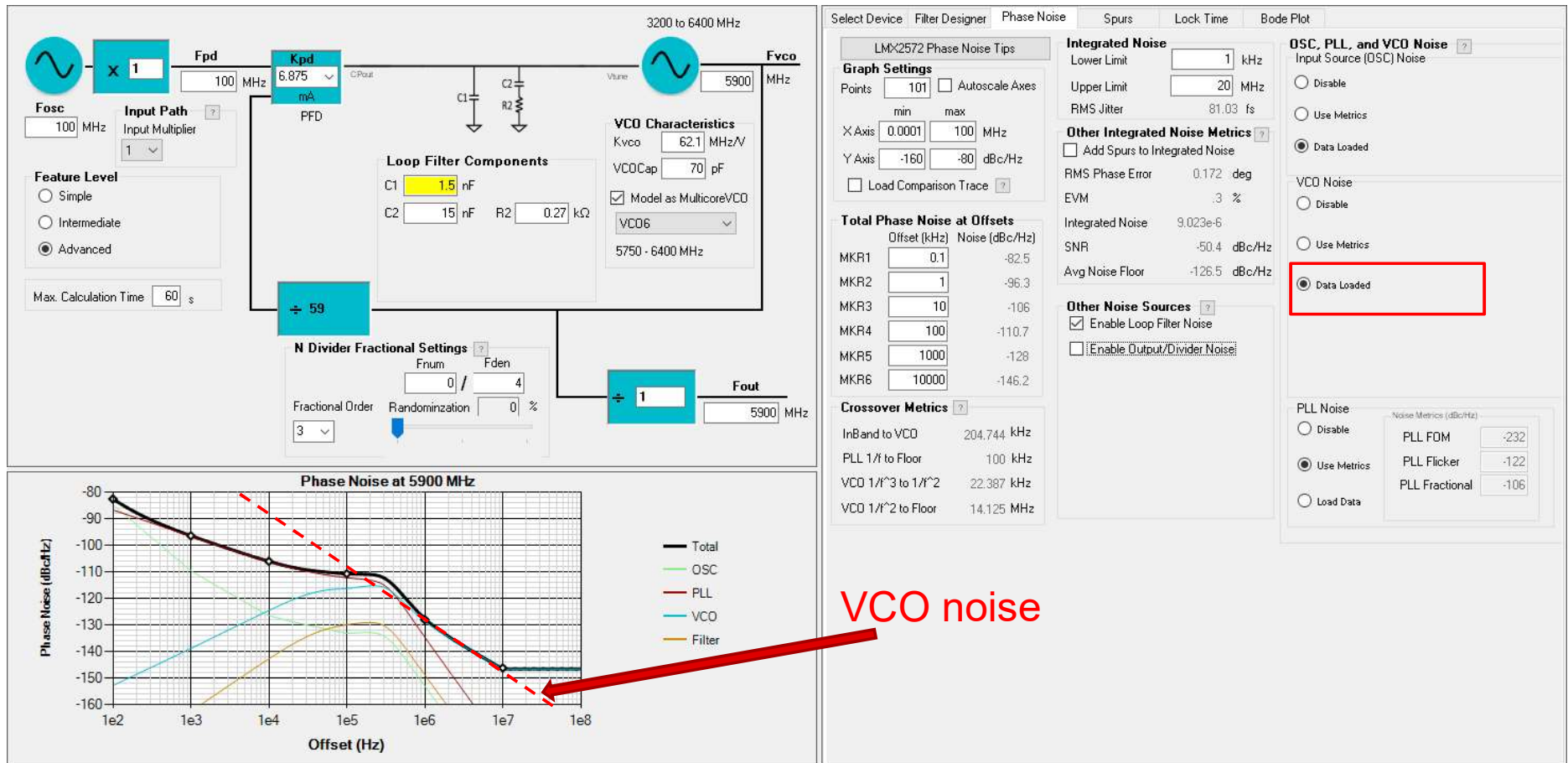
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MKR5: 1000	-128
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**Crossover Metrics**

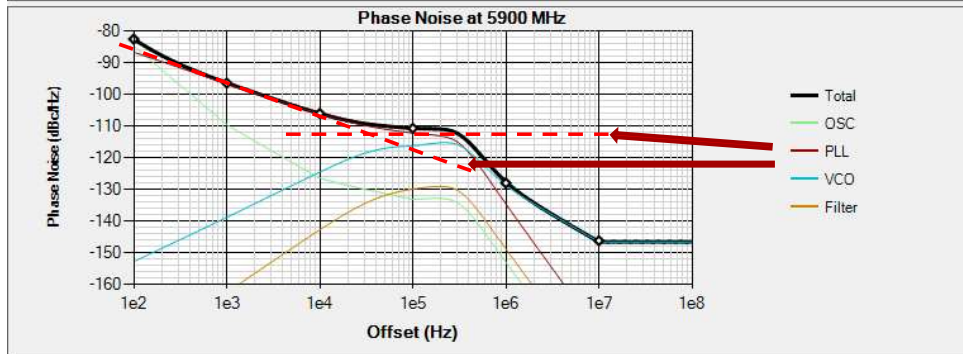
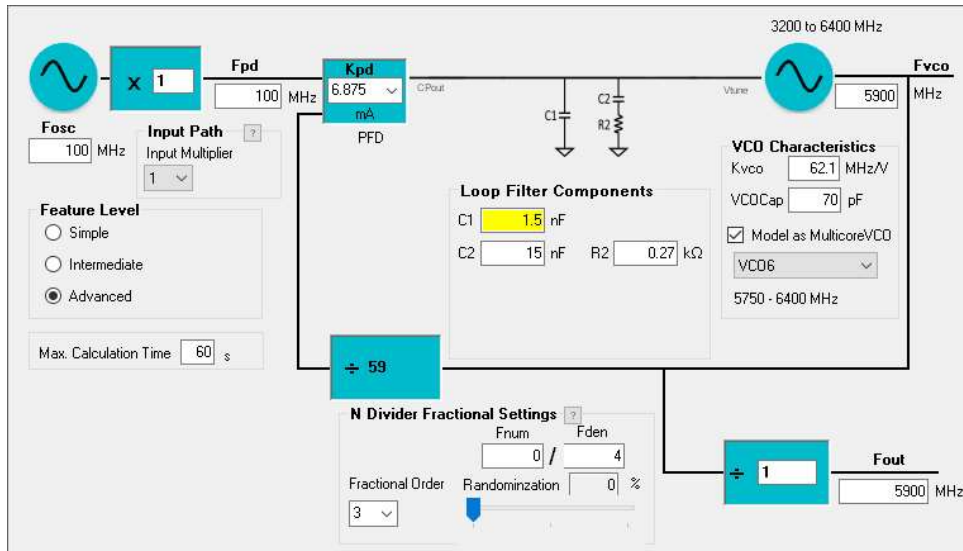
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VCO gain

# VCO phase noise



# PLL noise



Select Device: Filter Designer Phase Noise Spurs Lock Time Bode Plot

LMX2572 Phase Noise Tips

**Graph Settings**

Points: 101 Autoscale Axes:

X Axis: min 0.0001 max 100 MHz

Y Axis: -160 -80 dBc/Hz

Load Comparison Trace

**Integrated Noise**

Lower Limit: 1 kHz

Upper Limit: 20 MHz

RMS Jitter: 81.03 fs

**Other Integrated Noise Metrics**

Add Spurs to Integrated Noise

RMS Phase Error: 0.172 deg

EVM: .3 %

Integrated Noise: 9.023e-6

SNR: -50.4 dBc/Hz

Avg Noise Floor: -126.5 dBc/Hz

**Other Noise Sources**

Enable Loop Filter Noise

Enable Output/Divider Noise

**OSC, PLL, and VCO Noise**

Input Source (OSC) Noise

Disable

Use Metrics

Data Loaded

VCO Noise

Disable

Use Metrics

Data Loaded

**PLL Noise**

Disable

Use Metrics

Load Data

Noise Metrics (dBc/Hz)

PLL FOM: -232

PLL Flicker: -122

PLL Fractional: -106

**Total Phase Noise at Offsets**

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**Crossover Metrics**

InBand to VCO: 204.744 kHz

PLL 1/f to Floor: 100 kHz

VCO 1/f<sup>3</sup> to 1/f<sup>2</sup>: 22.387 kHz

VCO 1/f<sup>2</sup> to Floor: 14.125 MHz

PLL noise

To find more technical resources and search products, visit [ti.com/clocks](https://ti.com/clocks)

## Quiz

- True or false: VCO phase noise determines closed-loop close-in phase noise
- True or false: N-divider will increase PLL noise by  $20\log(N)$
- True or false: Phase detector is triggered by the rising edge of the N-divider signal
- True or false: Turn-on time of the charge pump is proportional to the phase difference between the signals from R-divider and N-divider
- True or false: Phase detector spur frequency is not predictable

# Quiz

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