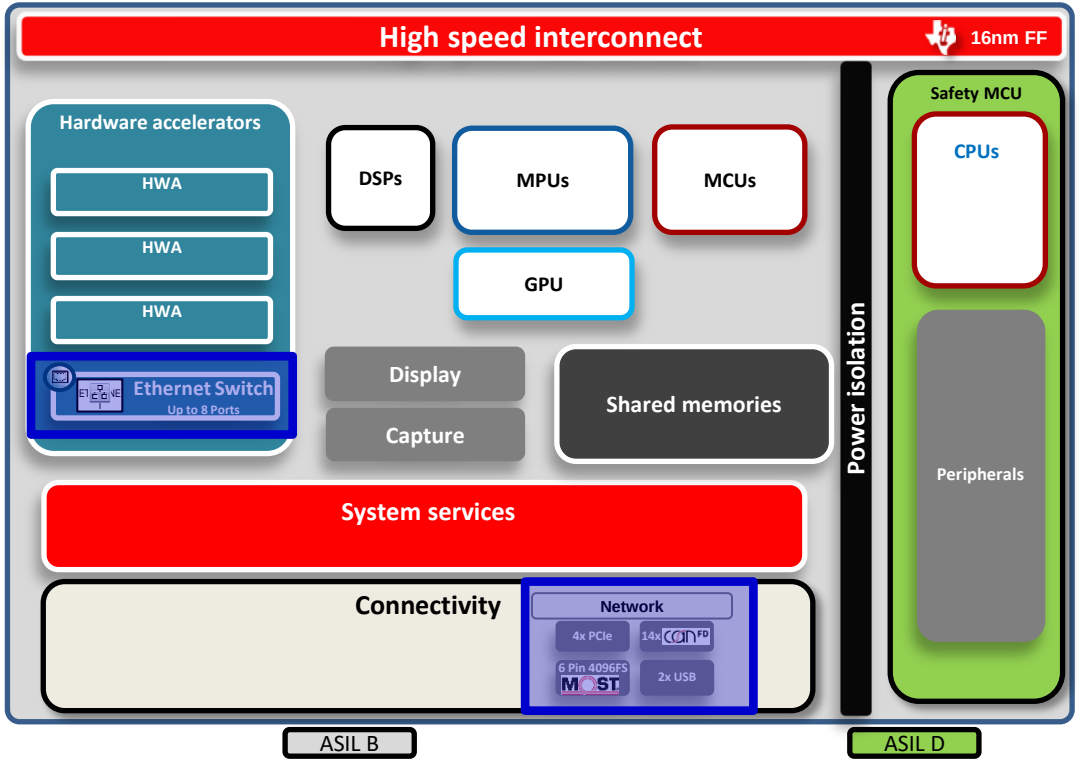
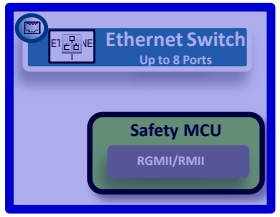
Jacinto™ 7 processors: network connectivity

Network connectivity

- Key features and benefits
- Heterogeneous processing cores
- Application-specific hardware accelerators
- Device management architecture
- Memory architecture and data movement
- Safety and isolation features
- Virtualization features
- Security features
- Power management features
- **Network connectivity**
- Flash and storage
- Serial connectivity

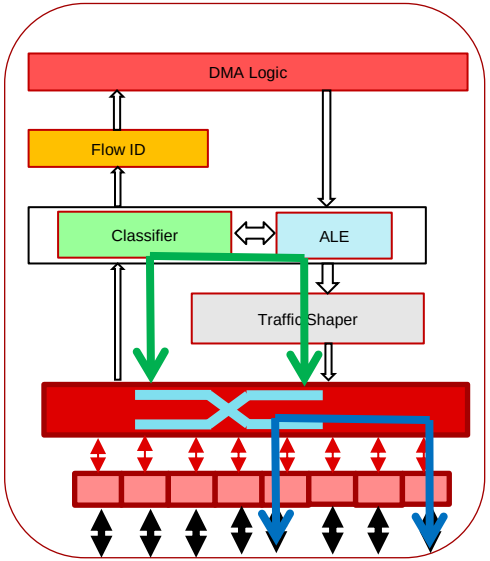


Network connectivity (Ethernet switch)

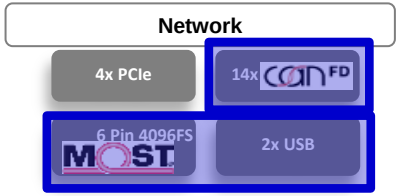


- Main Gigabit Ethernet switch (CPSW0):
  - Up to 8x external ports (SGMII, RGMII or RMII)
  - Up to 2x port QSGMII (4x 1Gb link on wire)
  - Each port 10/100/1000Mbps operation
  - Eight level Quality of Service (QoS)
  - Audio/Video Bridging (AVB) support
  - Time Sensitive Network support
  - Address Lookup Engine (ALE)
  - Inter-VLAN routing
  - Reset isolation with packet forwarding
  - Flexible SERDES I/O muxing with other protocols
- Safety MCU Gigabit Ethernet switch (CPSW0):
  - SW /feature compatible with Main domain switch
  - Single external port (RGMII or RMII) multiplexed
  - Up to 10/100/1000Mbps operation

Ethernet switch subsystem

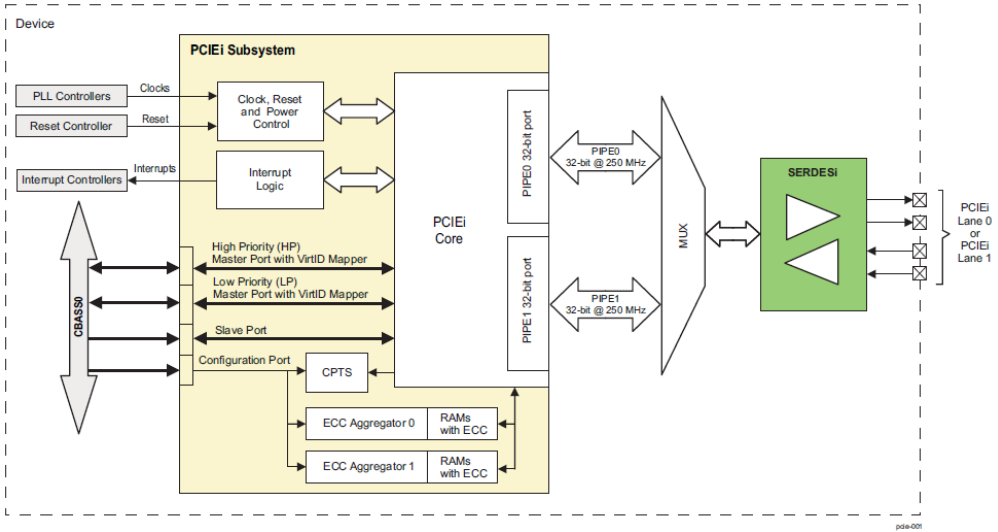


Network connectivity (PCIe)



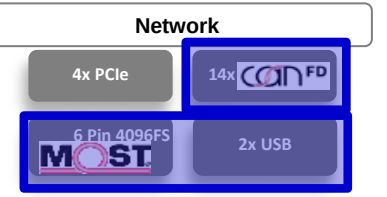
Peripheral Component Interconnect Express (PCIe) subsystem

- 4x instances of multi-lane, dual-mode PCIe Gen3 controller:
  - Rev4.0 compliance up to Gen3 speed up to 1/2/4 lane(s)
  - Max read request 4k with payload up to 256Byte
  - Root Complex (RC) or End Point (EP) modes
  - Address Translation Services (ATS)
  - Single-Root I/O Virtualization (SR-IOV)
    - Six Physical Functions (PF)
    - Sixteen Virtual Functions (VF)
      - 4 VF for each of PF0-3
      - 0 VF for PF4-5
    - Address translation via SMMU or PVU
  - 4 transaction class, 4 virtual channels for prioritization
    - High/low priority physical ports for quality of service *(not all derivatives)*
  - 32 outbound address translation regions (up to 4GB)
  - Precision Time Measurement (PTM)

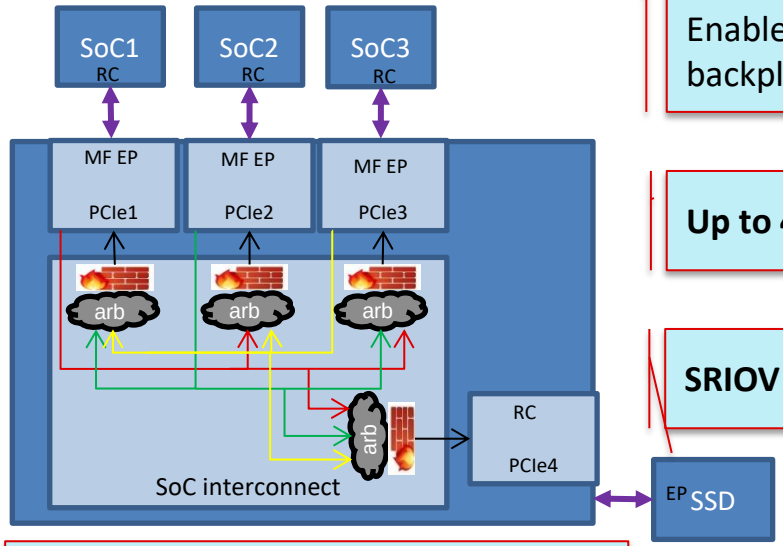


- External or internal 100MHz PCIe compliant reference clock: Separate Reference Clock with Independent Spread (SRIS)
- Flexible SERDES I/O muxing with other protocols (Ethernet, USB3.0)

Network connectivity (PCIe switching)



Non-Transparent Bridge (NTB) integration
Enables multi-SOC communication over PCIe backplane.



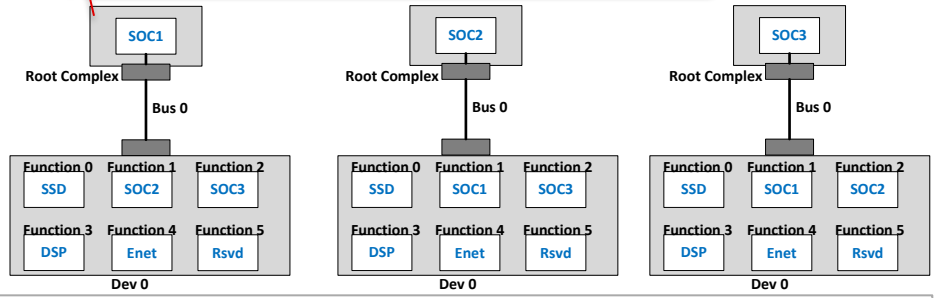
Up to 4 ports (Gen3/4)

SRIOV support enables shared SSD

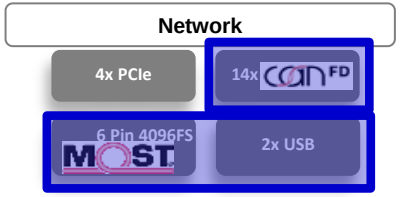
Auto-qualified and ASIL-B safety

Zero CPU and DDR bandwidth loading

Software view



Network connectivity



- Controller Area Network (CAN) interface:
  - 14x instances in Main domain and 2x instances in Safety MCU domain
  - Conforms to CAN Protocol 2.0 A, B and ISO 1189-1:2015
    - Classic CAN support
    - CAN FD (Flexible Data rate) support
  - Baud rates >1Mbps depending on transceivers
  - Parity /ECC (on message RAM) for safety
- USB:
  - 2x ports supporting USB2.0 and USB3.0 up to 5Gbps
  - xHCI1.0 compliant with internal DMA
  - Type-C internal lane swap support
  - Host Negotiation Protocol (HNP) and Dual-Role Device (DRD) capable
  - Flexible multiplexing with other SERDES I/O protocols (PCIe/Ethernet)
- Media Local Bus (MediaLB/MediaLB+) interface:
  - Connection to external Media Oriented Systems Transport (MOST) controllers
  - 3-pin mode to MOST50 and 6-pin up to MOST150

For more information

- For more training on Jacinto 7 processors: http://training.ti.com/jacinto7
- Download Processor SDK Automotive for Jacinto 7 processors: http://www.ti.com/tool/PROCESSOR-SDK-DRA8X-TDA4X
- Order TDA4VM Jacinto Automotive processors for ADAS & autonomous vehicles: http://www.ti.com/product/TDA4VM
- Order the TDA4VMx evaluation module: http://www.ti.com/tool/TDA4VMXEVM
- Order DRA829V Jacinto Automotive processors for gateway & vehicle compute: http://www.ti.com/product/DRA829V
- Order the DRA829Vx evaluation module: http://www.ti.com/tool/DRA829VXEVM
- For questions regarding topics covered in this training, visit the processors support forum at the TI E2E Community website: https://e2e.ti.com