

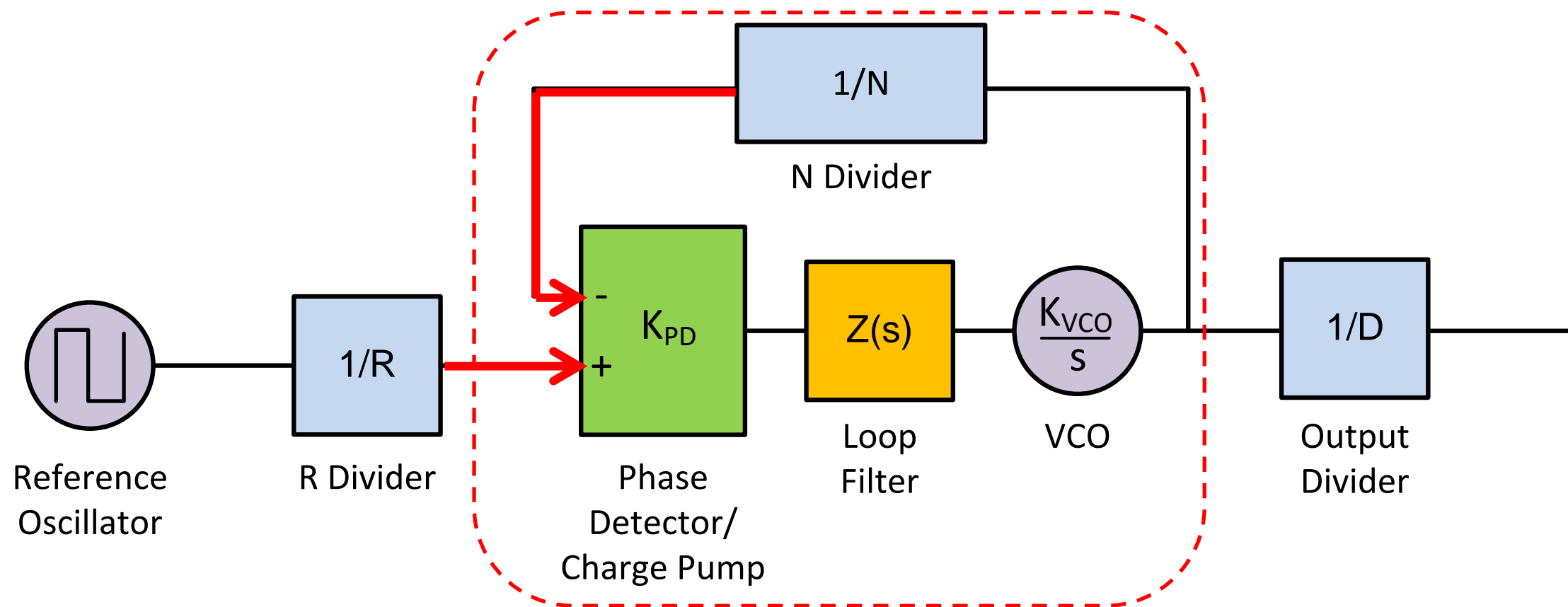
PLL Phase Noise Figures of Merit

TI Precision Labs – Clocks and Timing

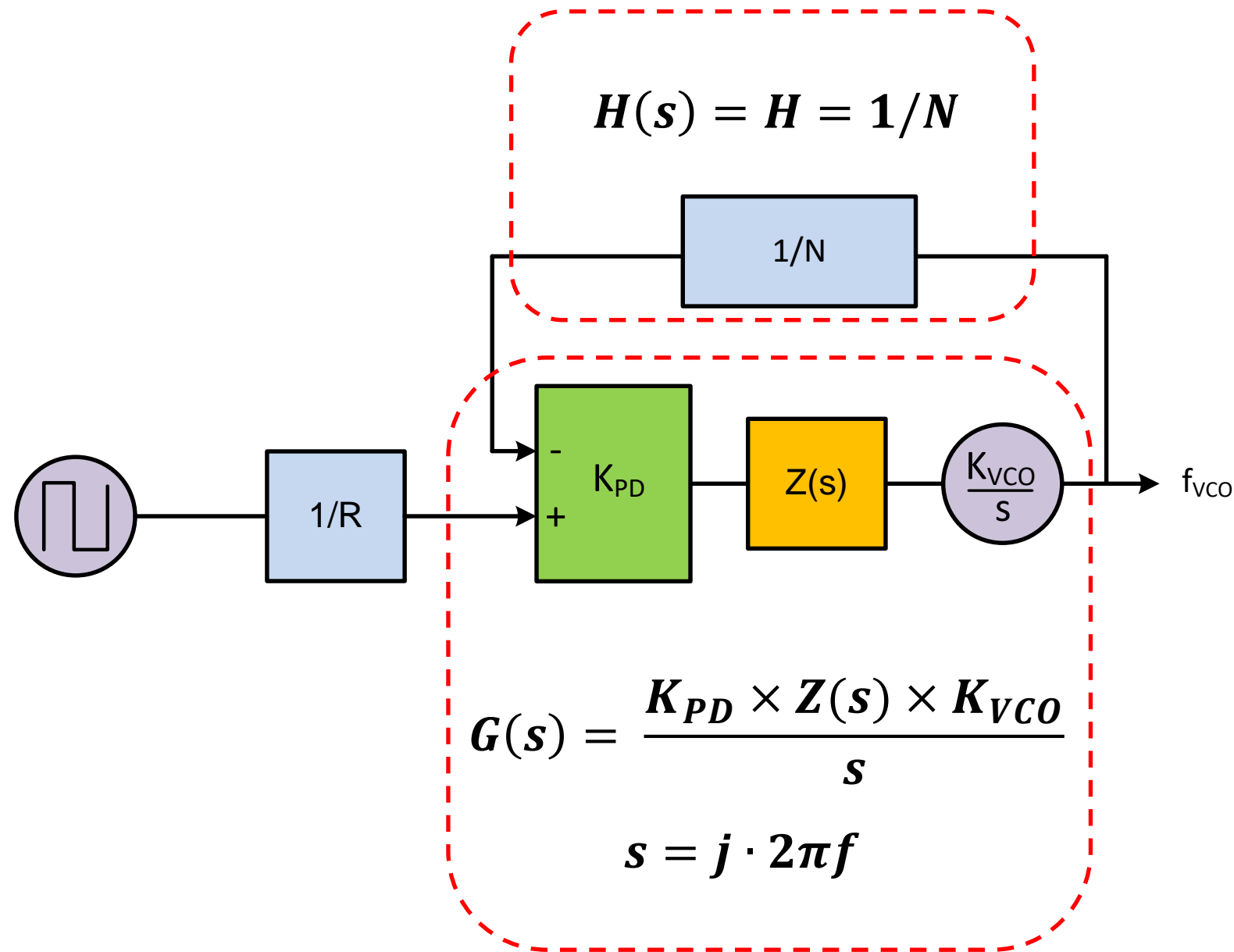
Presented by Dean Banerjee

Prepared by Liam Keese

Phase lock loop (PLL) overview

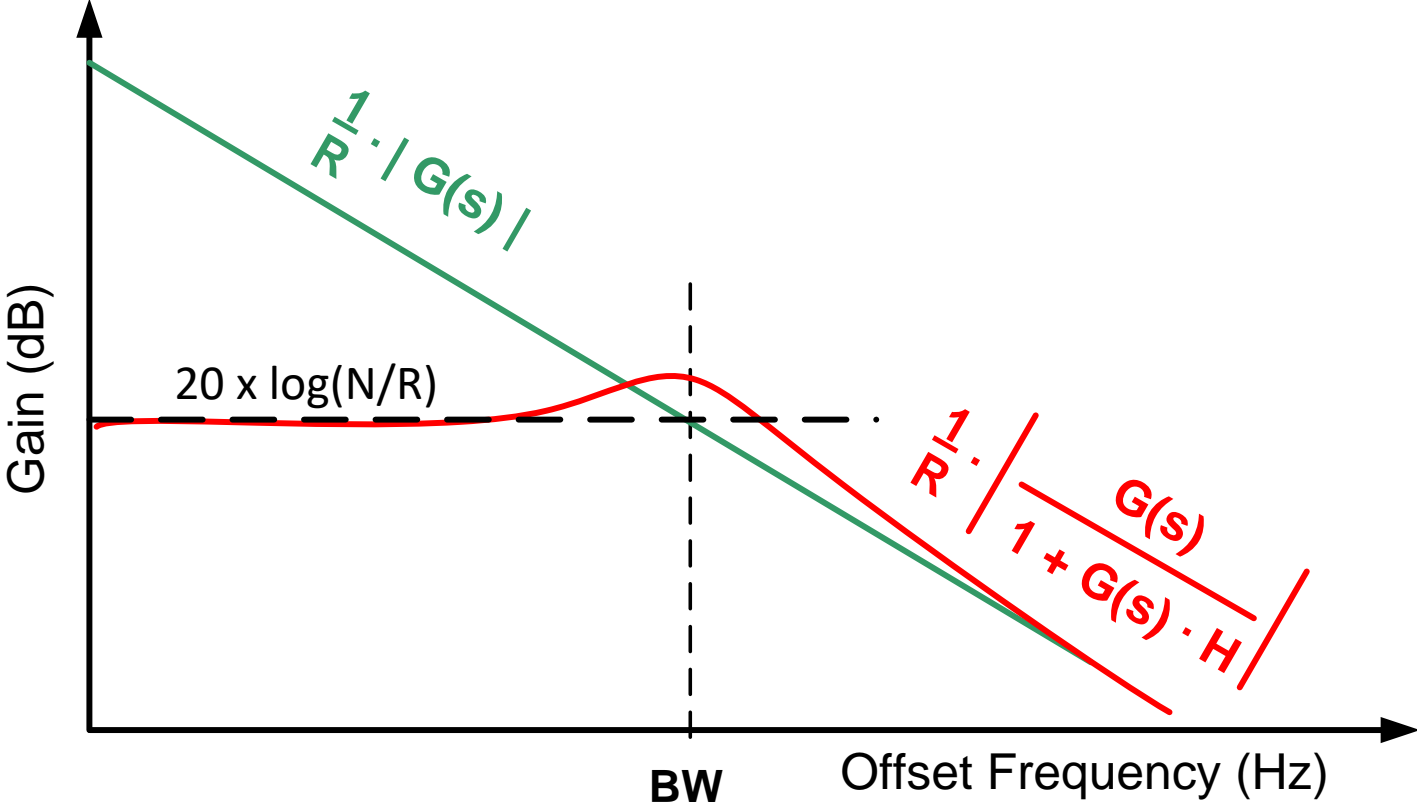


Phase lock loop (PLL) transfer functions



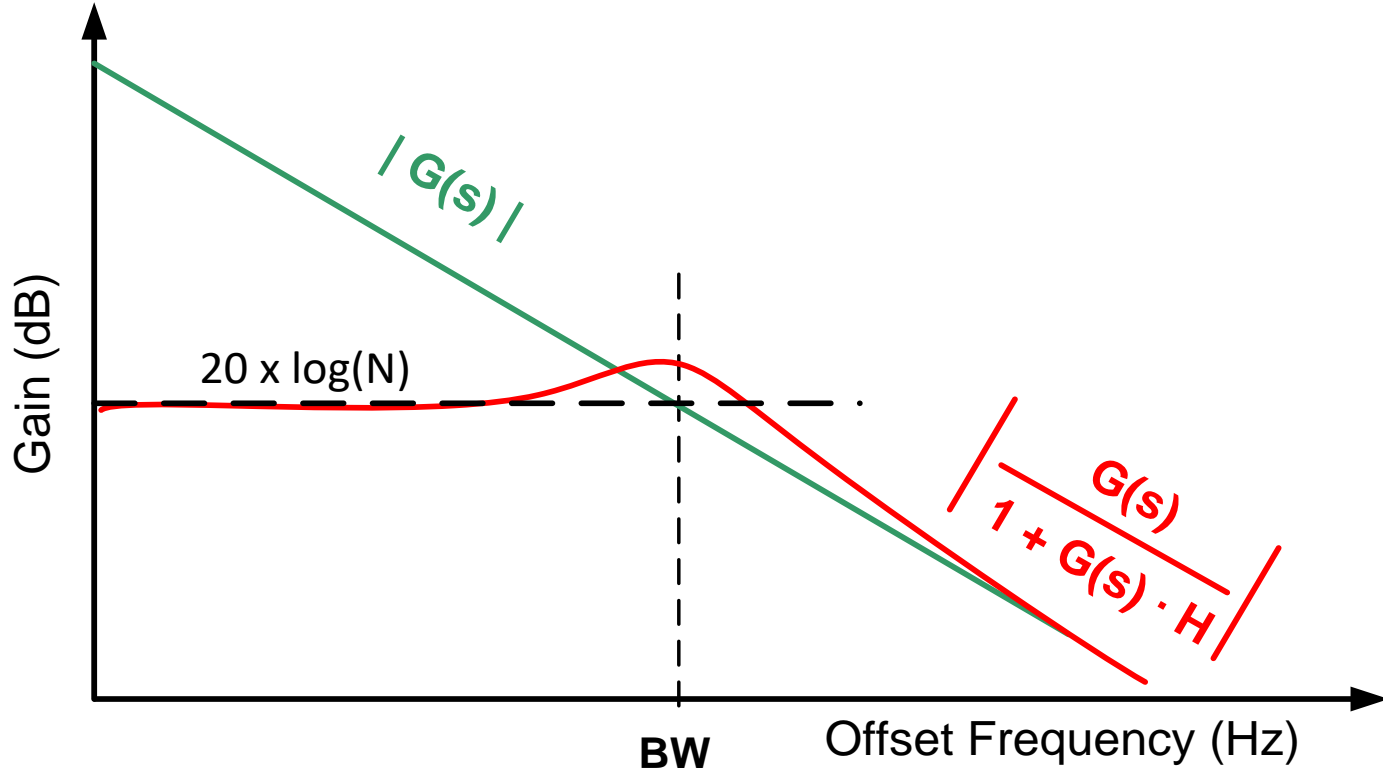
Block	Transfer Function
OSC	$\frac{1}{R} \cdot \frac{G(s)}{1 + G(s) \cdot H}$
R/N Dividers	$\frac{G(s)}{1 + G(s) \cdot H}$
Phase Detector	$\frac{1}{K_{PD}} \cdot \frac{G(s)}{1 + G(s) \cdot H}$
VCO	$\frac{1}{1 + G(s) \cdot H}$

Reference oscillator noise transfer function



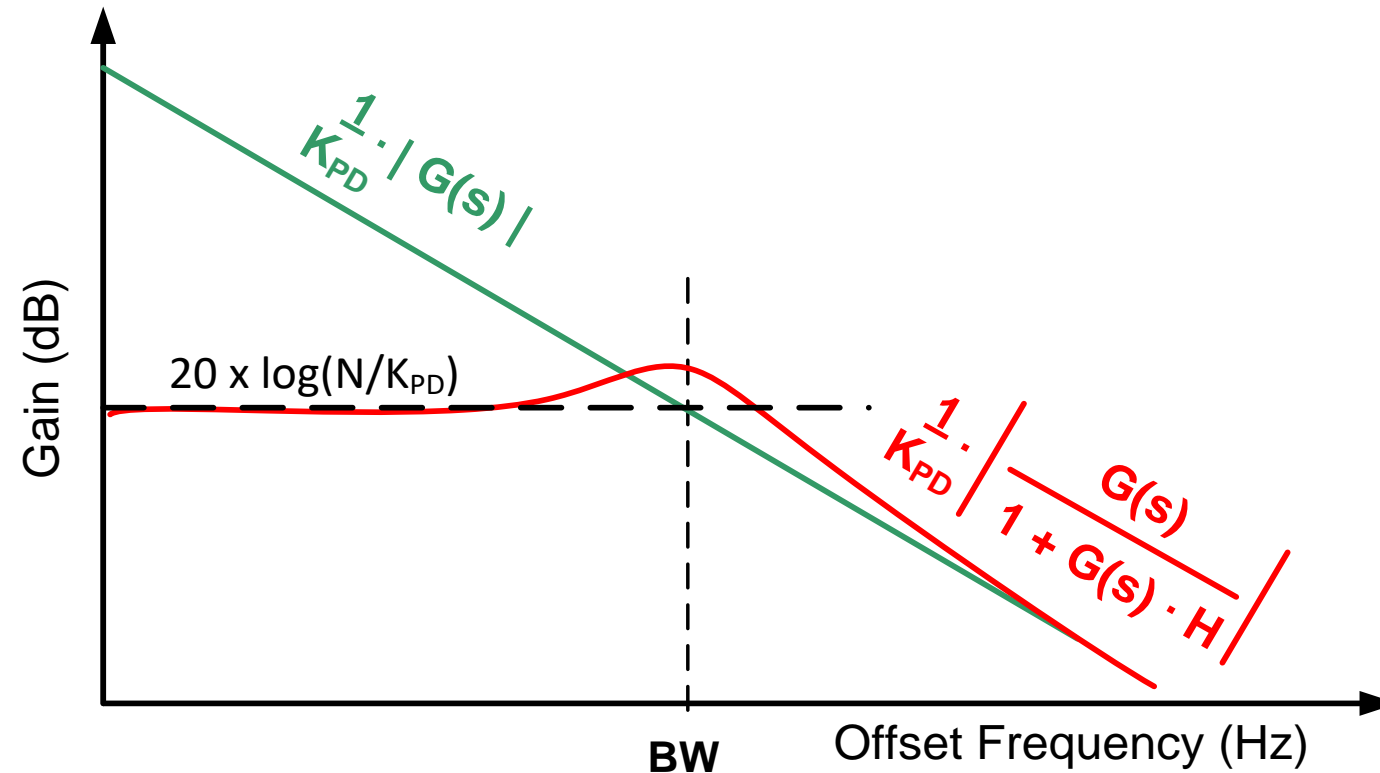
Block	Transfer Function	Response	Low Frequency Response	High Frequency Response
OSC	$\frac{1}{R} \cdot \frac{G(s)}{1 + G(s) \cdot H}$	Low Pass	$20 \cdot \log(N/R)$	$20 \cdot \log(G(s)/R)$

Feedback N divider noise transfer function



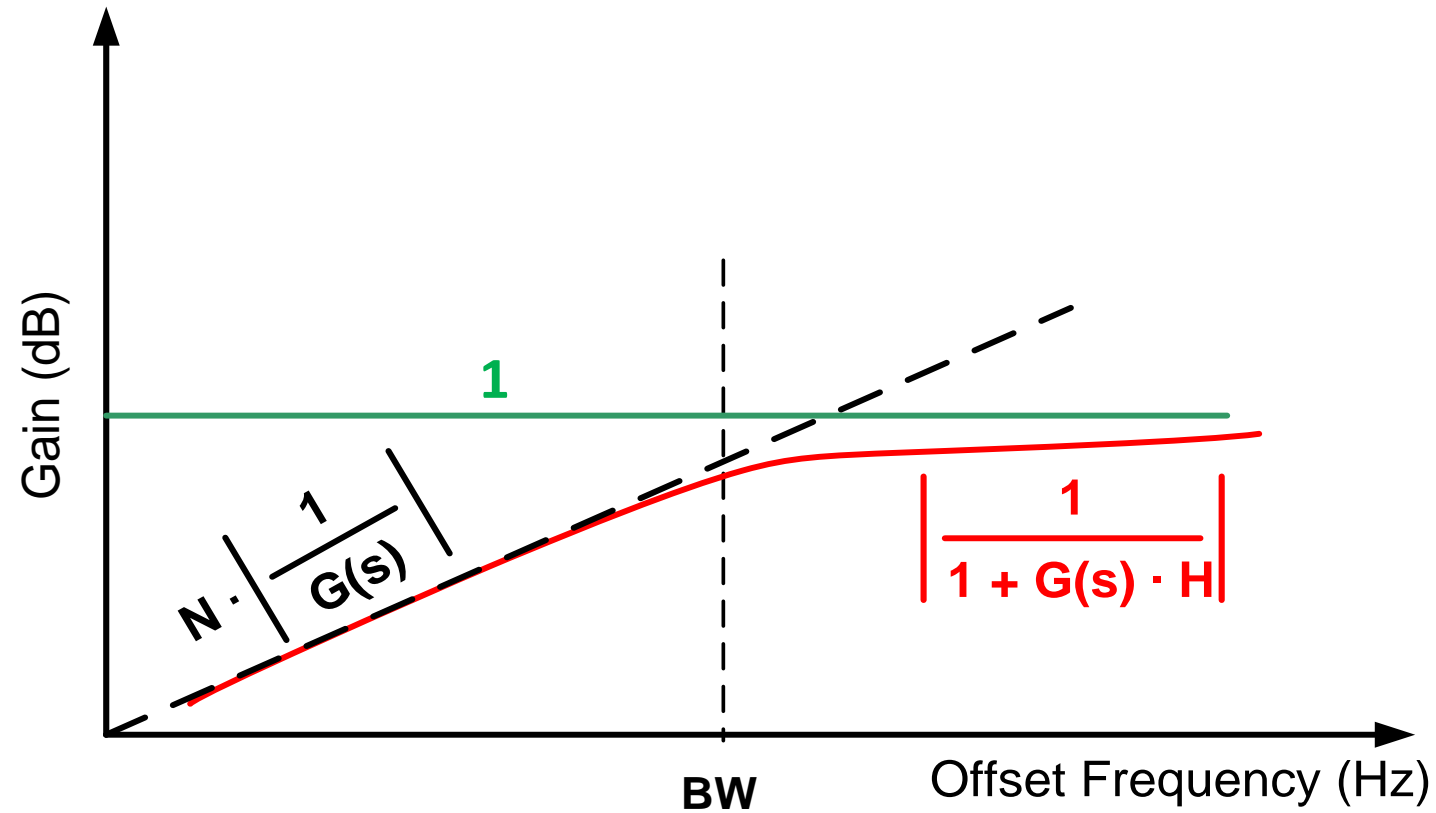
Block	Transfer Function	Response	Low Frequency Response	High Frequency Response
N (or R) Divider	$\frac{G(s)}{1 + G(s) \cdot H}$	Low Pass	$20 \cdot \log(N)$	$20 \cdot \log(G(s))$

Phase det./charge pump noise transfer function



Block	Transfer Function	Response	Low Frequency Response	High Frequency Response
Phase Det./ CP gain	$\frac{1}{K_{PD}} \cdot \frac{G(s)}{1 + G(s) \cdot H}$	Low Pass	$20 \cdot \log(N/K_{PD})$	$20 \cdot \log(G(s)/K_{PD})$

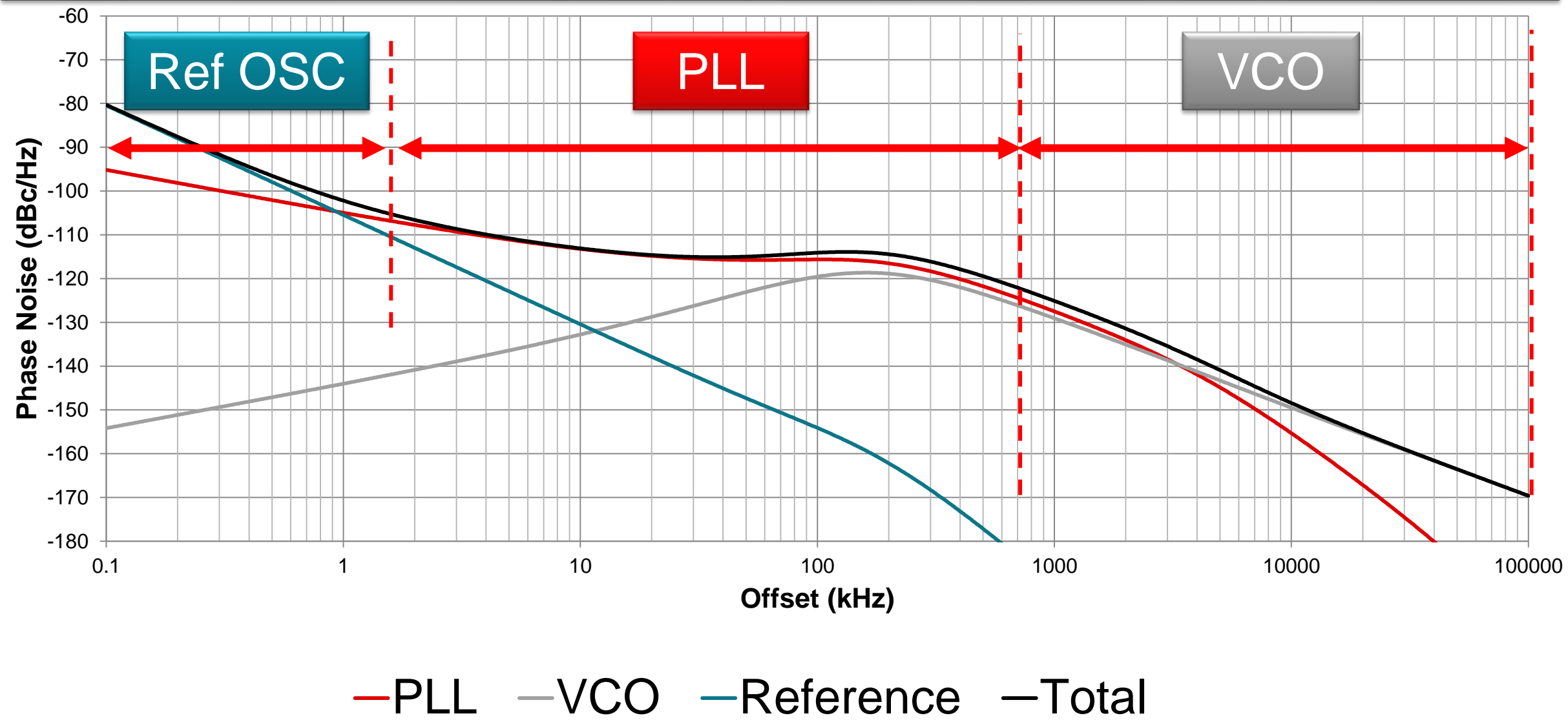
VCO noise transfer function



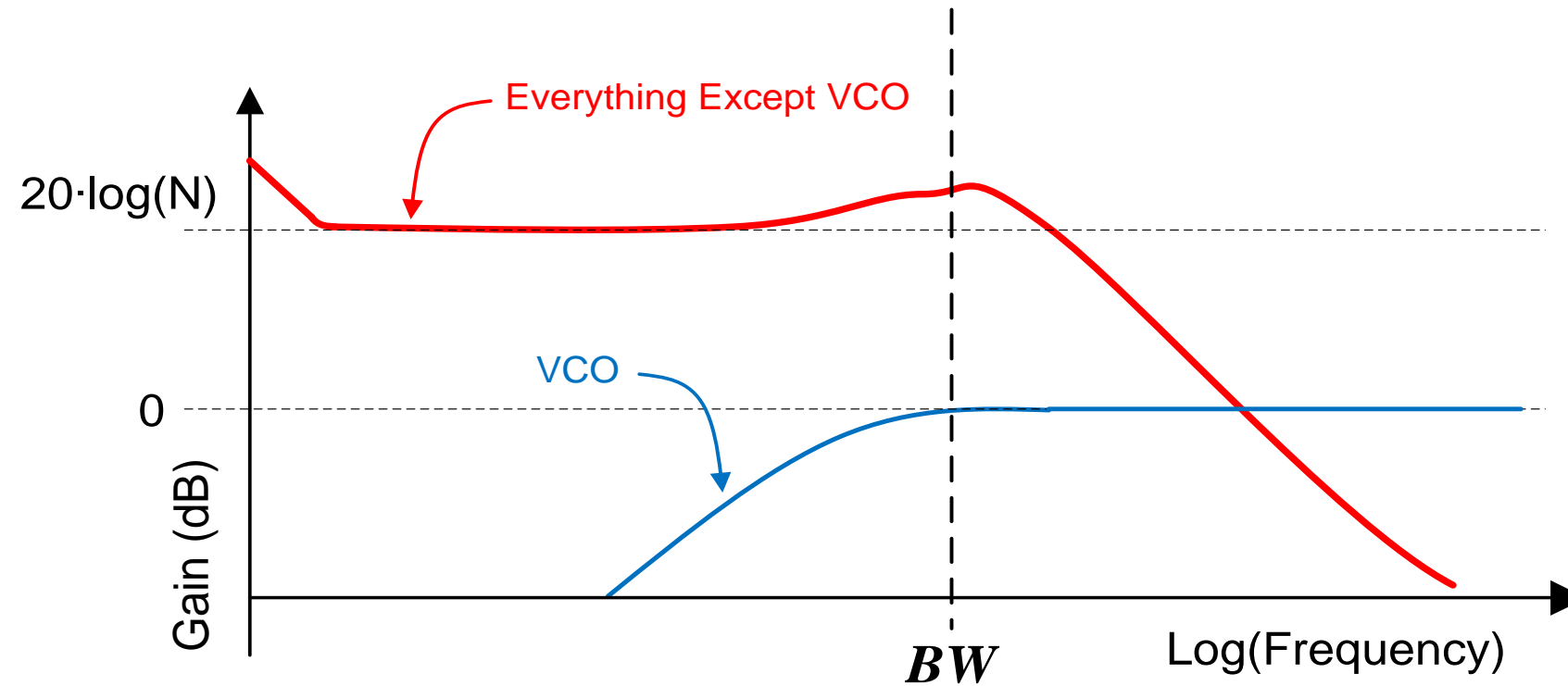
Block	Transfer Function	Response	Low Frequency Response	High Frequency Response
VCO	$\frac{1}{1 + G(s) \cdot H}$	High Pass	$-20 \cdot \log(G(s))$	1

PLL closed loop noise sources

The size of these regions will change depending on loop bandwidth

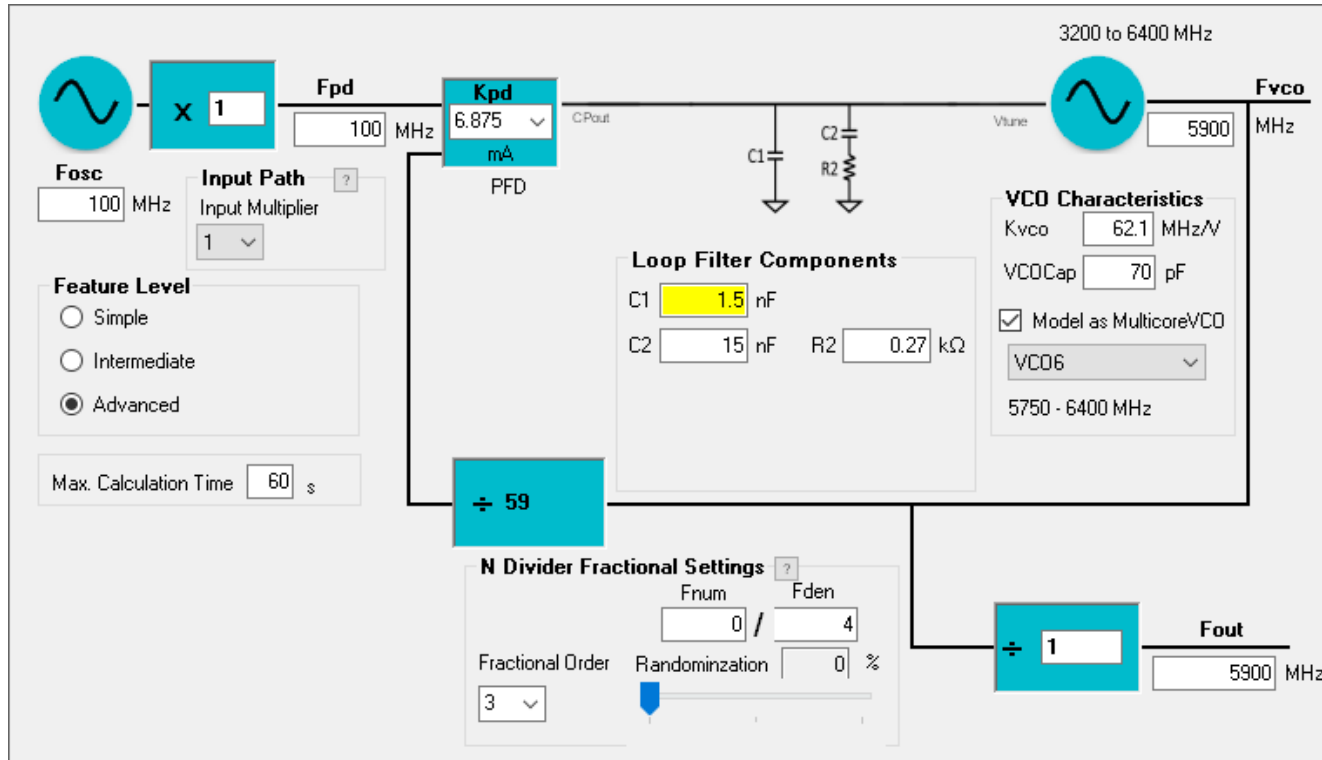


PLL normalized phase noise



- PLL flat noise FOM (PN1Hz)
 - PLL noise floor normalized to 1 Hz
 - N-counter added noise = $20 \log(N)$
- PLL flicker noise (PN10kHz)
 - Usually dominates at offset below 1 kHz
 - PLL $1/f$ normalized to 1 GHz output and 10kHz offset

PLL noise simulation



Select Device | Filter Designer | **Phase Noise** | Spurs | Lock Time | Bode Plot

LMX2572 Phase Noise Tips

Graph Settings
 Points: 101 | Autoscale Axes:
 X Axis: min 0.0001, max 100 MHz
 Y Axis: -160 to -80 dBc/Hz
 Load Comparison Trace

Integrated Noise
 Lower Limit: 1 kHz
 Upper Limit: 20 MHz
 RMS Jitter: 81.03 fs

Other Integrated Noise Metrics
 Add Spurs to Integrated Noise
 RMS Phase Error: 0.172 deg
 EVM: .3 %
 Integrated Noise: 9.023e-6
 SNR: -50.4 dBc/Hz
 Avg Noise Floor: -126.5 dBc/Hz

Other Noise Sources
 Enable Loop Filter Noise
 Enable Output/Divider Noise

OSC, PLL, and VCO Noise
 Input Source (OSC) Noise:
 Disable
 Use Metrics
 Data Loaded
 VCO Noise:
 Disable
 Use Metrics
 Data Loaded

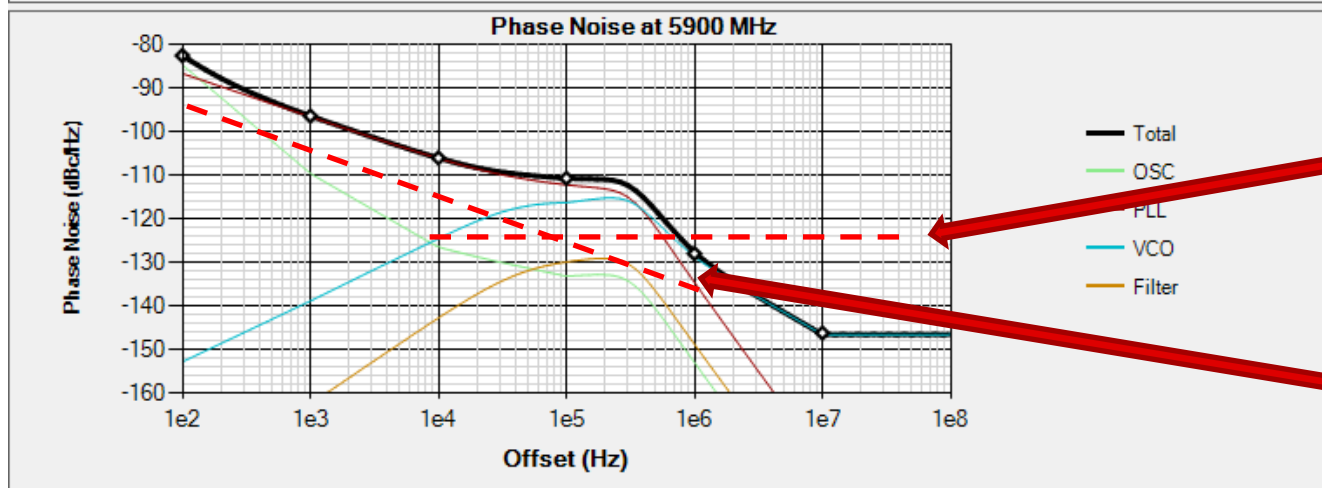
PLL Noise (Noise Metrics in dBc/Hz)
 Disable
 Use Metrics
 Load Data
 PLL FOM: -232
 PLL Flicker: -122
 PLL Fractional: -106

Total Phase Noise at Offsets

Offset (kHz)	Noise (dBc/Hz)
MKR1: 0.1	-82.5
MKR2: 1	-96.3
MKR3: 10	-106
MKR4: 100	-110.7
MKR5: 1000	-128
MKR6: 10000	-146.2

Crossover Metrics

InBand to VCO	204.744 kHz
PLL 1/f to Floor	100 kHz
VCO 1/f ³ to 1/f ²	22.387 kHz
VCO 1/f ² to Floor	14.125 MHz



- PLL FOM
 - $PN_{1\text{Hz}} = PN - 20 \cdot \log(N) - 10 \cdot \log(f_{PD})$
- PLL Flicker
 - $PN_{10\text{kHz}} = PN(\Delta f) - 20 \cdot \log(f_{out}/1\text{GHz}) - 10 \cdot \log(10\text{kHz}/\Delta f)$

PLL phase noise shaping levers

PLL Functional Block	To minimize Noise contribution...	Why?
Phase Detector/Charge Pump	Maximize charge pump gain (K_{PD}) (up to a certain point)	The phase detector noise contribution is proportional to $1/(K_{PD})^2$
R-counter and N-counter divide ratios	Maximize phase detector compare frequency \rightarrow this minimizes N	The noise contribution of the R and N dividers is proportional to N^2 .
Reference oscillator	Use highest frequency practical and use $R > 1$ if possible. If deciding between maximizing R and minimizing N, minimize N.	The noise contribution from the reference oscillator is proportional to $(N/R)^2$

To find more technical resources and search products, visit ti.com/clocks

Quiz

- True or false: Reducing N-divider value will decrease PLL noise by $20\log(N)$
- True or false: The reference oscillator does not contribute to PLL in band noise
- True or false: Increasing the charge pump current setting will reduce PLL noise
- True or false: The VCO tuning constant K_{VCO} only has an effect on noise outside of the PLL loop bandwidth

Quiz

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PLL Transient Response Quiz

TI Precision Labs – Clocks and Timing

Presented by Dean Banerjee

Prepared by Vibhu Vanjari

Quiz

- **True or False: The phase margin is the phase of the open loop transfer function when the gain of the PLL is equal to 0 dB.**
- **True or False: Phase margins under 30° should be avoided to enhance the stability of the PLL and minimize ringing.**
- **True or False: Larger bandwidths lead to shorter lock times.**

Quiz

- **True or False: The phase margin is the phase of the open loop transfer function when the gain of the PLL is equal to 0 dB.**
 - The phase margin is the distance of the phase from **-180 degrees** when the gain of the PLL is equal to 0 dB.
- **True or False: Phase margins under 30° should be avoided to enhance the stability of the PLL, and minimize ringing.**
 - Phase margins under 30° can lead to instability, peaking in the closed loop filter response, and ringing in the transient response.
- **True or False: Larger bandwidths lead to shorter lock times.**
 - Wider loop bandwidths allow the PLL to track changes in frequency faster.