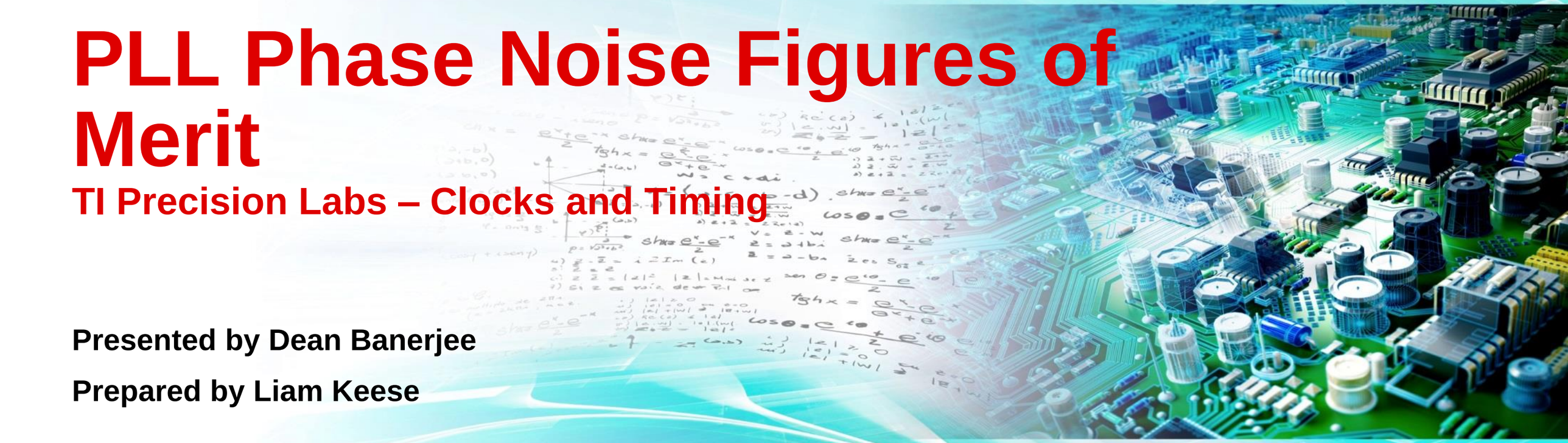
PLL Phase Noise Figures of Merit

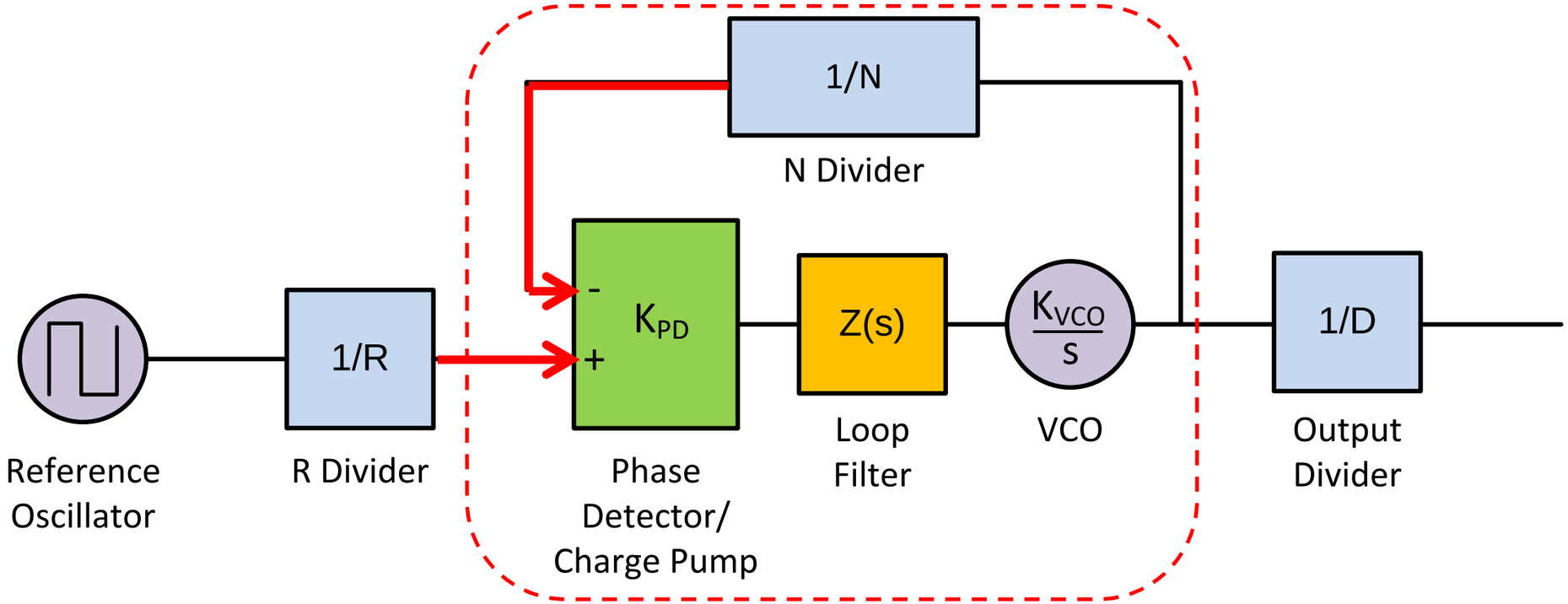
TI Precision Labs – Clocks and Timing



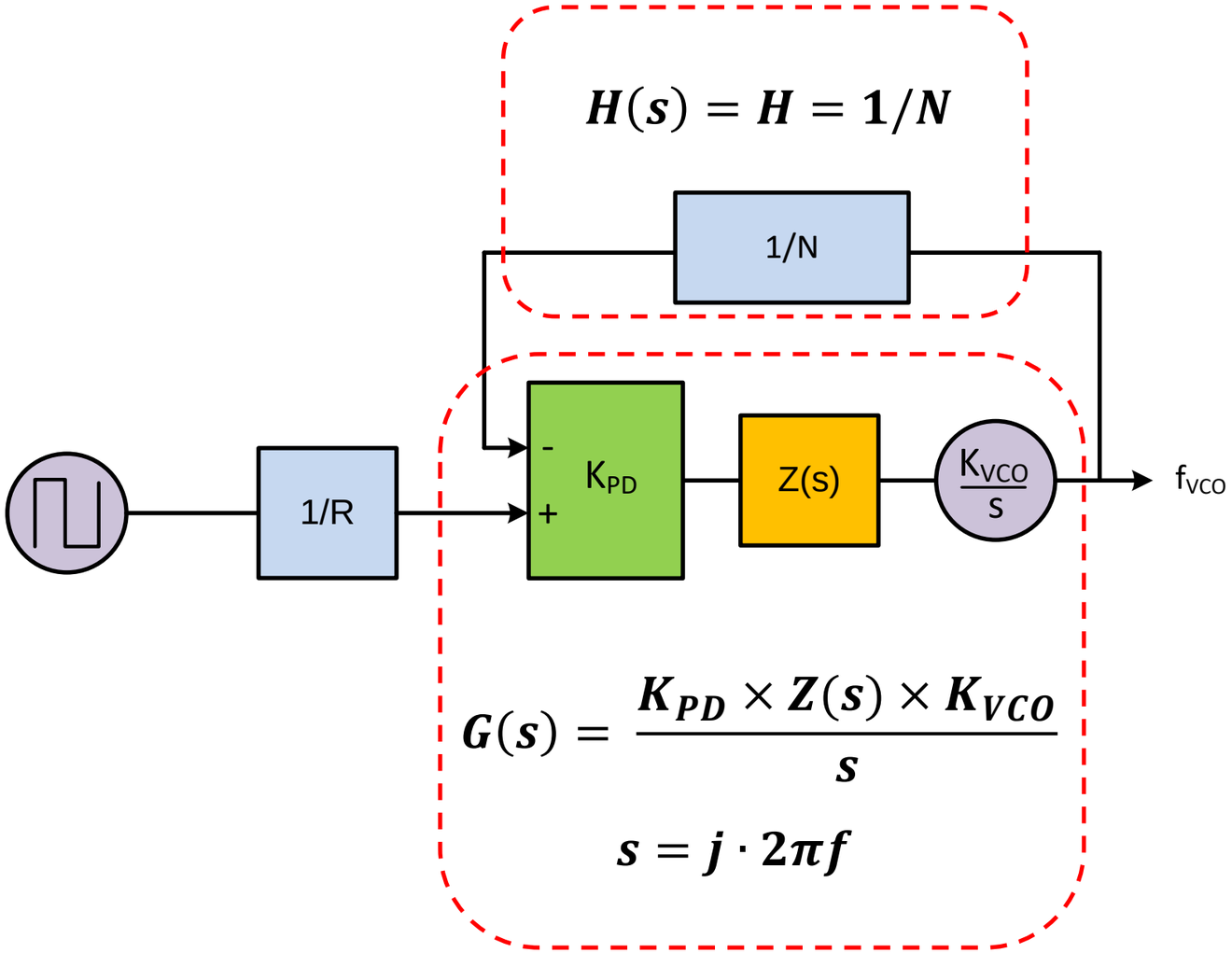
Presented by Dean Banerjee

Prepared by Liam Keese

Phase lock loop (PLL) overview

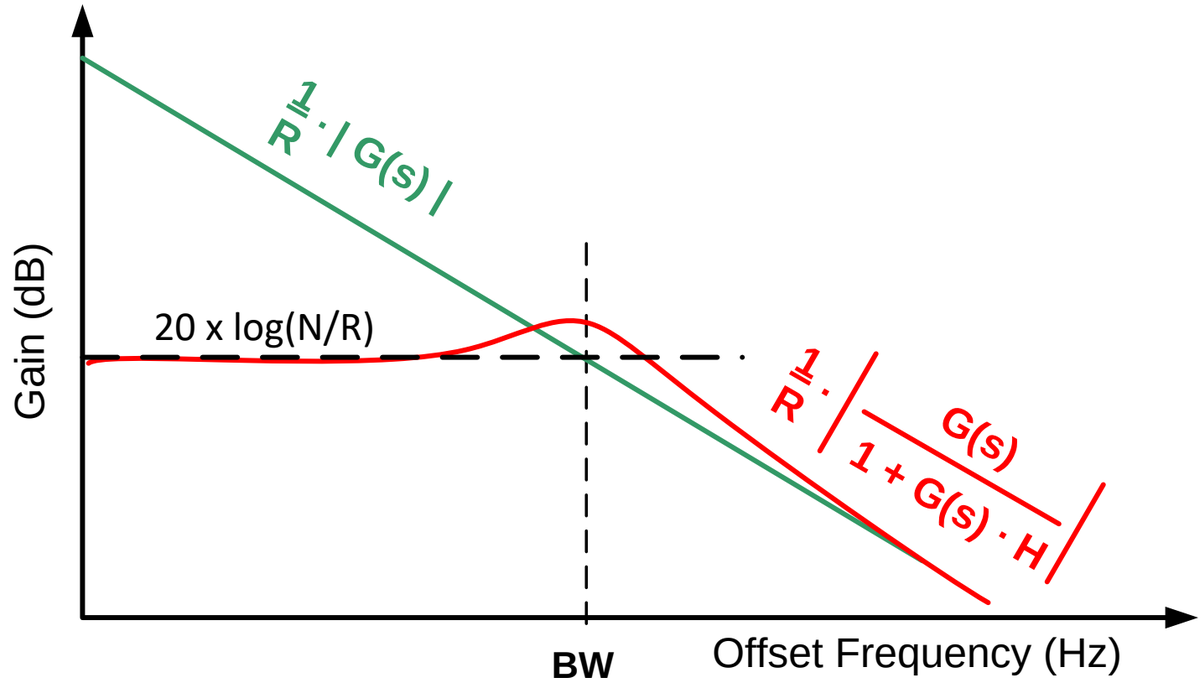


Phase lock loop (PLL) transfer functions



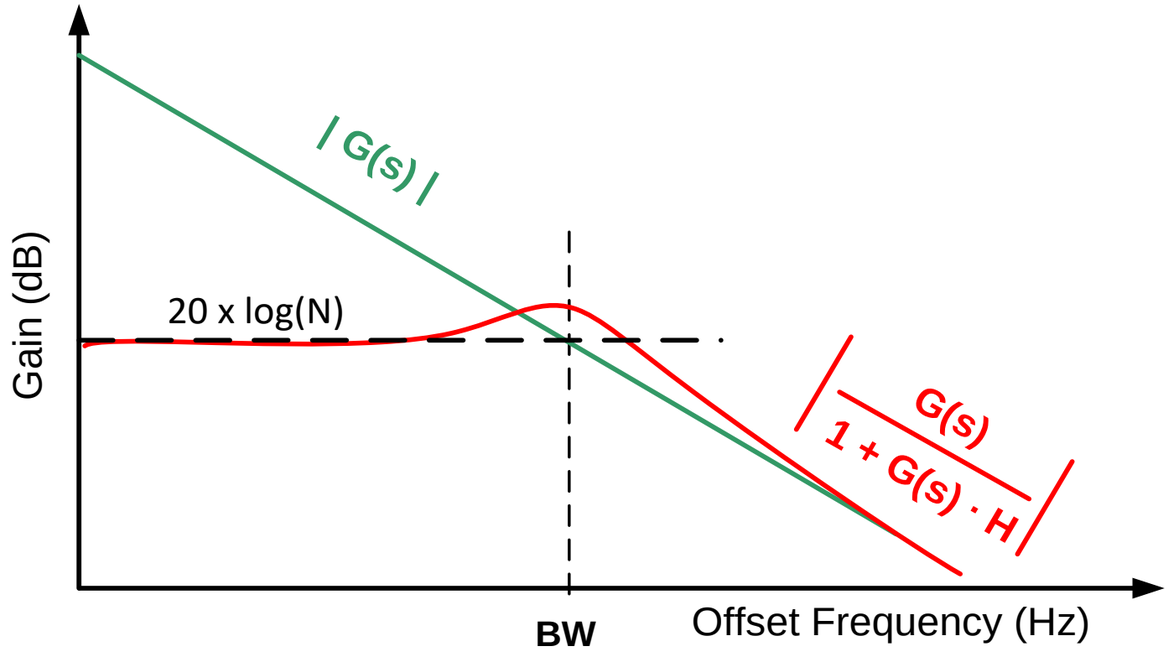
Block	Transfer Function
OSC	$\frac{1}{R} \cdot \frac{G(s)}{1 + G(s) \cdot H}$
R/N Dividers	$\frac{G(s)}{1 + G(s) \cdot H}$
Phase Detector	$\frac{1}{K_{PD}} \cdot \frac{G(s)}{1 + G(s) \cdot H}$
VCO	$\frac{1}{1 + G(s) \cdot H}$

Reference oscillator noise transfer function



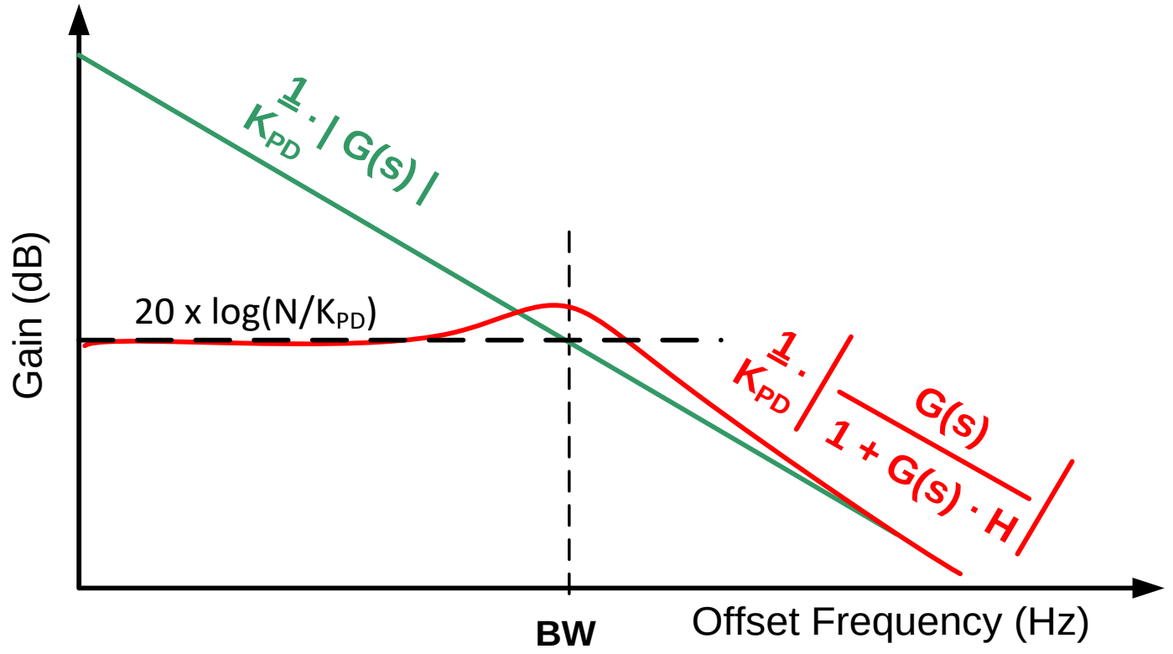
Block	Transfer Function	Response	Low Frequency Response	High Frequency Response
OSC	$\frac{1}{R} \cdot \frac{G(s)}{1 + G(s) \cdot H}$	Low Pass	$20 \cdot \log(N/R)$	$20 \cdot \log(G(s)/R)$

Feedback N divider noise transfer function



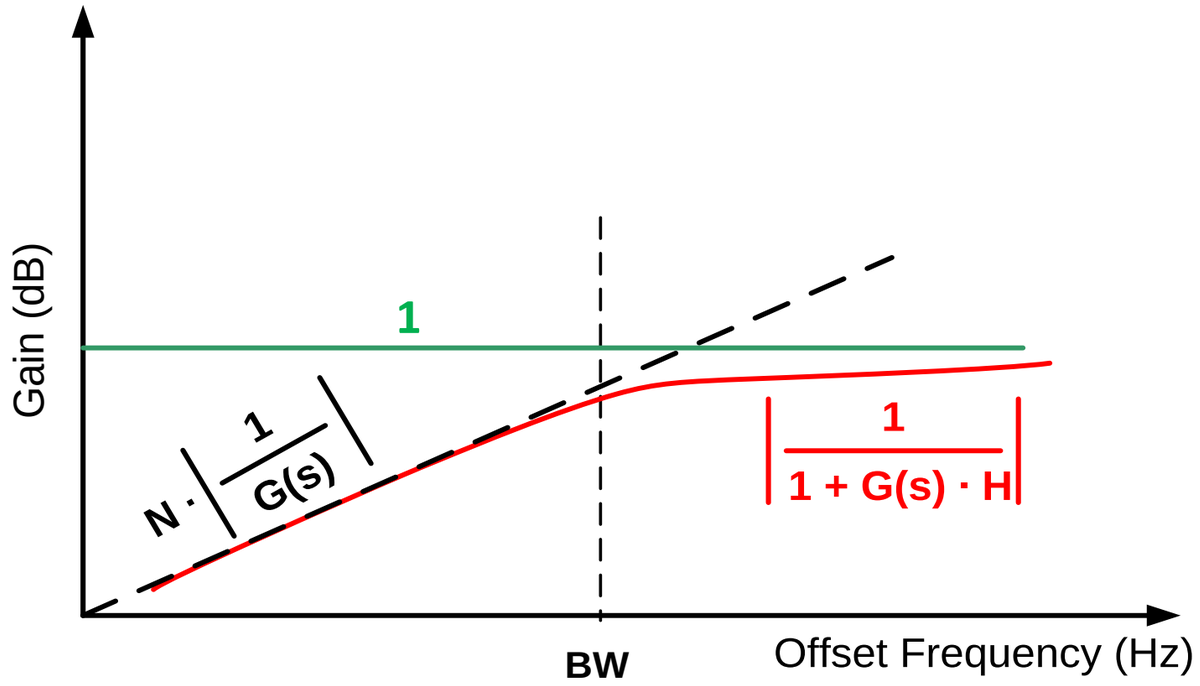
Block	Transfer Function	Response	Low Frequency Response	High Frequency Response
N (or R) Divider	$\frac{G(s)}{1+G(s)\cdot H}$	Low Pass	$20\cdot\log(N)$	$20\cdot\log(G(s))$

Phase det./charge pump noise transfer function



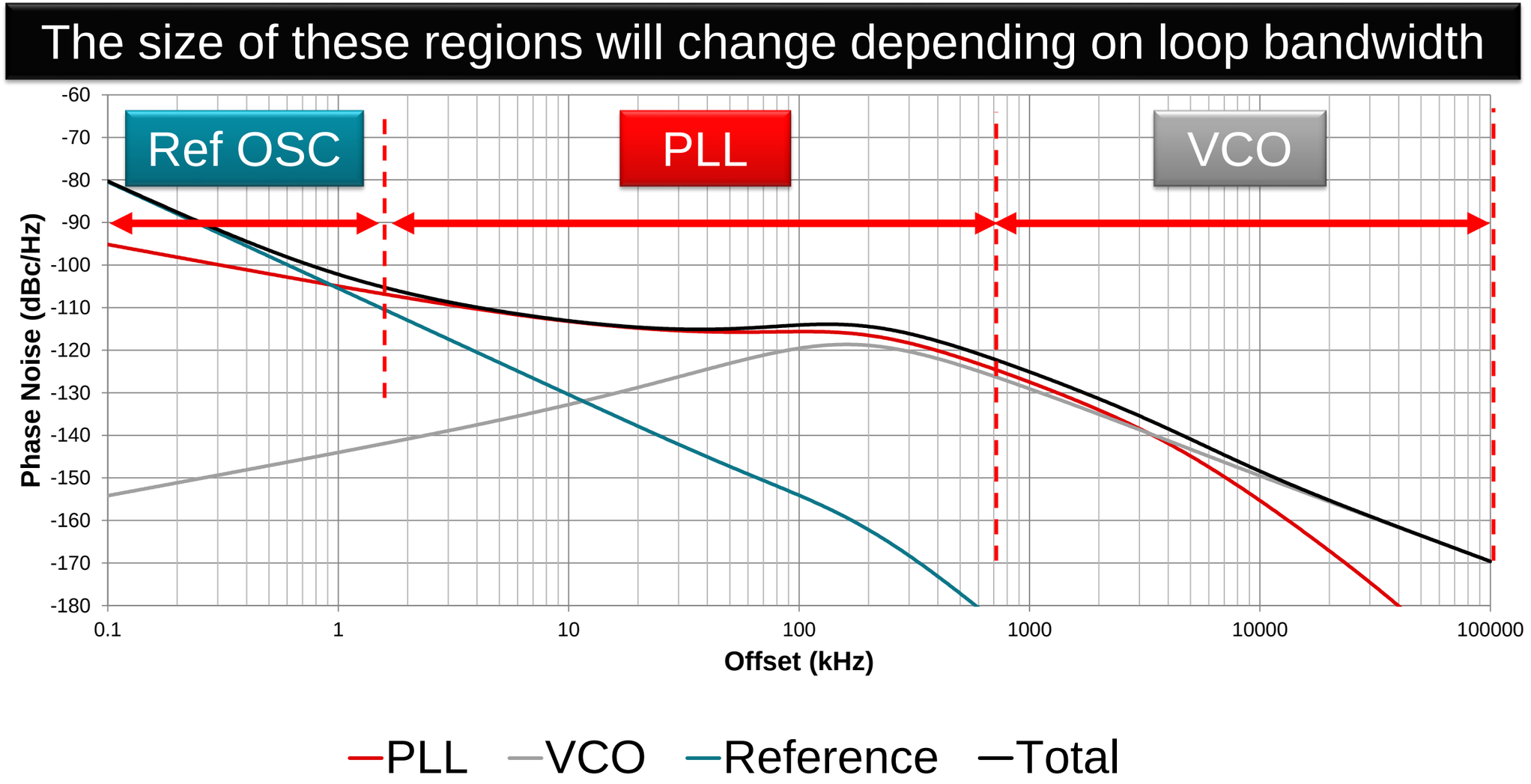
Block	Transfer Function	Response	Low Frequency Response	High Frequency Response
Phase Det./ CP gain	$\frac{1}{K_{PD}} \cdot \frac{G(s)}{1 + G(s) \cdot H}$	Low Pass	$20 \cdot \log(N/K_{PD})$	$20 \cdot \log(G(s)/K_{PD})$

VCO noise transfer function

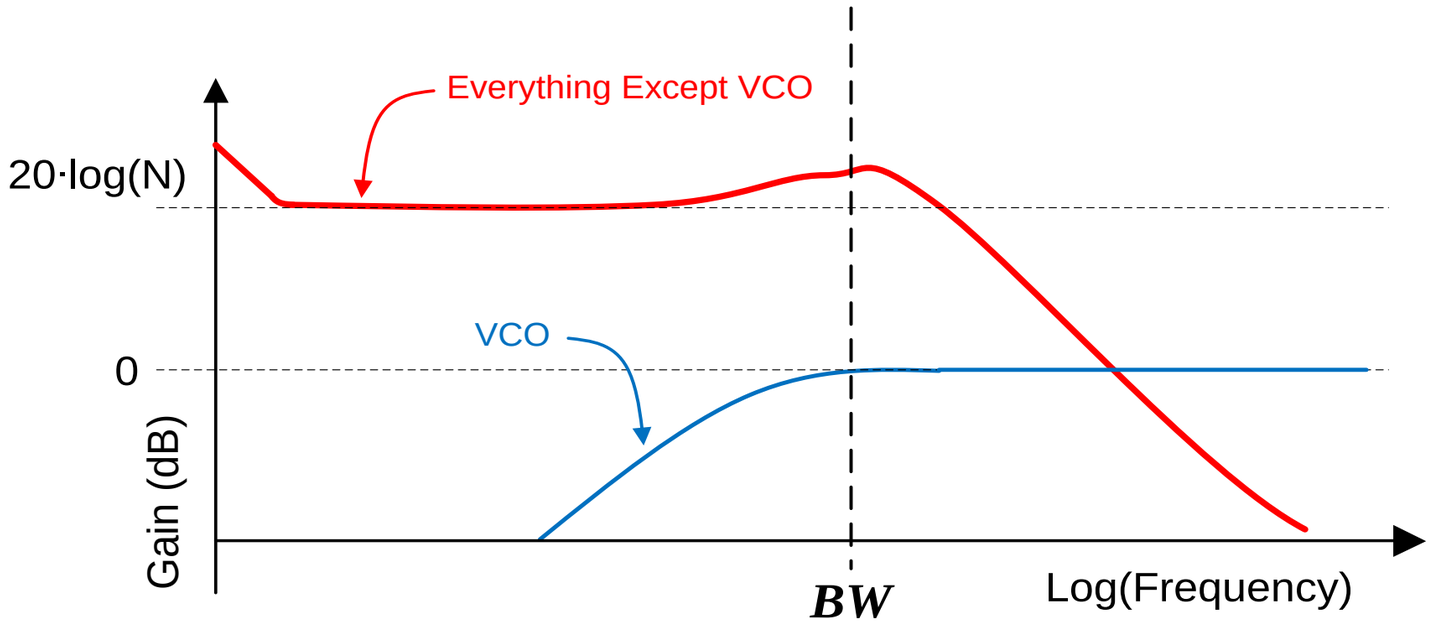


Block	Transfer Function	Response	Low Frequency Response	High Frequency Response
VCO	$\frac{1}{1+G(s)\cdot H}$	High Pass	$-20\cdot\log(G(s))$	1

PLL closed loop noise sources

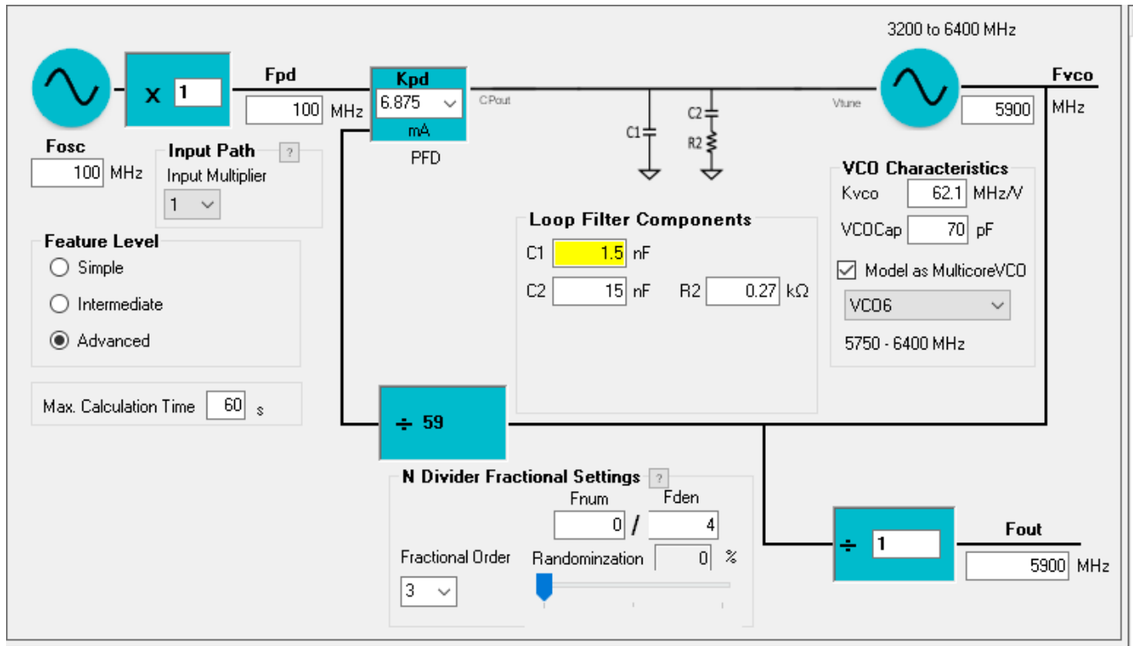


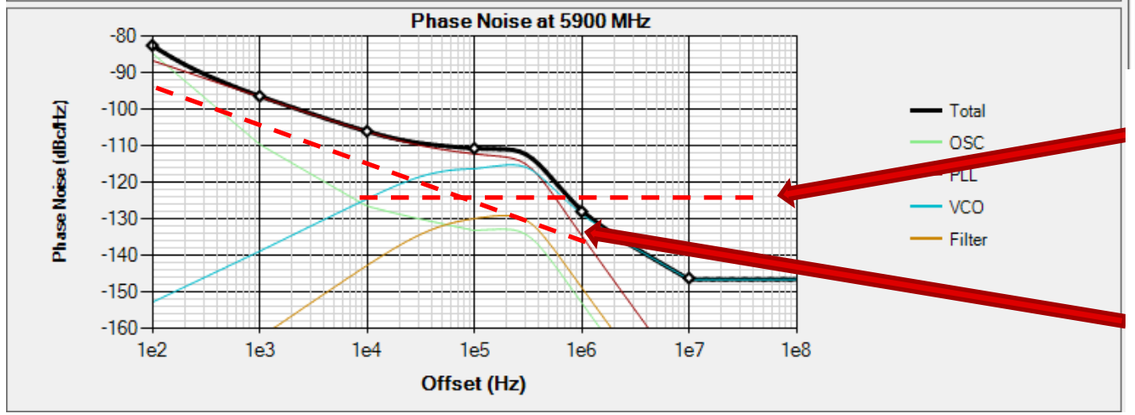
PLL normalized phase noise

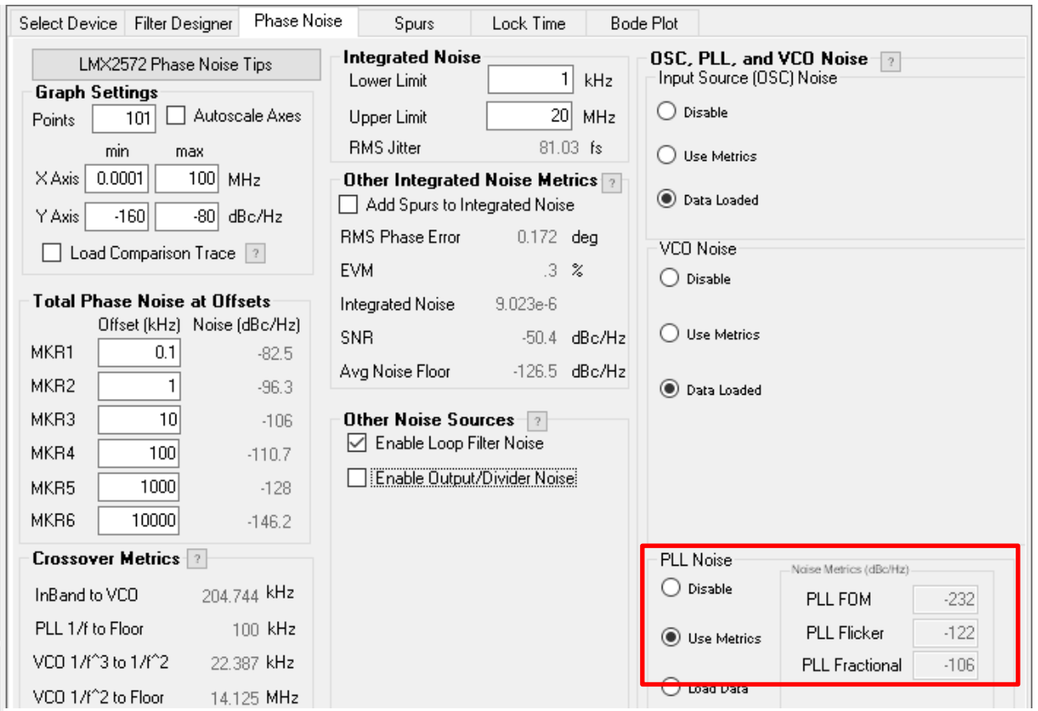


- PLL flat noise FOM (PN1Hz)
  - PLL noise floor normalized to1 Hz
  - N-counter added noise = 20 log (N)
- PLL flicker noise (PN10kHz)
  - Usually dominates at offset below 1 kHz
  - PLL 1/f normalized to 1 GHz output and 10kHz offset

PLL noise simulation







- PLL FOM
  - $PN1Hz = PN - 20 \cdot \log(N) - 10 \cdot \log(f_{PD})$
- PLL Flicker
  - $PN10kHz = PN(\Delta f) \; -20 \cdot \log(f_{out}/1GHz) \; -10 \cdot \log(10kHz/\Delta f)$

PLL phase noise shaping levers

PLL Functional Block	To minimize Noise contribution…	Why?
Phase Detector/Charge Pump	Maximize charge pump gain (K_{PD}) (up to a certain point)	The phase detector noise contribution is proportional to $1/(K_{PD})^2$
R-counter and N-counter divide ratios	Maximize phase detector compare frequency → this minimizes N	The noise contribution of the R and N dividers is proportional to N^2.
Reference oscillator	Use highest frequency practical and use R > 1 if possible. If deciding between maximizing R and minimizing N, minimize N.	The noise contribution from the reference oscillator is proportional to $(N/R)^2$

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Quiz

- True or false: Reducing N-divider value will decrease PLL noise by 20log(N)
- True or false: The reference oscillator does not contribute to PLL in band noise
- True or false: Increasing the charge pump current setting will reduce PLL noise
- True or false: The VCO tuning constant K_{VCO} only has an effect on noise outside of the PLL loop bandwidth

Quiz

- True or false: Reducing N-divider value will decrease PLL noise by 20log(N)
- True or false: The reference oscillator does not contribute to PLL in band noise
- True or false: Increasing the charge pump current setting will reduce PLL noise
- True or false: The VCO tuning constant K_{VCO} only has an effect on noise outside of the PLL loop bandwidth

PLL Transient Response Quiz

TI Precision Labs – Clocks and Timing

Presented by Dean Banerjee

Prepared by Vibhu Vanjari

Quiz

- **True or False: The phase margin is the phase of the open loop transfer function when the gain of the PLL is equal to 0 dB.**

- **True or False: Phase margins under 30º should be avoided to enhance the stability of the PLL and minimize ringing.**

- **True or False: Larger bandwidths lead to shorter lock times.**

Quiz

- **True or False: The phase margin is the phase of the open loop transfer function when the gain of the PLL is equal to 0 dB.**
  - The phase margin is the distance of the phase from **-180 degrees** when the gain of the PLL is equal to 0 dB.

- **True or False: Phase margins under 30º should be avoided to enhance the stability of the PLL, and minimize ringing.**
  - Phase margins under 30º can lead to instability, peaking in the closed loop filter response, and ringing in the transient response.

- **True or False: Larger bandwidths lead to shorter lock times.**
  - Wider loop bandwidths allow the PLL to track changes in frequency faster.