Frequency Planning Part 2

TI Precision Labs – Clocks and Timing

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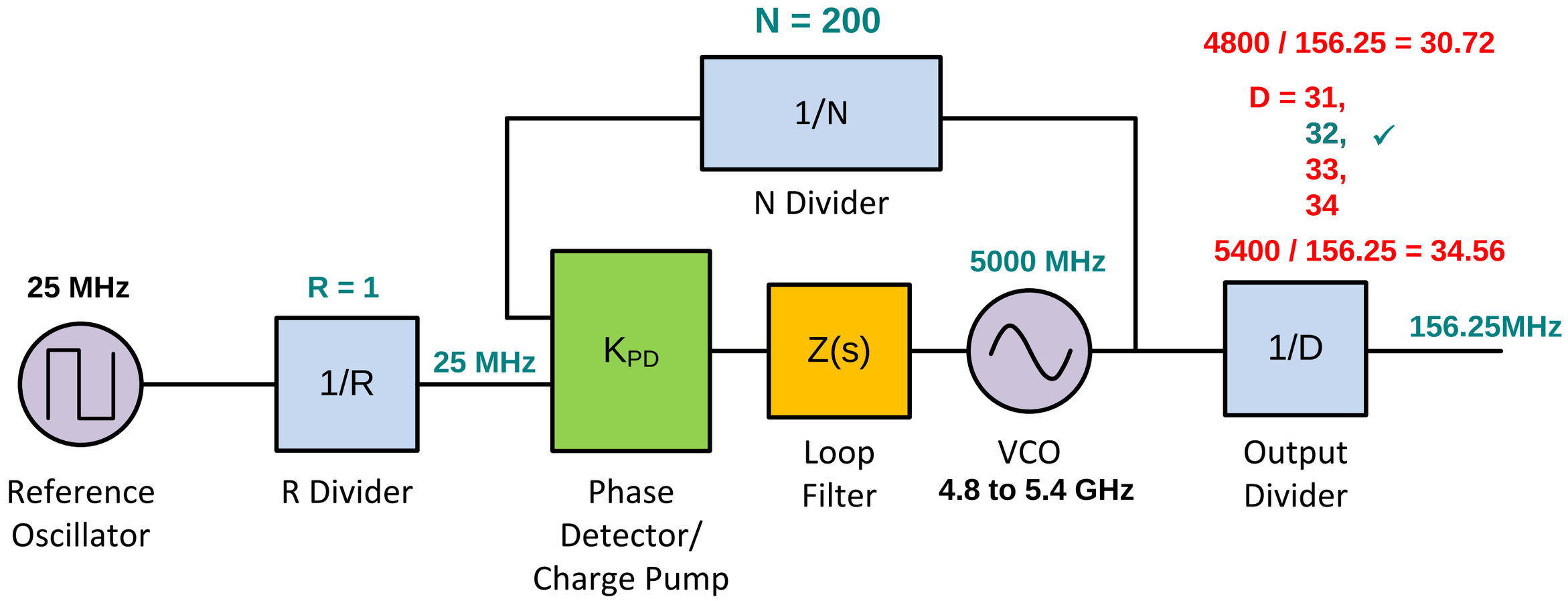
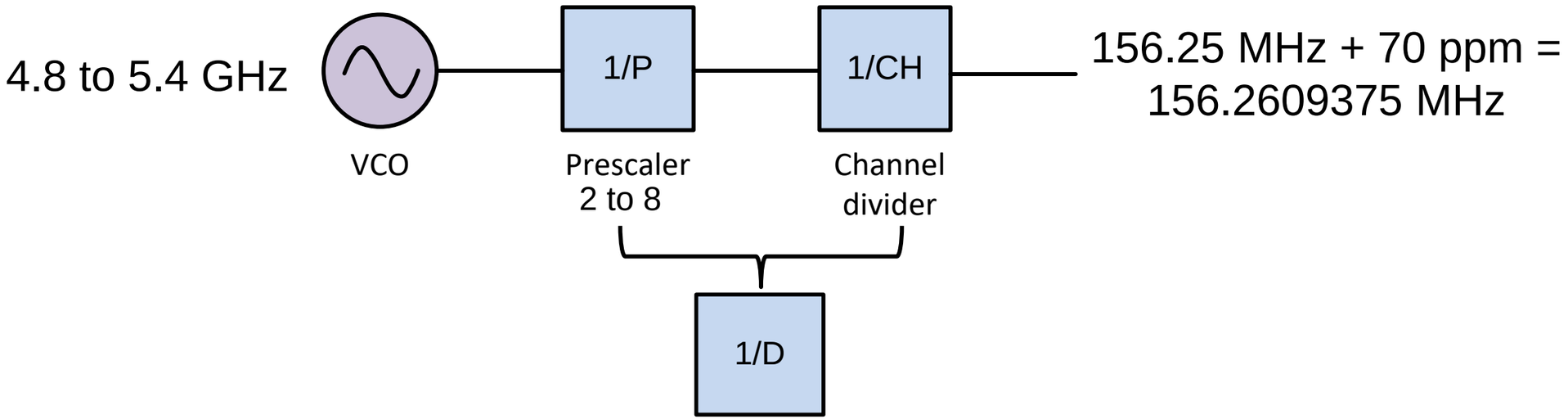
Frequency calculation quick review



VCO selection and spur mitigation

How to generate 156.25 MHz + 70 ppm from 100 MHz PFD frequency?

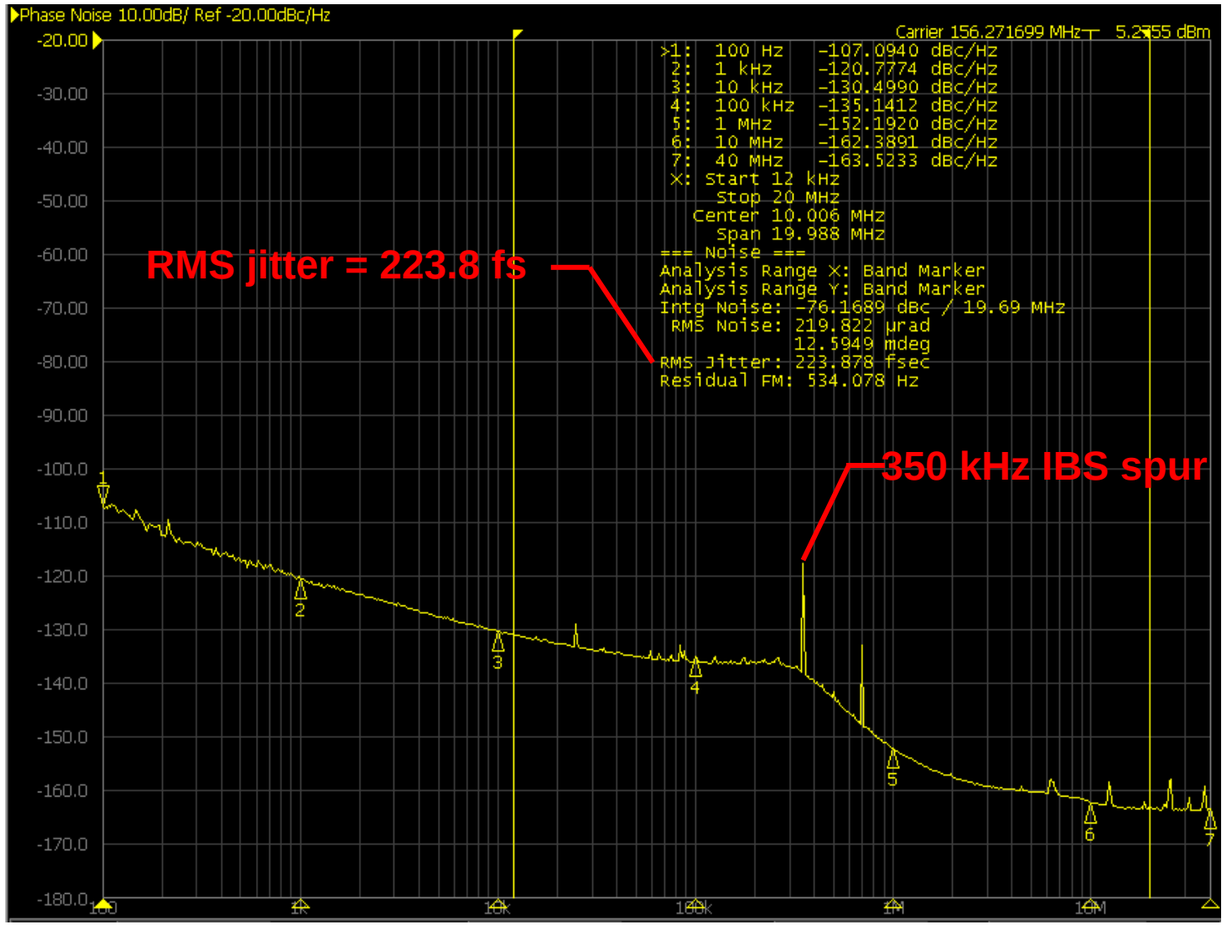


VCO frequency		31		IBS frequency	
5000.35 MHz	⟵	32 = 4 x 8	✓ ⟶	350 kHz	✘
5156.6109375 MHz	⟵	33 = 3 x 11	✓ ⟶	56.61 MHz	
5312.871875 MHz	⟵	34 = 2 x 17	✓ ⟶	12.87 MHz	

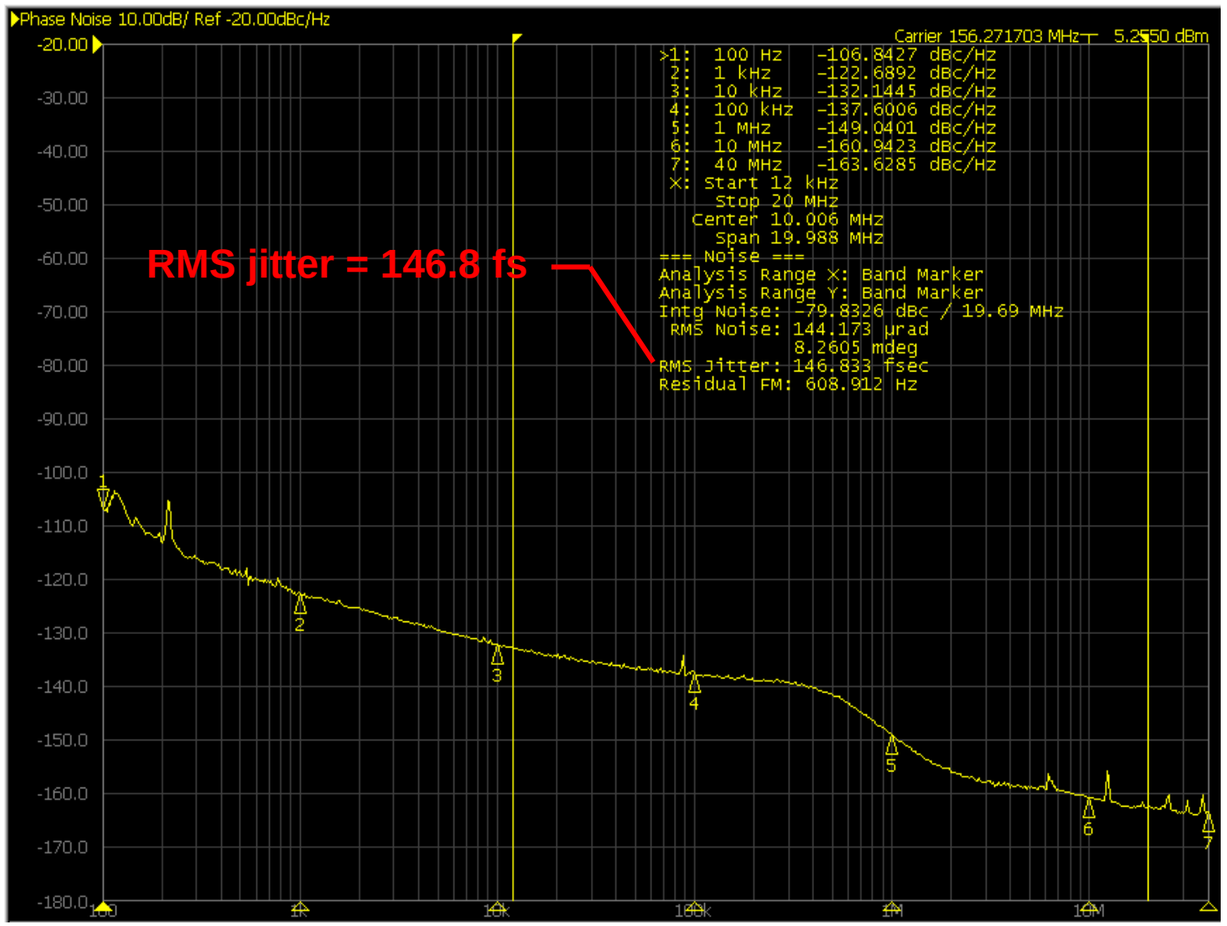
$$f_{IBS} = f_{VCO} \% f_{PFD}$$

Mitigate spurs (cont.)

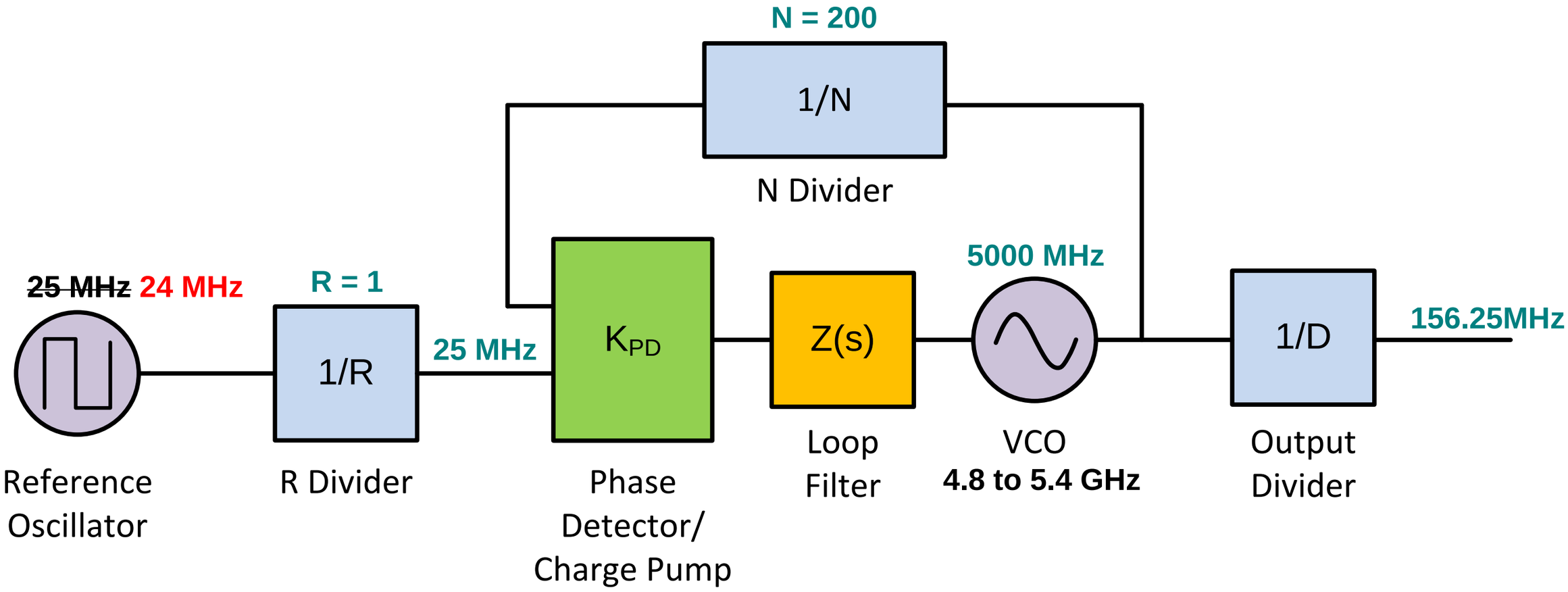
D = 32



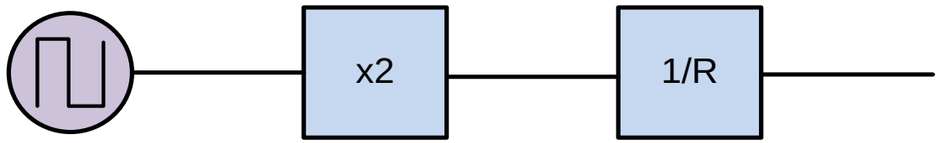
D = 33



Frequency calculation and PFD frequency



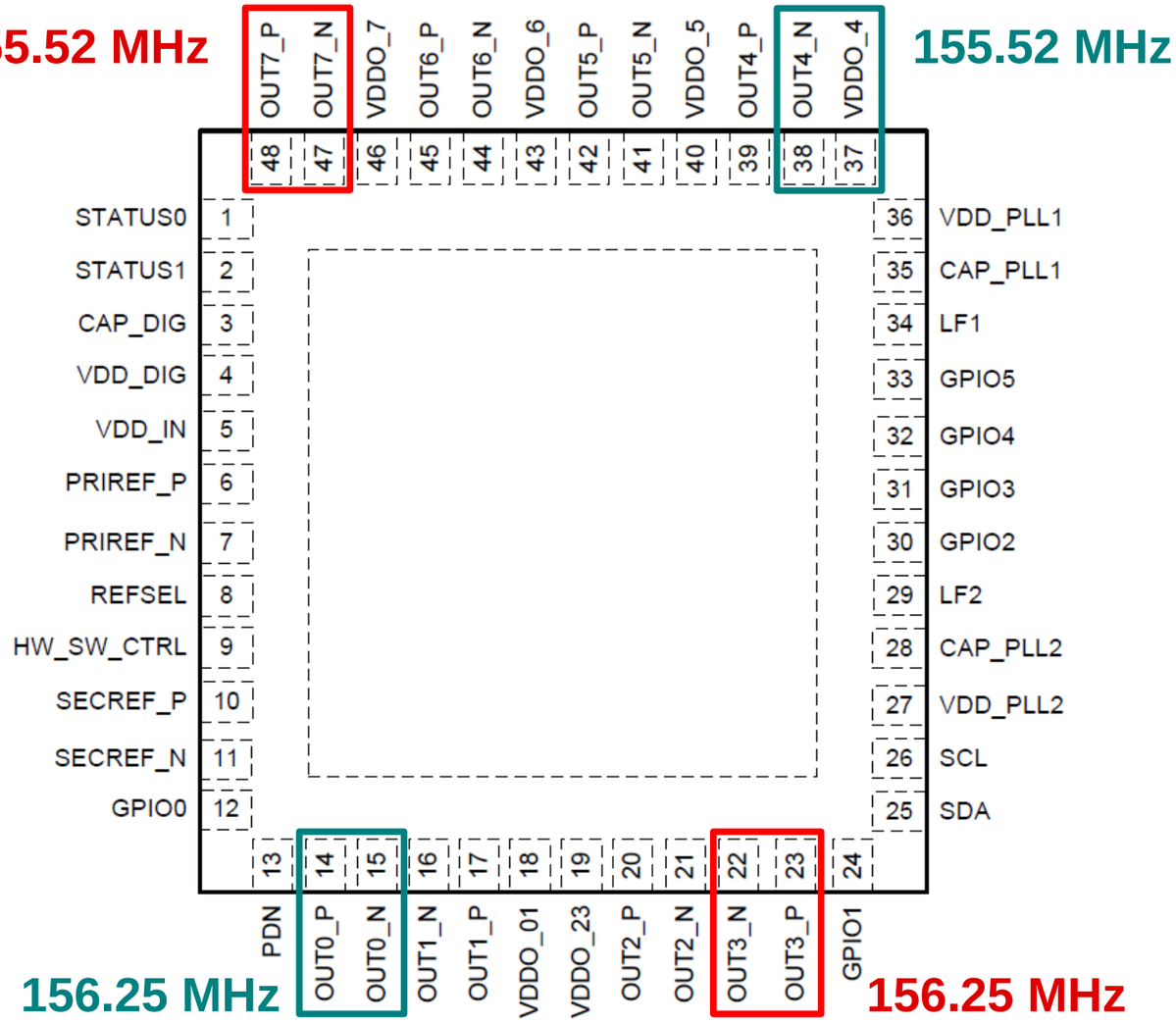
Setting PFD frequency



Reference Oscillator | Doubler | R Divider | **PFD Frequency**

	x2	**/1**	**= 48 MHz**
24 MHz	**x1**	**/1**	**= 24 MHz**
	x2	**/3**	**= 16 MHz**

Crosstalk considerations



To find more clocks and timing technical resources and search products, visit ti.com/clocks

TEXAS INSTRUMENTS

Short Quiz

1. True or False:

The Integer Boundary Spur should be as close to the carrier frequency as possible.

Short Quiz

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The Integer Boundary Spur should be as close to the carrier frequency as possible.

Short Quiz

2. True or False:

The PFD frequency should be as low as possible for the PLL to always work in integer mode.

Short Quiz

2. True or False:

The PFD frequency should be as low as possible for the PLL to work in integer mode.

Short Quiz

3. True or False:

Channel crosstalk is intrinsic and cannot be improved or worsened by board design.

Short Quiz

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Channel crosstalk is intrinsic and cannot be improved or worsened by board design.