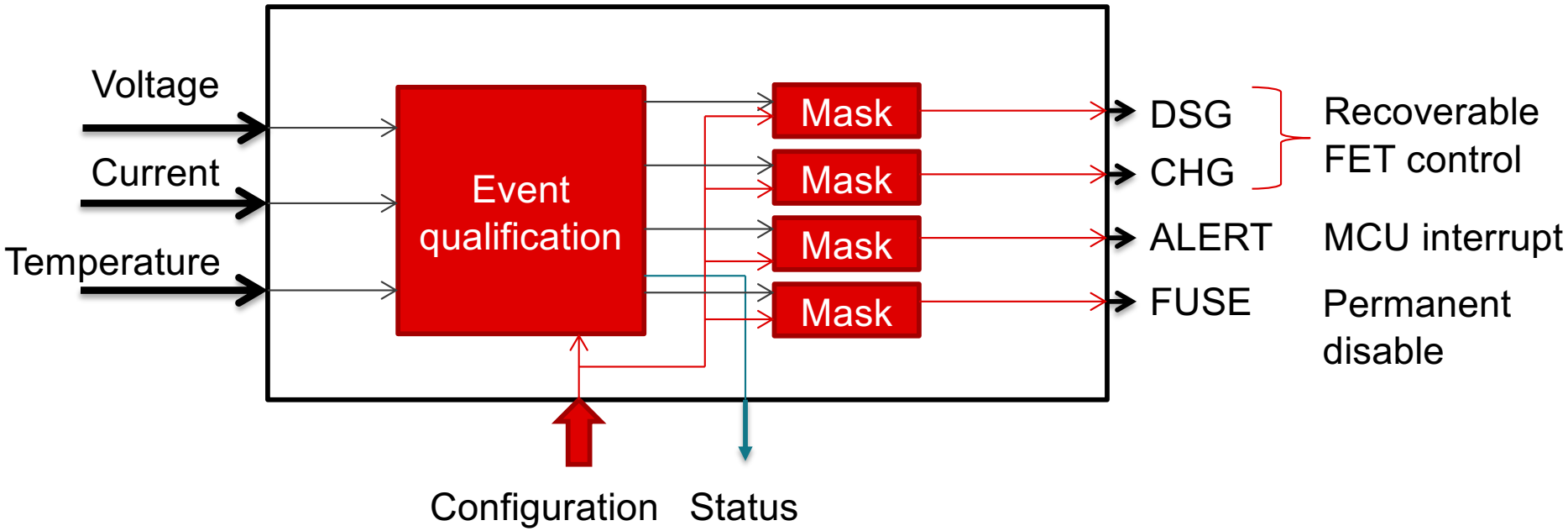
BQ76942 / BQ76952 battery monitors: FET configurations and cell balancing

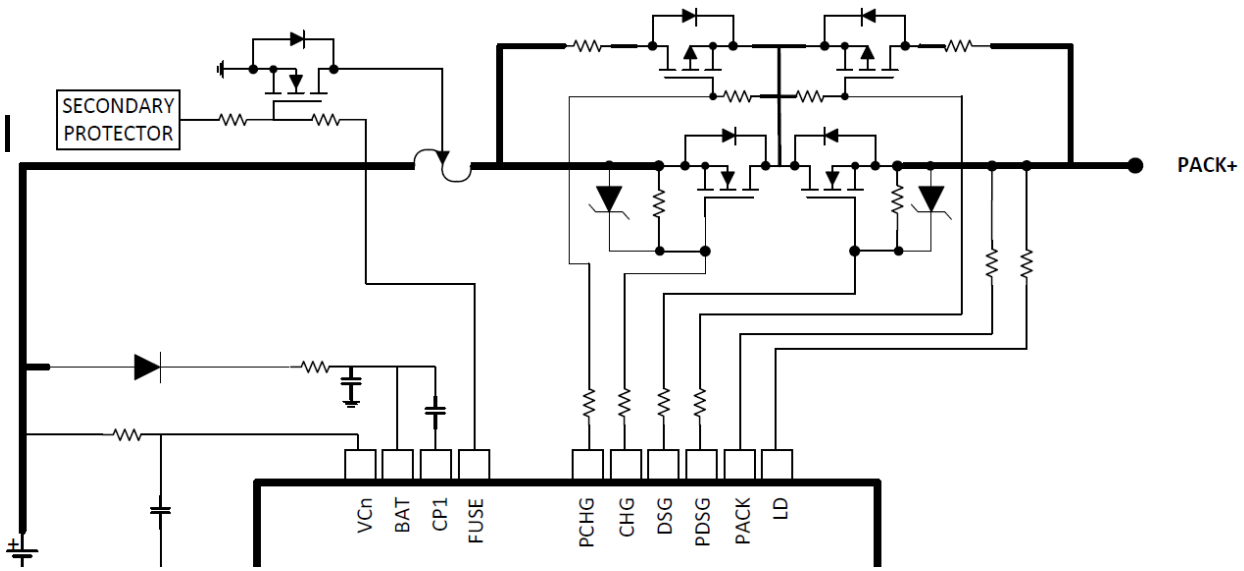
Flexible protection configuration

- BQ76942 / BQ76952 have configurable options for enabling protection



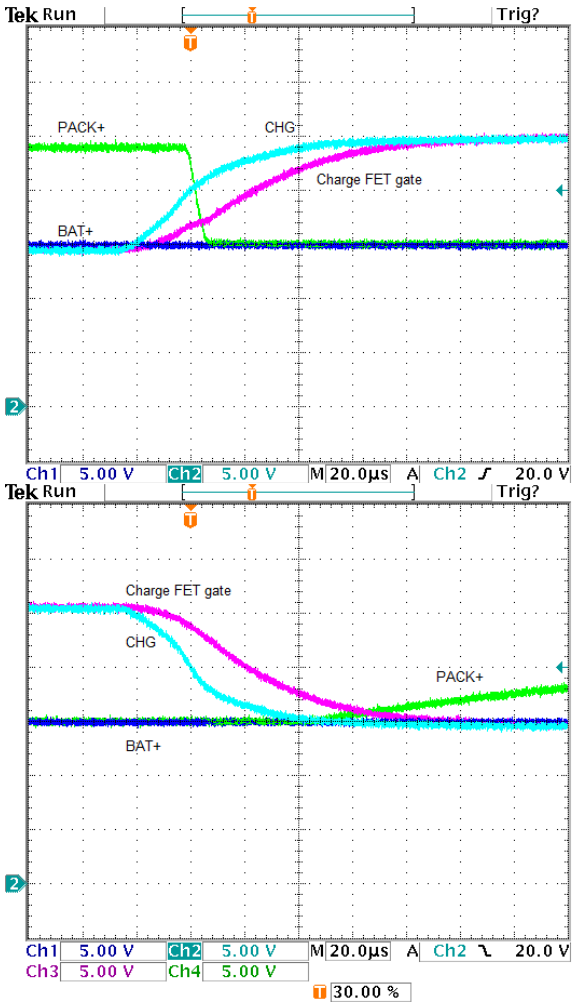
FET drivers

- Supports high side N-channel main charge and discharge FETs
  - Charge pump integrated
  - CP1 capacitor external
    - Can be increased
    - No UVLO
- Supports high side P-channel precharge and predischarge FETs
  - Drive to pre-set low value
  - High impedance when off



CHG driver

- CHG driver turn on
  - Switches to CP
  - Resistive
  - Ideally C1V1 = C2V2
  - Switching time in 10’s of us
- CHG driver turn off
  - Switches to BAT
  - Resistive
  - Switching time in 10’s of us

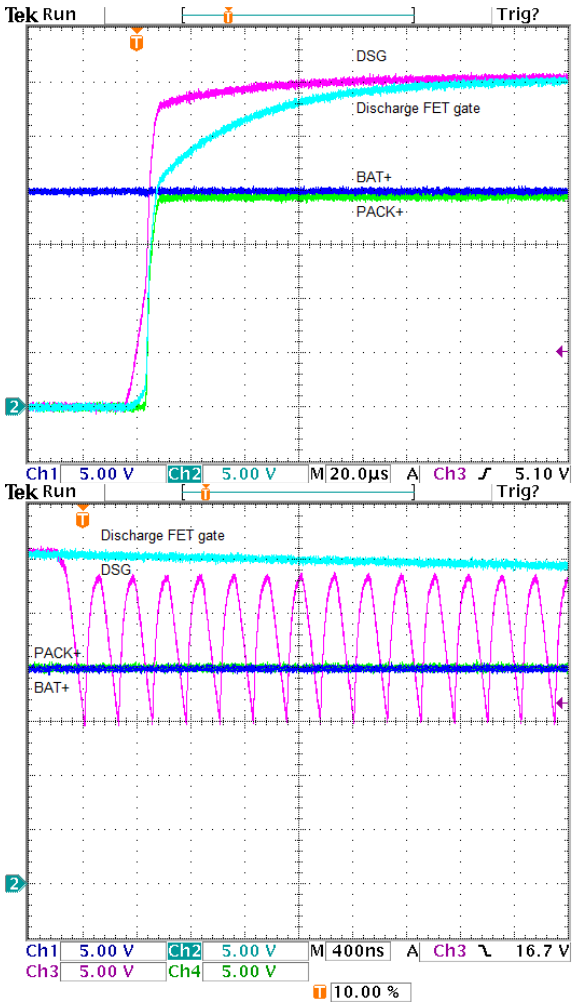


5.1-kΩ resistor between CHG pin and FET gate

FET gate capacitance ~4nF

DSG driver

- DSG driver turn on
  - Switches to CP
  - Resistive
  - Switching time in 10’s of us
- DSG driver turn off
  - Pulses to voltage below LD
  - Switching time from < 10 us to 10’s of us
  - Switching stops after time

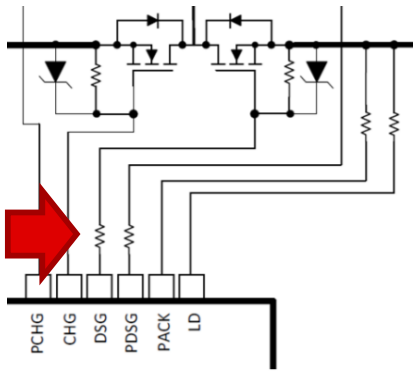


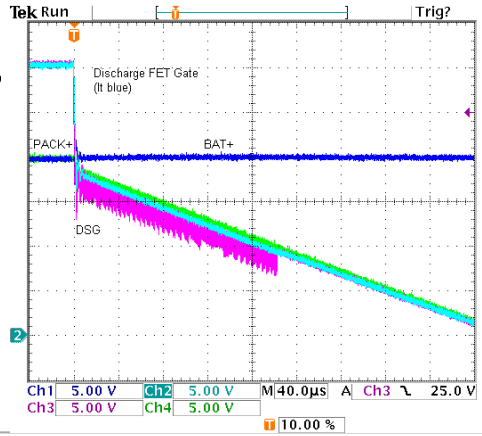
5.1-kΩ resistor between DSG pin and FET gate

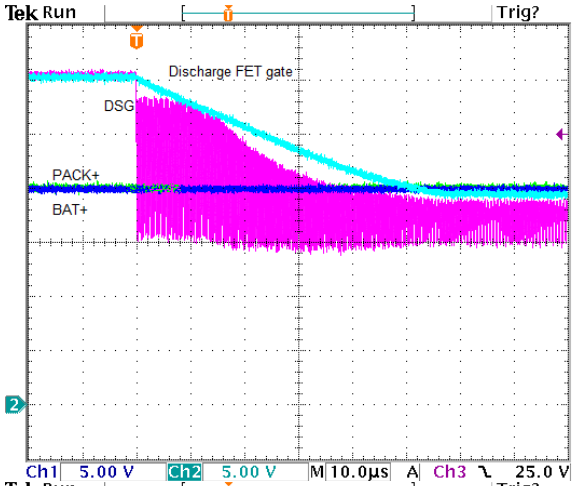
FET gate capacitance ~4nF

DSG continued

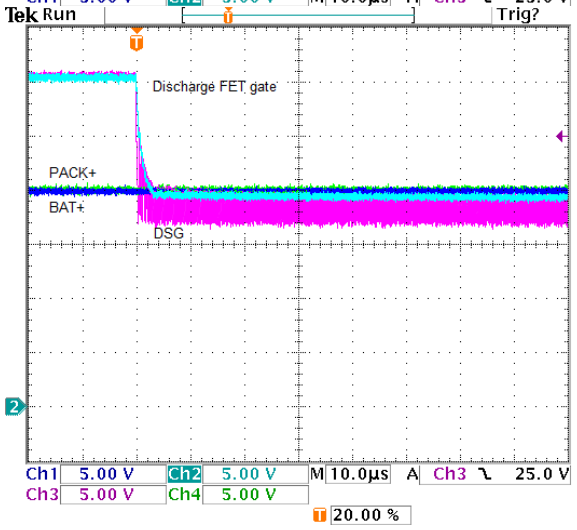
- Series resistor to gate acts with gate capacitance to adjust turn off time
- Small resistor gives faster turn off or similar turn off for more FETs
- PACK+ still must discharge from system load







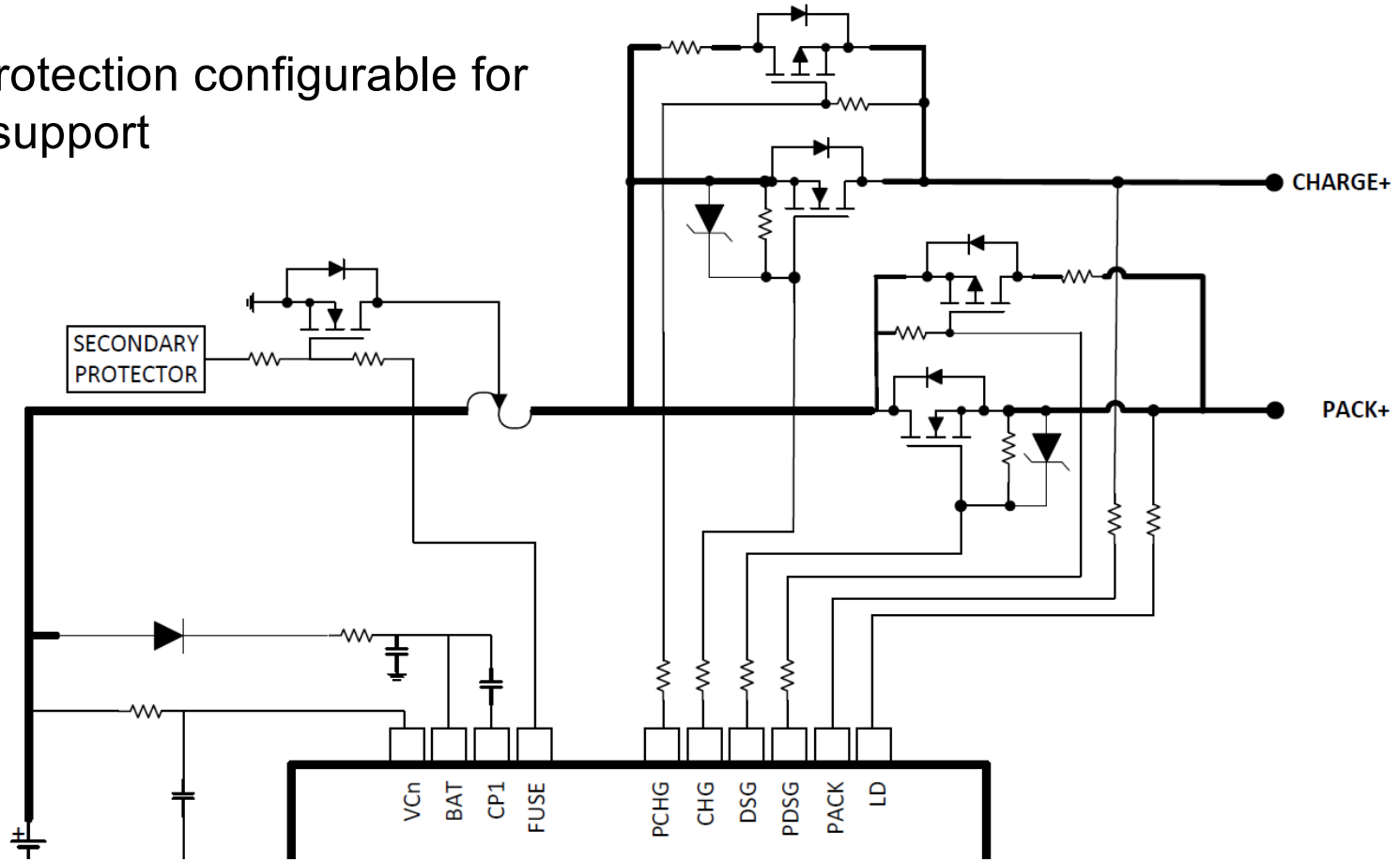
5.1-kΩ resistor between DSG pin and FET gate



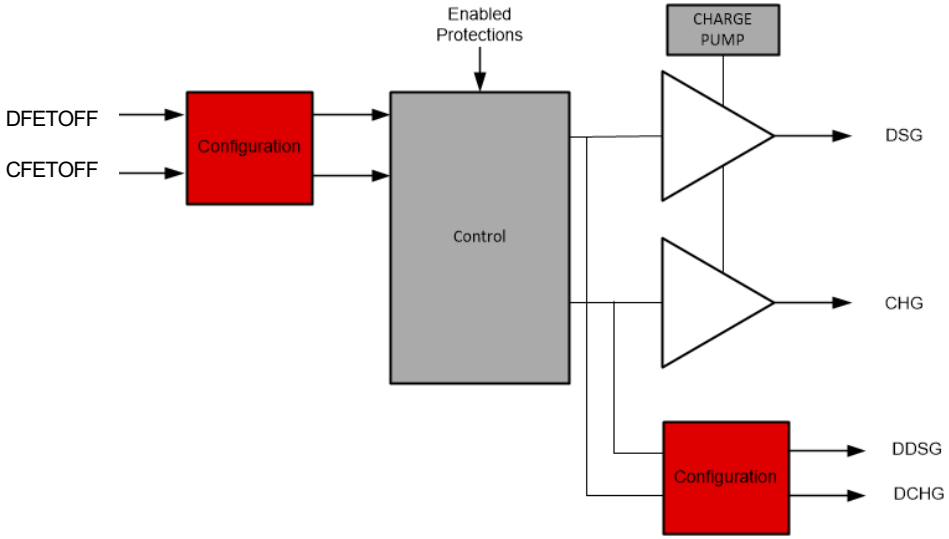
120-Ω resistor between DSG pin and FET gate

Parallel FETs

- Body diode protection configurable for parallel path support



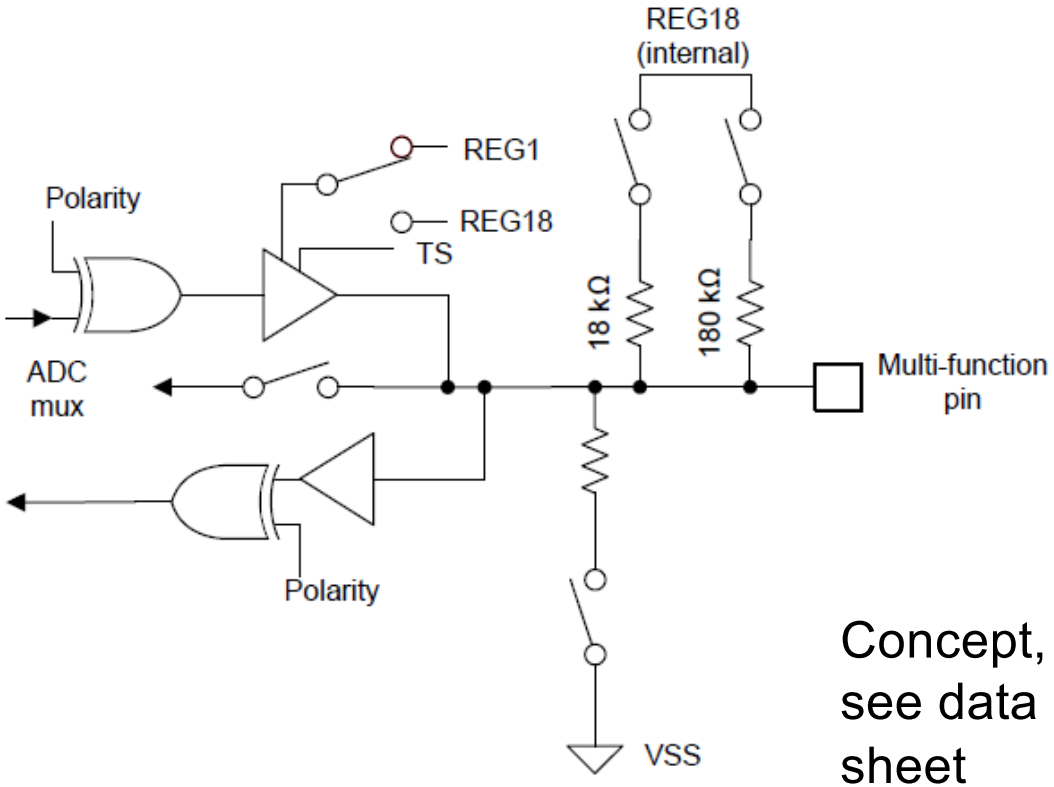
FET driver control



Signal output	Dependency	Charge pump?	Hardware input
DSG	System conditions, configuration, commands	Yes	DFETOFF with configuration
CHG	System conditions, configuration, commands	Yes	CFETOFF with configuration
DDSG	Same as DSG with extra configuration	N/A	Same as DSG
DCHG	Same as CHG with extra configuration	N/A	Same as CHG

DDSG and DCHG are on multi-function pins

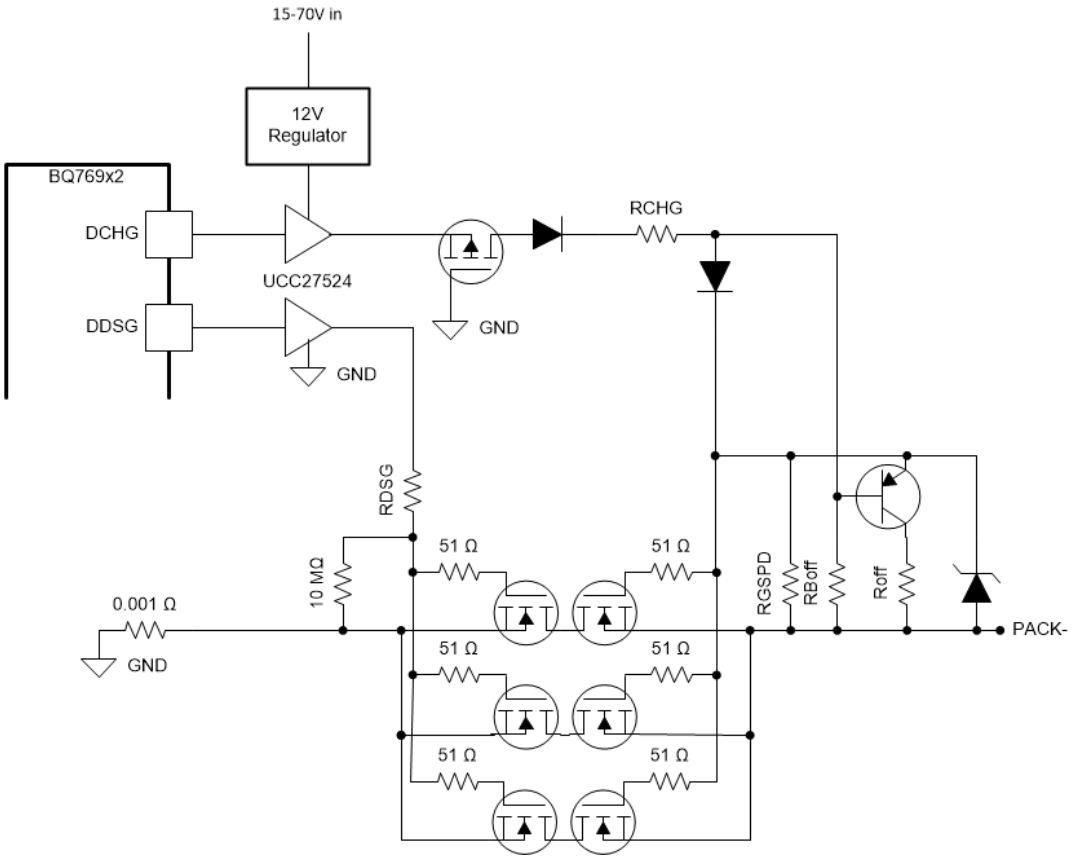
- Must be configured for FET output control
- CFETOFF and DFETOFF for FET control



Concept, see data sheet

Low side FET drive

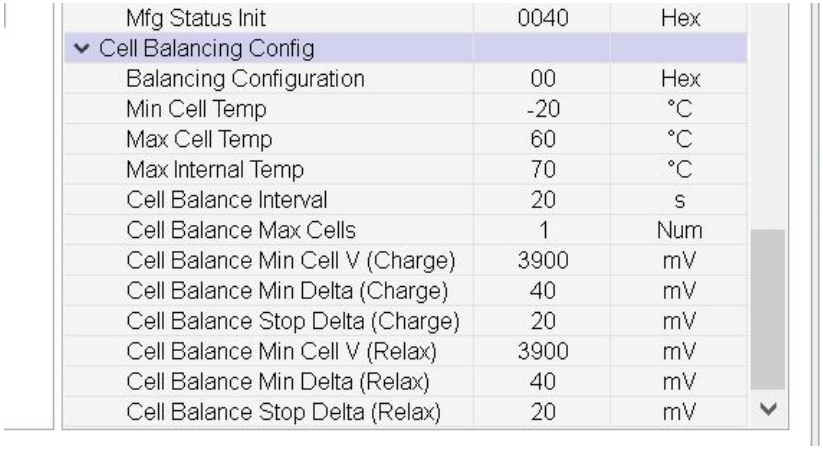
- DDSG and DCHG are logic signals,
  - REG1
- For FET drive need:
  - Gate drive voltage
  - Gate driver
  - Protect CHG from high voltage
    - Series FETs
  - Allow charge gate to fall below GND
- Low side supports multiple FETs
    - Limited by power supply and driver



Cell balancing

Cell balancing

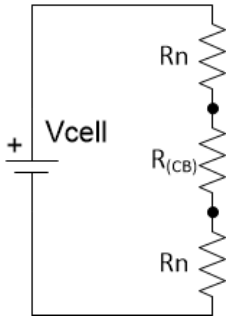
- Autonomous or Host controlled
  - Autonomous will balance only non-adjacent cells
  - Host controlled allows any balancing
    - Accessible in SEALED mode
    - Blocked by temperature
    - Times out each Cell Balance Interval
    - Can be blocked in configuration
- Power dissipation limitations
  - 65 mA in 25 ohm is 0.1 W
  - Will heat the part



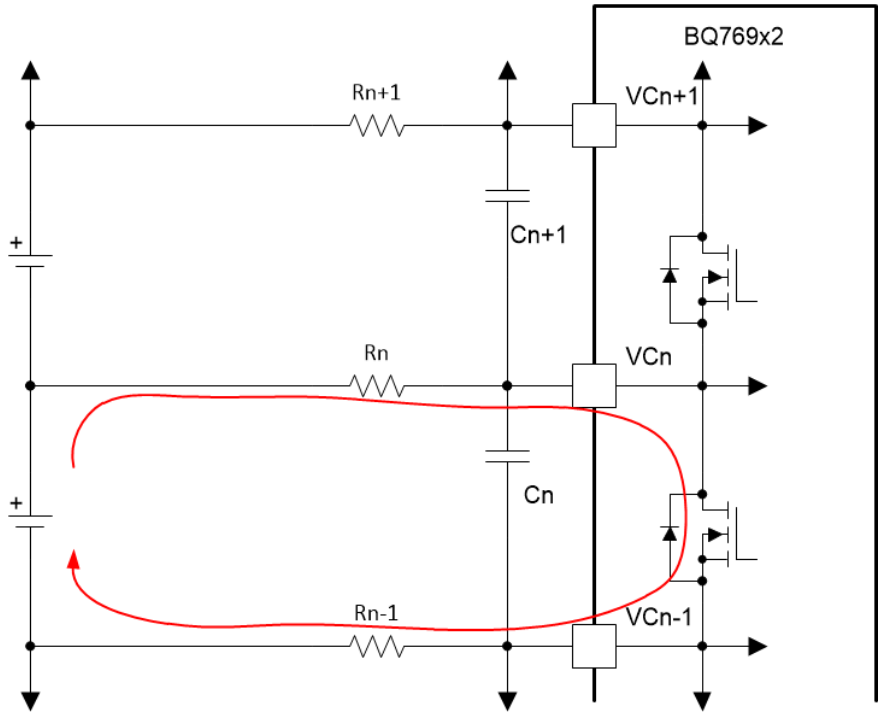
Mfg Status Init	0040	Hex
Cell Balancing Config		
Balancing Configuration	00	Hex
Min Cell Temp	-20	°C
Max Cell Temp	60	°C
Max Internal Temp	70	°C
Cell Balance Interval	20	s
Cell Balance Max Cells	1	Num
Cell Balance Min Cell V (Charge)	3900	mV
Cell Balance Min Delta (Charge)	40	mV
Cell Balance Stop Delta (Charge)	20	mV
Cell Balance Min Cell V (Relax)	3900	mV
Cell Balance Min Delta (Relax)	40	mV
Cell Balance Stop Delta (Relax)	20	mV

Cell balancing current

- Low external resistors
- Internal resistance $R_{(CB)}$ 25 ohm typical

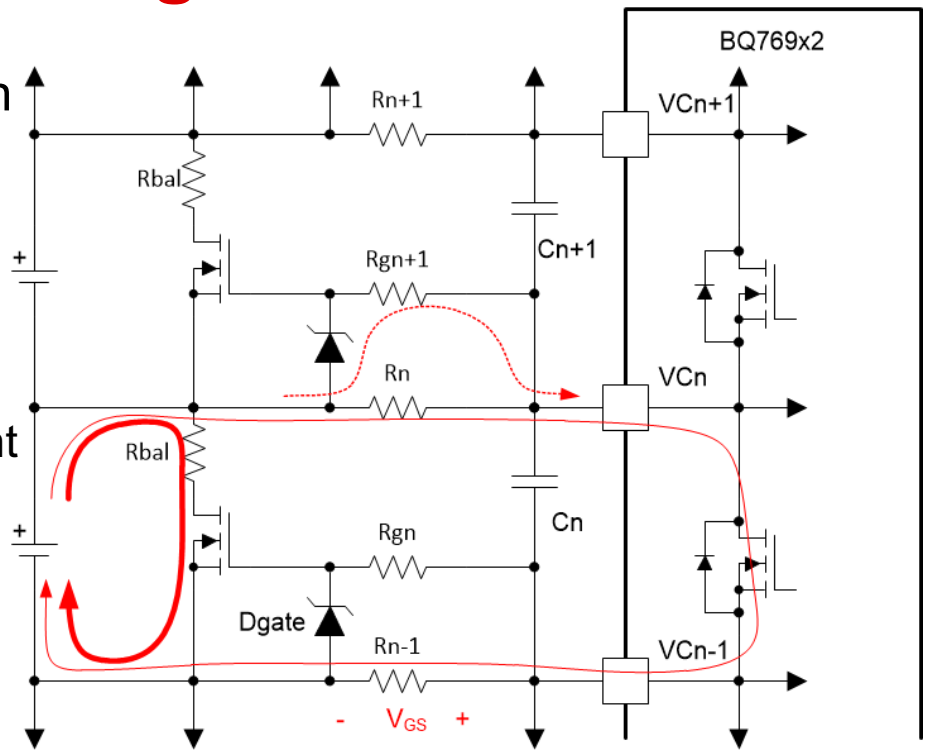


I balance =
Vcell/(2xRn + $R_{(CB)}$
Rn typically 20 ohm
$R_{(CB)}$ typ 25 ohm
I balance typical =
4.2V/65ohm = 65 mA



N-channel external cell balancing

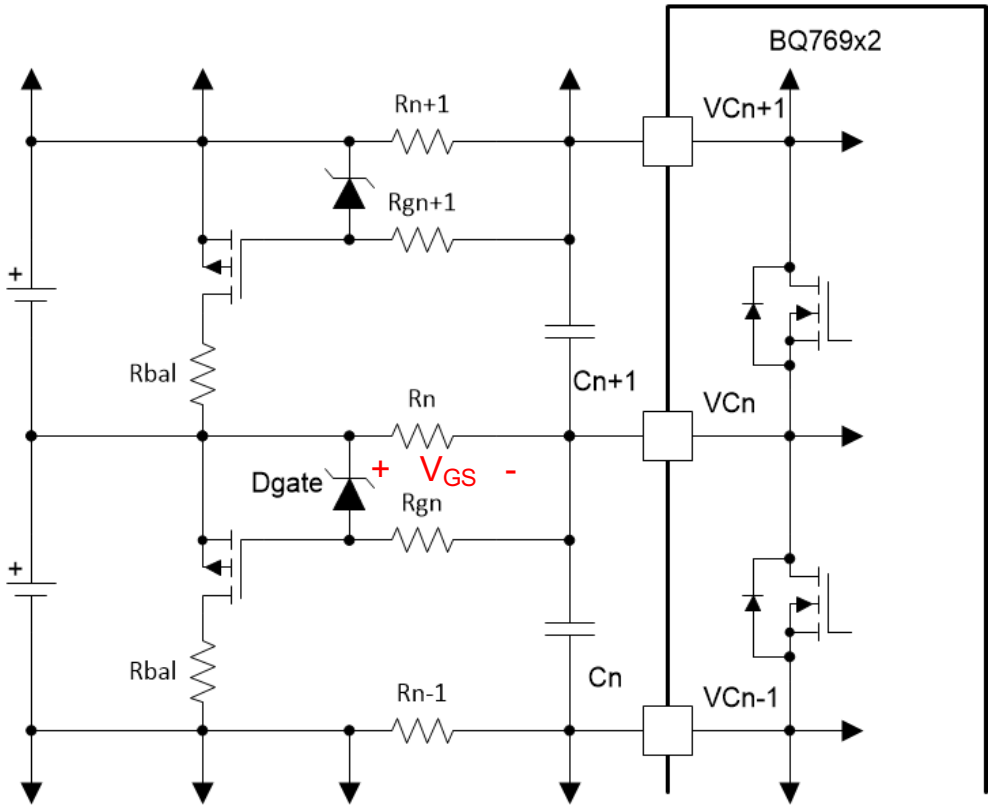
- Cell balance current can be enhanced with external FET
  - N-ch shown
  - Rn can increase to 100 ohm for larger V_{GS}
- Internal current creates voltage for gate
  - High gain of FET allows high external current
- V_{GSth} must be low, R_{DSON} specified at low voltage
- Gate must be protected by zener for pack transients
  - Cell 10 has approximately 40V across Rn during short circuit
  - Opposite transient at SCD release



4 V x (100/(200 + 25)) = 1.78 V

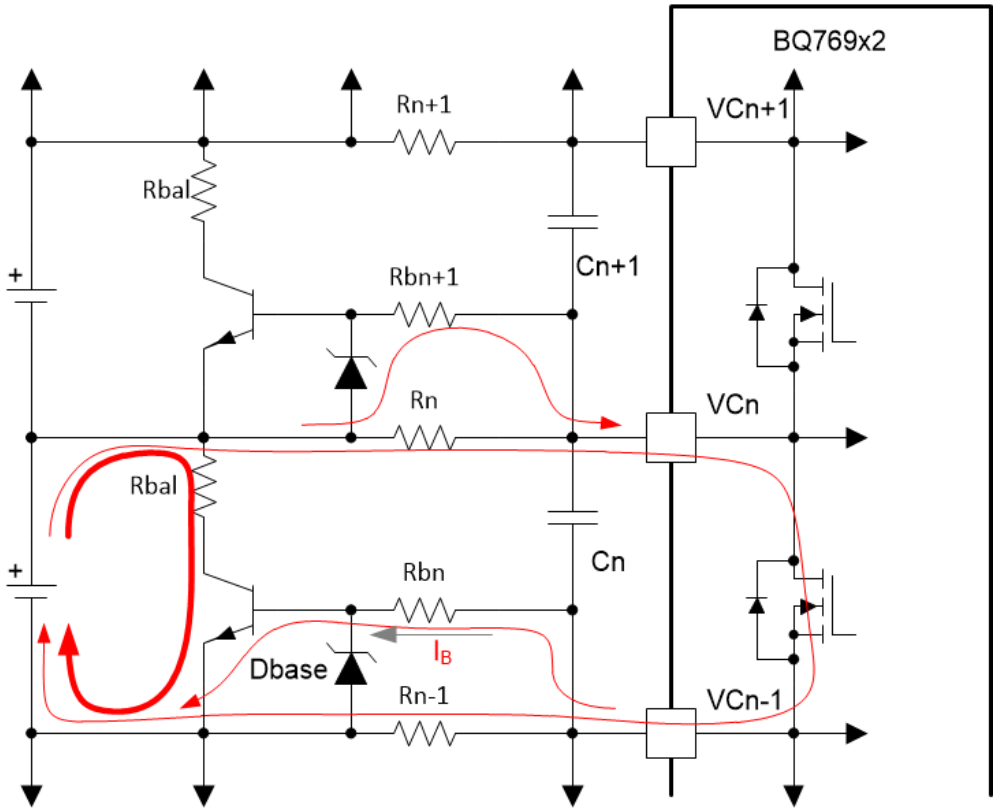
P-ch external balancing

- P-ch external balancing works also
  - V_{GS} developed on top resistor for cell



BJT cell balancing

- NPN or PNP can be used
- Rn can increase to 100 ohm
- Base current must be kept low
  - Do not connect VCn to cell with B-E diode
- Still need Zener or diode to limit below V_{EBO}
- Balance current may be limited by h_{FE}



Summary

- The BQ76942 / BQ76952 family controls high side FETs by default
  - Charge pump current is limited
  - Can support multiple FETs for higher current applications
  - Can be configured for serial or parallel FETs
- FET Configuration is flexible
  - FETs can be manually or autonomously controlled
  - Many protections can be configured to control the FETs or send an interrupt to the host
  - DCHG and DDSG pins can be configured to drive a low-side FET driver
- Cell Balance
  - Supports high internal balance current
  - External FETs or BJTs can be used to increase balance current

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