SAR & Delta-Sigma ADCs Understanding Basic Operation

TIPL 4010
TI Precision Labs – ADCs

Created by Many Authors

Presented by Ryan Andrews

Texas Instruments

Hello, and welcome to the TI Precision Lab series introducing the basic operation of the SAR and Delta-Sigma converters. The objective of this content is to give a very high level understanding of how the two topologies work. This overview in conjunction with subsequent videos should help you decide which topology is best for your application.

ADC Architecture Comparison

SAR

Advantages
- Data “snap-shot”
- Lowest latency
- Low power with power scaling
- High precision - Linearity
- Data rates up to 10MSPS

Limitations
- Limited resolution to 20 bits
- Performance determined by analog front end – application dependent

Typical applications
- Motor control
- Closed loop control systems
- Protection relays
- Medical imaging, T&M, ECG

Wide Bandwidth Delta-Sigma

Advantages
- High speed operation
- Low noise and distortion
- Integrated calibration topologies
- Data rates up to 10MSPS
- High resolution options (up to 32 bits)

Limitations
- Higher power
- Higher latency (e.g. 55 samples)

Typical applications
- Communication systems
- CCD imaging
- Radar applications
- Wide band radio

DC Optimized Delta-Sigma

Advantages
- Very high resolution ADCs (up to 32 bits)
- Ultra Low noise by digital filtering
- Application specific integration
- Simpler front-end design

Limitations
- Lower latency (1-3 samples)
- Typically useful for lower bandwidth signals

Typical applications
- Industrial sensing – RTD, thermistor, etc.
- Seismic measurements
- Power metering
- Medical ECG, EMG

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This slide provides a basic summary of the advantages and disadvantages of each topology. Notice that the Delta-Sigma topology is separated into the DC optimized and wide bandwidth subcategories. This distinction was made because the advantages, disadvantages, and usage considerations are very different for the two different types of delta sigma converters. Unfortunately, this distinction is not directly stated in the data sheet and you need to infer the difference by looking at the internal digital filter type and device sampling rate. From an applications perspective, the wide bandwidth delta-sigma behaves closer to a SAR converter.

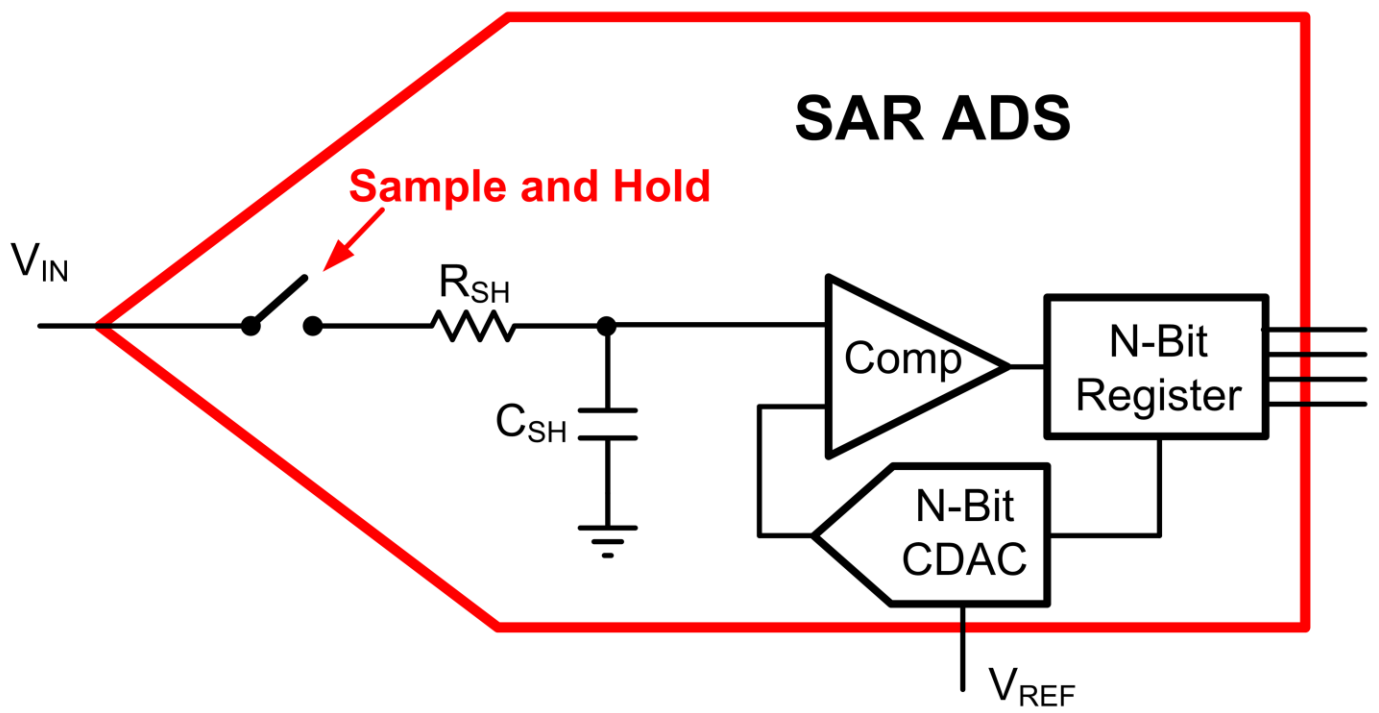
Let’s take a closer look at each category. First the SAR converter is most commonly used to capture a snap-shot in time for a transient signal. Also, SAR converters have the advantage of low latency. Latency is the delay between when the input signal is applied and the output conversion is available. We will discuss latency in detail in this presentation series.

The wide band delta-sigma has many similar characteristics to the SAR except that they frequently will have a noise and resolution advantage. On the other hand, the wide bandwidth delta-sigma has the disadvantage of higher latency than SAR.

Finally, the DC optimized delta-sigma converters are designed to measure very low bandwidth signals. These ADCs have internal digital filters that substantially limit the bandwidth and reduce noise. This category of converter typically has low latency compared to the wide bandwidth delta sigma converter.

This brief introduction is just a preview of the content that will be covered in the next few videos. In this video we will cover the basic internal mechanism used to convert voltage in a SAR and Delta-Sigma converter.

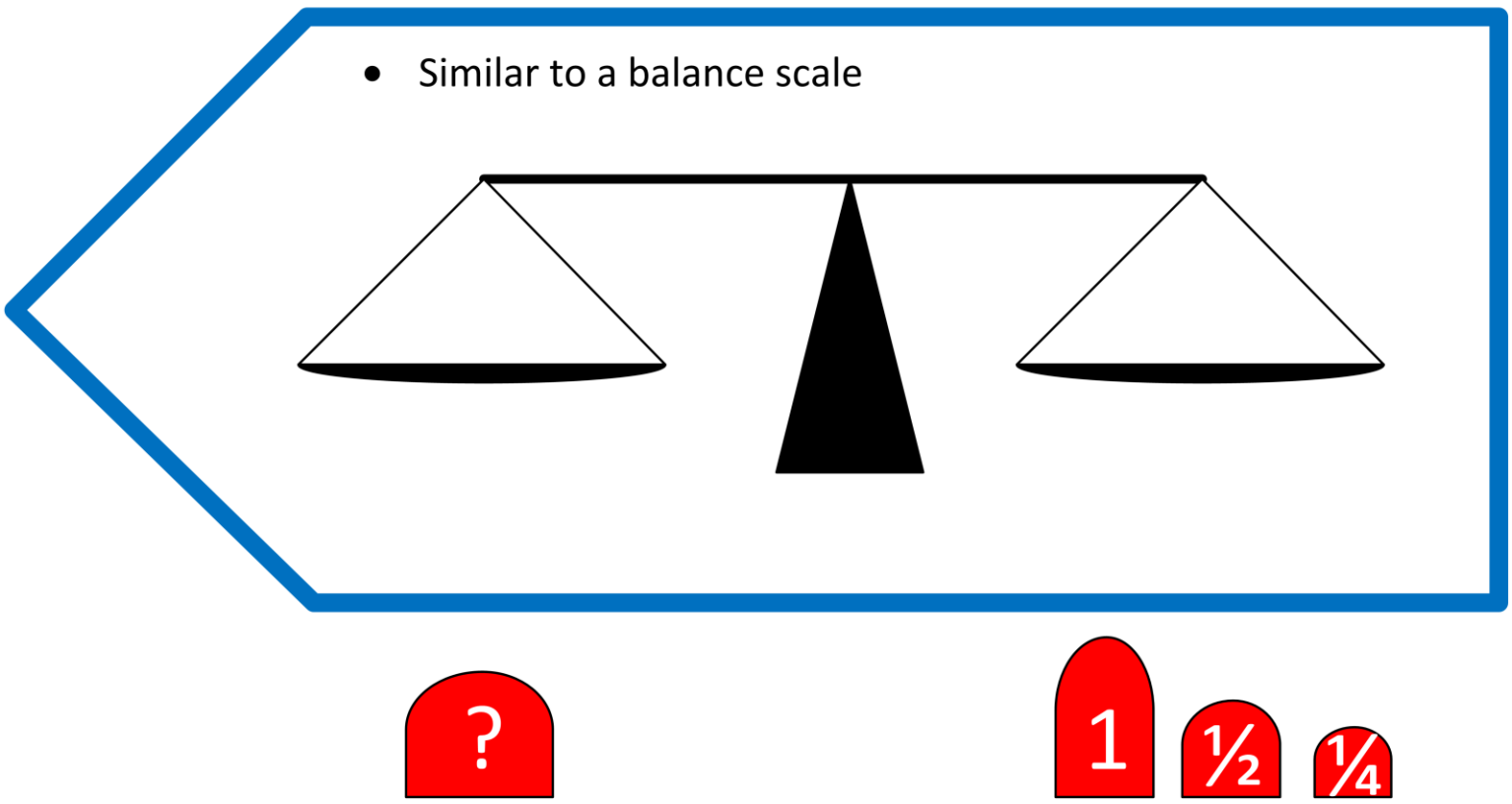
Basic diagram of SAR ADC
Successive Approximation Register



A very simple block diagram of a SAR converter is shown here. The switch, Rsh, and Csh form the sample-and-hold circuit. When the switch is closed, the sample and hold circuit will charge up to the input signal, Vin. When the switch opens the voltage on the capacitor will maintain, or hold, the voltage sampled in the previous step. While the voltage is held the converter will translate this voltage into a conversion result. The conversion is done in multiple steps by adjusting the output of the CDAC during each step and comparing it to the held voltage. In fact, the acronym SAR, stands for Successive Approximation Register. The name refers to the process where CDAC is adjusted in successive approximations to try and match the voltage stored in the sample in hold. The word register refers to the fact that the result for each conversion step is stored in a register.

Let’s consider an analogy to help clarify the SAR operation.

How Does a SAR ADC Work?



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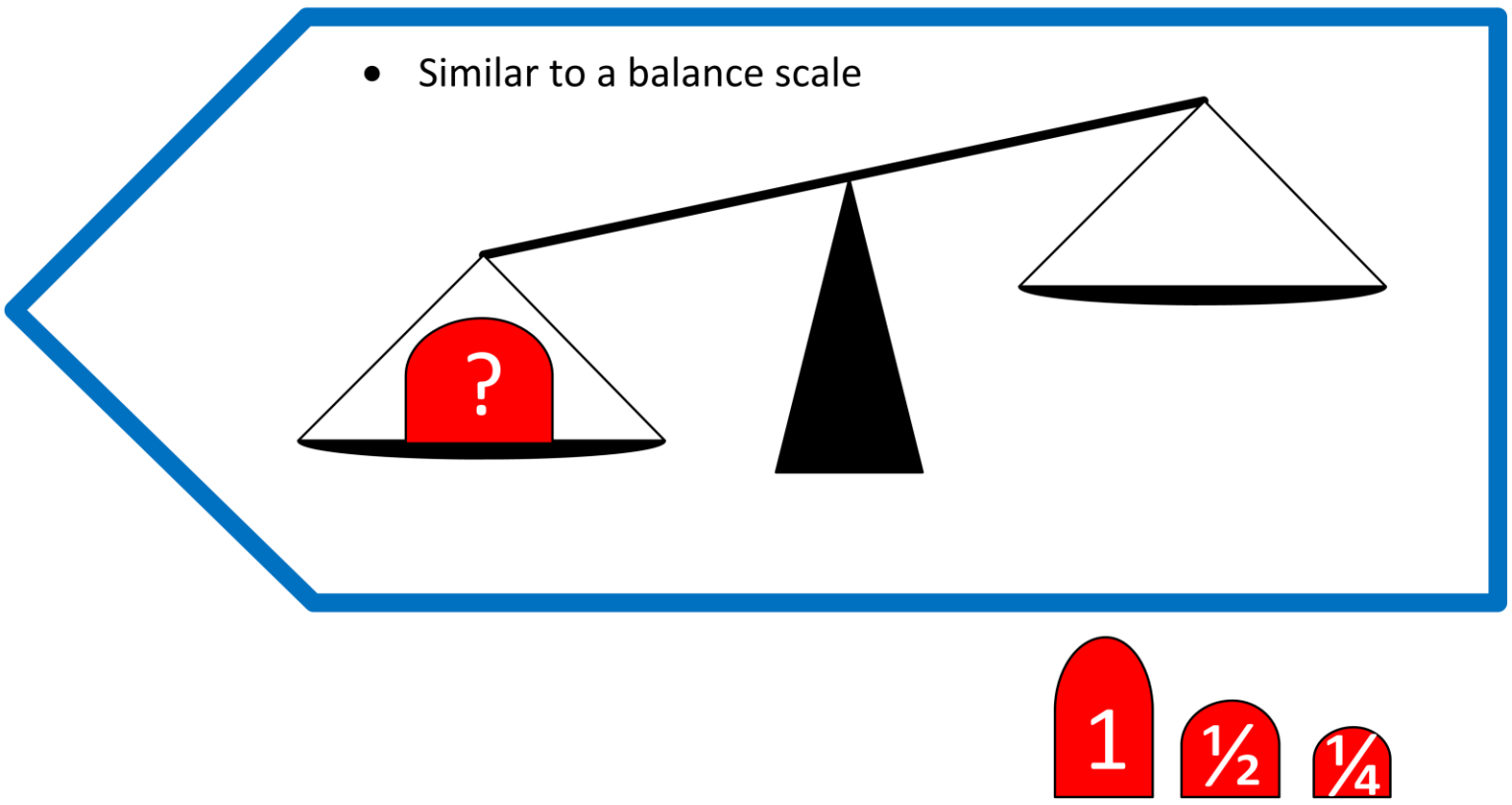
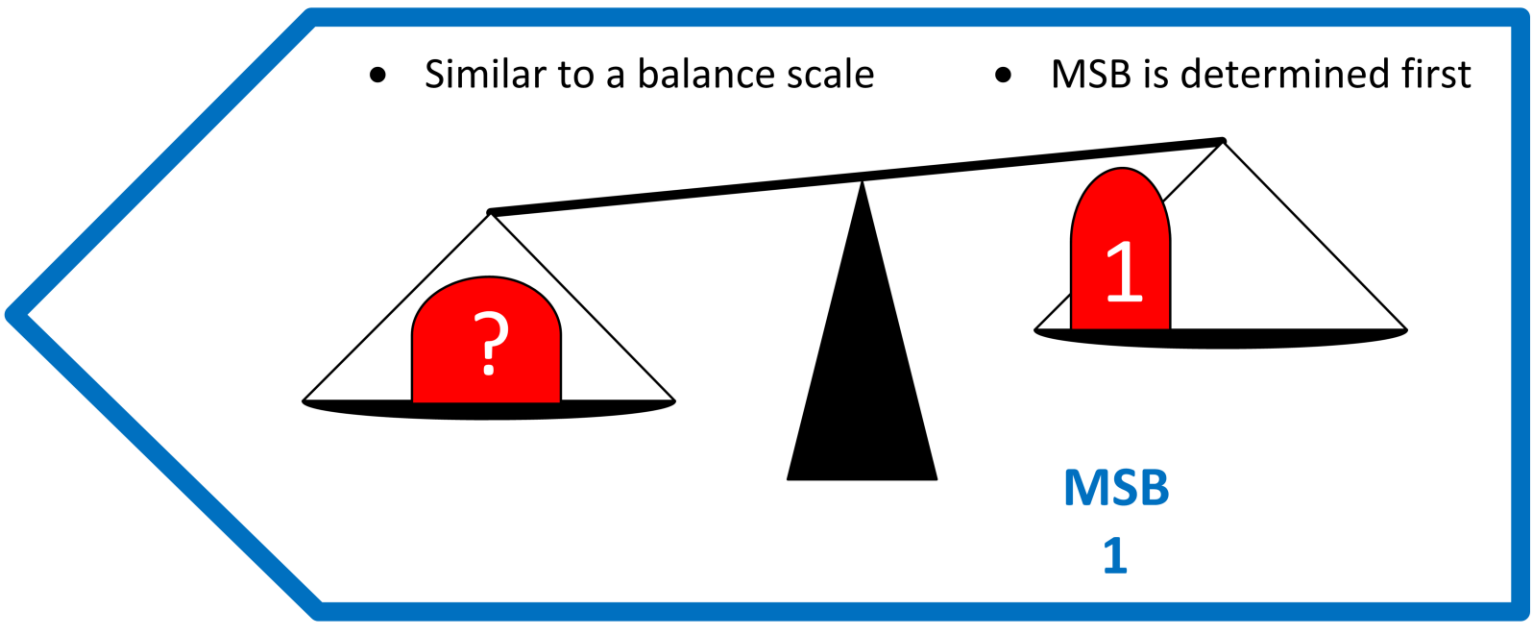
Consider the SAR to be like a balance weight scale, where the input voltage is an unknown weight. On the right side, we have several calibrated counter balance weights. These weights are scaled in binary. Since we have three counter weights, this is essentially represents a three bit converter.

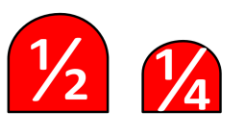
How Does a SAR ADC Work?



The first step to making the measurement is to apply the unknown weight to the left hand side of the scale. This is analogous to the sampling period, also called acquisition period, of a SAR ADC.

How Does a SAR ADC Work?





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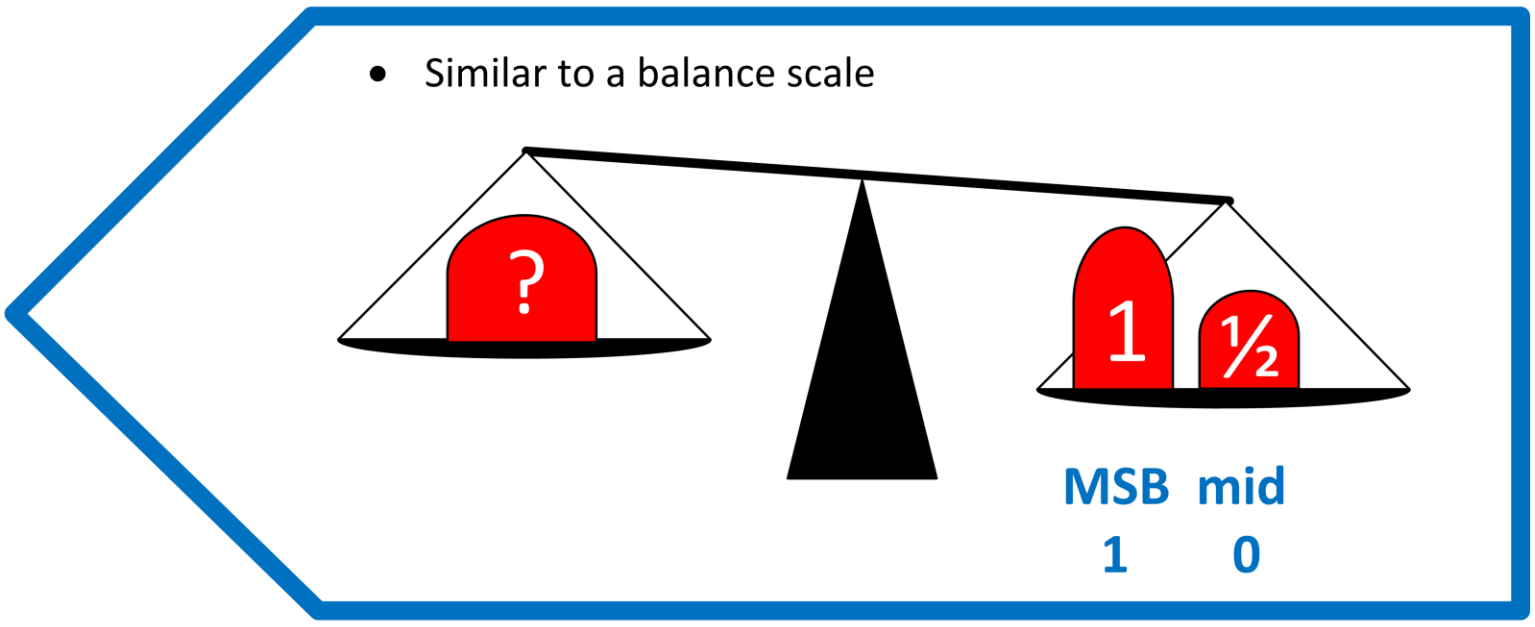
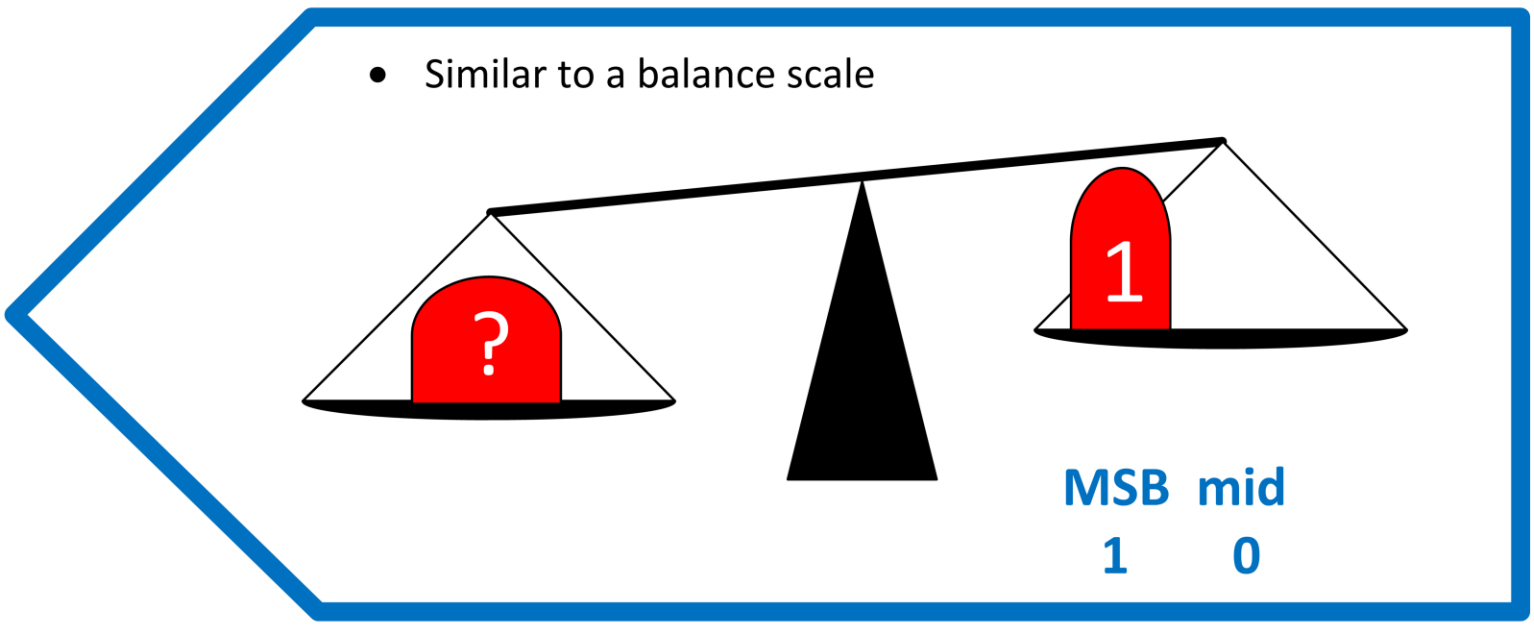
Next, we begin adding the calibrated counter balance weights, starting with the heaviest weight. This is analogous to testing the most significant bit, or MSB, in a conversion. You can see in this example that the unknown quantity is heavier than the counter weight, so it is kept on the scale and the MSB value is assigned to a binary one.

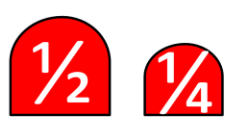
How Does a SAR ADC Work?



In the next step we add the ½ counter weight and notice that the counter weights exceed the unknown value.

How Does a SAR ADC Work?





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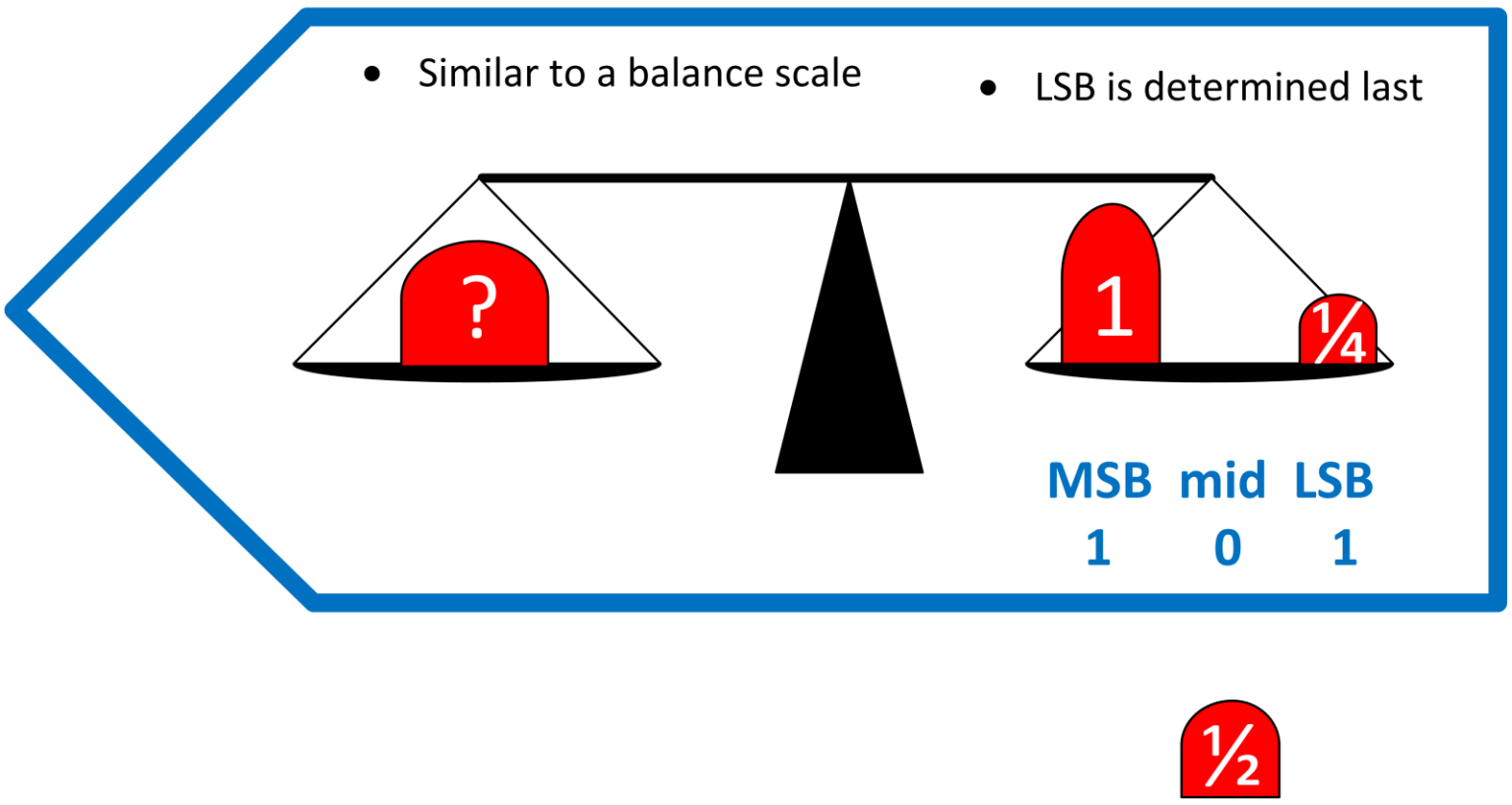
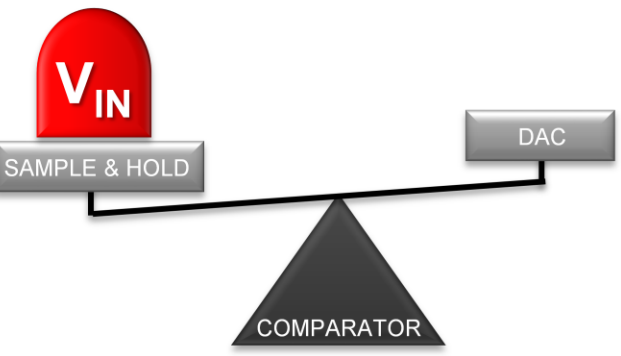
Thus, the ½ weight will be removed and the mid scale bit is assigned to zero.

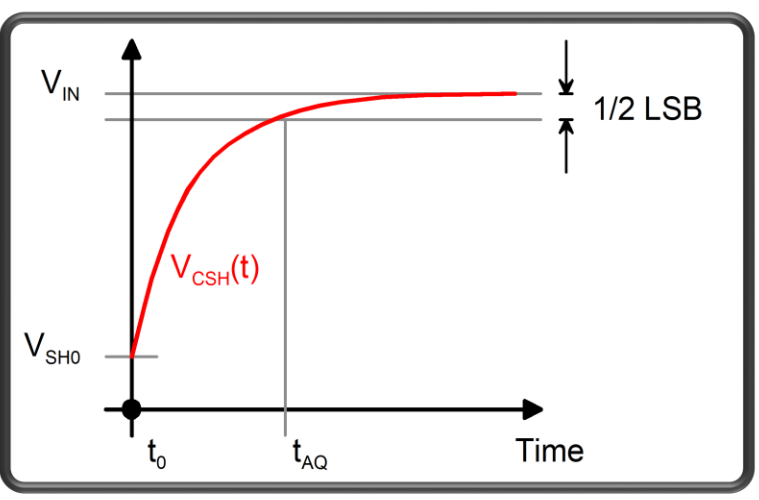
How Does a SAR ADC Work?

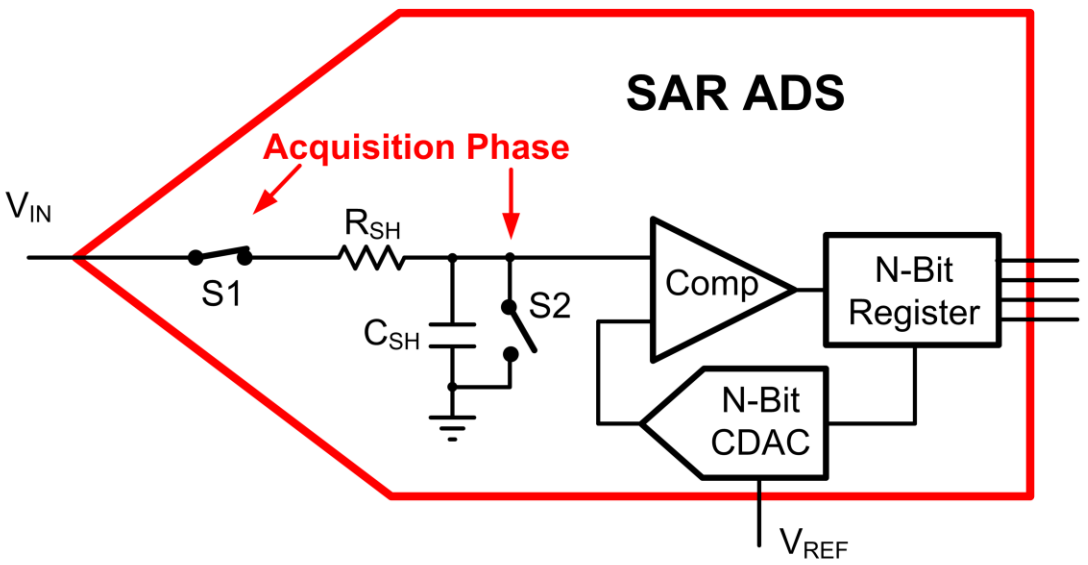


In the last step we apply the ¼ counter weight and notice that the scale is balanced. Thus, the ¼ weight will remain and the binary equivalent of the unknown weight is 101. In this analogy, the sample and hold is the left hand side of the scale, the balance point is the comparator, and the calibrated counter weights are the CDAC output. Now let's revisit the actual circuit and look deeper into some of the details.

SAR ADC Acquisition & Conversion Phase







$$V_{CSH}(t) = V_{CSH}(t_0) + [V_{IN} - V_{CSH}(t_0)] \times (1 - e^{-\frac{t}{\tau}})$$

$$\tau = R_{SH} \times C_{SH}$$

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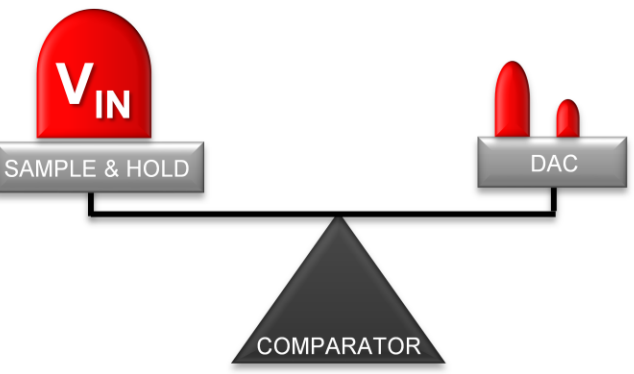
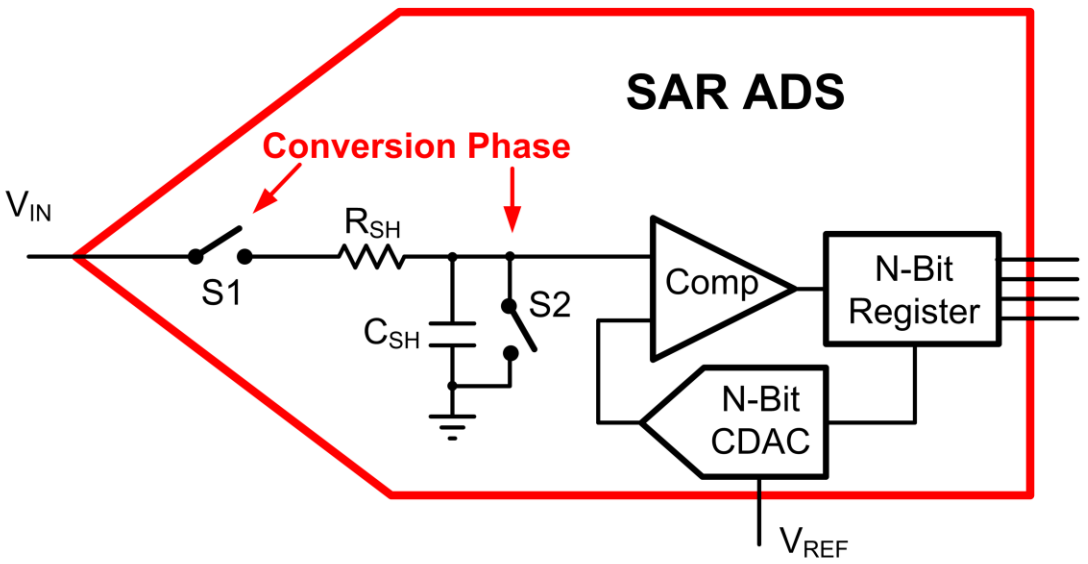
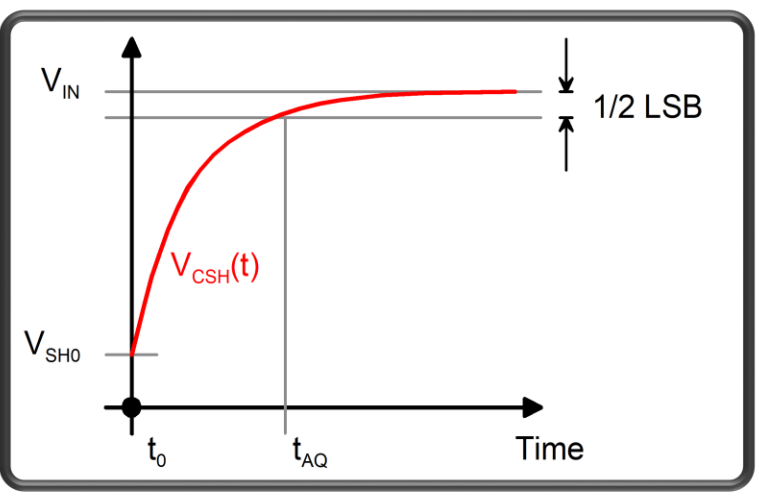
TEXAS INSTRUMENTS

Previously we mentioned that the switch and RC circuit form the sample-and-hold for the ADC. The period where the switch is closed and the ADC is sampling is called the acquisition cycle for the ADC. The length of this period depends on the sampling rate of the converter and will be given in the data sheet. For example, the ADS8860 has an acquisition period is 290ns for a sampling rate of 1MSPS. During the acquisition period, the voltage applied to the input needs to charge up the internal capacitor, Csh. Since this is an RC circuit, the capacitor will charge at an exponential rate as is shown in the graph on the left. For best accuracy, the sample-and-hold must be designed to charge to within ½ LSB of the input voltage. The ½ LSB is the maximum error that will not be detected by the ADC as it is smaller than the ADC resolution. The process of selecting the best external components to assure that the settling error is minimized is covered in detail in a later precision lab series.

SAR ADC Acquisition & Conversion Phase





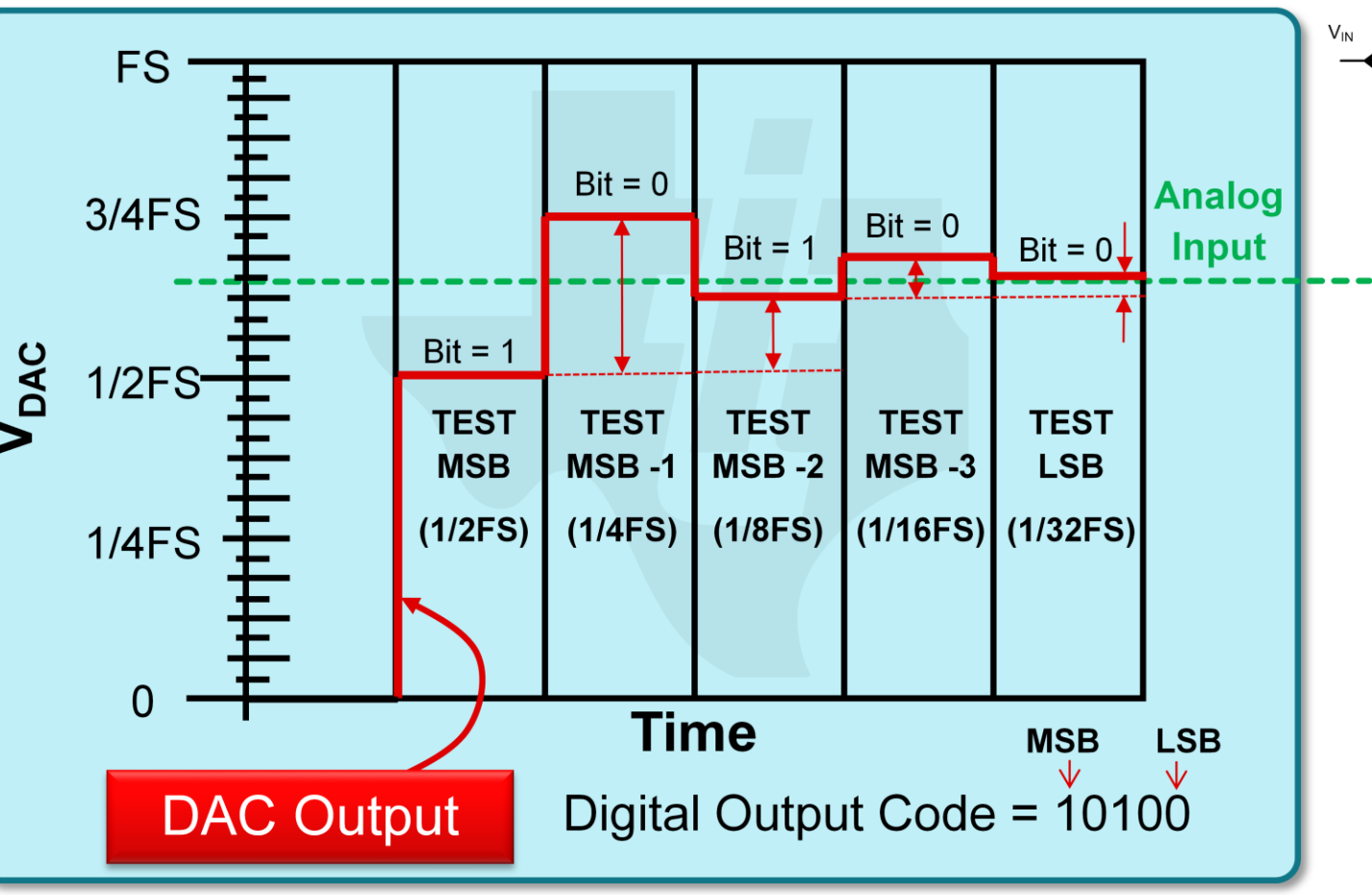


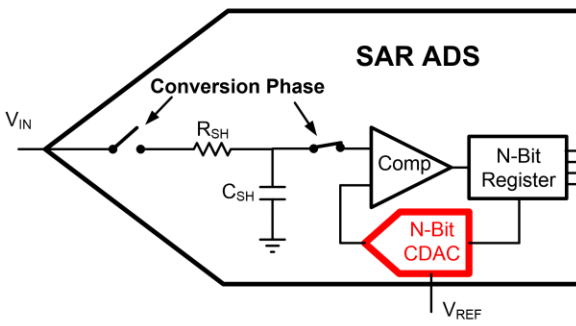
$$V_{CSH}(t) = V_{CSH}(t_0) + [V_{IN} - V_{CSH}(t_0)] \times (1 - e^{-\frac{t}{\tau}})$$

$$\tau = R_{SH} \times C_{SH}$$

After the acquisition period, the ADC begins to convert the sampled signal. It does this by adjusting the CDAC to try and match the voltage stored on the sample-and-hold capacitor, Csh. Each time the CDAC is adjusted one bit in the conversion result is calculated. Thus, a 12 bit converter will adjust the CDAC 12 times. The result of each successive approximation is stored in the N-Bit register.

SAR ADC Conversion Phase



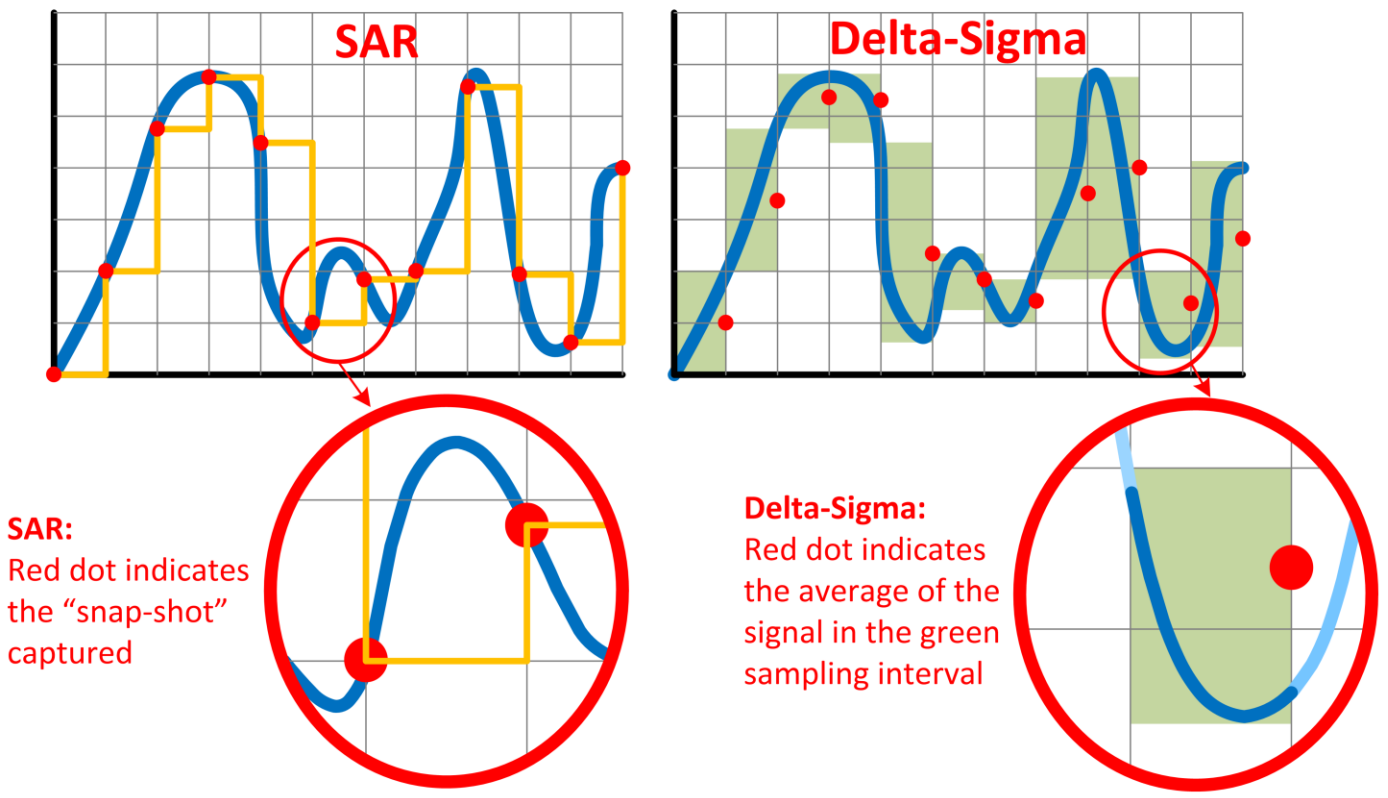


This diagram shows the conversion cycle for a five bit converter. In this example, the analog input voltage, which is stored on Csh, is shown by a green dotted line. The CDAC output is shown by a red line and always start with the heaviest bit weight, the MSB. This bit weight will be equal to ½ of the full scale range. As we step through the successive conversion steps, we will keep ON any DAC output that does not exceed the analog input, and we will turn OFF any DAC output that does exceed the analog input.

Let's step through the conversion. The MSB does not exceed the analog input so we keep this bit and set its binary value to one. The next bit test, MSB-1, does exceed the analog input, so this one is turned off and its equivalent is a binary zero. The MSB-2 test does not exceed the analog so it is kept on and has a binary value of one. The last two bits both exceed the analog input and they are turned off and have binary equivalents of zero. Thus the overall conversion result for this example is 10100.

In following videos we will revisit this simplified view of the SAR ADC and use it to help with input drive and voltage reference drive topics.

SAR vs Delta-Sigma Sampling

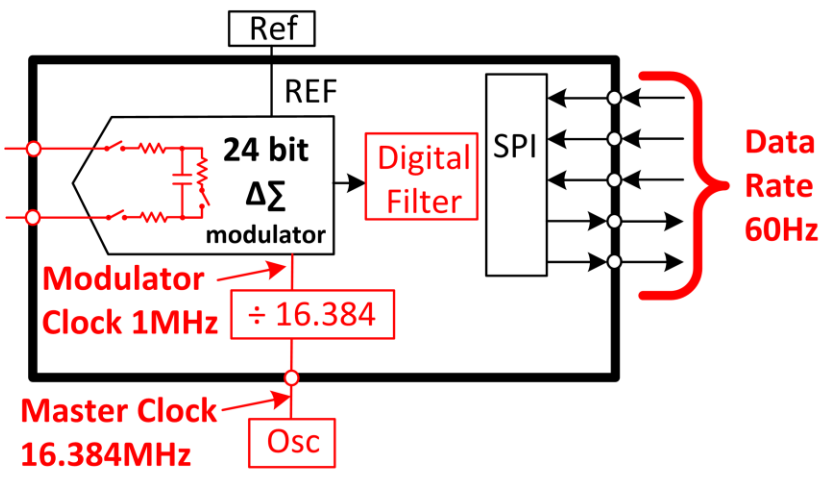


This figure compares the SAR conversion method on the left to the delta-sigma conversion method on the right.

The points in time where the SAR sample-and-hold captures the signal are shown with the red dots. People often refer to the SAR conversion as a snap-shot, because the sample-and-hold circuit "freezes" the voltage level during the hold period similar to the way that a camera captures a picture when the shutter snaps.

The delta-sigma, on the other hand, has more of an averaging effect over a time interval. Looking at the figure on the right, you can see that each green interval indicates the conversion period for the delta sigma. At the end of the conversion period, the conversion result is calculated as the average value of the signal across the interval. This average value is represented by a red dot in this figure. Of course, saying that the delta-sigma simply averages across the time interval is an oversimplification. For the remainder of this video, we will provide some more details about the internal operation of the delta-sigma converter. These details will help you to better understand the advantages and disadvantages of this topology, as will as give you insight into their data sheet specifications.

Simplified model of ΔΣ ADC



Oversampling Ratio:
OSR = Modulator Clock / Data Rate
OSR = 1MHz/60Hz = 16k

Simplified Model of ΔΣ operation

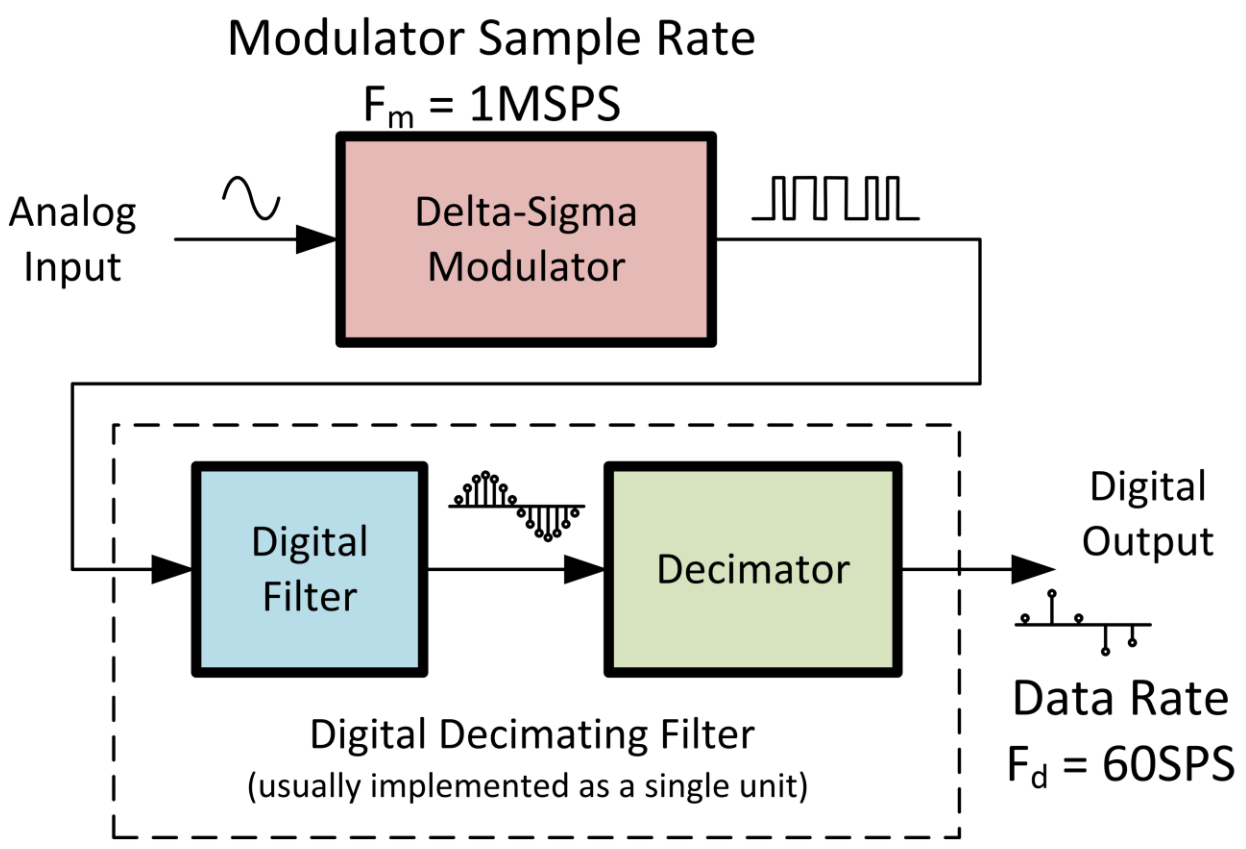
- The input 1-bit converter is sampling at 1MHz rate (**modulator clock rate**)
- The ***master clock*** is divided by 16.384 to set ***modulator clock*** to 1MHz
- 16,000 samples are "averaged" for each output sample
  - ✓ The ratio of input to output samples is called oversampling ratio (**OSR**)
- The output **data rate** is the frequency that output samples are read at (e.g. 60SPS)
  - ✓ The OSR can be calculated OSR = Modulator Clock / Data Rate
  - ✓ In this example OSR = 1MHz / 60Hz = 16k
- The "Data Rate" is analogous to the "Sampling rate" of a SAR ADC

Let's start by considering a very simplified model of a delta-sigma ADC.

One key point to remember with the delta-sigma is that the input circuit, called a modulator, is sampling at a faster rate then the output data rate. In this example, the modulator is sampling at a 1MSPS rate. Note that the modulator clock is derived from and external master clock. In this example, the external master clock is running at a rate of 16.384MHz and is divided down to a rate of 1MHz for the modulator.

The conversions from the modulator are averaged and filtered by a digital filter. The output data rate is always lower than the modulator sampling rate. In this example the modulator is sampling at 1MHz and the output data rate is only 60Hz, or 60 SPS. Thus for each data word read at the output of the converter, 16,000 input samples are averaged together. The ratio of the modulator rate divided by the output data rate is called the oversampling ratio, or OSR. In this example the OSR is 16,000. Throughout the remainder of this presentation, we will focus on the operation of the delta-sigma converter.

Understanding the Delta-Sigma ADC



Input and Output Sampling Rate

Modulator Data Rate = F_m = 1MSPS

Output Data Rate = F_d = 60SPS

OSR = F_m/F_d = 16,000

OSR = 1MSPS/60SPS = 16,000

OSR = Oversampling Ratio

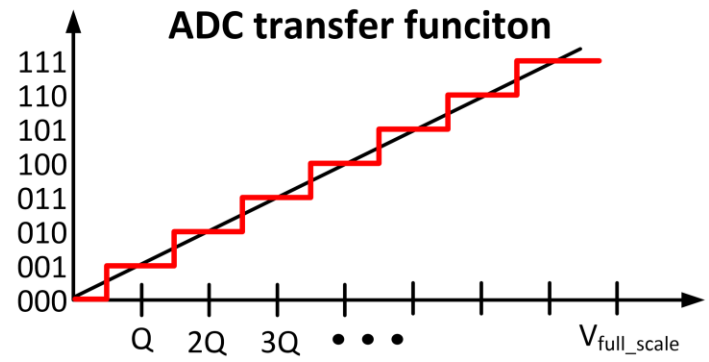
The simplified model on the previous page can be redrawn like this block diagram.

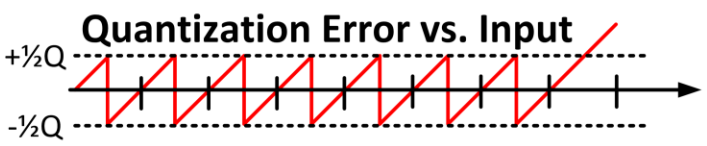
Starting on the left, analog input signal is applied to the modulator. The modulator essentially behaves like a one-bit converter and converts the analog input to a pulse-code modulated or PCM signal. This PCM signal is applied to a digital filter which uses averaging to convert this bitstream to a higher resolution signal. The decimator eliminates samples so that the output data rate is a fraction of the input data rate.

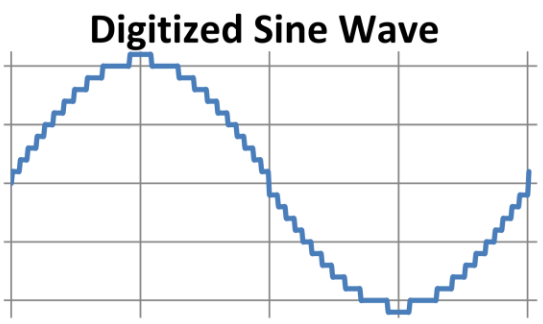
Again, if the input is averaged 16,000 times, the decimator will output one sample for every 16,000 input samples. A large oversampling ratio indicates a lot of averaging has been done to the signal. Oversampling reduces noise and increases output resolution.

To understand more details on the modulator and digital filter, we first must cover a very short explanation of quantization noise and oversampling. The objective here is to briefly introduce these topics to help with the explanation of the delta-sigma topology, and in later videos, we will do a more comprehensive discussion on these topics.

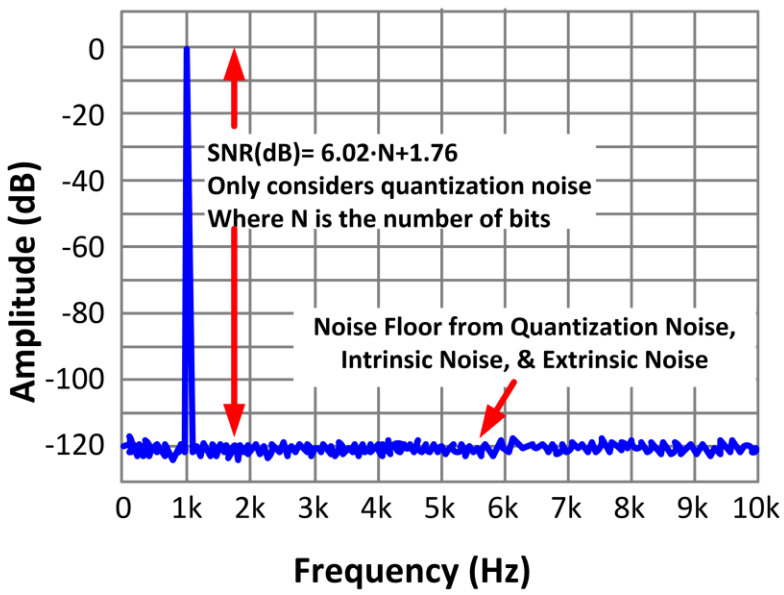
Quick Introduction to Quantization Noise







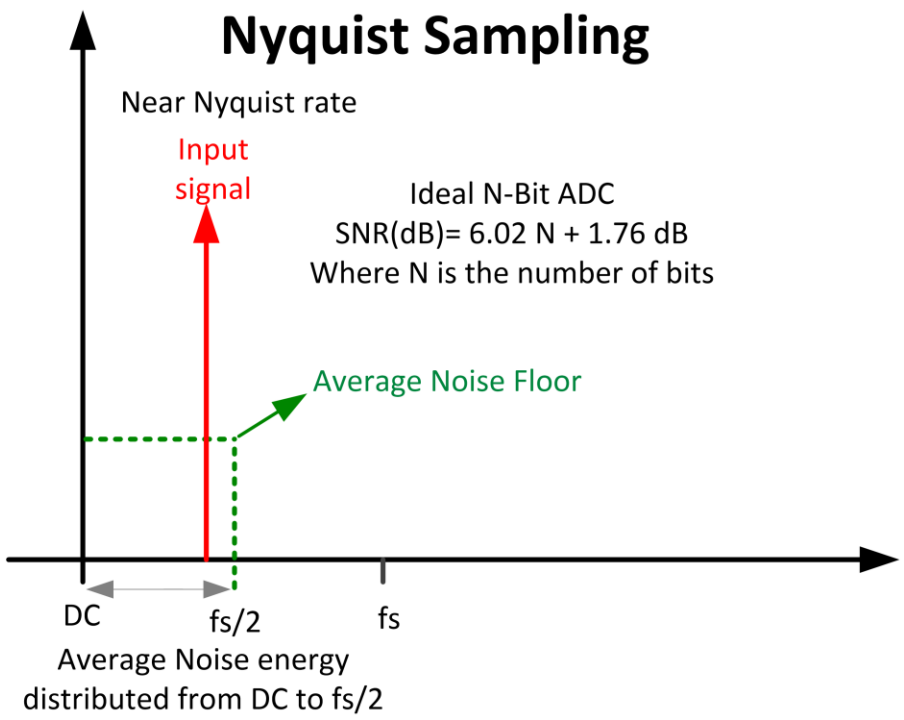
- Quantization noise is a “rounding” error
- The error looks triangular in time domain
- In frequency domain, harmonics fold back to create “white noise” floor



First let’s discuss the concept of quantization noise. All data converters, will “round” the analog input signal to discrete digital levels. This process is referred to as quantizing the signal, and the associated error is called quantization error. If you apply an ac sine wave to an analog-to-digital converter, the resultant digitized waveform will have an error that looks like a saw tooth waveform vs time. The FFT of that saw tooth waveform will produce harmonics across a wide frequency range, and the harmonics will alias back into the Nyquist frequency band. The result is that the noise floor appears like “white” noise. In fact, the signal-to-noise ratio due only to quantization noise can be mathematically predicted with the equation SNR (expressed in decibels) = 6.02*N+1.76., where N is the number of bits in the converter. Note that this equation only applies to a sinusoidal wave input.

The important thing to note here is that the noise floor of an ideal analog-to-digital converter is determined by the quantization noise.

Nyquist Sampling Rate



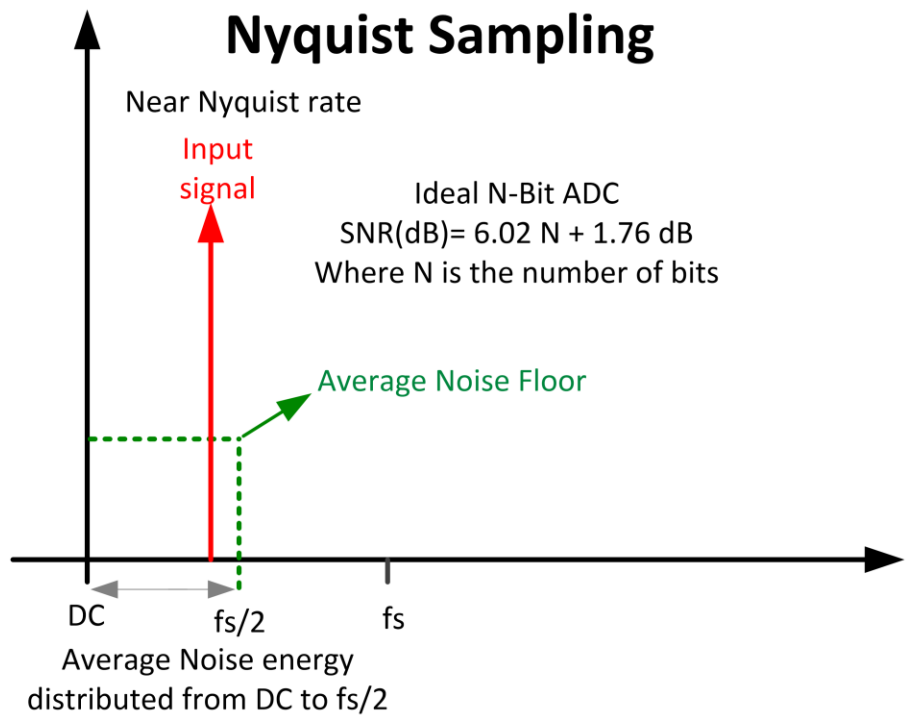
Definition of Terms:

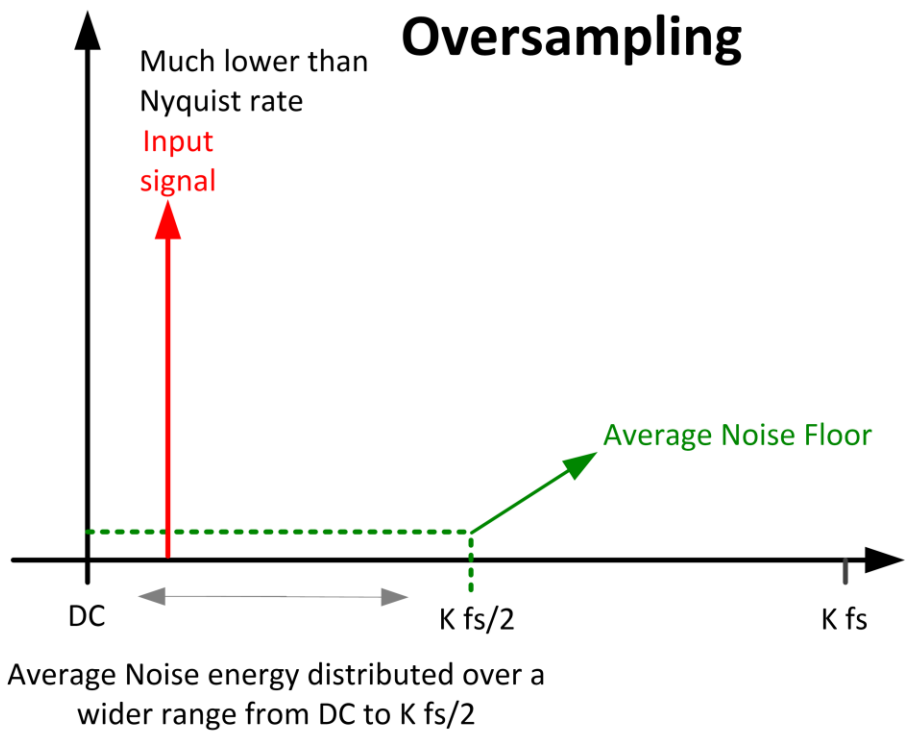
Nyquist Sampling	The input signal may be at or near the Nyquist rate
$f_s/2$	Nyquist frequency. The maximum applied frequency with out aliasing
f_s	Sampling frequency
Noise Floor	The noise floor is set by quantization noise. SNR(dB) = 6.02N + 1.76
N	Number of bits

When sampling a signal at discrete intervals, the Nyquist-Shannon sampling theorem states that the sampling frequency (Fs) must be greater than twice the highest frequency component of the input signal in order to reconstruct the original signal from the sampled version. This minimum sampling rate is known as the Nyquist rate. In later videos, we will discuss aliasing in more detail, but for now, just realize that our usable frequency range is from dc to the sampling frequency divided by two, known as the Nyquist frequency. Applying an input signal beyond the Nyquist frequency will cause alias frequencies to fold back into the Nyquist frequency band. Most ADC's sample at frequencies close to the Nyquist rate.

The quantization noise for an ADC with N-Bit resolution is evenly distributed over the sampled bandwidth between DC and the Nyquist Frequency. The signal-to-noise ratio (or SNR) for an ideal ADC is given by the equation SNR (expressed in decibels) = 6.02*N+1.76, where N is the number of bits.

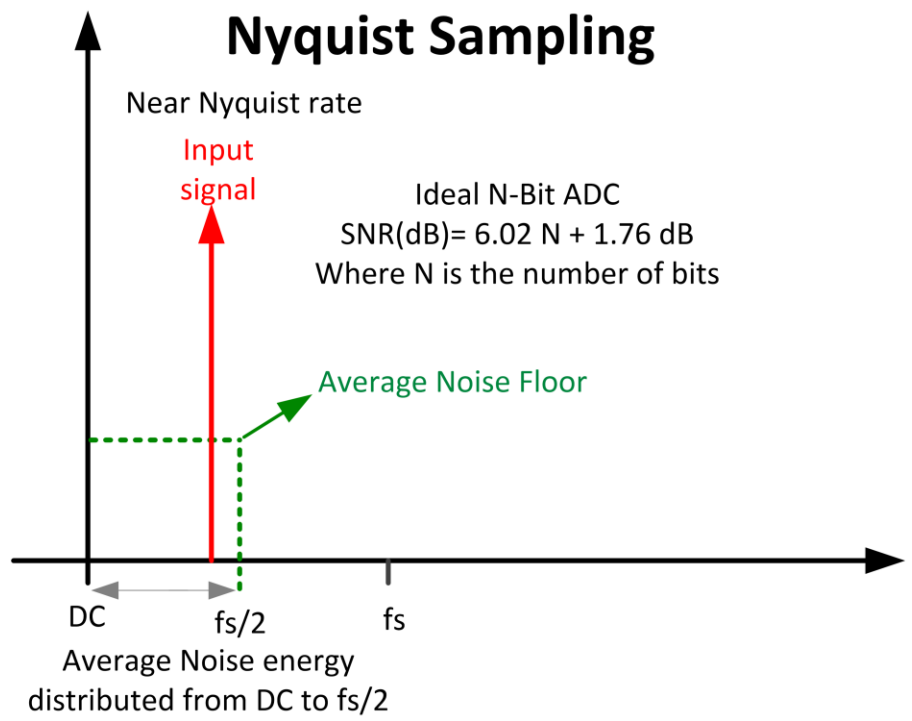
Oversampling vs. Nyquist Sampling

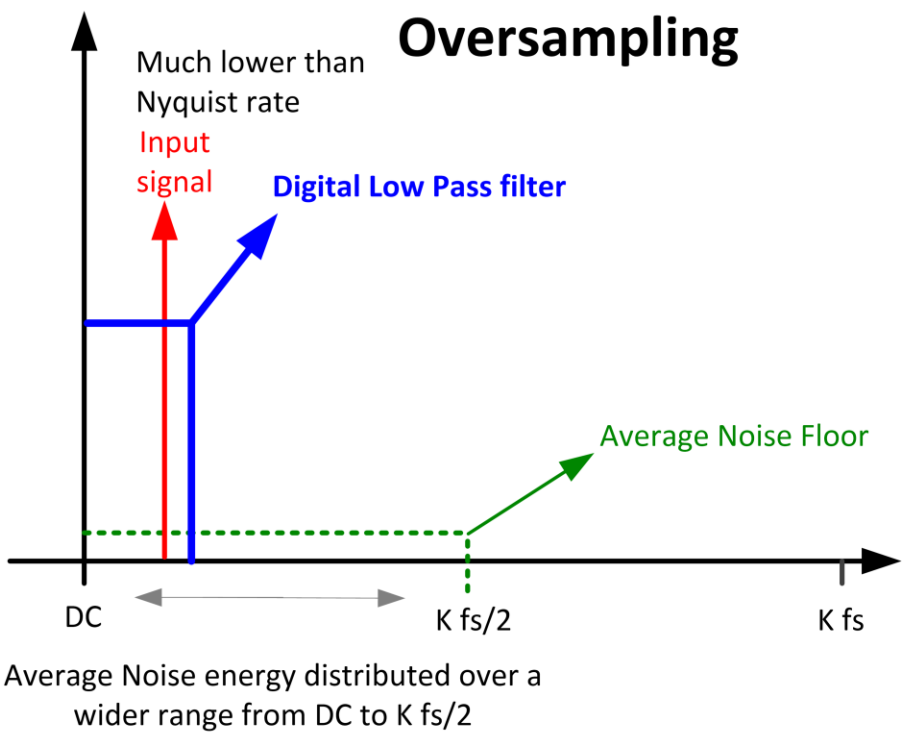




The Oversampling FFT plot (on the right), shows the effect of oversampling. The input signal frequency is the same, but the sampling frequency has been increased by an oversampling ratio k. Oversampling increases the bandwidth considerably, hence it spreads the quantization noise over a wider bandwidth. The quantization noise power remains constant, but the quantization noise is now spread over a higher sampled bandwidth from DC to K Fs/2. It is important to realize that the total amount of noise power remains the same, but the noise has been spread over a wider frequency range, and the noise level in each frequency bin in the FFT has been reduced.

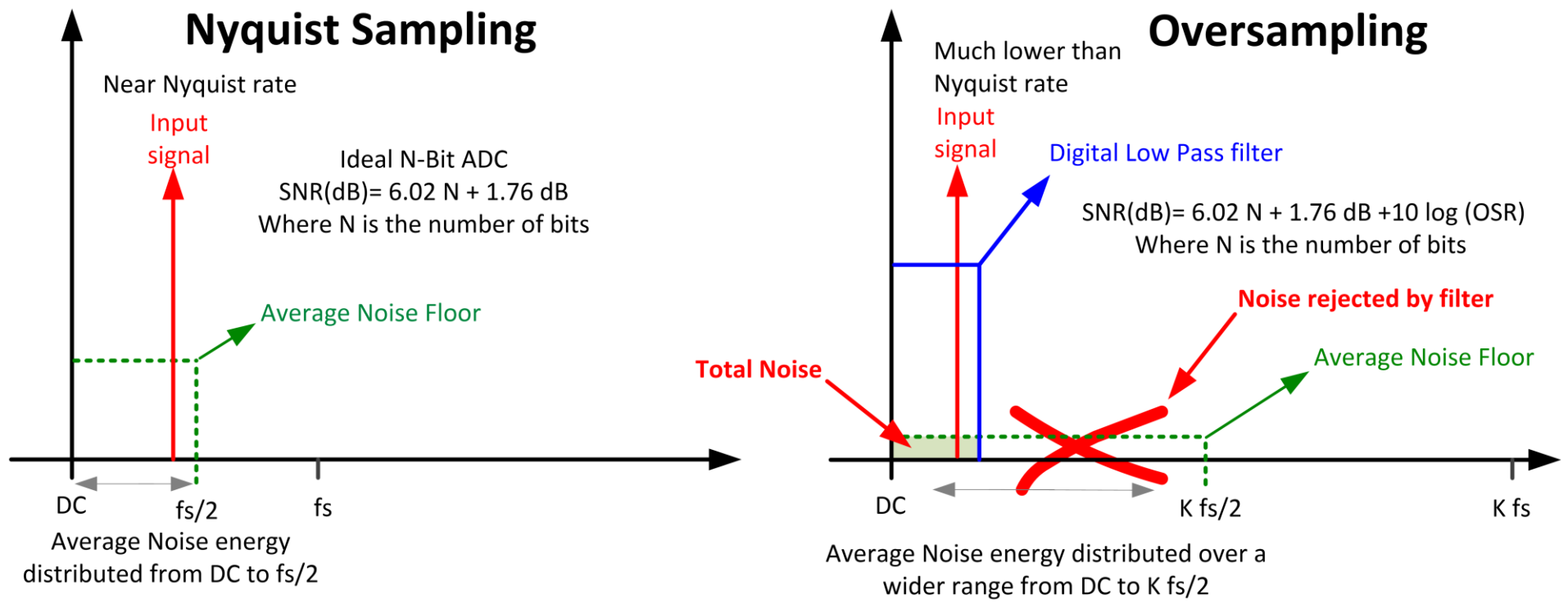
Oversampling vs. Nyquist Sampling





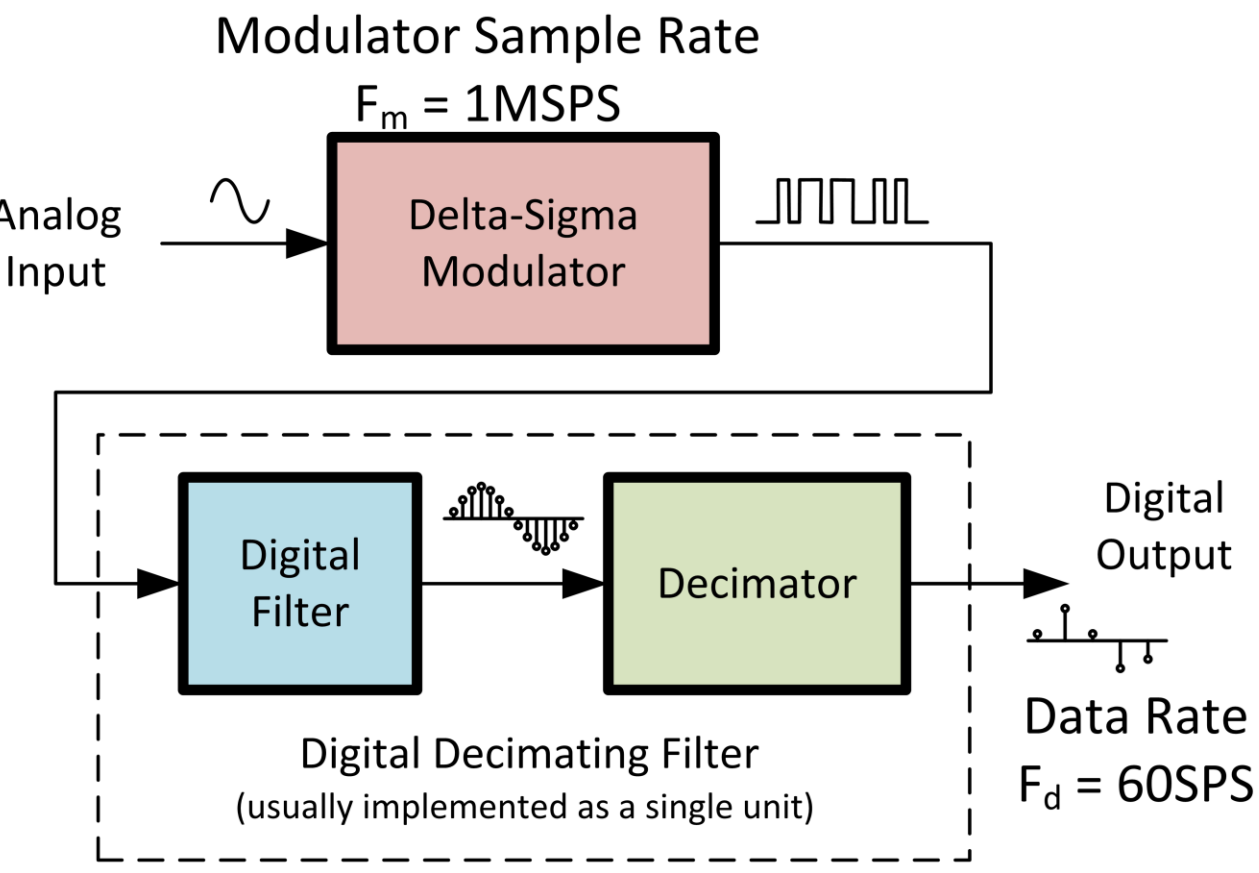
A digital low-pass filter can be used to eliminate the high frequency noise, while keeping the input frequency signals of interest.
In this example the digital filter in the oversampling example has the same bandwidth as the Nyquist sampling.

Oversampling vs. Nyquist Sampling



The digital filter retains a small amount of the total noise and rejects the noise outside the filters bandwidth. In this manner, oversampling can be used to increase resolution. After filtering the high frequency components, the ideal SNR can now be calculated by the equation [SNR (dB) = 6.02N+1.76 + 10LOG(OSR)] where OSR is the oversampling ratio. The term 10*log(OSR) is the noise improvement gained from oversampling. Notice that both formulas are the same except for this term.

Delta-Sigma ADC Topology



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OSR = 1MSPS/60SPS = 16,000

OSR = Oversampling Ratio

With the concepts of quantization noise and oversampling in mind, let's return to this slide which illustrates the internal delta-sigma signal chain.

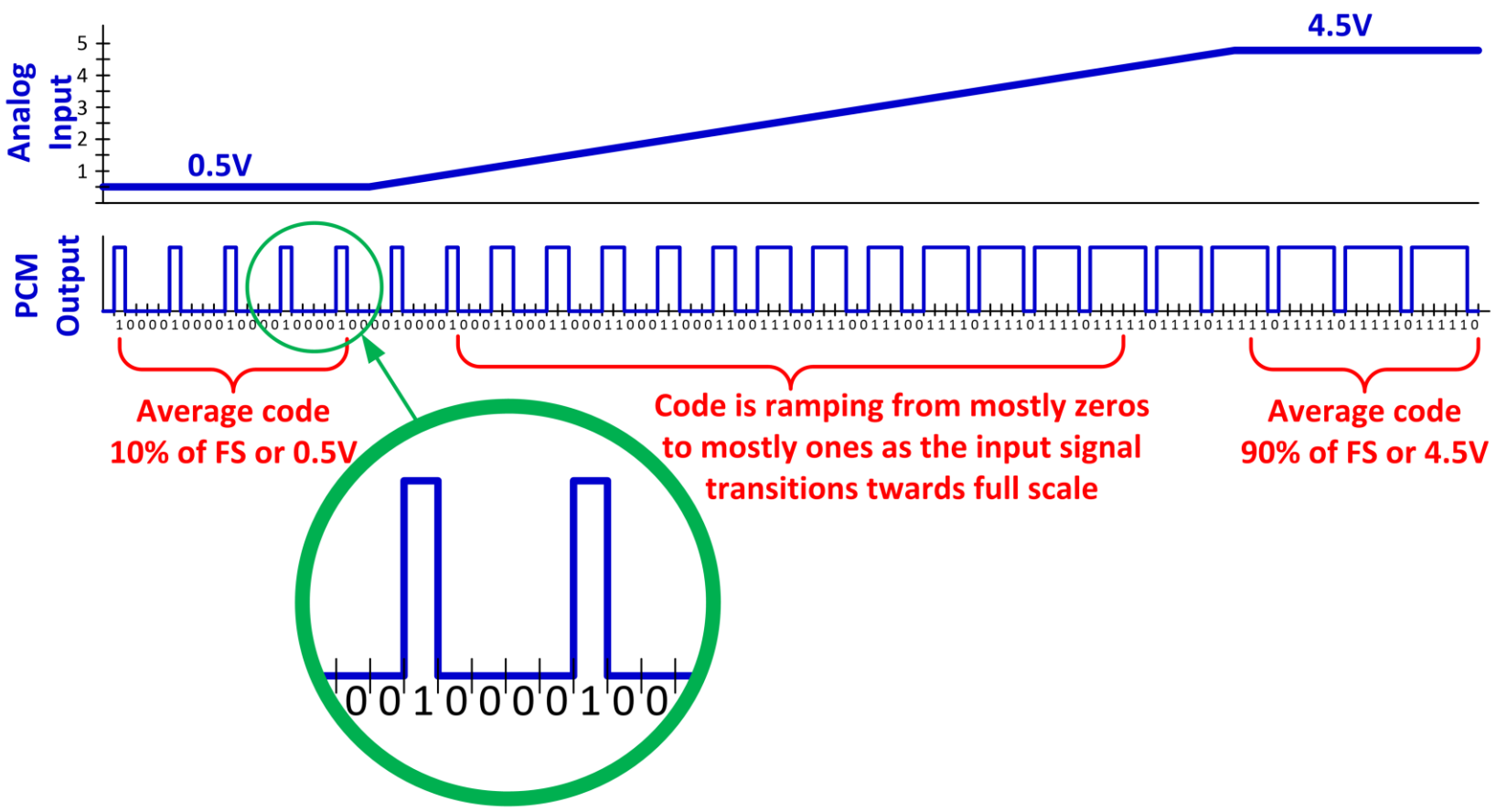
The main purpose of the modulator is to convert an analog input to a pulse code modulation output, or PCM. Pulse code modulation is a bit stream where the average value is proportionate to the analog input. So for small analog inputs the PCM bit stream is mostly zeros and for a large analog input the bit stream is mostly ones. In this example the modulator is running at a 1MSPS frequency, so the PCM bit stream is also output at that rate.

(can skip for recording)

~~The PCM bit stream output is then applied to the digital filter. The filter will average the bit stream as well as limit the frequency of the digitized analog input. In this example the filter averages 16,000 samples to produce one output sample. The decimator removes unneeded data and only provides a single result for 16,0000 input samples. The number of averages being done is the oversampling ratio, or OSR. Sometimes this is called the decimation ratio as well since decimator will keep only one of the 16,000 samples. Finally, the output sampling rate is often called the "data rate". This sampling rate can be calculated by dividing the modulator sampling rate by the over sampling rate. In this example dividing 1MSPS by 16,000 gives a sampling rate of 60SPS.~~

In the next slide we will take a closer look at the modulator and a PCM example.

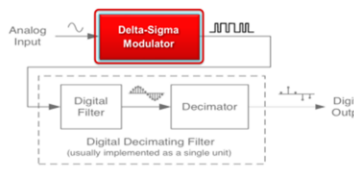
What is pulse code modulation (PCM)

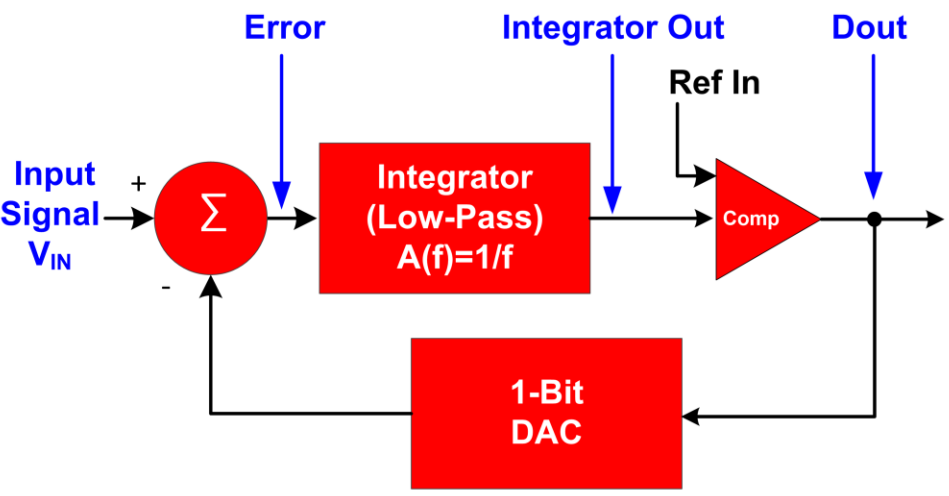


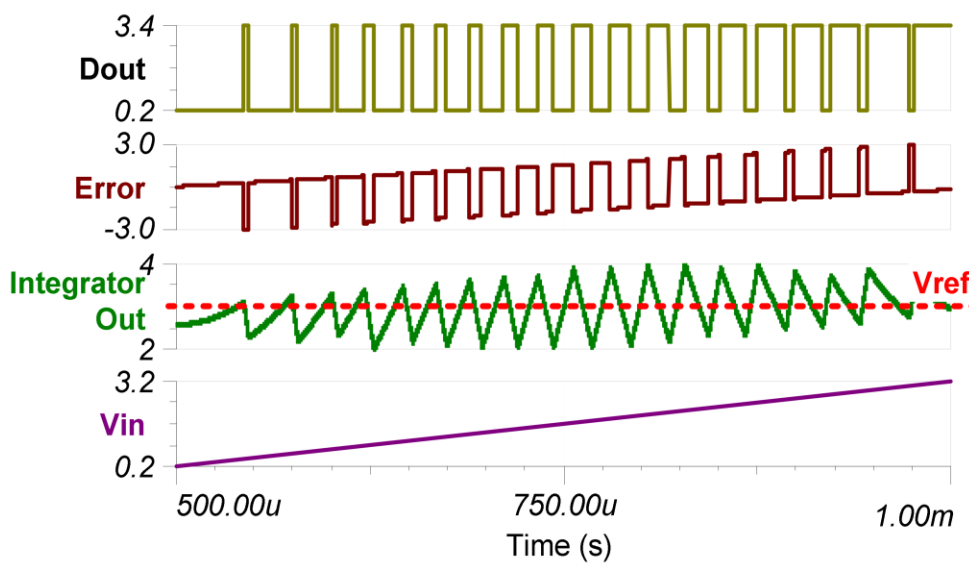
This slide show a pulse code modulation example. Note that the occurrence of ones and zeros relates to the analog input. For low analog input levels the PCM bits will be mostly logic zeros, and for high analog input levels the PCM bits will be mostly logic ones. Averaging the PCM bit stream is done by adding the ones and zeros and dividing by the number of bits averaged. If we consider the example from the last slide, 16,000 bits would be averaged to produce one output sample. Also, the frequency of the digital output bit stream is the frequency that the modulator is running at, so this bit stream would be output at a rate of 1MHz. Now lets take a closer look at how the modulator converts its analog input to a PCM output.

1st Order Delta-Sigma Modulator

Time Domain





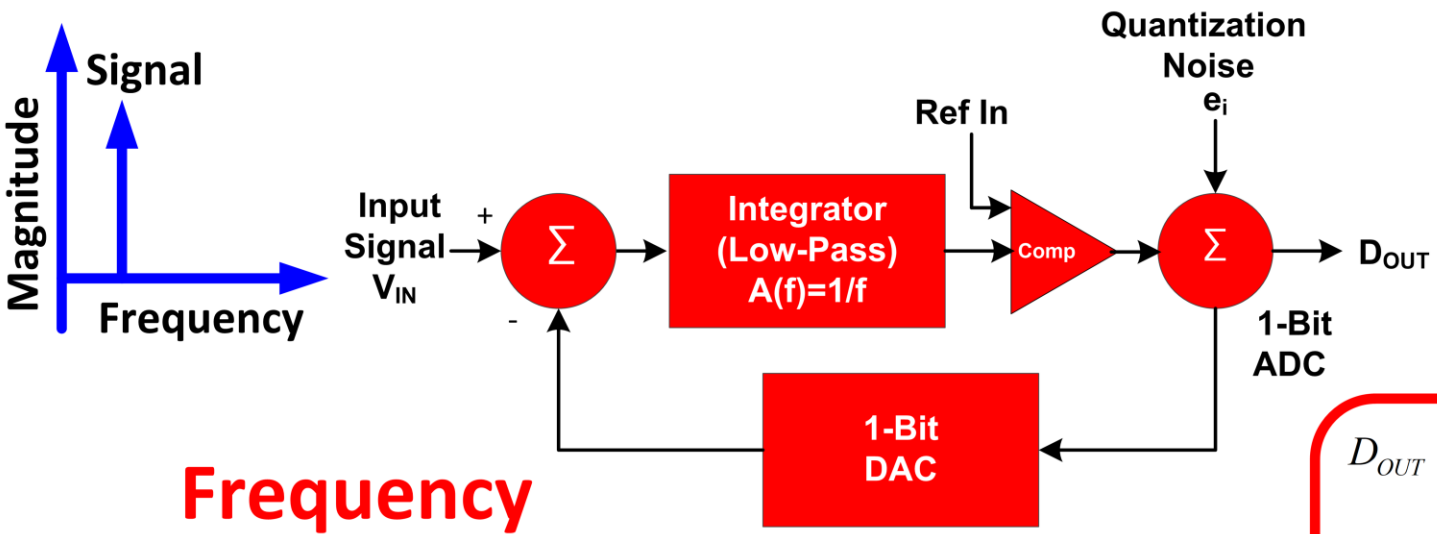


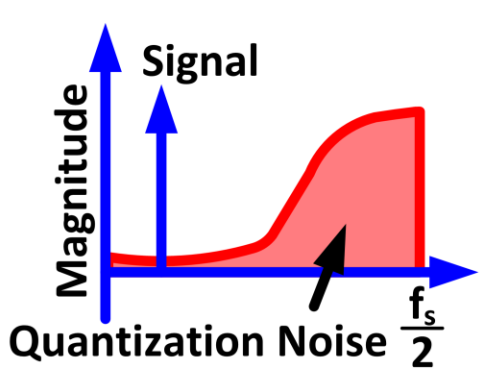
This slide shows the block diagram internal to the modulator. This is a control systems style diagram. The objective of this control loop is to keep the error between the analog input and digital output as small as possible.

In order to compare the analog input to the digital output, the output is converted back to analog with a 1-bit digital-to-analog converter. This is shown in the feedback loop and input error summing block. The error from the input summing block is integrated as is commonly done in many control systems. As the output of the integrator gets larger, the comparator will trip the digital output to a logic one. This action will cause the error to go negative and the integrator will then ramp in the opposite direction. Thus, the closed-loop system will tend to keep the error minimized by periodically transitioning the output of the comparator to a one or zero. If you average the ones and zeros after a long period of time, you will get a digital equivalent of the analog input.

As with many of the explanations here, this is an oversimplification. However, this description should give you some intuition into how the delta-sigma modulator operates, which will be helpful in interpreting the data sheet and comparing and contrasting other converters.

1st Order Delta-Sigma Modulator





Frequency Domain Analysis

$$D_{OUT} = (V_{IN} - D_{OUT})\frac{1}{f} + e_n$$

$$D_{OUT} = e_n\left(\frac{f}{1+f}\right) + V_{IN}\left(\frac{1}{1+f}\right)$$

HPF Noise Transfer Function

LPF Signal Transfer Function

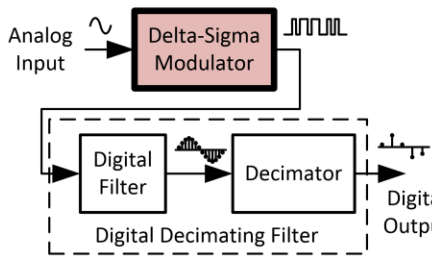
This block diagram of the Delta-sigma modulator shows the input signal and noise transfer function in the frequency domain. Analyzing the transfer function, you can see that the output is fed back and subtracted from the input signal. Assume that the one bit DAC is essentially a gain of one. Thus, the output of the summing block is Vin – Dout. This is then multiplied by the integrator, with a gain of 1/f. Finally, the quantization noise term is added in the output summing block. This is where we get the first first equation, Dout = (Vin – Dout)*1/f +e_n.

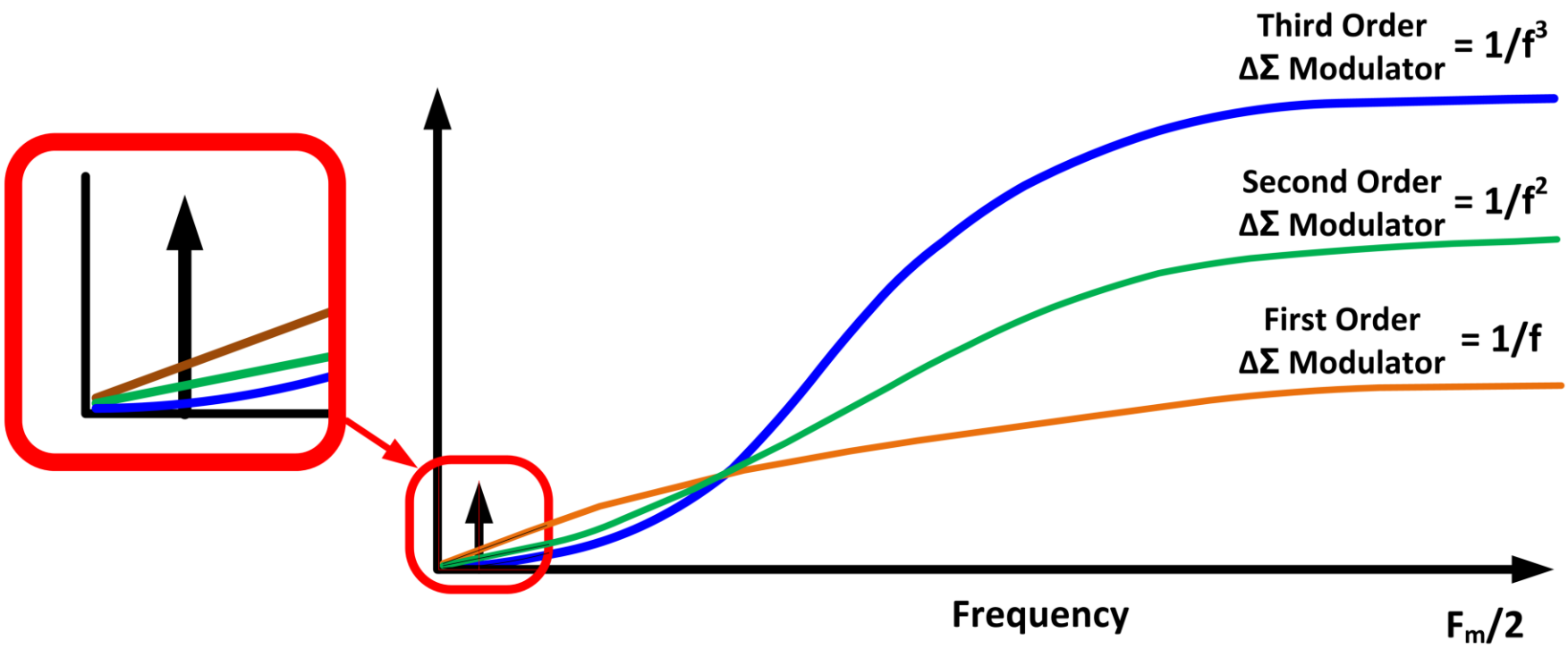
Notice that Dout is on both sides of the equation. Solving for Dout with some algebra, you can get the second equation. Looking closely at the second equation, the noise is multiplied by a high pass filter, and the input voltage is multiplied by a low pass filter. This result has very important implications into understanding how a delta-sigma operates.

First note that applying the input signal to a low pass filter means that the desired signal will pass through the modulator, but higher frequency noise signals will be limited. Next, notice that multiplying the quantization noise by the high pass filter shapes the noise. It effectively minimizes the noise at low frequencies and does not attenuate the noise at high frequencies. Later we will see that a digital filter will be applied to the modulator output to eliminate the high frequency noise.

This example shows a modulator with a first order integration. Some delta sigma converters will use higher order integrations. In the next slide we will look at how higher order modulators impact the noise shaping for a delta sigma converter.

Higher Order Delta-Sigma Modulators

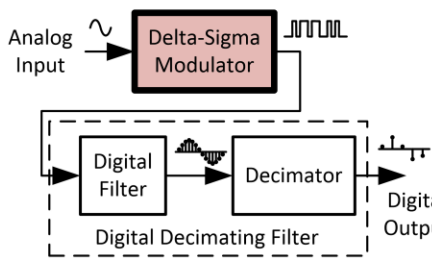




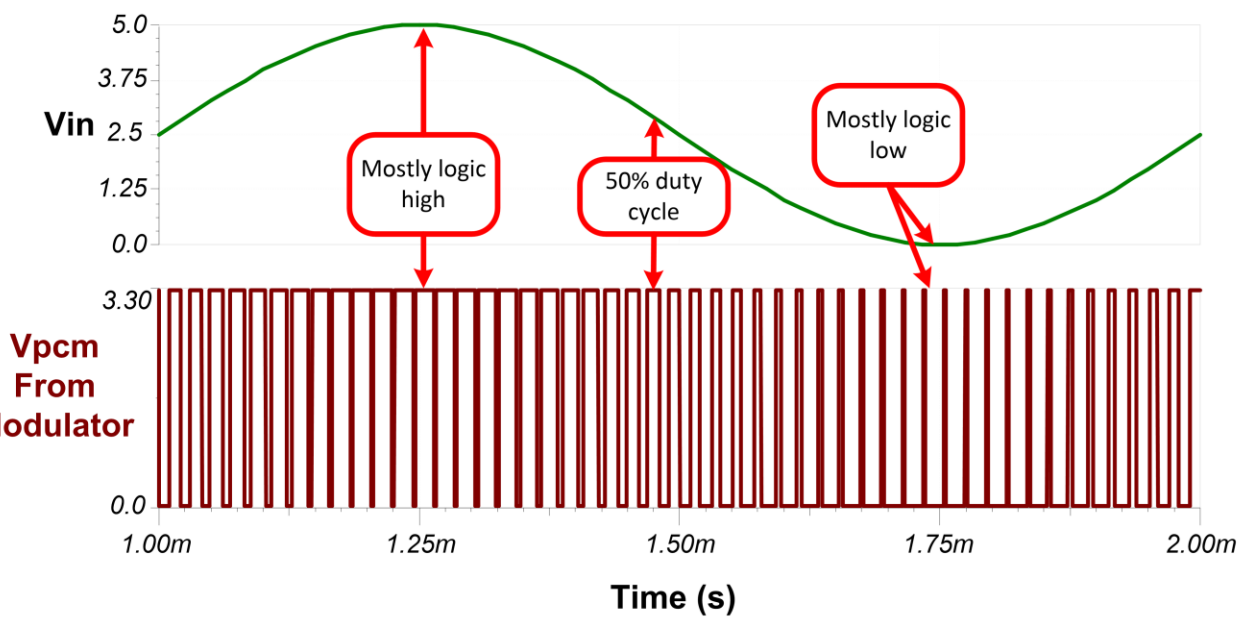
Texas Instruments

This diagram shows the spectral noise densities for 1st, 2nd, and 3rd order modulators with a sampling frequency of F_S. Higher order modulators can be used to get better SNR at lower data rates. This is because the higher order modulator shifts more of the noise to high frequencies and reduces the quantization noise near the signal of interest. If you look at this example, you can see that the third order modulator, shown in blue, is the lowest noise near the signal of interest, because that noise was shifted to high frequencies. Later we will see that the noise at high frequencies is not important as it will be filtered out by a low pass digital filter in the next stage. Before we look at the digital filter, let's review what the input and output of the modulator look like in both the time and frequency domain.

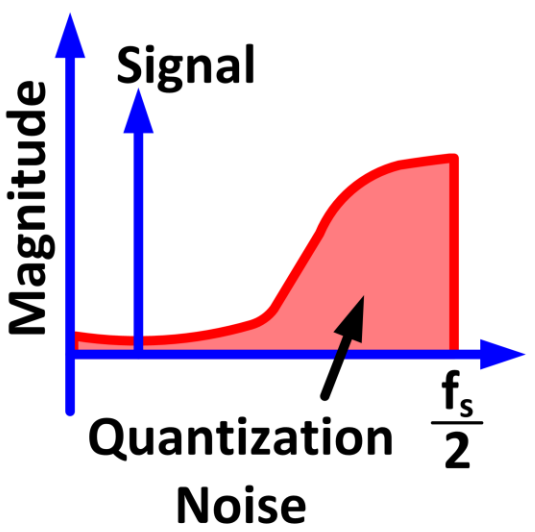
Modulator Output Signal



Modulator Output:
TIME DOMAIN

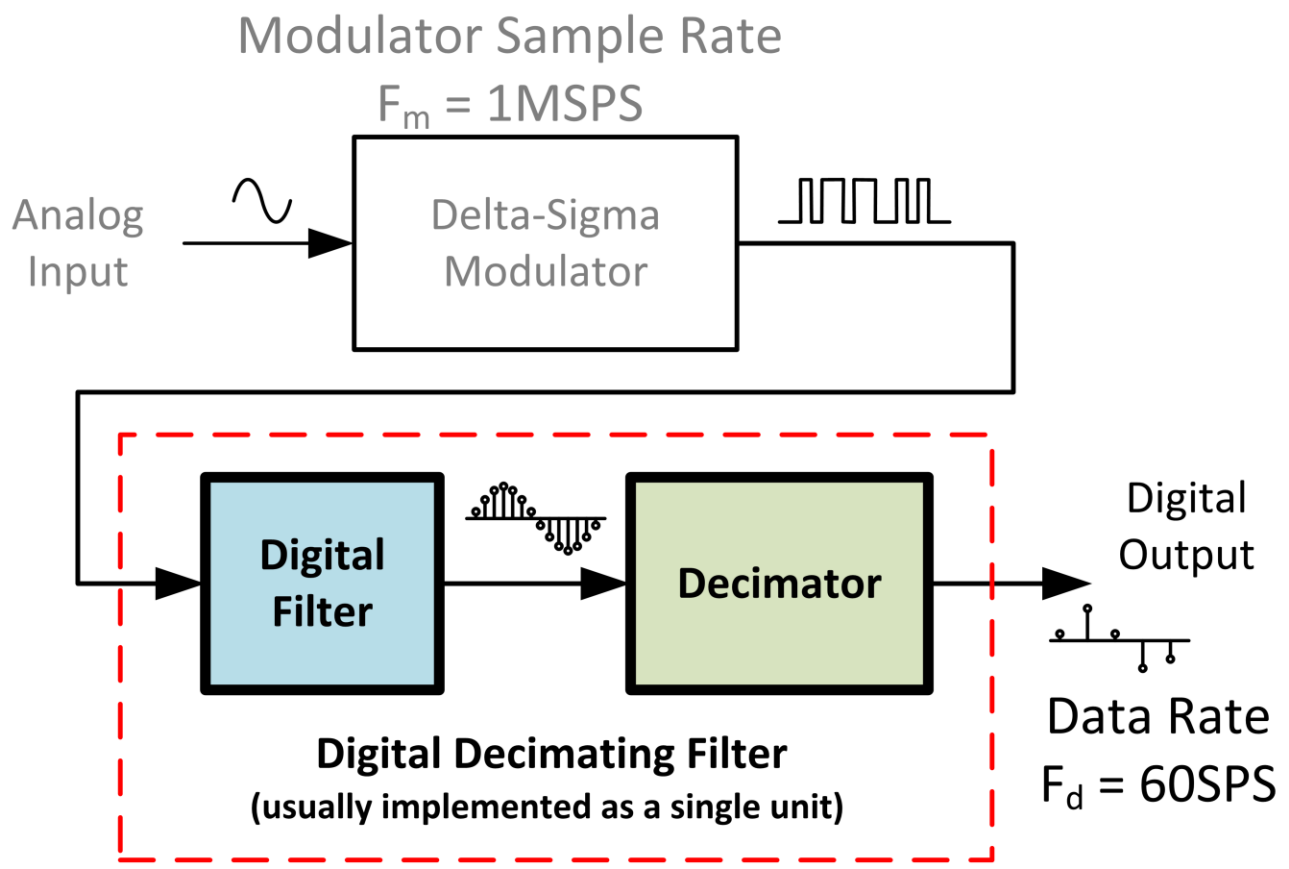


Modulator Output:
FREQUENCY DOMAIN



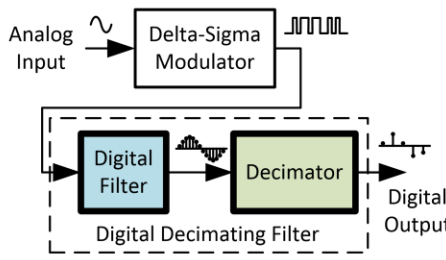
Here is what the signal looks like at the output of the modulator in the time and frequency domain. The time domain signal is a pulse code modulation bit-stream. If this signal is averaged it would equal to value of the input signal. The PCM signal is applied to a digital filter which will perform the averaging function and will also impact the frequency domain response. The frequency domain plot shows the effect of noise shaping. Notice that the noise near the signal is low where the noise is higher at high frequencies. Let's review the block diagram.

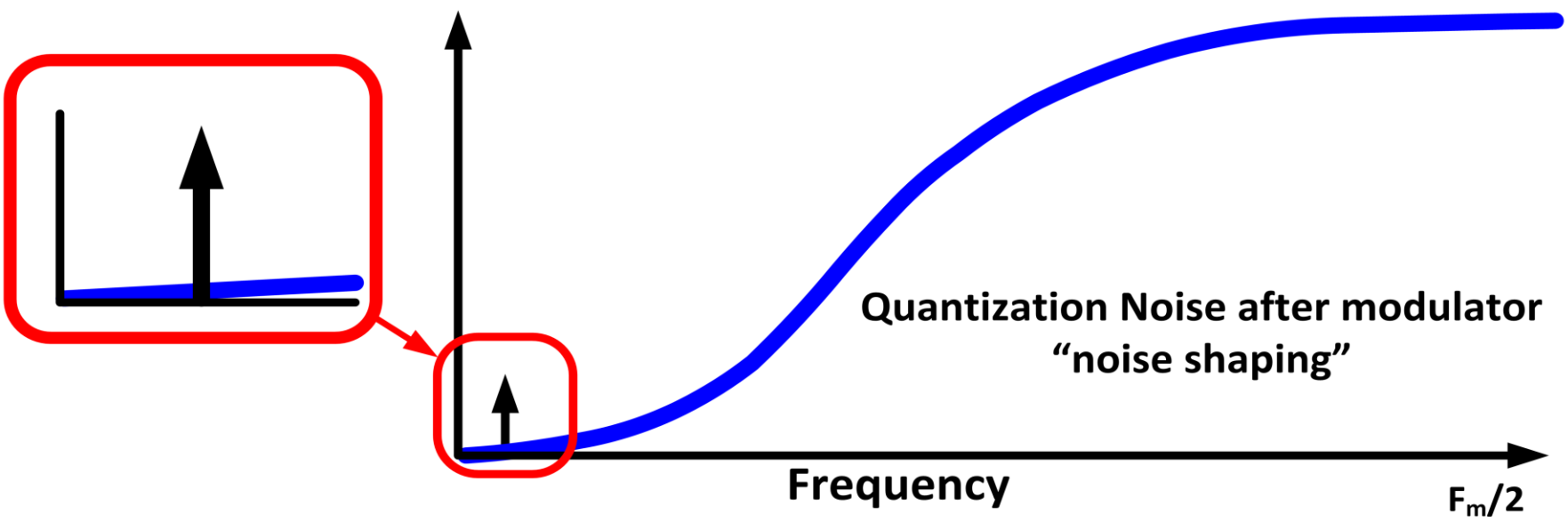
Delta-Sigma ADC Signal Path: Digital Filter



In this diagram you can see that the PCM bit stream from the modulator is applied to the digital filter and decimator. The digital filter will average the bit stream to effectively re-create the analog signal as a high resolution result. Remember that the process of oversampling averages many modulator samples to produce one high resolution output sample. The digital filter is also used to filter the high frequency noise from the modulator output. The filter is followed by the decimator block which limits the number of samples at the output according to the oversampling ratio. Let's look more closely at how the digital filter minimizes the modulator noise.

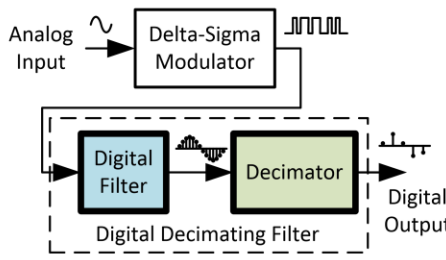
ΔΣ Principal – Digital Filter

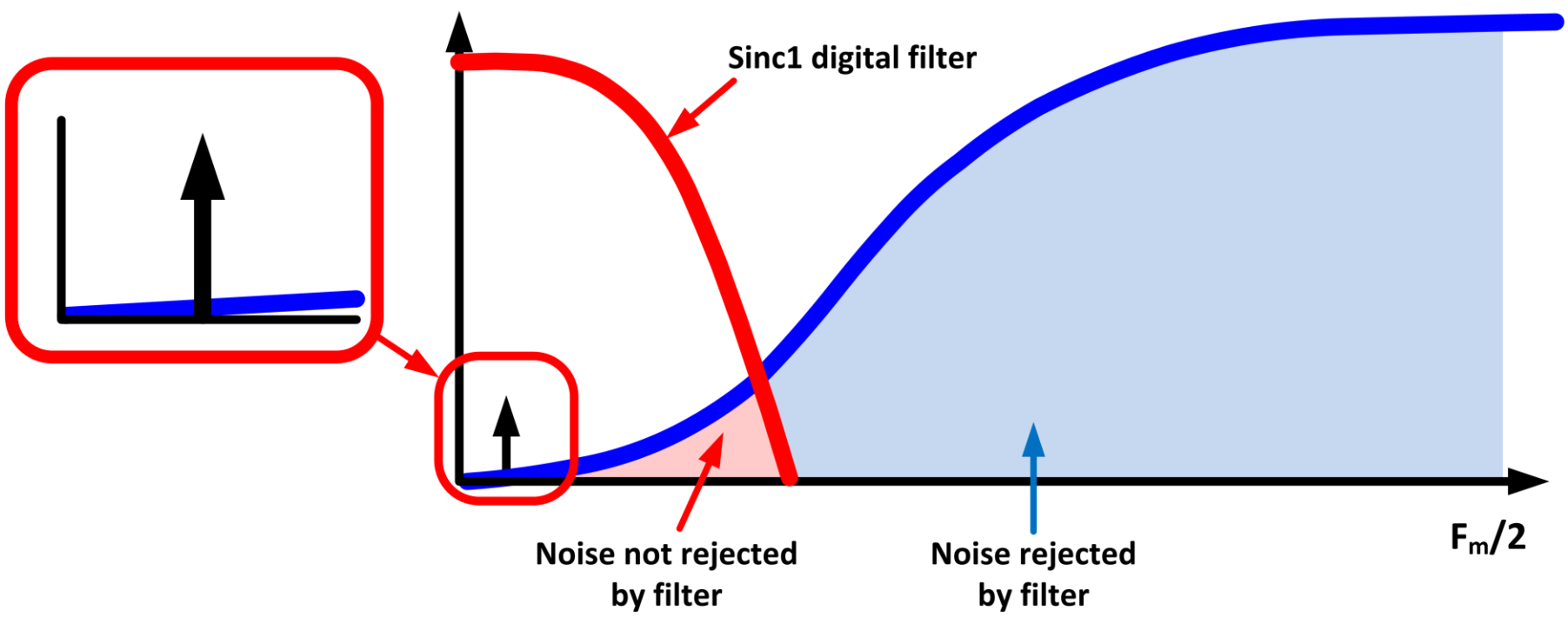




This slide shows the quantization noise at the output of the modulator. Notice that the noise is minimal near the signal of interest.

ΔΣ Principal – Digital Filter

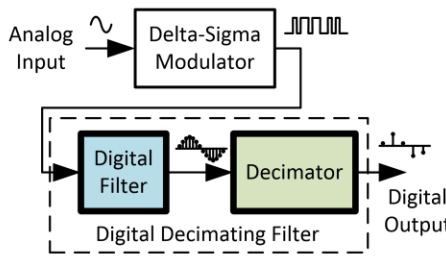


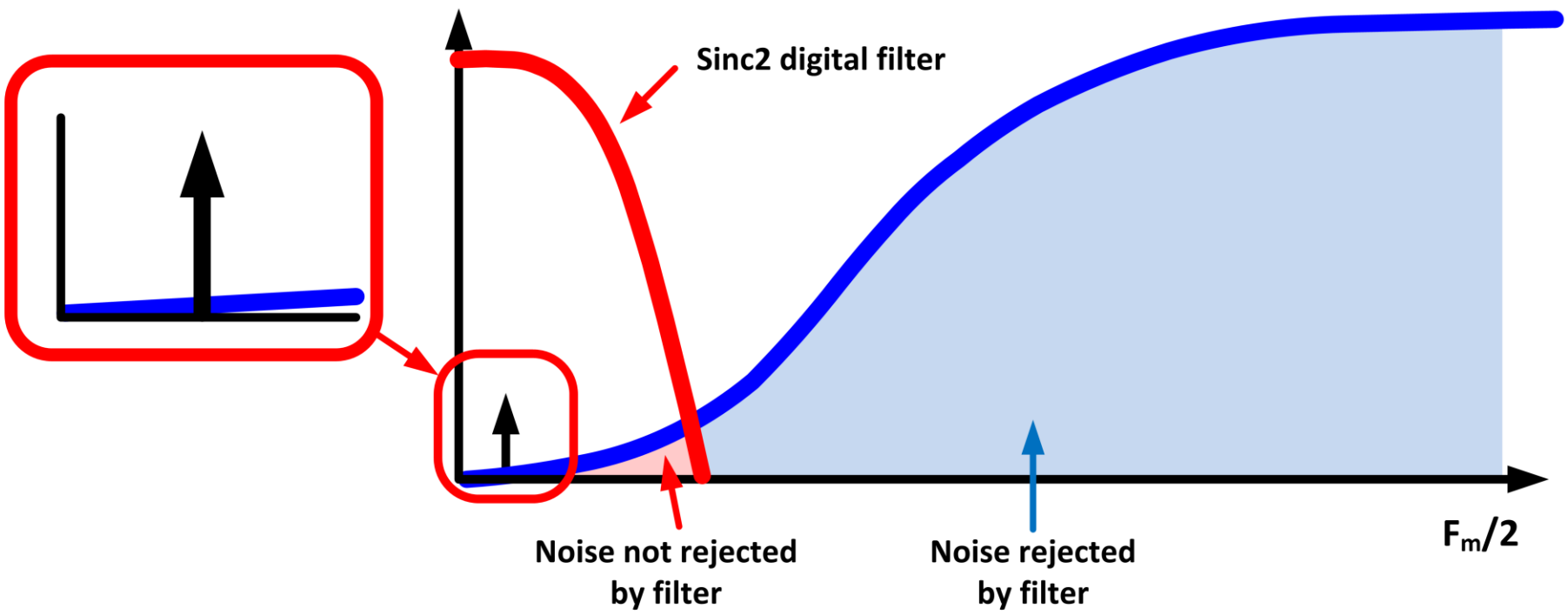


Texas Instruments

Adding a digital filter will eliminate the large noise at higher frequencies. The noise that passes through the digital filter is minimal compared to the overall noise power. This example uses a Sinc1 filter to eliminate the high frequency noise. Using a higher order filter will further reduce the noise.

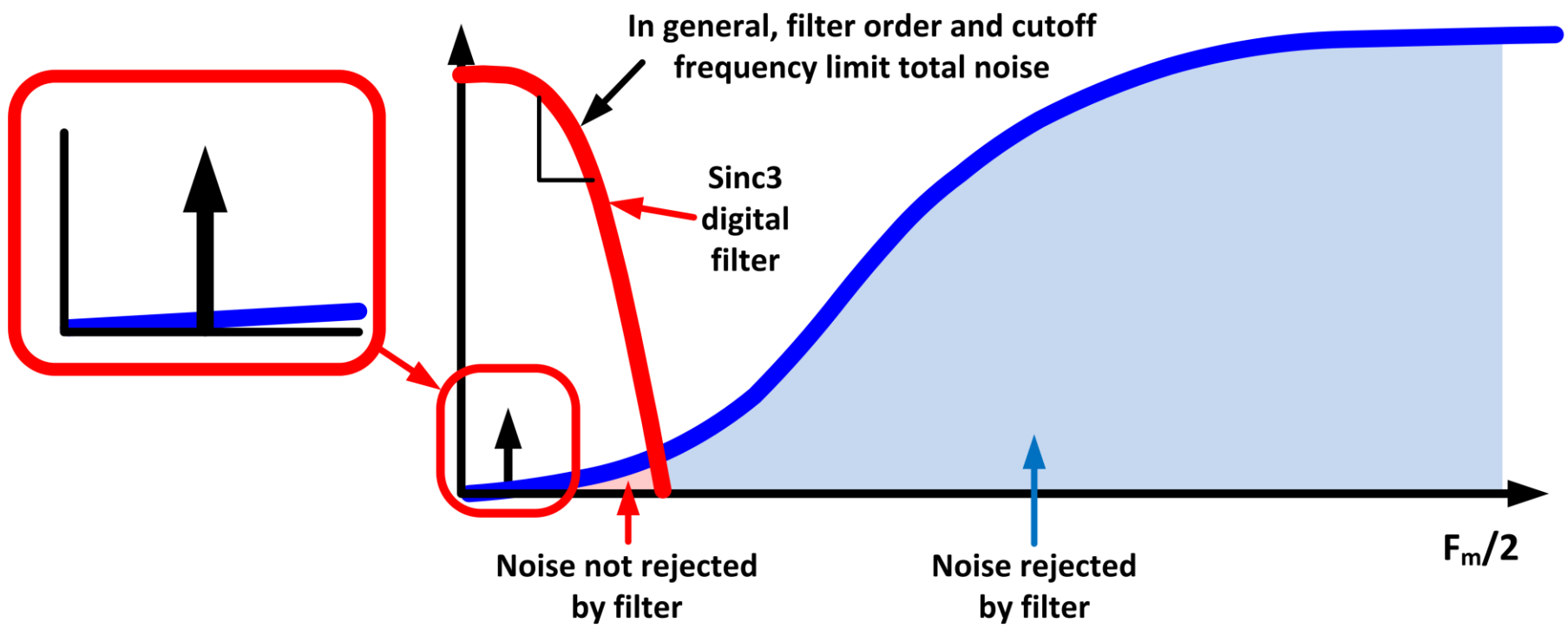
ΔΣ Principal – Digital Filter





Here we see a sinc2 filter. This filter rejects more noise than the sinc1 as it has a sharper passband transition.

ΔΣ Principal – Digital Filter



This last example shows a sinc3 filter. This one reduces the noise even further. In general, choosing a higher order filter, or reducing the cutoff frequency are two approaches to minimizing the quantization noise.

For some practical DC optimized delta-sigma converters, the cutoff frequency of this filter may be as low as a few hertz. For wide band delta sigma converters, the noise may be hundreds of kilohertz. If you compare the noise specifications between low and wide bandwidth delta sigma converter, you will see that the wider bandwidth device generally has more noise.

Thanks for your time!
Please try the quiz.

That concludes the theory part of this video – thank you for your time! Continue watching to try the quiz and check your understanding of this video's content.

Questions: SAR & Delta-Sigma Introduction

1. Which ADC topology has an acquisition cycle and a conversion cycle.
   a. SAR
   b. Wide Bandwidth Delta Sigma
   c. Precision Delta Sigma
   d. Pipeline

2. (T/F) SAR ADCs use noise shaping and oversampling to reduce noise.
   a. True
   b. False

Question 1: Which ADC topology has an acquisition cycle and a conversion cycle?

The answer here, of course, is A.) a SAR ADC.

Question 2: True or False – SAR ADCs use noise-shaping and oversampling to reduce quantization noise?

The answer is False – Delta-Sigma ADCs, not SAR ADCs, feature an integration stage to shape the noise, and a digital filter to average the modulator output by the oversampling ratio.

Questions: SAR & Delta-Sigma Introduction

3. Which ADC topology conversion acts as a snapshot in time?
   a. SAR
   b. Wide Bandwidth Delta Sigma
   c. Precision Delta Sigma
   d. Pipeline

4. The modulator of a delta-sigma converter is sampling at 1MHz. The data rate of the converter is 100SPS. What is the OSR?
   a. 0.0001
   b. 100
   c. 1,000,000
   d. 10,000

Question 3: Which ADC topology conversion acts as a snapshot in time?

The answer is A.) a SAR converter, which takes one sample at a time and converts the result.

Final question: The modulator of a delta-sigma converter is sampling at 1 MHz. The data rate of the converter is 100 SPS. What is the OSR?

The answer is D.) 1 MHz divided by 100 SPS gives us an oversampling ratio of 10,000.

This slide should be leveraged for external recordings. Leave on screen for 5 seconds.

SAR & Delta-Sigma ADCs Understanding Basic Operation

TIPL 4010
TI Precision Labs – ADCs

Created by Many Authors

Presented by Ryan Andrews

ADC Architecture Comparison

SAR

Advantages
- Data “snap-shot”
- Lowest latency
- Low power with power scaling
- High precision - Linearity
- Data rates up to 10MSPS

Limitations
- Limited resolution to 20 bits
- Performance determined by analog front end – application dependent

Typical applications
- Motor control
- Closed loop control systems
- Protection relays
- Medical imaging, T&M, ECG

Wide Bandwidth Delta-Sigma

Advantages
- High speed operation
- Low noise and distortion
- Integrated calibration topologies
- Data rates up to 10MSPS
- High resolution options (up to 32 bits)

Limitations
- Higher power
- Higher latency (e.g. 55 samples)

Typical applications
- Communication systems
- CCD imaging
- Radar applications
- Wide band radio

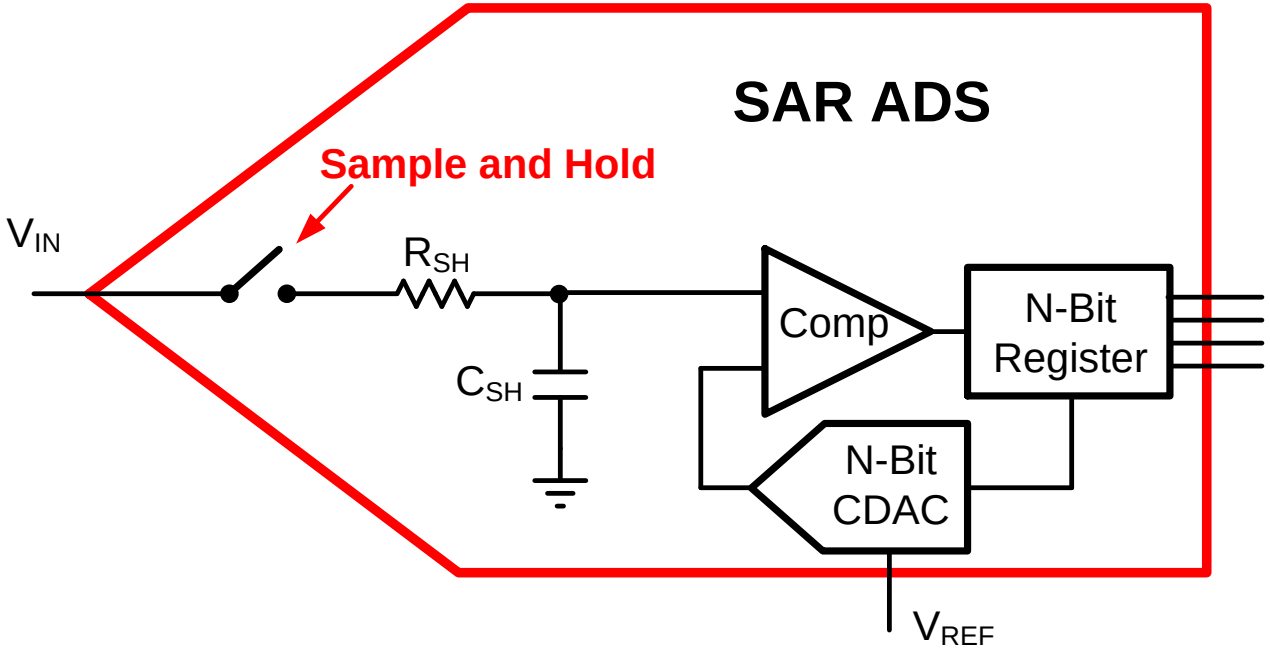
DC Optimized Delta-Sigma

Advantages
- Very high resolution ADCs (up to 32 bits)
- Ultra Low noise by digital filtering
- Application specific integration
- Simpler front-end design

Limitations
- Lower latency (1-3 samples)
- Typically useful for lower bandwidth signals

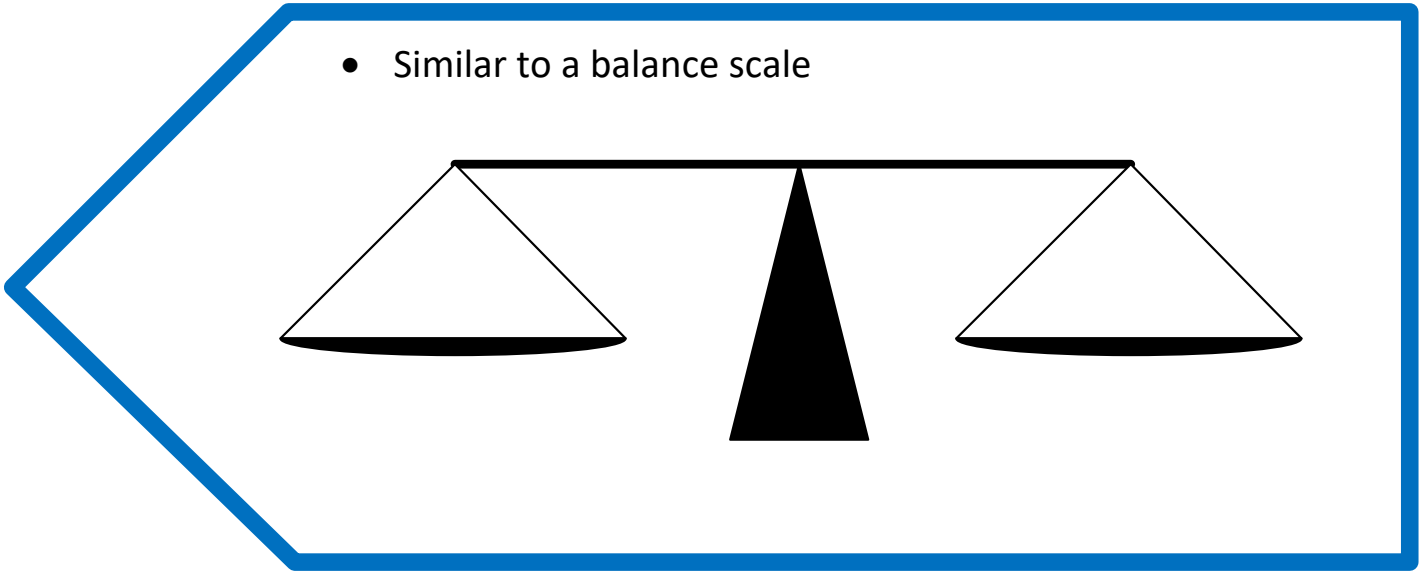
Typical applications
- Industrial sensing – RTD, thermistor, etc.
- Seismic measurements
- Power metering
- Medical ECG, EMG

Basic diagram of SAR ADC
Successive Approximation Register



How Does a SAR ADC Work?

- Similar to a balance scale



How Does a SAR ADC Work?

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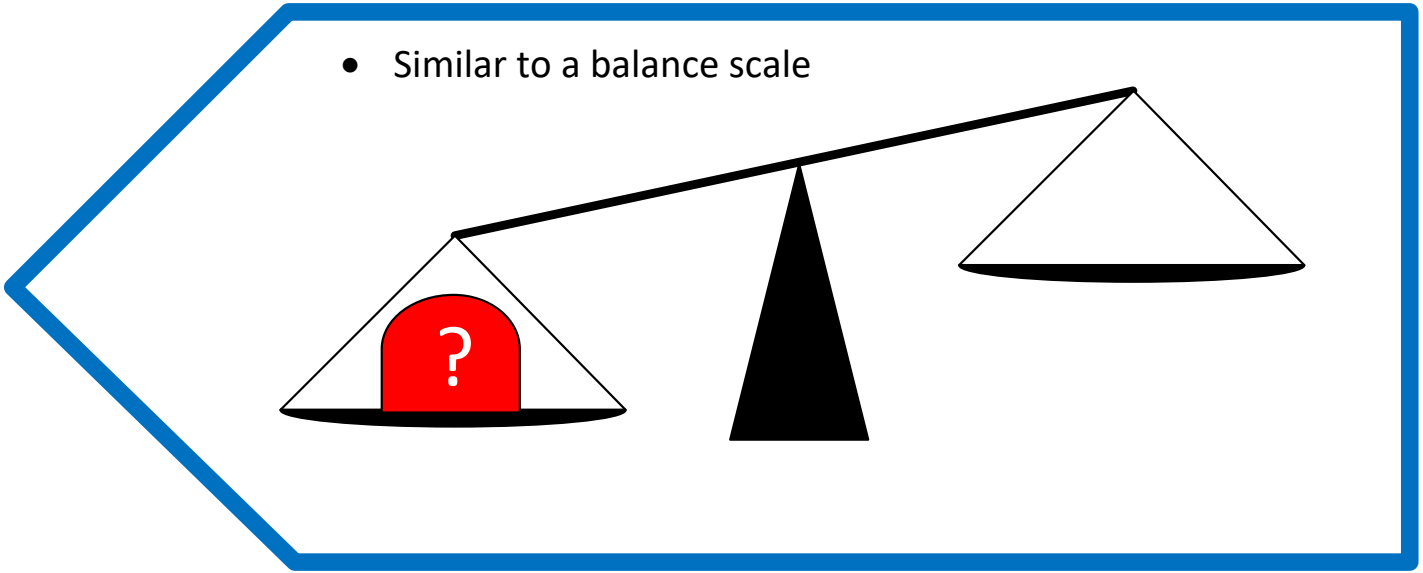
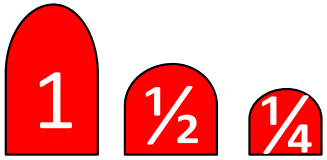
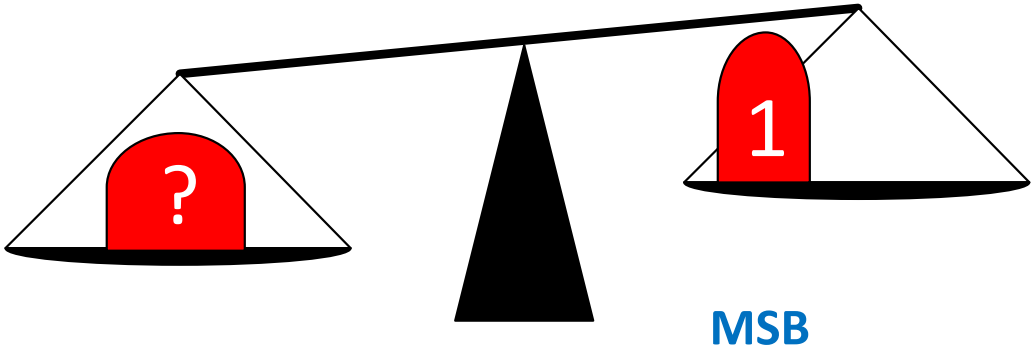
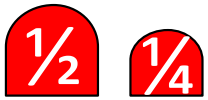




How Does a SAR ADC Work?

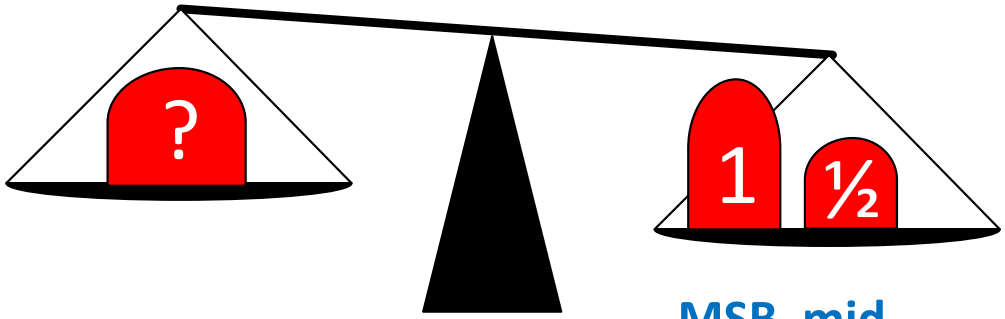
- Similar to a balance scale
- MSB is determined first





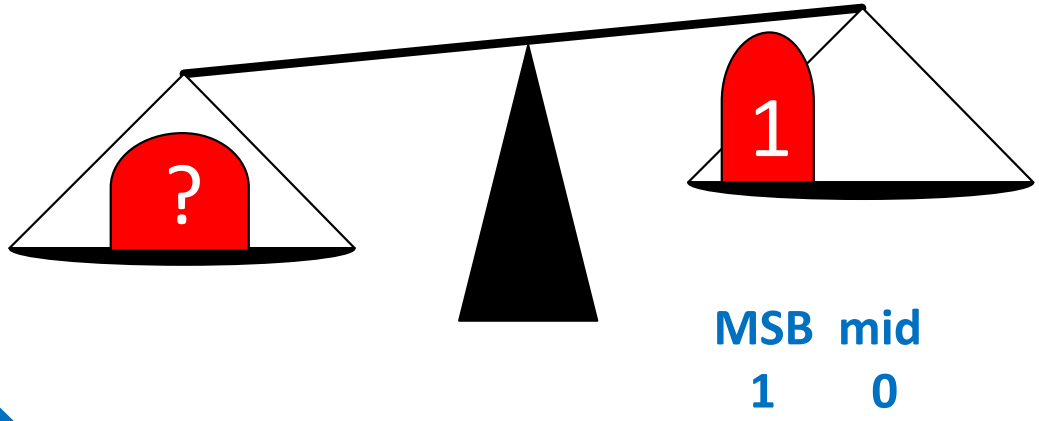
How Does a SAR ADC Work?

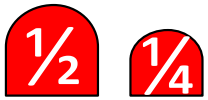
- Similar to a balance scale



How Does a SAR ADC Work?

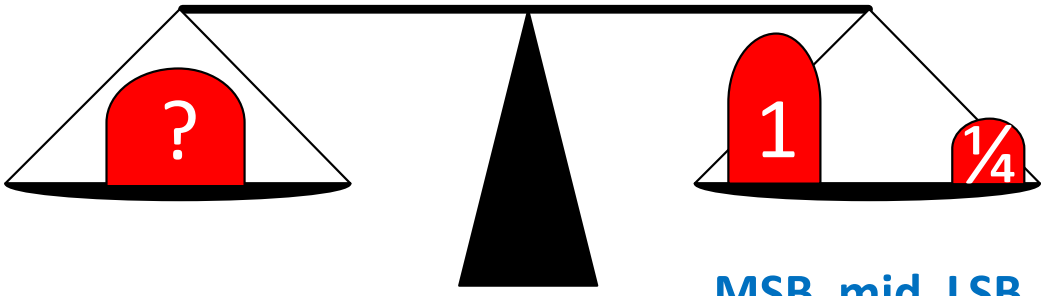
- Similar to a balance scale





How Does a SAR ADC Work?

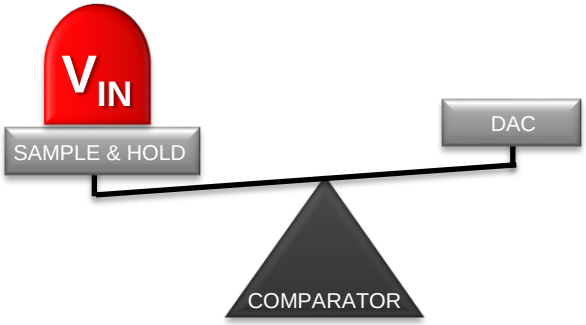
- Similar to a balance scale
- LSB is determined last

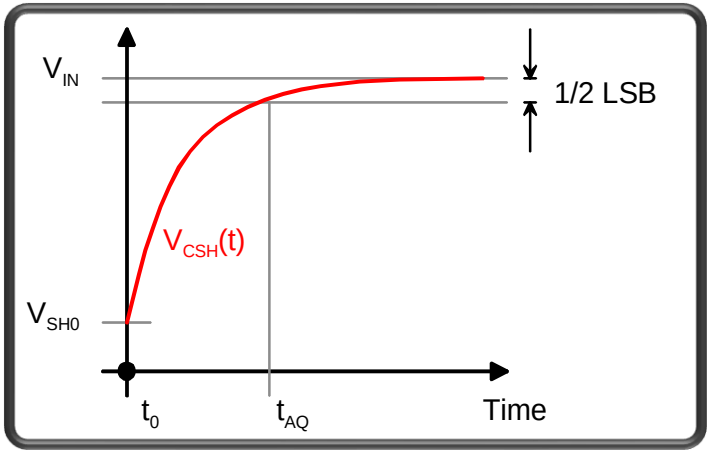


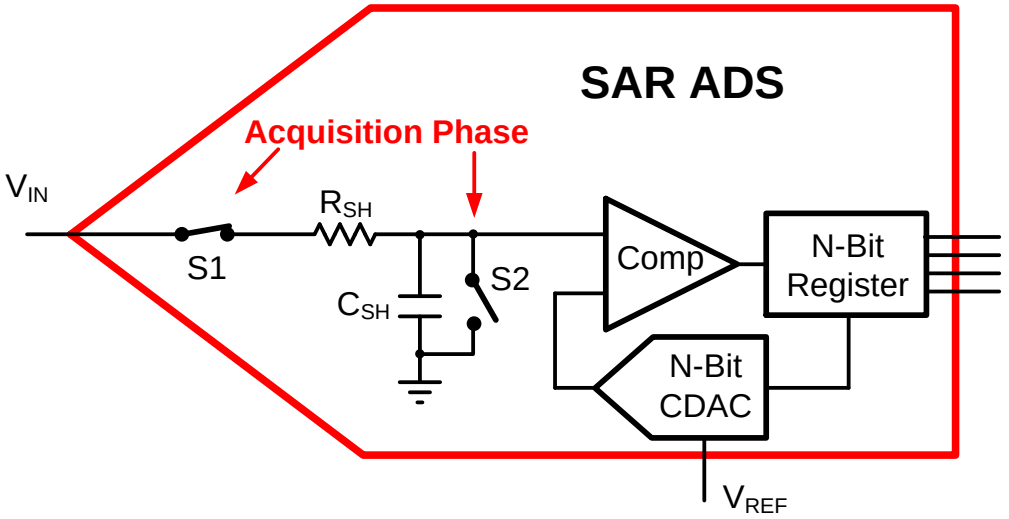
MSB mid LSB
1 0 1

½

SAR ADC Acquisition & Conversion Phase



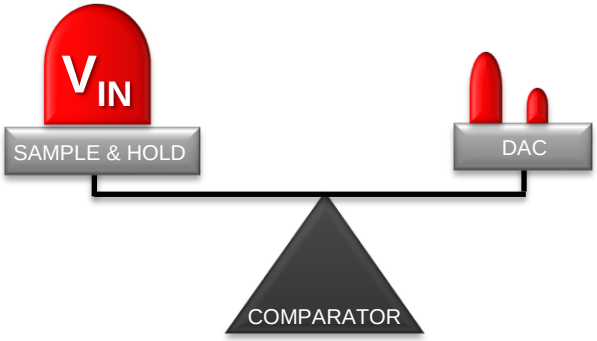


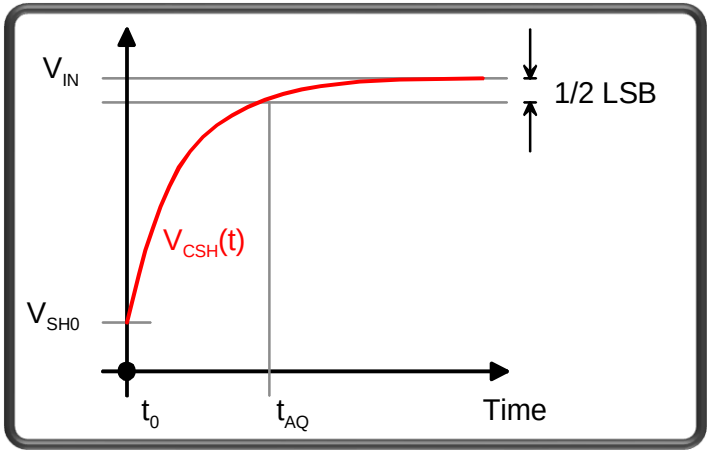


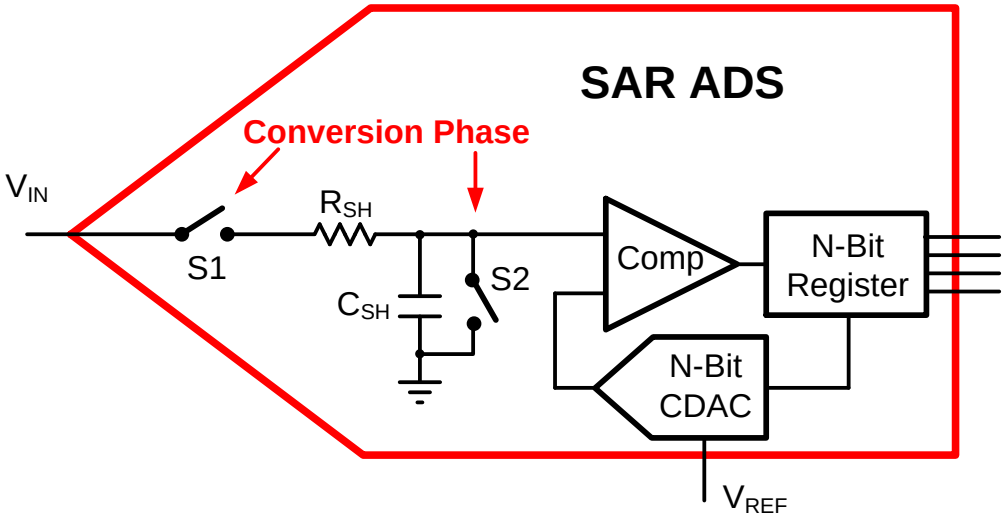
$$V_{CSH}(t) = V_{CSH}(t_0) + [V_{IN} - V_{CSH}(t_0)] \times (1 - e^{-\frac{t}{\tau}})$$

$$\tau = R_{SH} \times C_{SH}$$

SAR ADC Acquisition & Conversion Phase



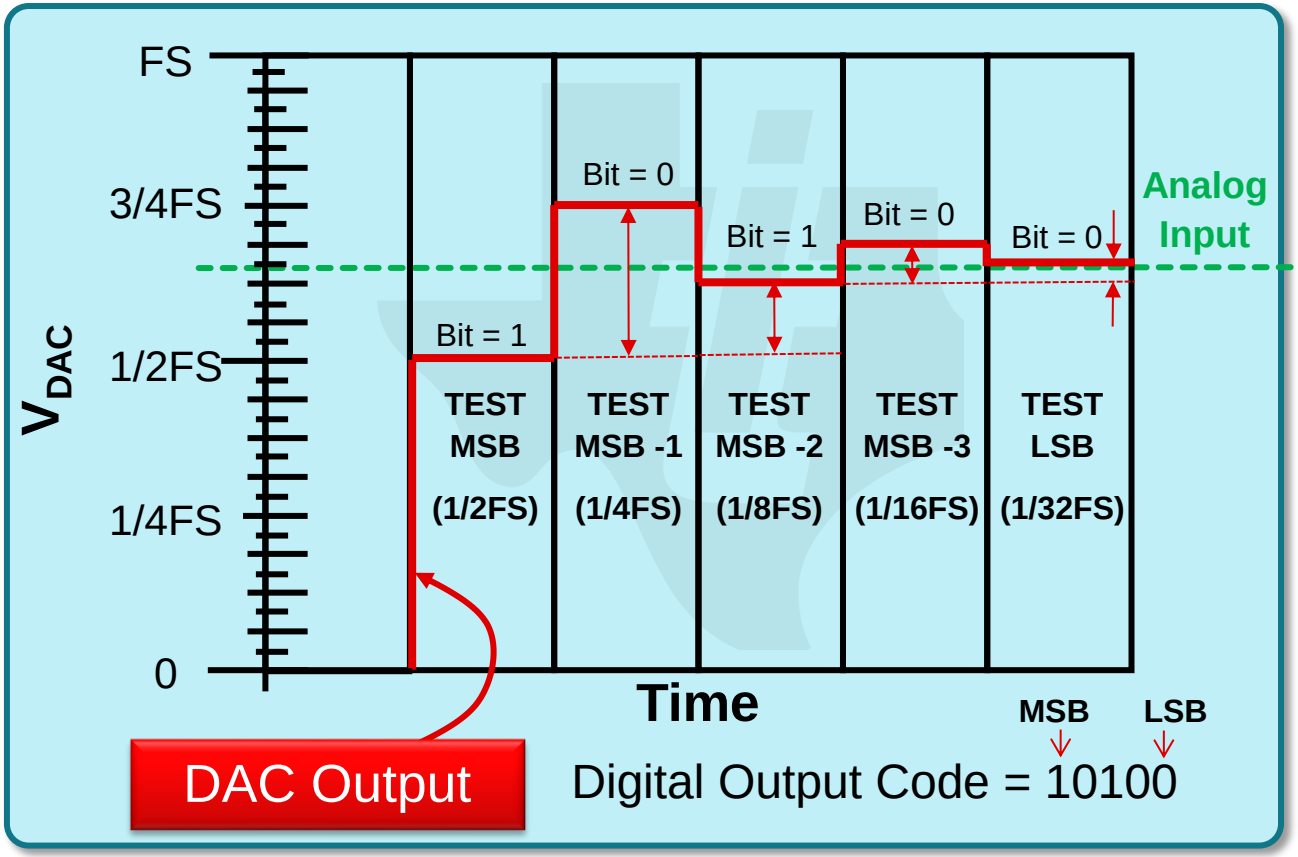


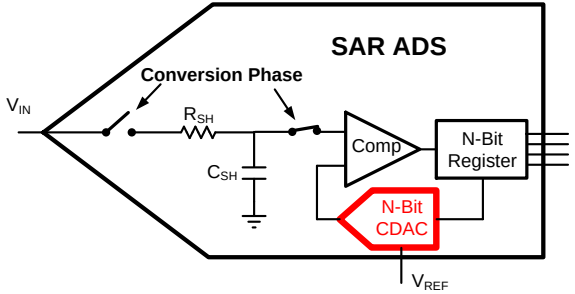


$$V_{CSH}(t) = V_{CSH}(t_0) + [V_{IN} - V_{CSH}(t_0)] \times (1 - e^{-\frac{t}{\tau}})$$

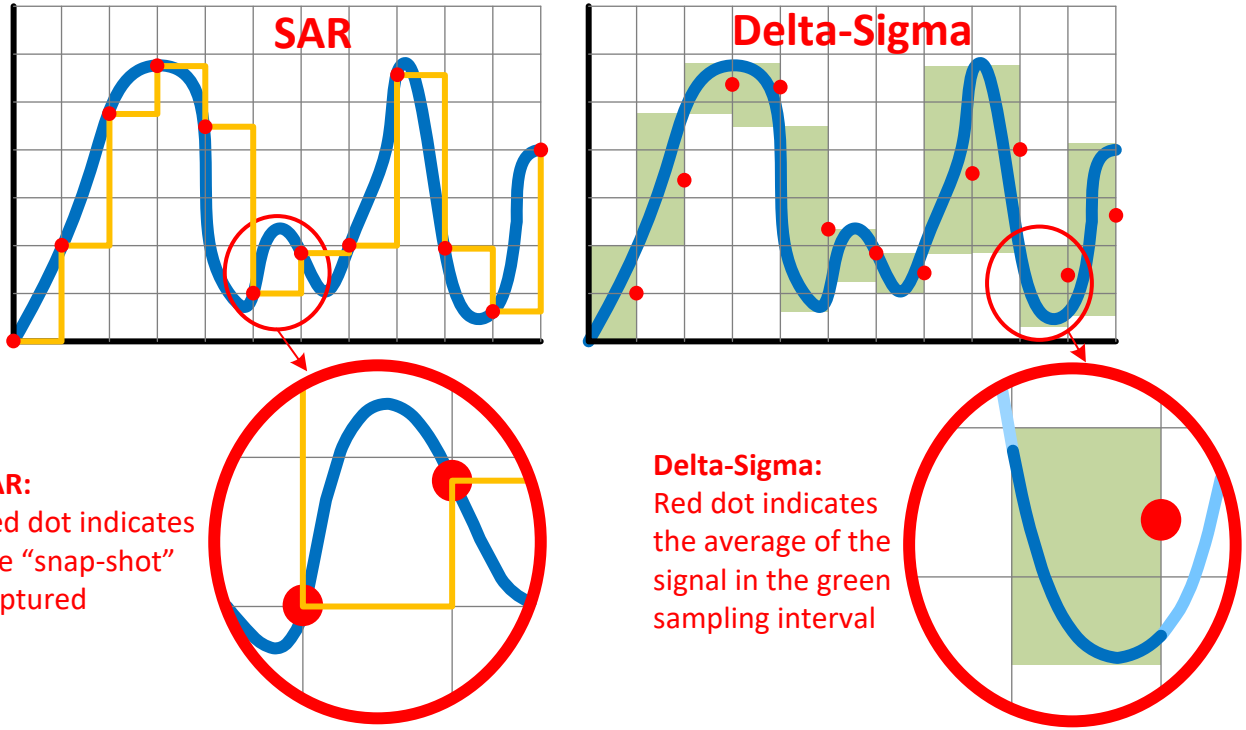
$$\tau = R_{SH} \times C_{SH}$$

SAR ADC Conversion Phase





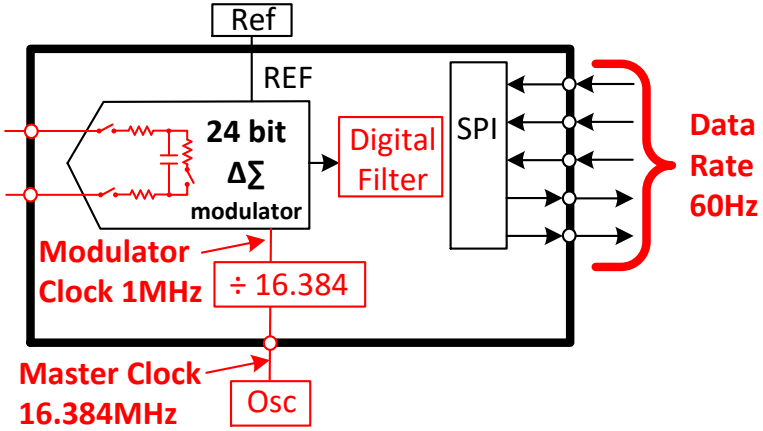
SAR vs Delta-Sigma Sampling



SAR:
Red dot indicates the "snap-shot" captured

Delta-Sigma:
Red dot indicates the average of the signal in the green sampling interval

Simplified model of ΔΣ ADC

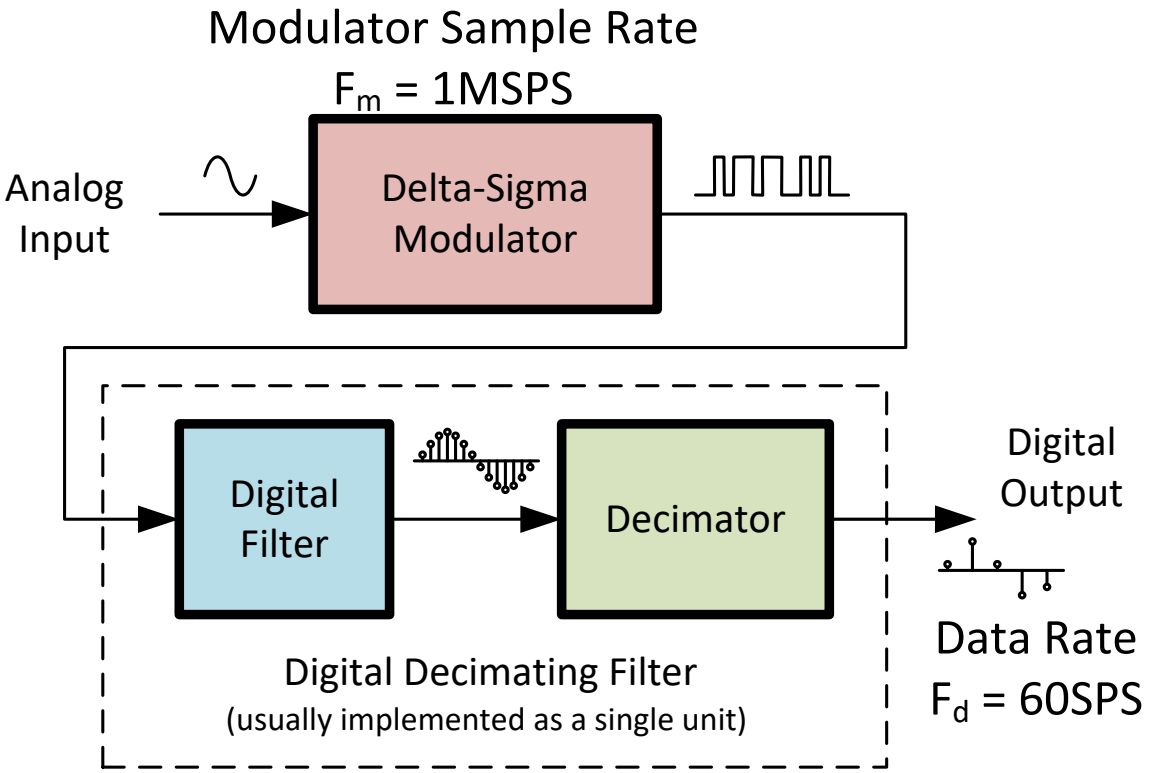


Oversampling Ratio:
OSR = Modulator Clock / Data Rate
OSR = 1MHz/60Hz = 16k

Simplified Model of ΔΣ operation

- The input 1-bit converter is sampling at 1MHz rate (**modulator clock rate**)
- The ***master clock*** is divided by 16.384 to set ***modulator clock*** to 1MHz
- 16,000 samples are "averaged" for each output sample
  - ✓ The ratio of input to output samples is called oversampling ratio (**OSR**)
- The output **data rate** is the frequency that output samples are read at (e.g. 60SPS)
  - ✓ The OSR can be calculated OSR = Modulator Clock / Data Rate
  - ✓ In this example OSR = 1MHz / 60Hz = 16k
- The "Data Rate" is analogous to the "Sampling rate" of a SAR ADC

Understanding the Delta-Sigma ADC



Input and Output Sampling Rate

Modulator Data Rate = F_m = 1MSPS

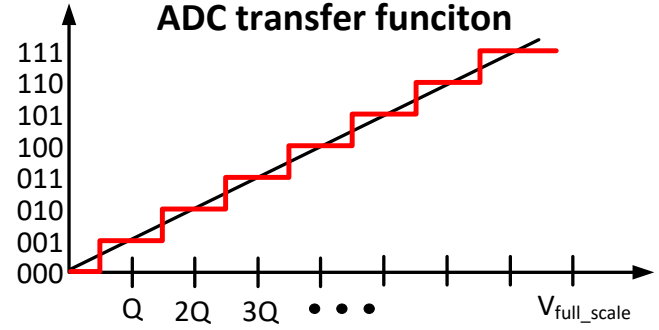
Output Data Rate = F_d = 60SPS

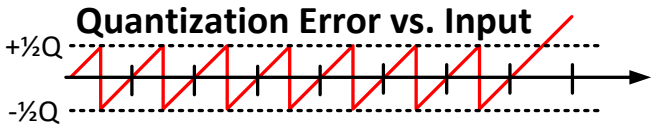
OSR = F_m/F_d = 16,000

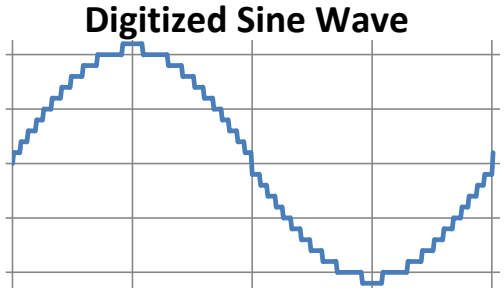
OSR = 1MSPS/60SPS = 16,000

OSR = Oversampling Ratio

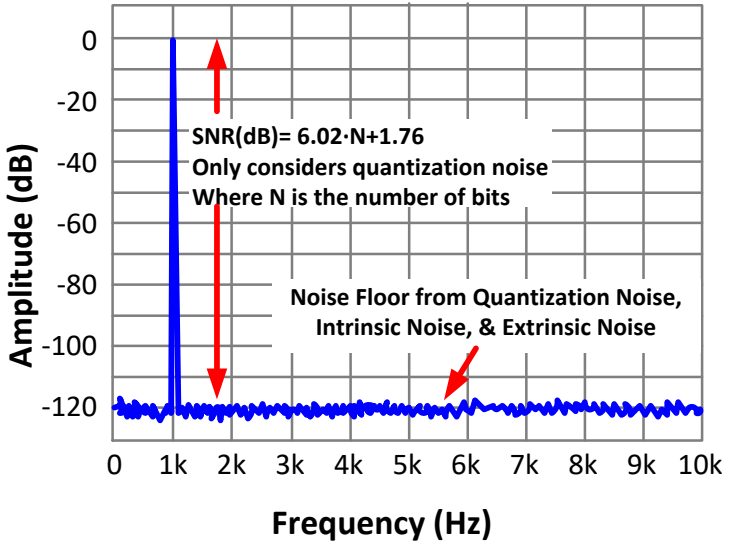
Quick Introduction to Quantization Noise



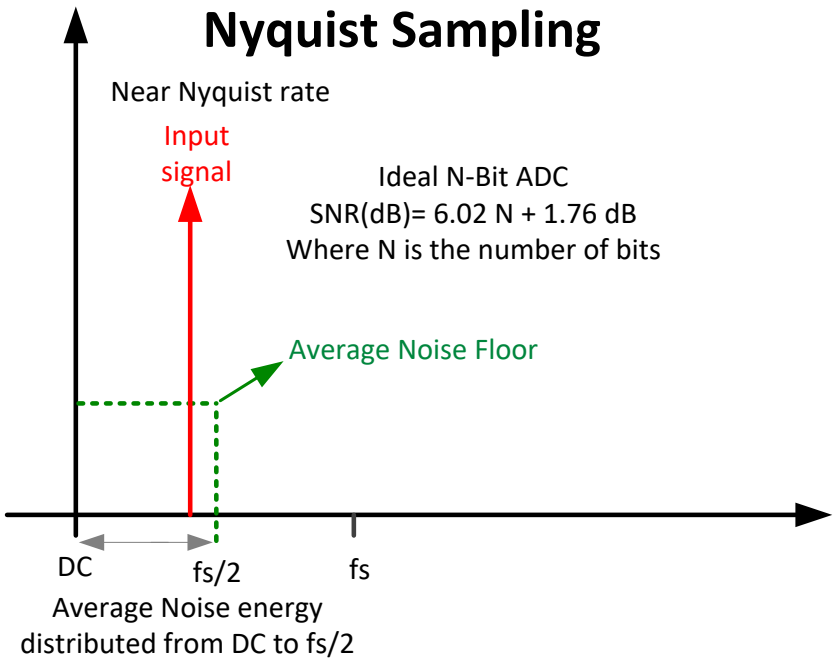




- Quantization noise is a “rounding” error
- The error looks triangular in time domain
- In frequency domain, harmonics fold back to create “white noise” floor



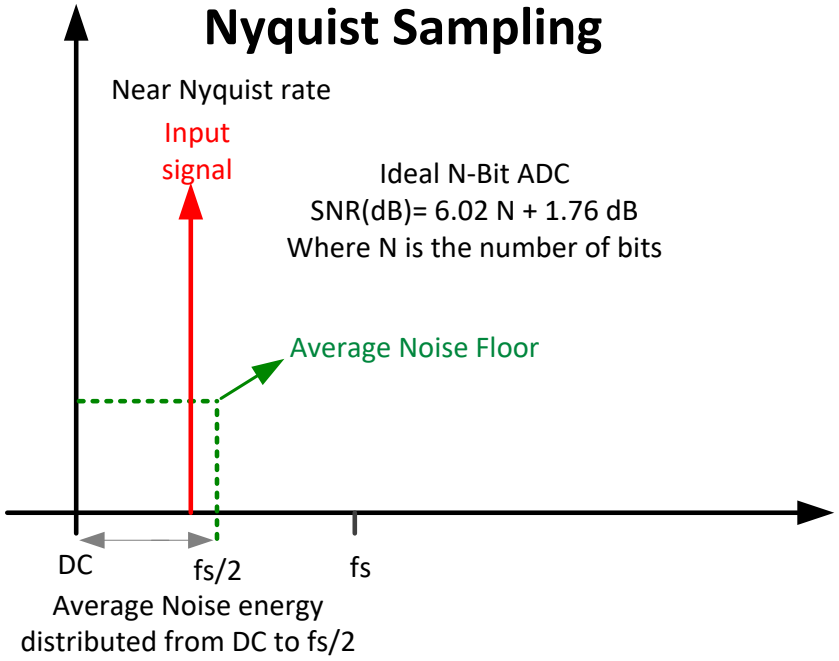
Nyquist Sampling Rate

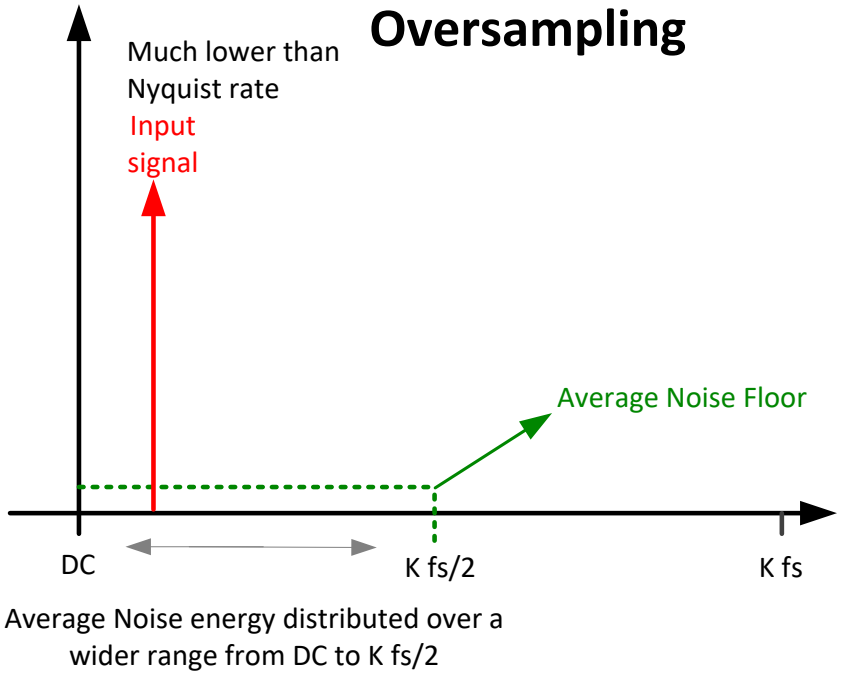


Definition of Terms:

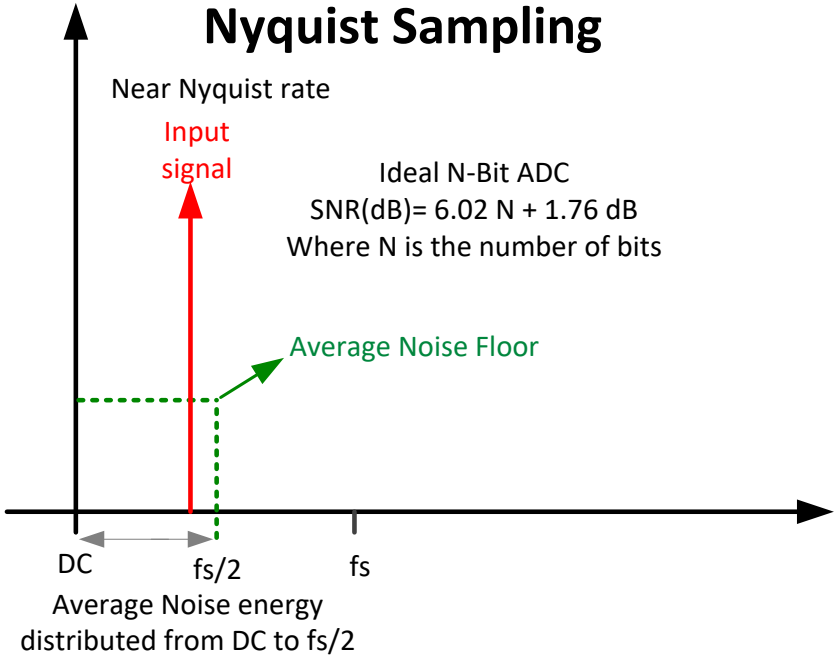
Nyquist Sampling	The input signal may be at or near the Nyquist rate
$f_s/2$	Nyquist frequency. The maximum applied frequency with out aliasing
f_s	Sampling frequency
Noise Floor	The noise floor is set by quantization noise. SNR(dB) = 6.02N + 1.76
N	Number of bits

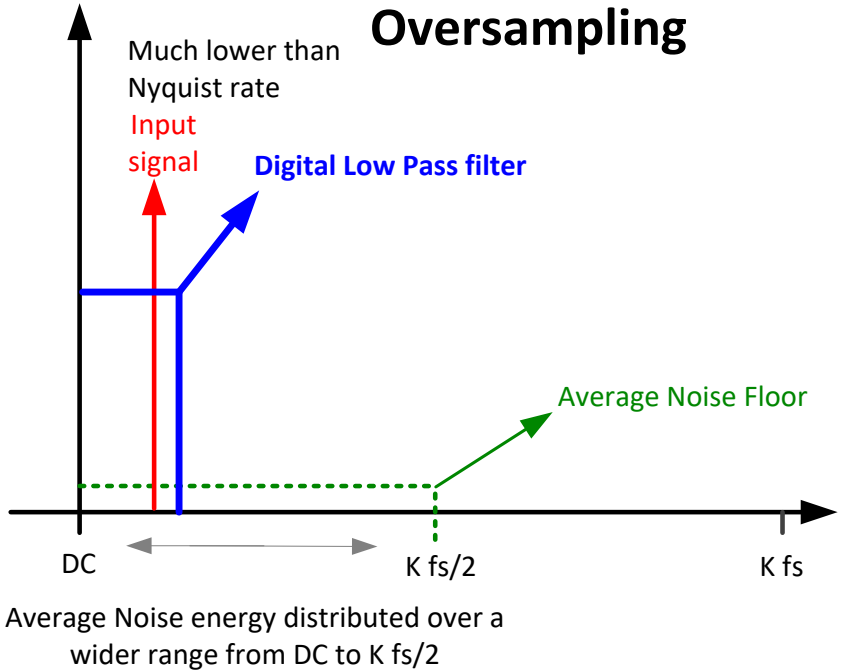
Oversampling vs. Nyquist Sampling



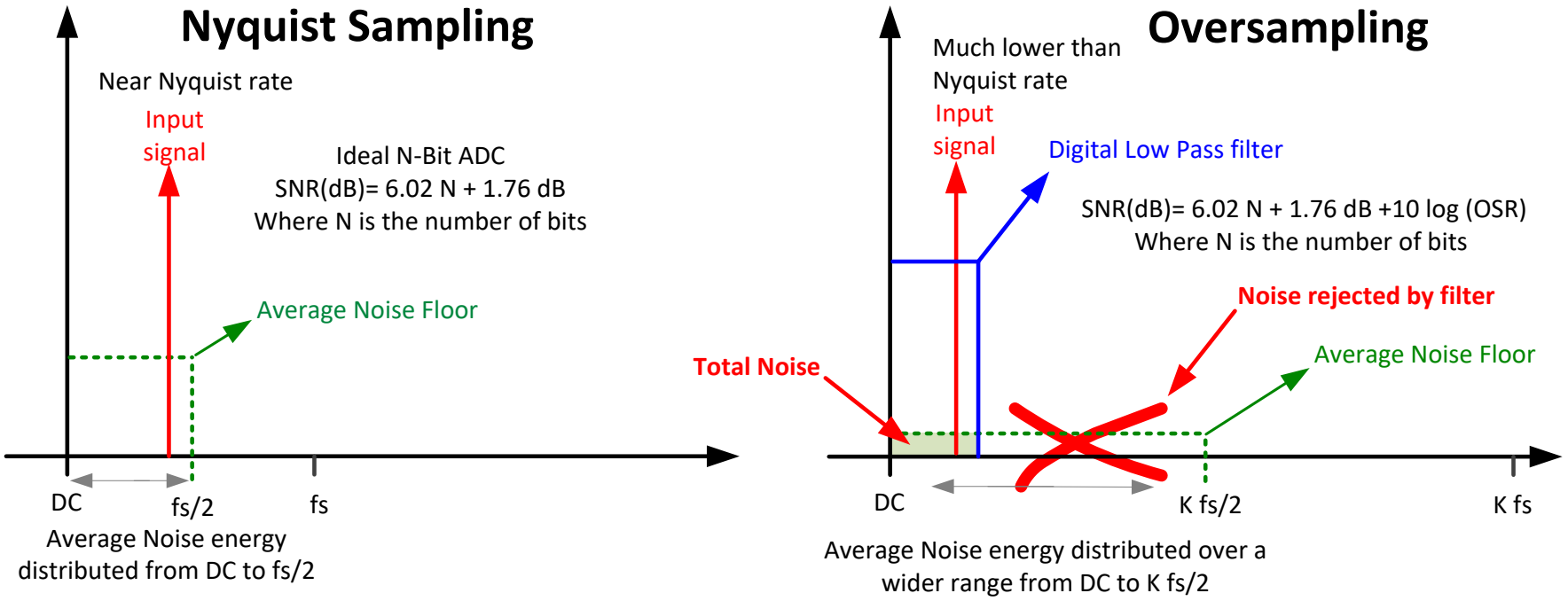


Oversampling vs. Nyquist Sampling

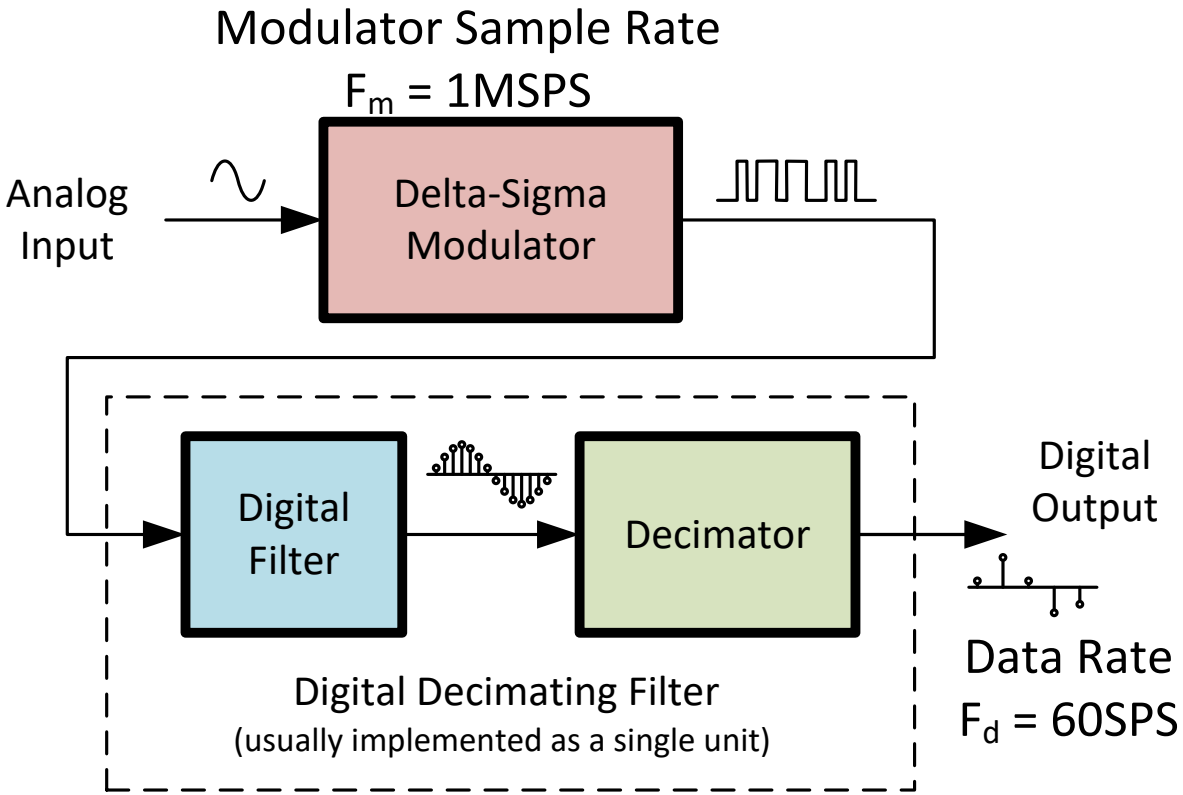




Oversampling vs. Nyquist Sampling



Delta-Sigma ADC Topology



Input and Output Sampling Rate

Modulator Data Rate = F_m = 1MSPS

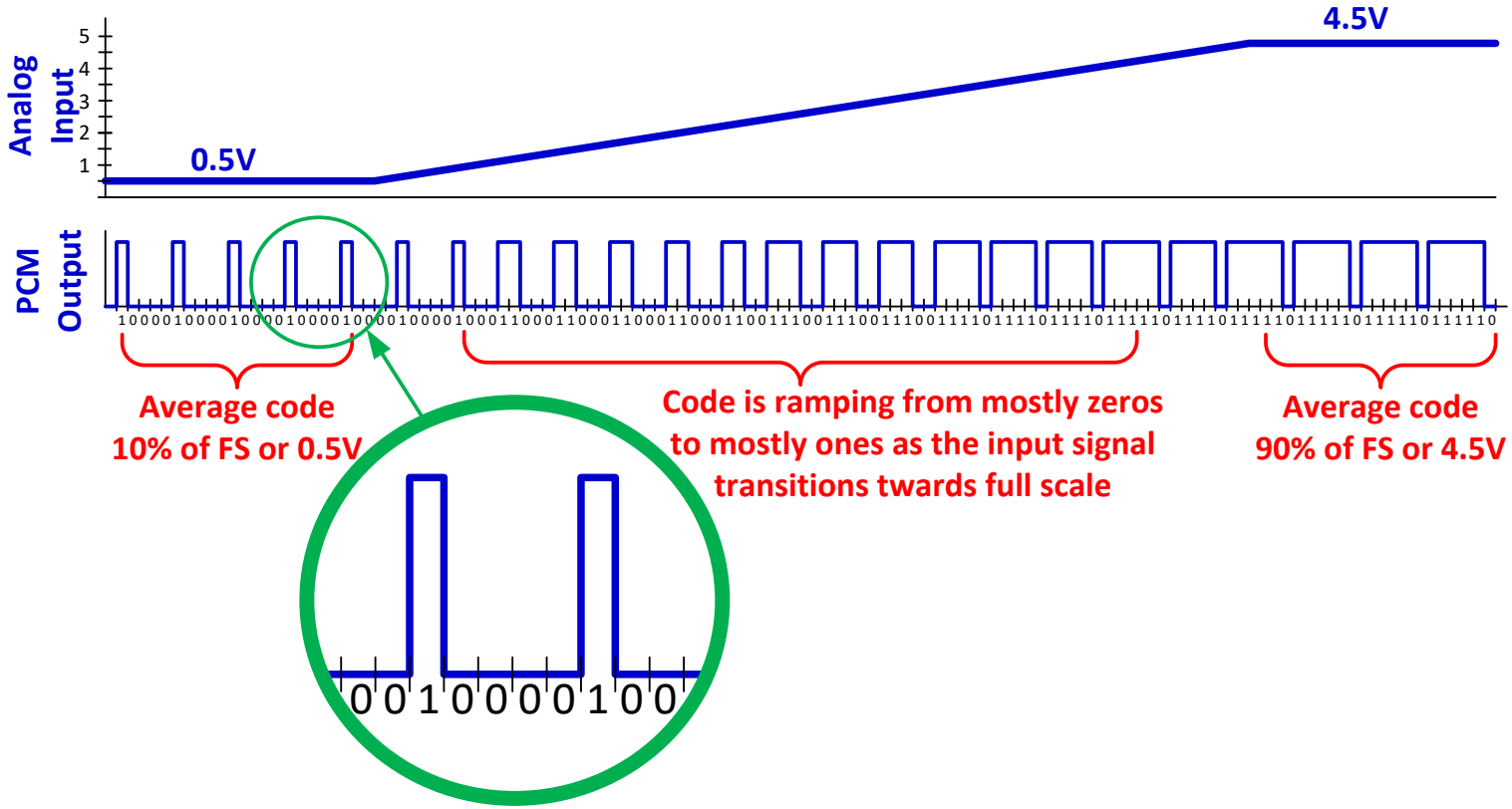
Output Data Rate = F_d = 60SPS

OSR = F_m/F_d = 16,000

OSR = 1MSPS/60SPS = 16,000

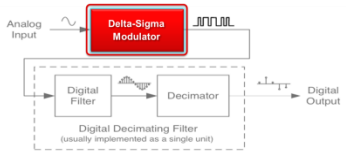
OSR = Oversampling Ratio

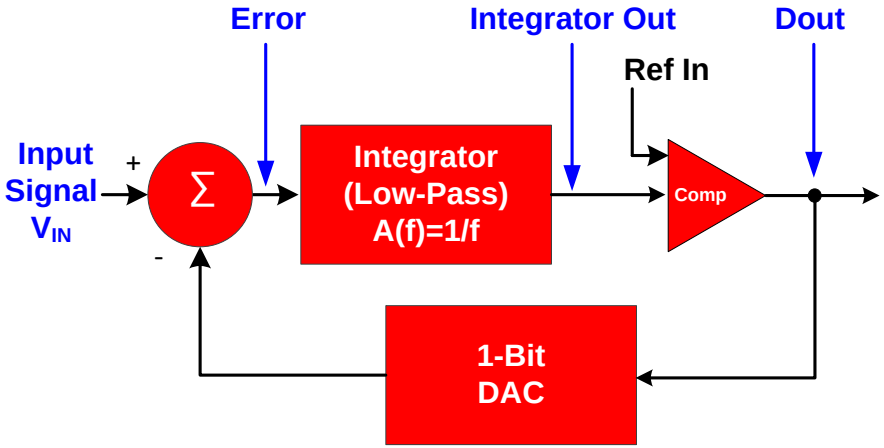
What is pulse code modulation (PCM)

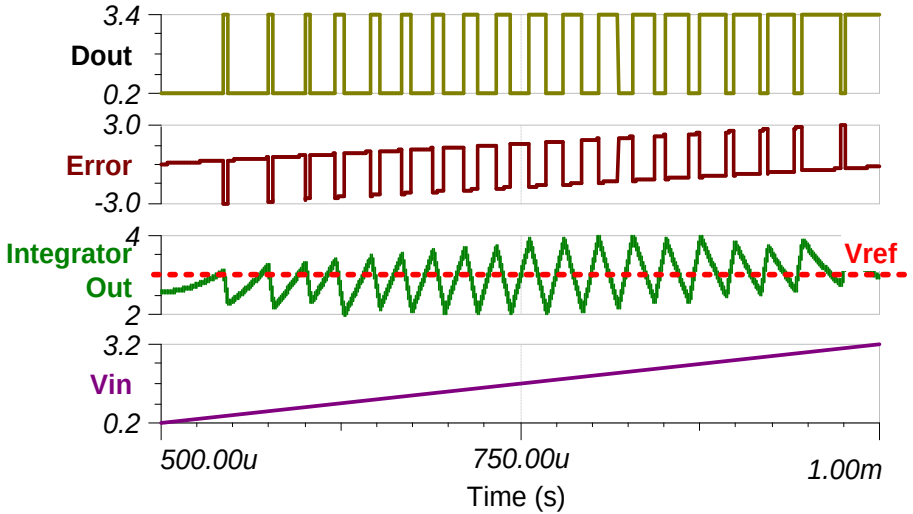


1st Order Delta-Sigma Modulator

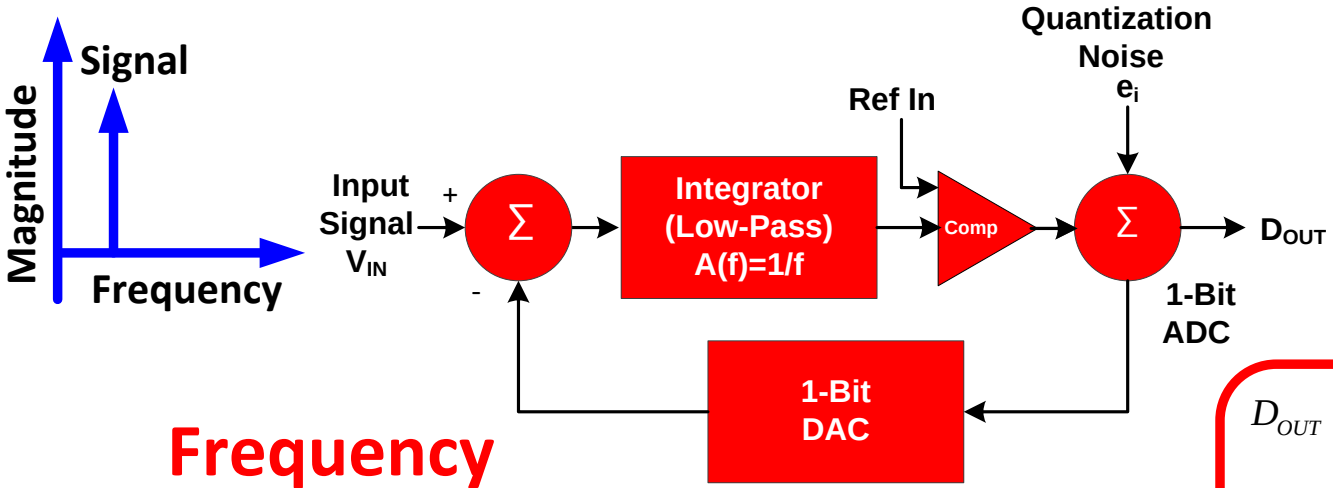
Time Domain

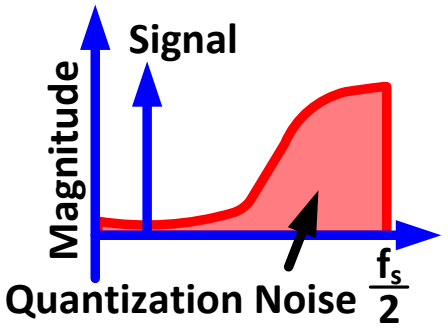






1st Order Delta-Sigma Modulator





Frequency Domain Analysis

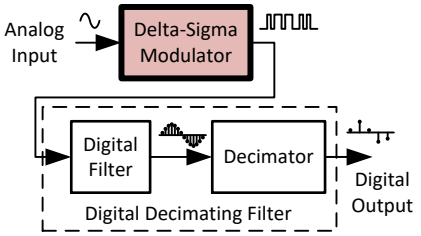
$$D_{OUT} = (V_{IN} - D_{OUT})\frac{1}{f} + e_n$$

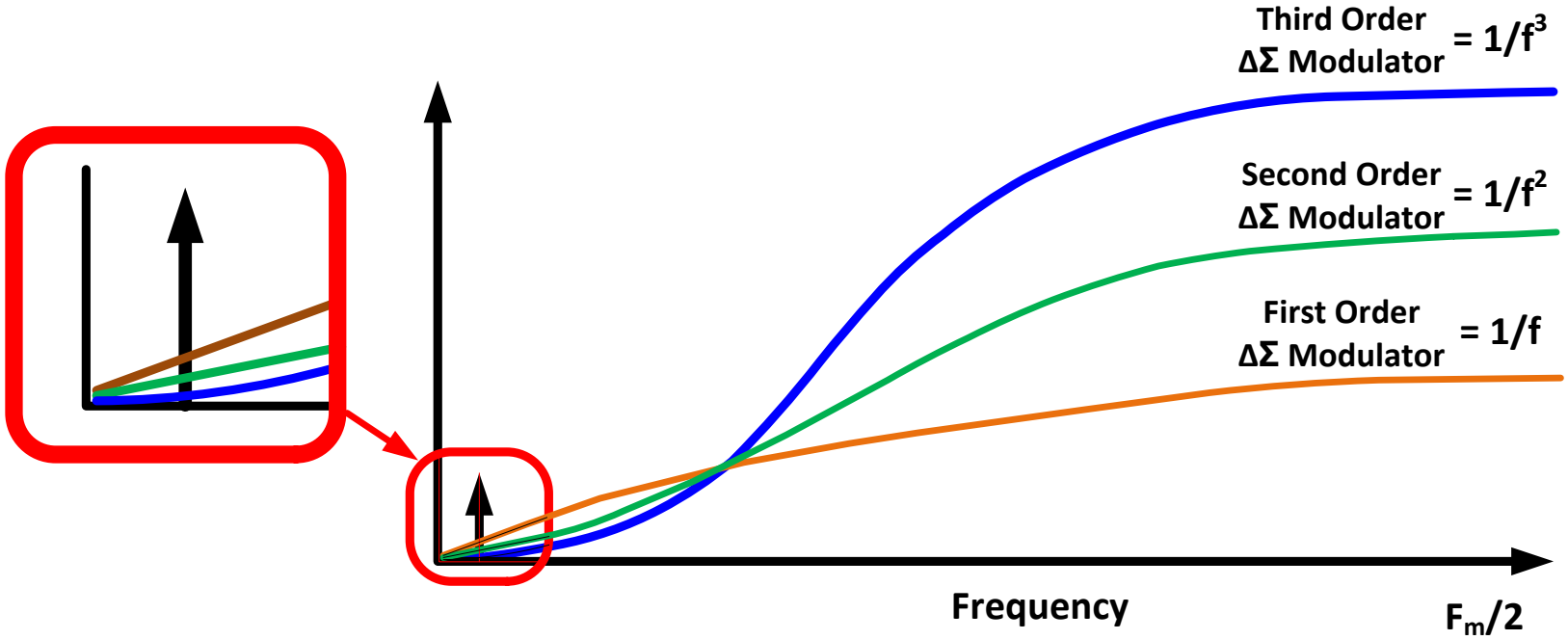
$$D_{OUT} = e_n\left(\frac{f}{1+f}\right) + V_{IN}\left(\frac{1}{1+f}\right)$$

HPF Noise Transfer Function

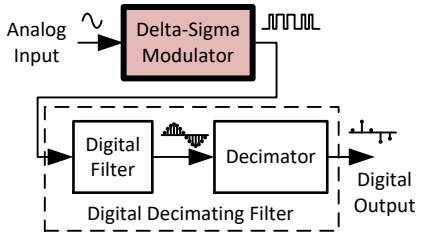
LPF Signal Transfer Function

Higher Order Delta-Sigma Modulators

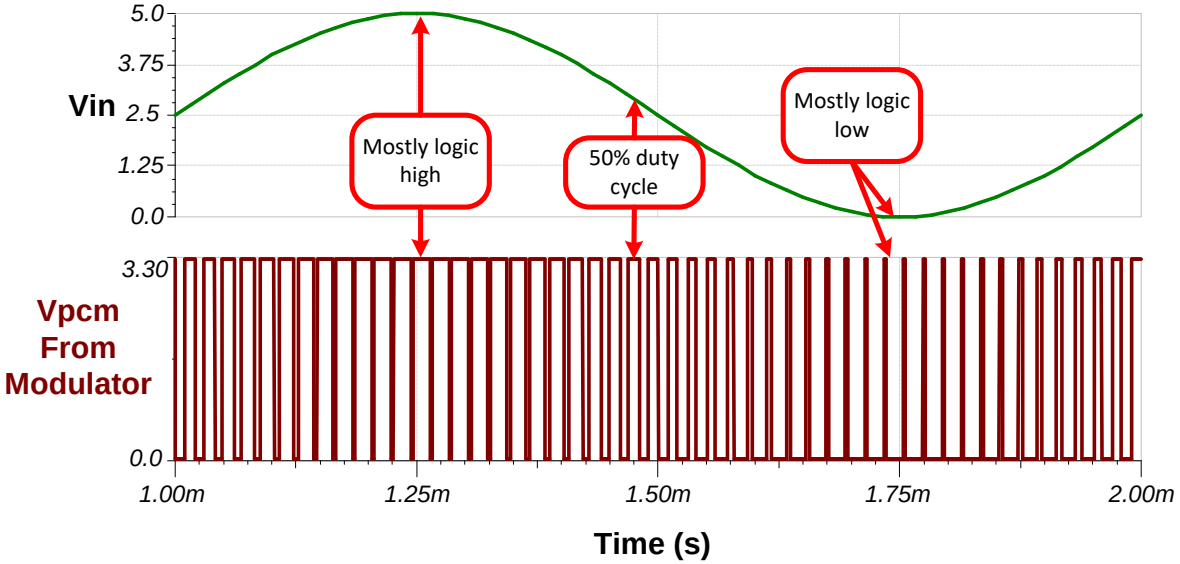




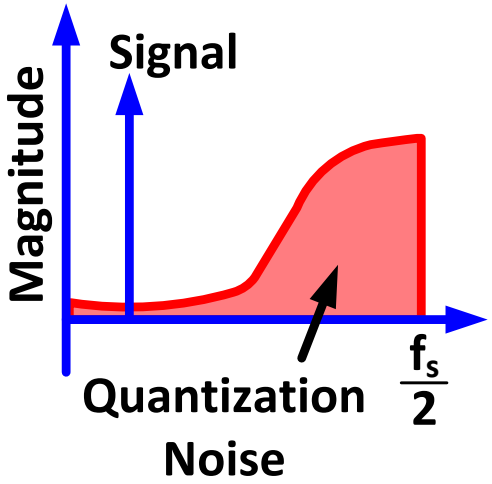
Modulator Output Signal



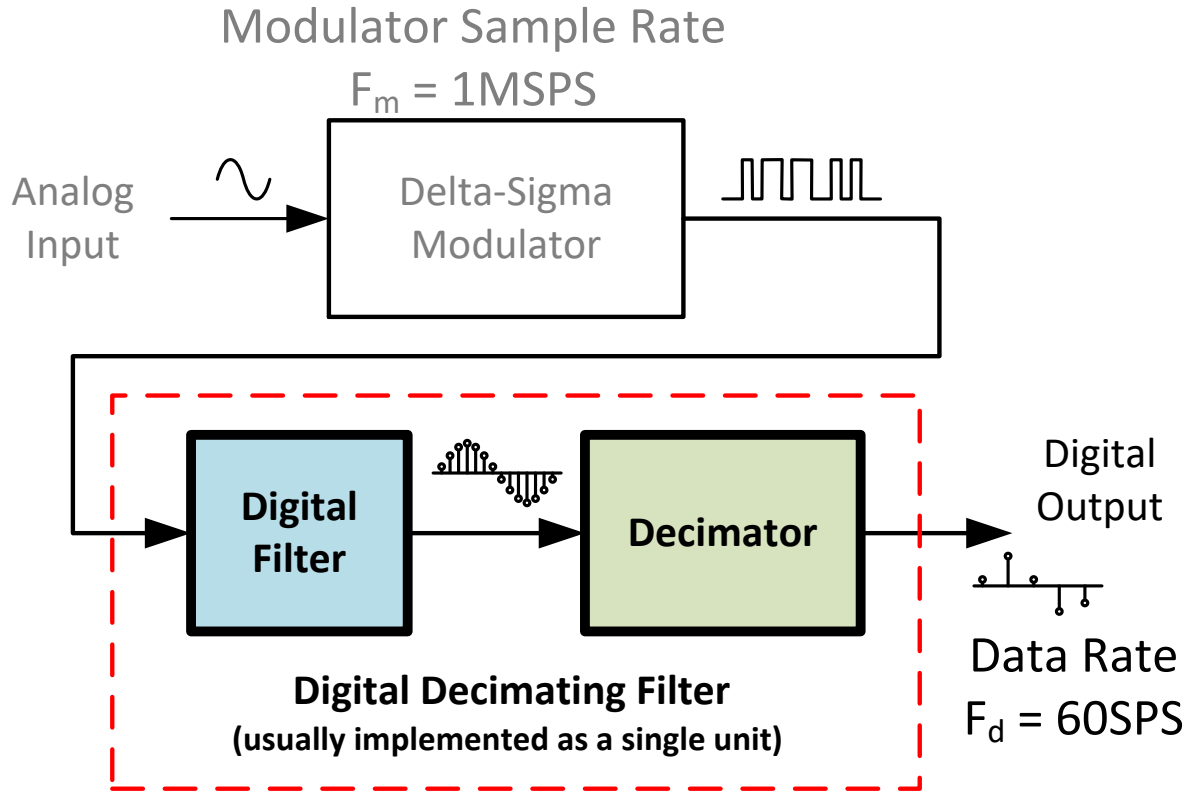
Modulator Output:
TIME DOMAIN



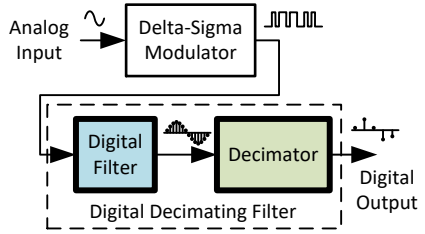
Modulator Output:
FREQUENCY DOMAIN

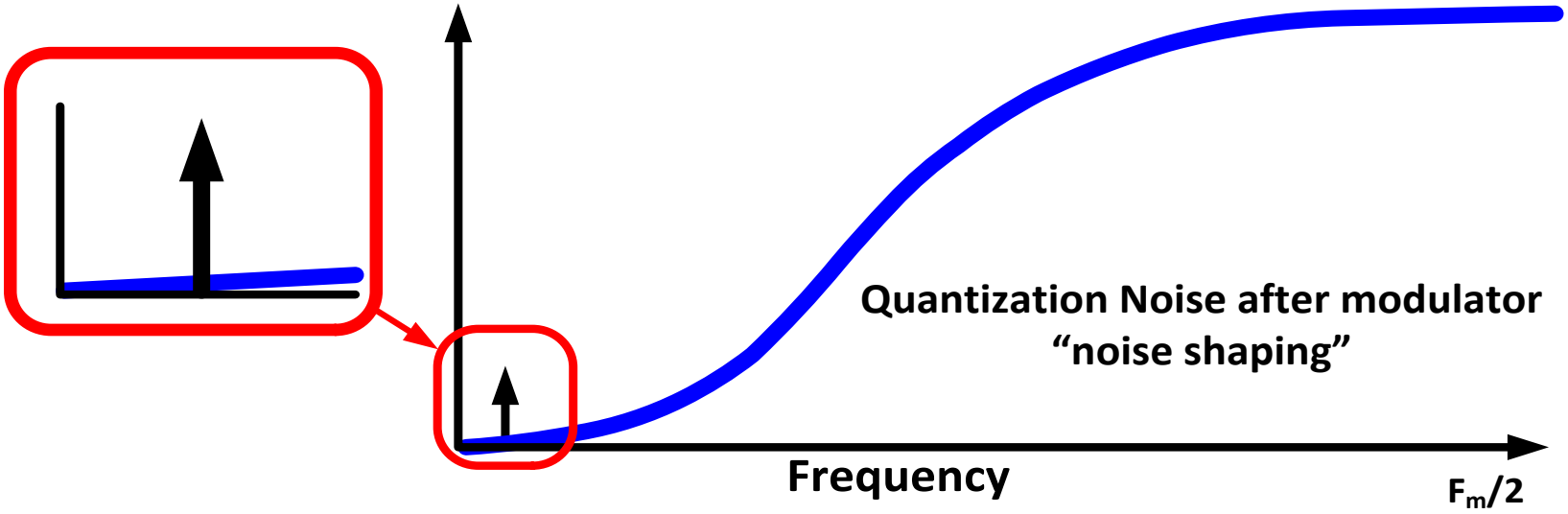


Delta-Sigma ADC Signal Path: Digital Filter

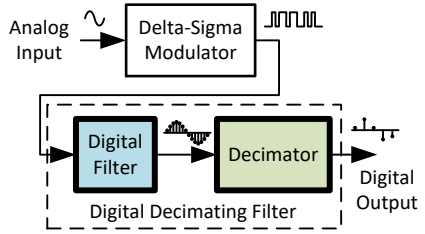


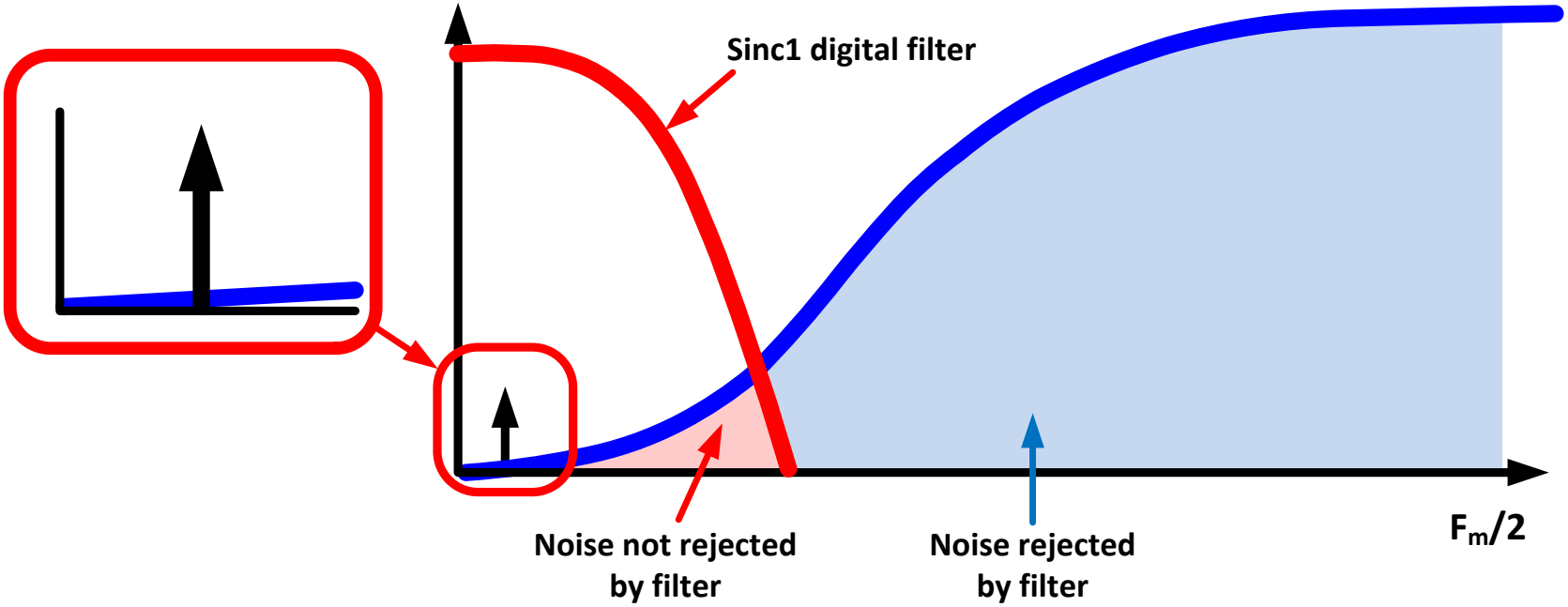
ΔΣ Principal – Digital Filter



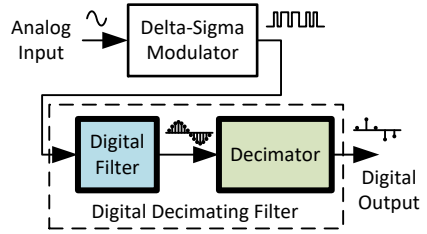


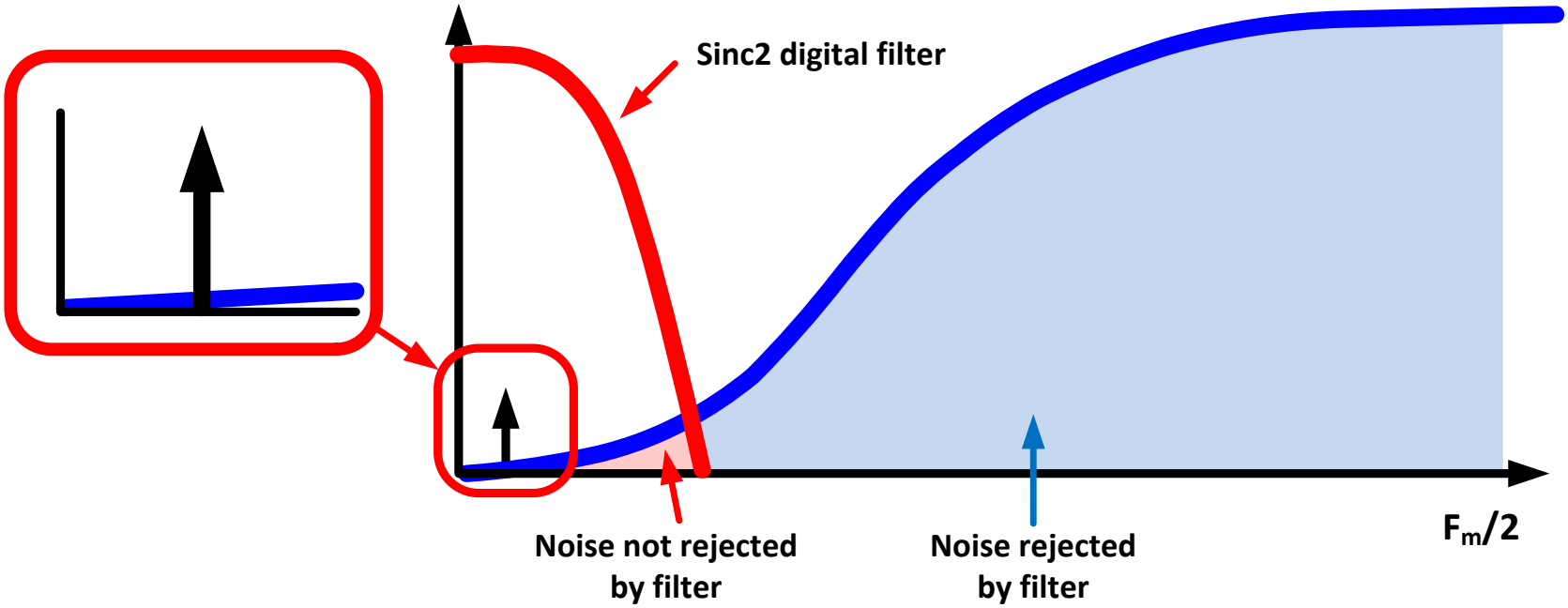
ΔΣ Principal – Digital Filter



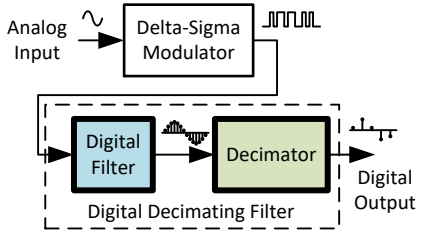


ΔΣ Principal – Digital Filter





ΔΣ Principal – Digital Filter



In general, filter order and cutoff frequency limit total noise

Sinc3 digital filter

Noise not rejected by filter

Noise rejected by filter

$F_m/2$

Thanks for your time!
Please try the quiz.

Questions: SAR & Delta-Sigma Introduction

1. Which ADC topology has an acquisition cycle and a conversion cycle.
   a. SAR
   b. Wide Bandwidth Delta Sigma
   c. Precision Delta Sigma
   d. Pipeline

2. (T/F) SAR ADCs use noise shaping and oversampling to reduce noise.
   a. True
   b. False

Questions: SAR & Delta-Sigma Introduction

3. Which ADC topology conversion acts as a snapshot in time?
   a. SAR
   b. Wide Bandwidth Delta Sigma
   c. Precision Delta Sigma
   d. Pipeline

4. The modulator of a delta-sigma converter is sampling at 1MHz. The data rate of the converter is 100SPS. What is the OSR?
   a. 0.0001
   b. 100
   c. 1,000,000
   d. 10,000