PCIe board layout recommendations

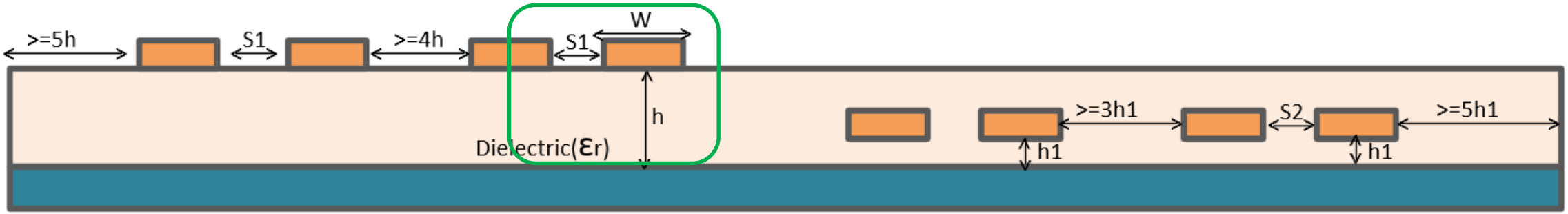
TI Precision Labs – PCIe

Prepared by Nasser Mohammadi

Presented by Nicholaus Malone

Differential board trace width and spacing

- Design trace width, height, and spacing to meet 85 ±20% Ohm for PCIe connector
  - 100 ±20% Ohm for chip to chip



Differential board trace width and spacing

- Design trace width, height, and spacing to meet 85 ±20% Ohm for PCIe connector
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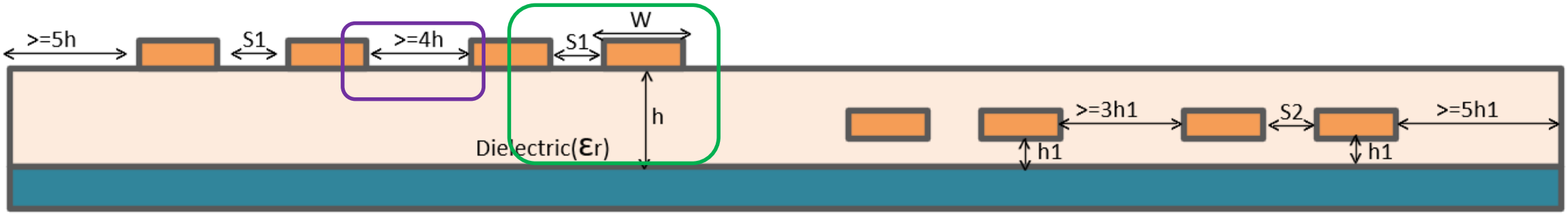
- Distance between adjacent traces should be at least 4 times dielectric height(h)
  - Stripline traces should be 3 times



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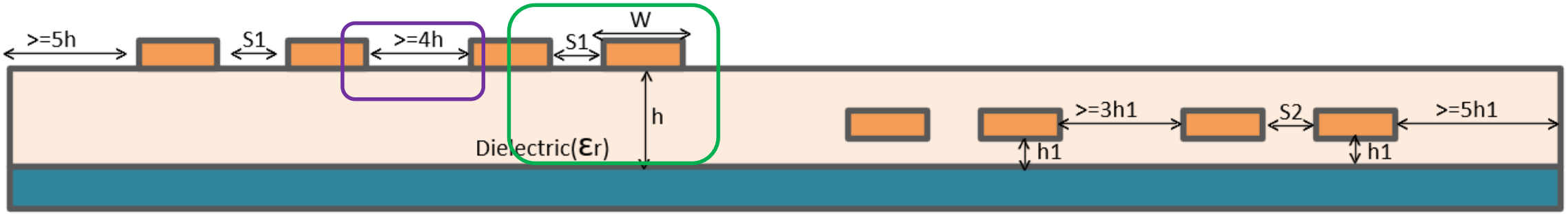
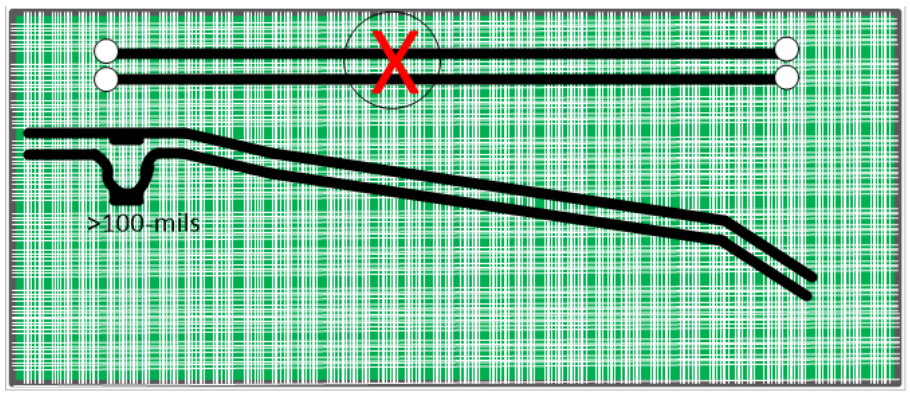
- Distance between PCIe pair and non-PCIe signals should be at least 4 times height
  - If non-PCIe signal has higher slew rate or level, then this distance should be 6 times height



Trace length matching and trace length

- Avoid running long traces in parallel with grain of the fiber.



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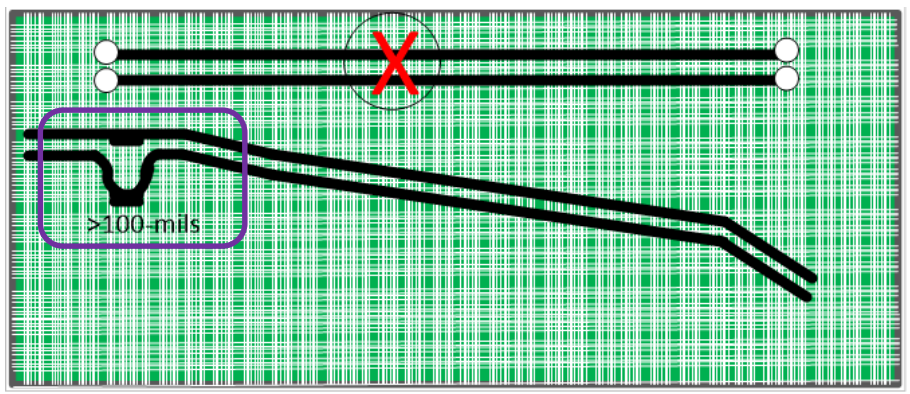
- Intra-pair trace should be matched to within 5-mils.
  - Trace mis-match compensation should be done at the point of mis-match.



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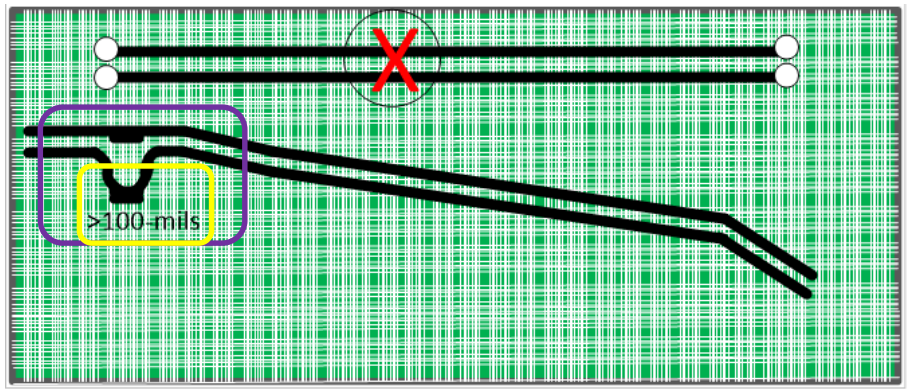

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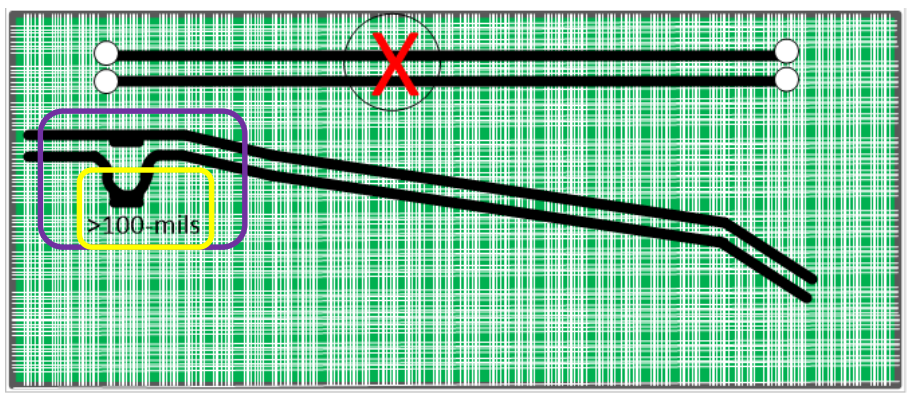
- Trace length to a connector is limited to 12 inches – this includes breakout area
  - Trace length from the edge-finger to add-in card chip set is limited to 4 inches
    - Board stack up and material can impact this length



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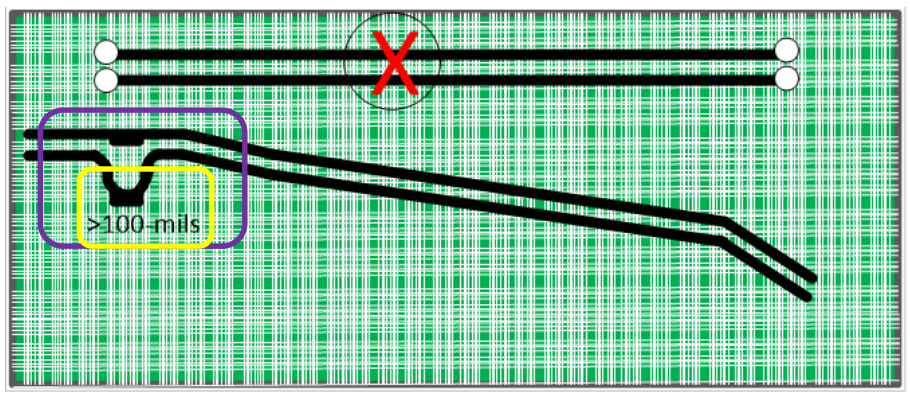

Via placement and guidelines

- Avoid vias as much as possible
  - Maximum of 6 via pairs are allowed on entire transmission line
  - In terms of loss, each via pair contributes to the loss budget per data rate 1dB at Gen4 and 0.5dB at Gen3
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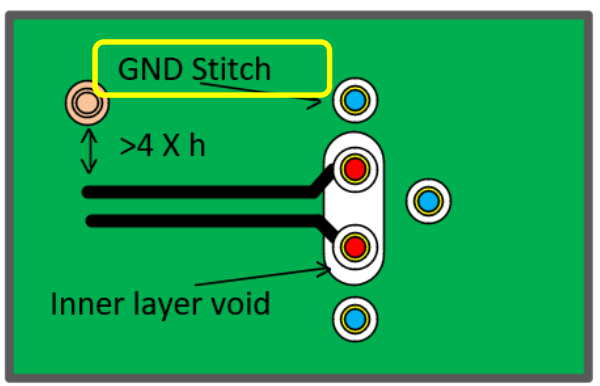
  - Location of via should be simulated. Else via should be placed at > via center to center spacing and < 100mils away from the via
  - Signal vias should have pads removed on unused internal layer
  - GND Stitch should be between the signal two reference planes



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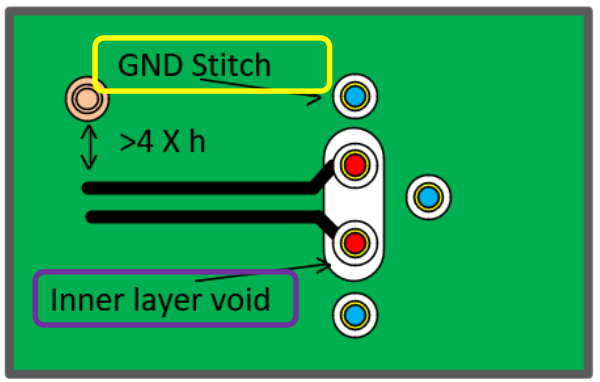
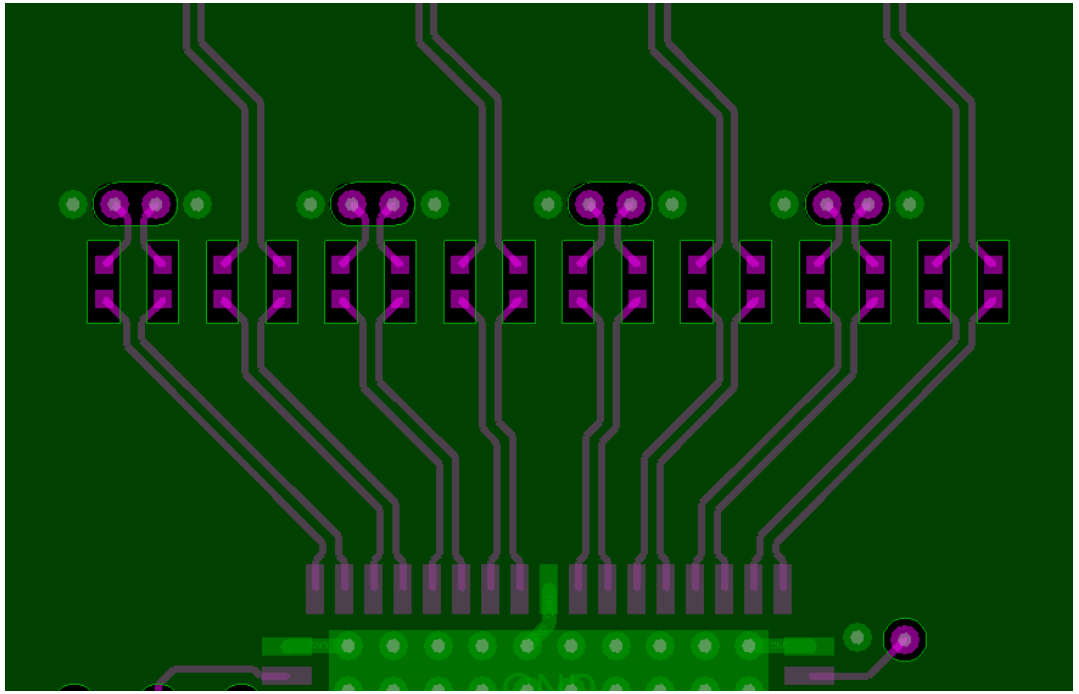
- Provide inner layer void – no GND or VCC – to reduce parasitic



AC Coupling Cap void

- Void under AC coupling Caps pad:
  - Through as many layers as possible



AC Coupling Cap void

- Void under AC coupling Caps pad:
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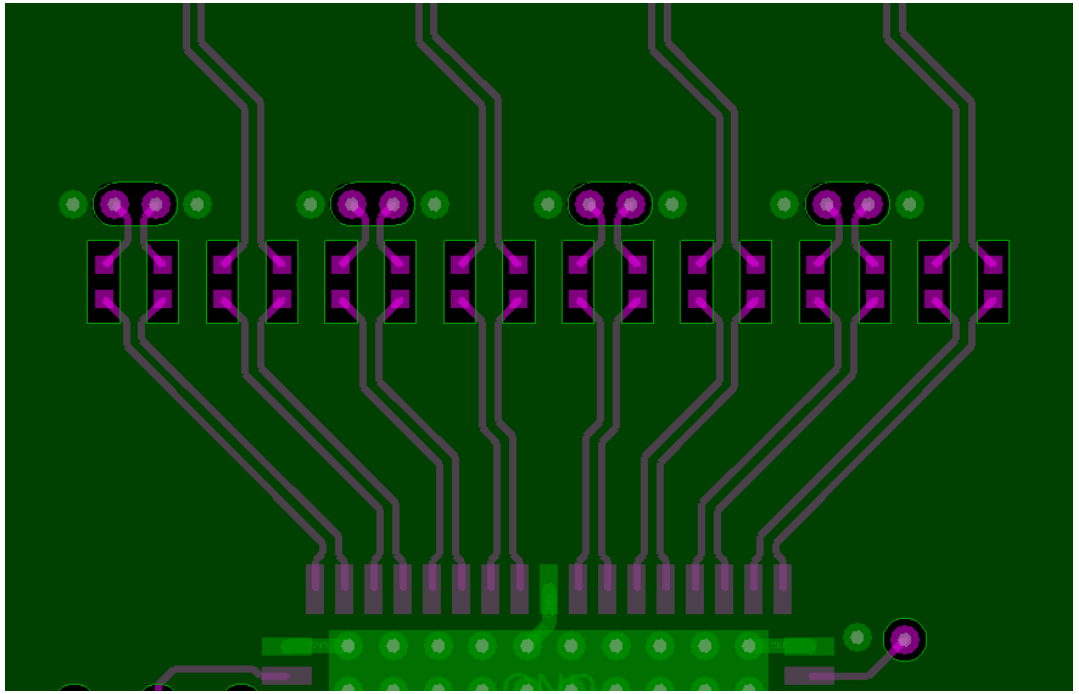
- Via to differential trace should have at least 3 times differential trace spacing



AC coupling capacitors placement

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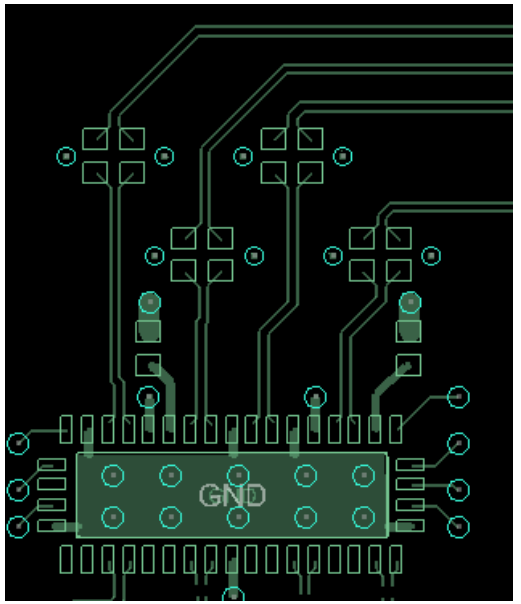
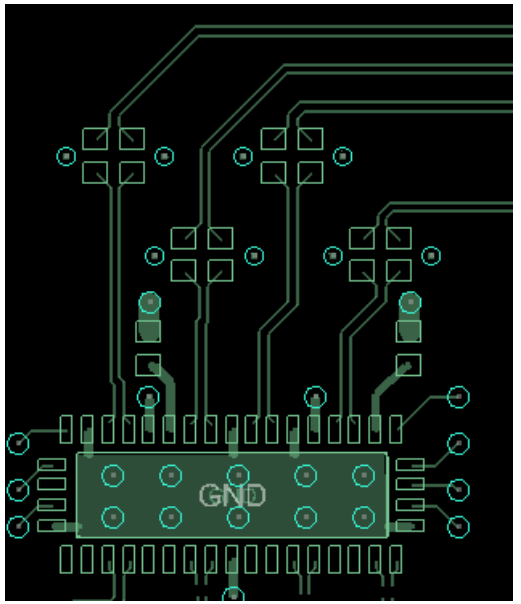


AC coupling capacitors placement

- Add-In Cards: Within 400mils of the CEM connectors
- Add-In Cards: Within 250mils of the finger edge



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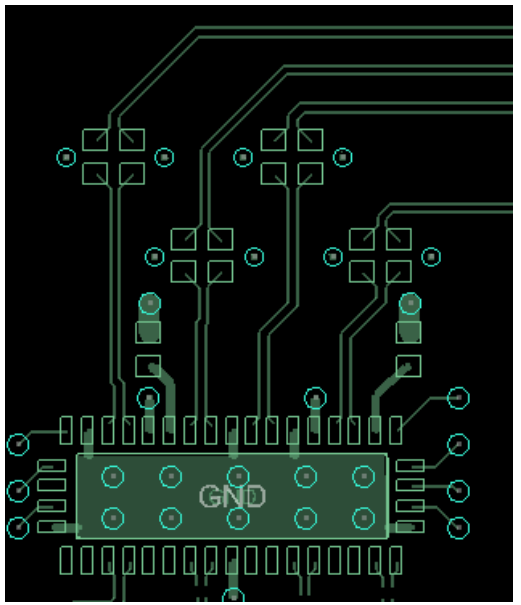

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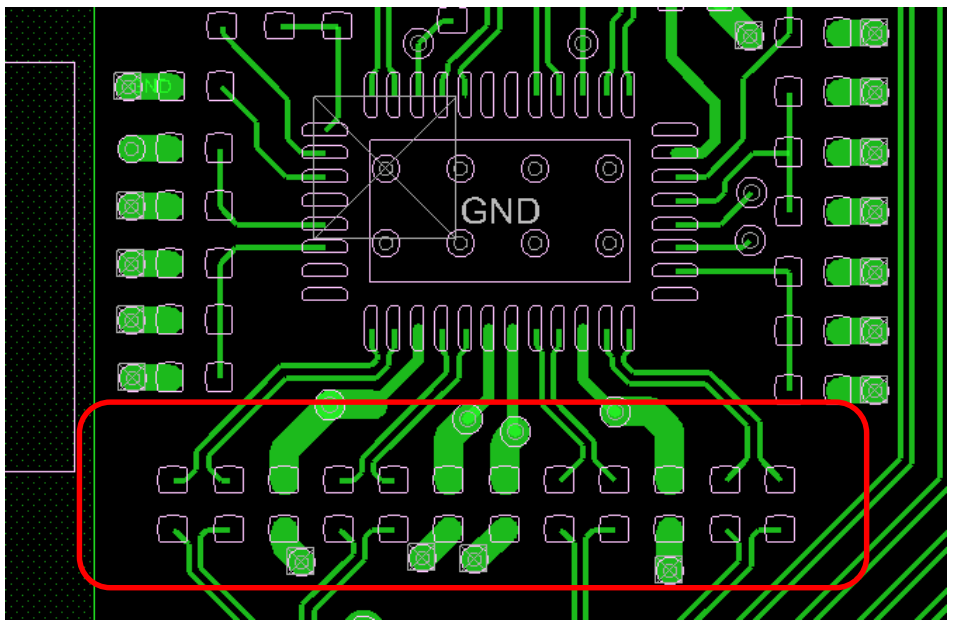
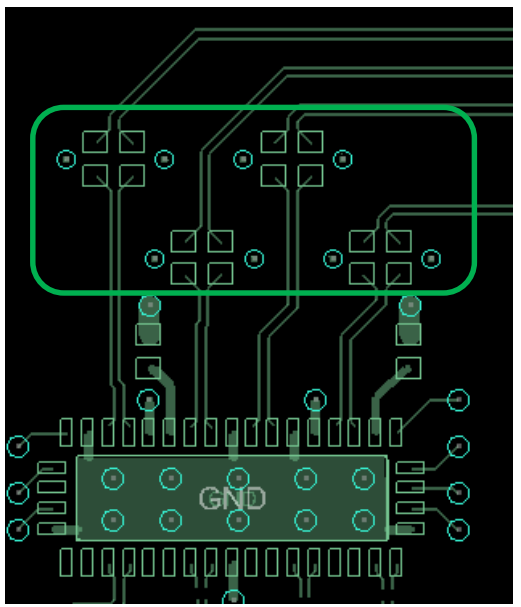
- Should be staggered to reduce plane disruption as much as possible
  - Improves high speed signal isolation as well





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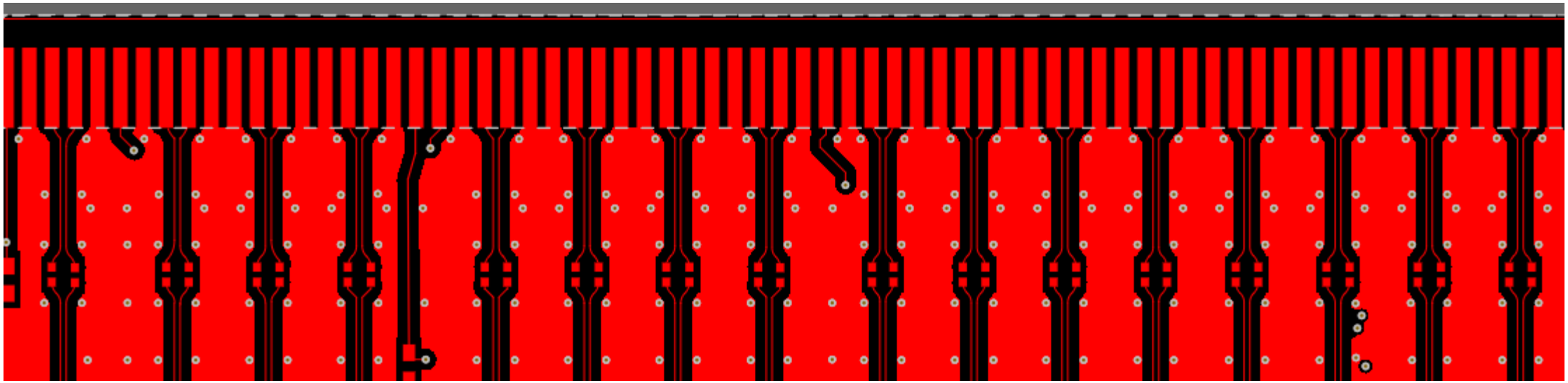

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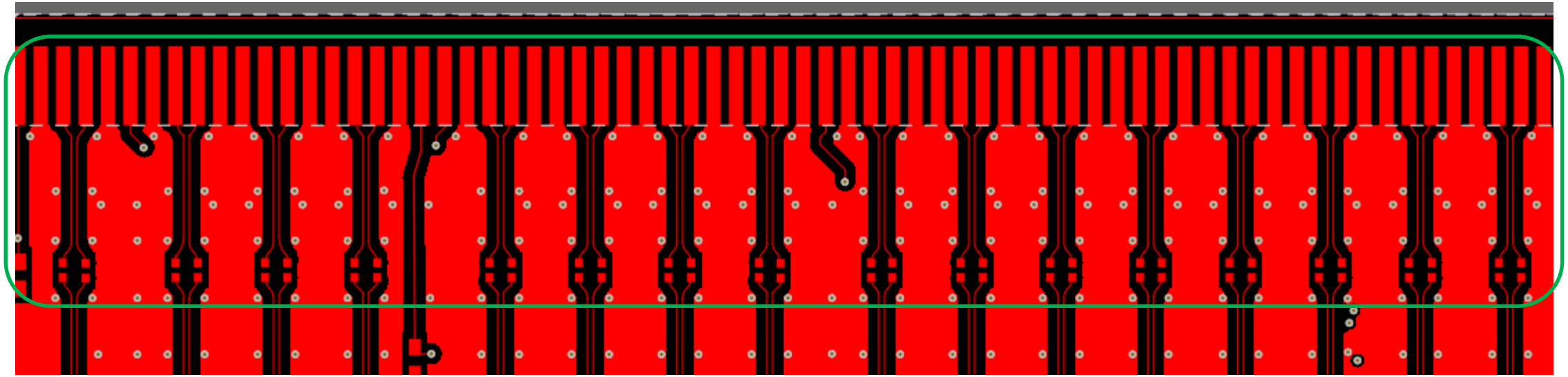
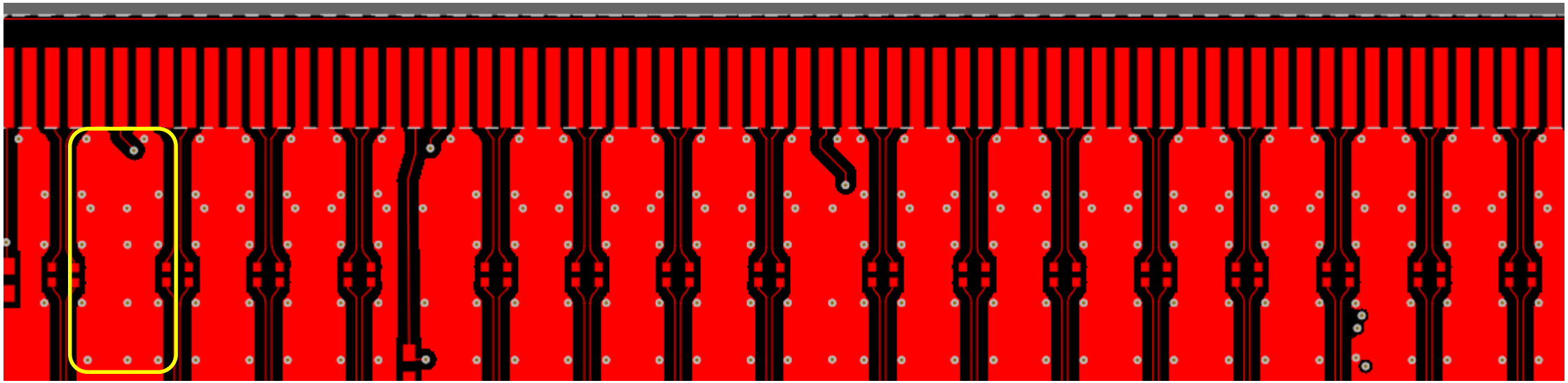


Cross talk mitigation

- GND Stitches along GND fill and vias



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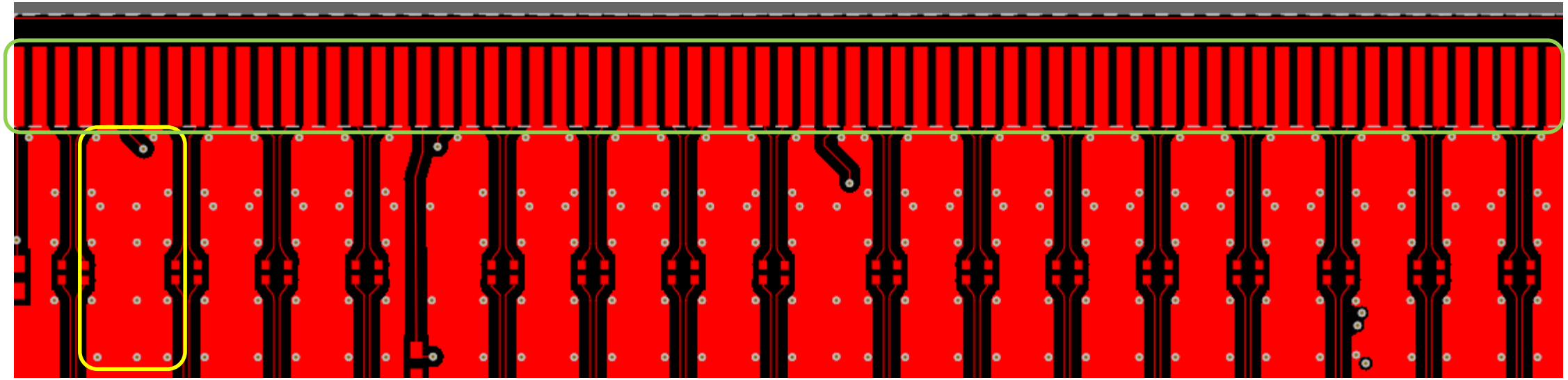

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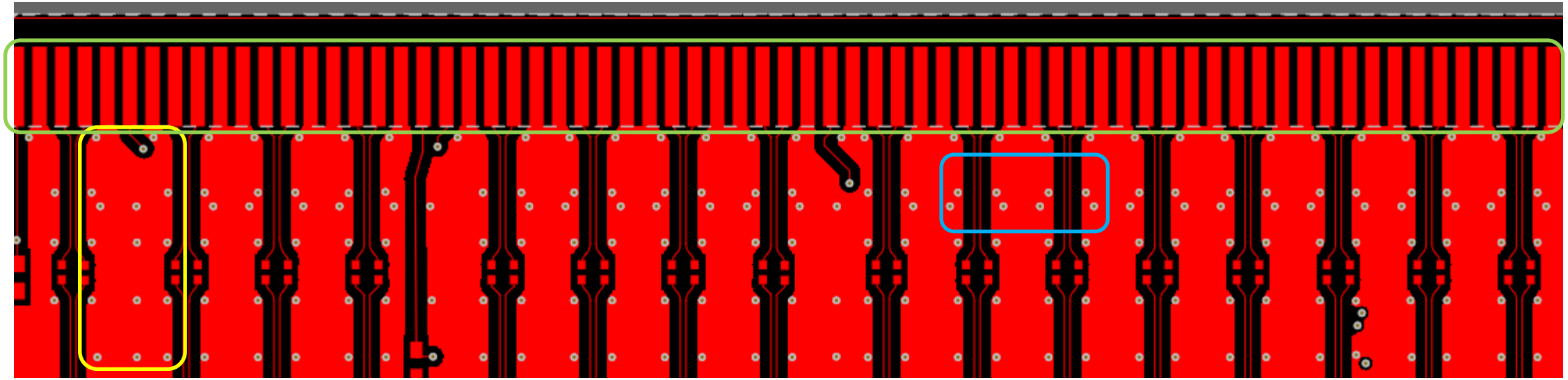

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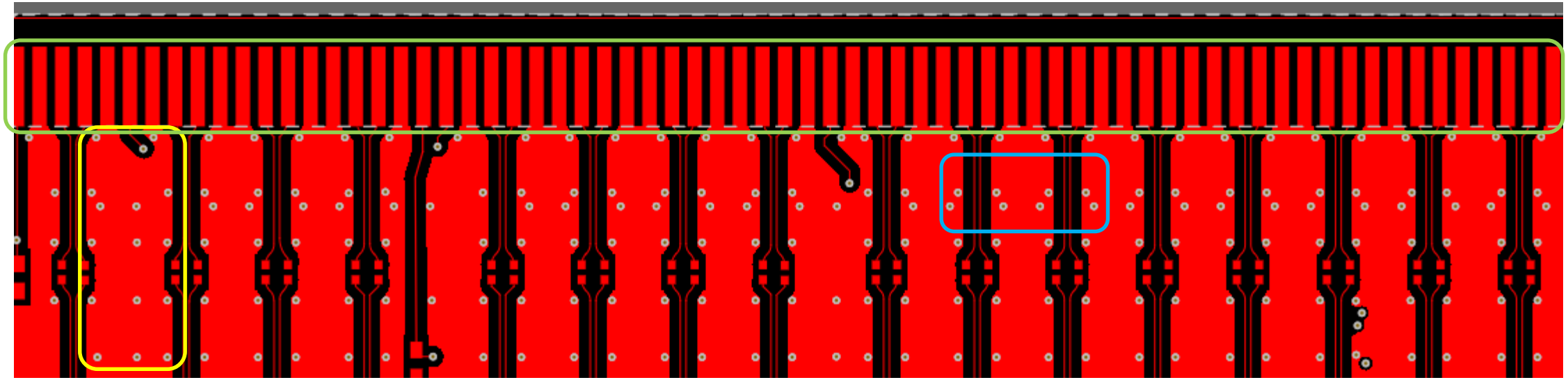

Thank you

- TI Precision Labs – PCIe Solving Signal Integrity Challenges