Protecting Delta-Sigma ADC from EOS – RTD Measurement Overview in PLC

TI Precision Labs – ADCs

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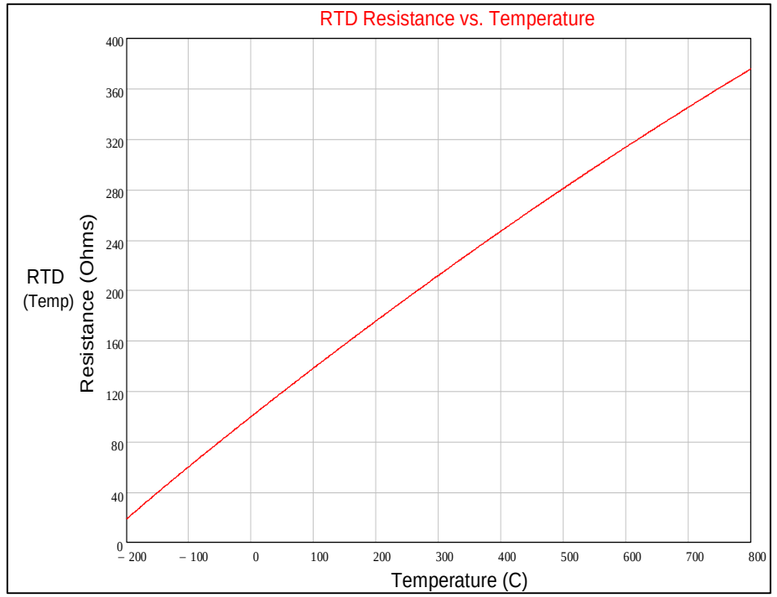
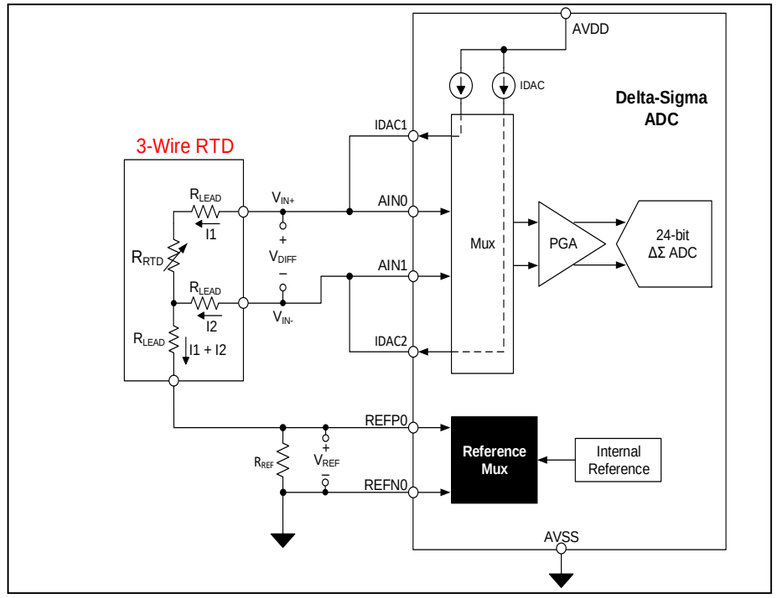
Prepared by Dale Li

RTD (Resistance Temperature Detector) Sensor





Application Notes:
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sbaa310.pdf
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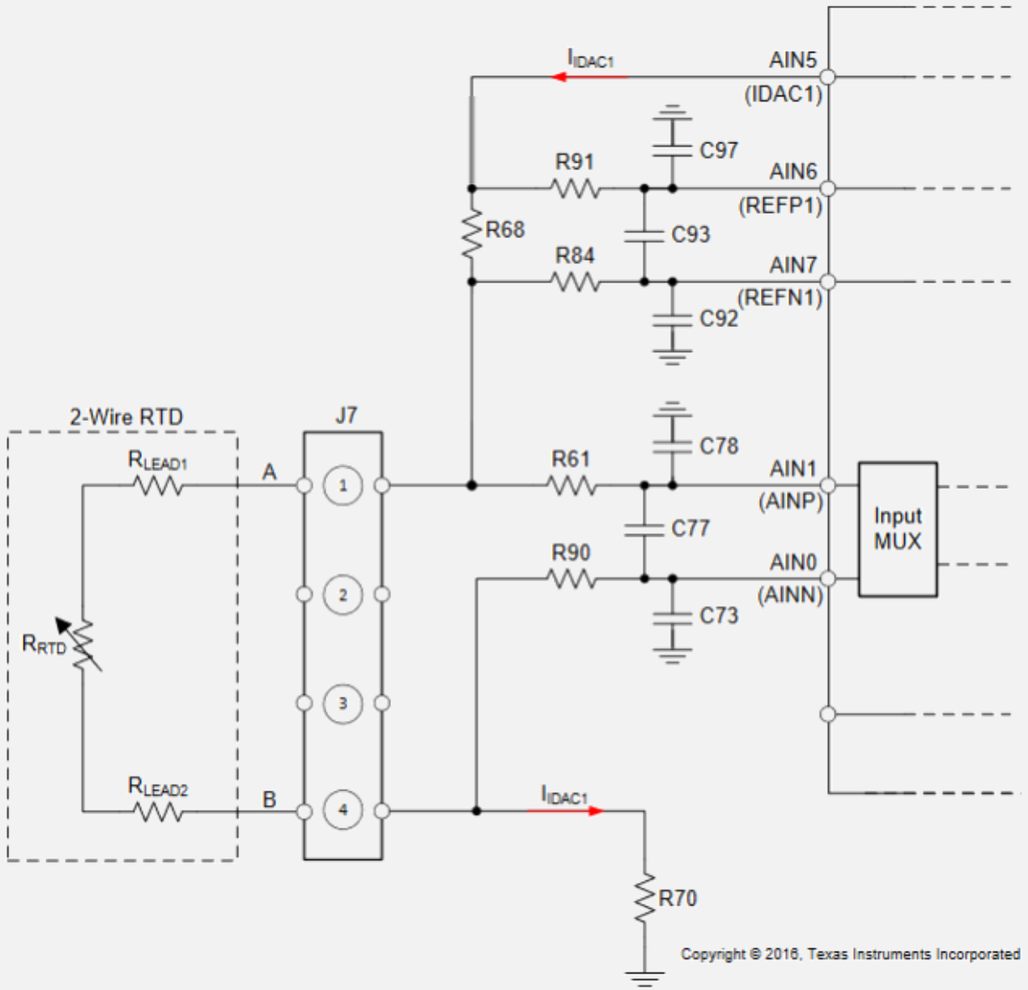
sbaa329a.pd
sbaa201.pdf

- **PT-100** exhibits 100Ω resistance at 0ºC and has wide temp range: **-200ºC to 850ºC**
- R varies from **20Ω to 400Ω**, Currents are pumped into RTD and voltage is measured
- Sensor with a predictable resistance vs. temperature
- Measure the resistance and calculate temperature based on the Resistance vs. Temperature characteristics of the RTD material
- Overstress (EOS) protection is an increasingly popular requirement from customers.

Typical Block Diagram: 2-wire RTD Inputs

2-Wire RTD Block Diagram



Circuit Notes

- 2 terminal input (minimum)
- High-side reference (low-side is possible as well)
- One excitation current required
- No lead wire compensation
- R_{REF} is typically largest source of error

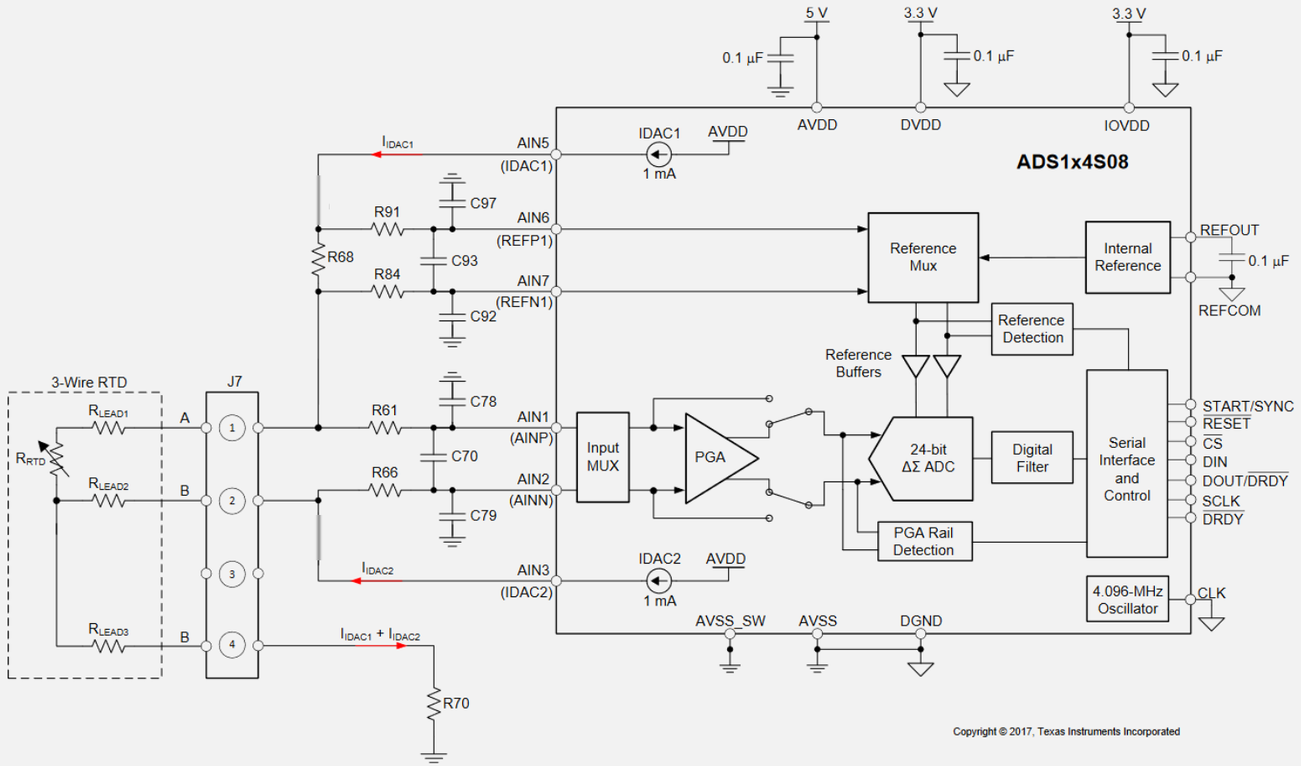
Key ADC Specs

- Differential VREF inputs
- 1x current sources
- Low-noise
- Integrated gain stage

**From ADS124S08 EVM

Typical Block Diagram: 3-wire RTD Input

3-Wire RTD Block Diagram



Circuit Notes

- 3 terminal input (minimum)
- High-side reference (low-side is possible as well)
- Excitation via 1x or 2x current sources (1x IDAC requires 2x measurements)
- Lead wire compensation is possible
- R_{REF} is typically largest source of error

Key ADC Specs

- Differential VREF inputs
- 2x or 1x current sources
- Low-noise
- Integrated gain stage

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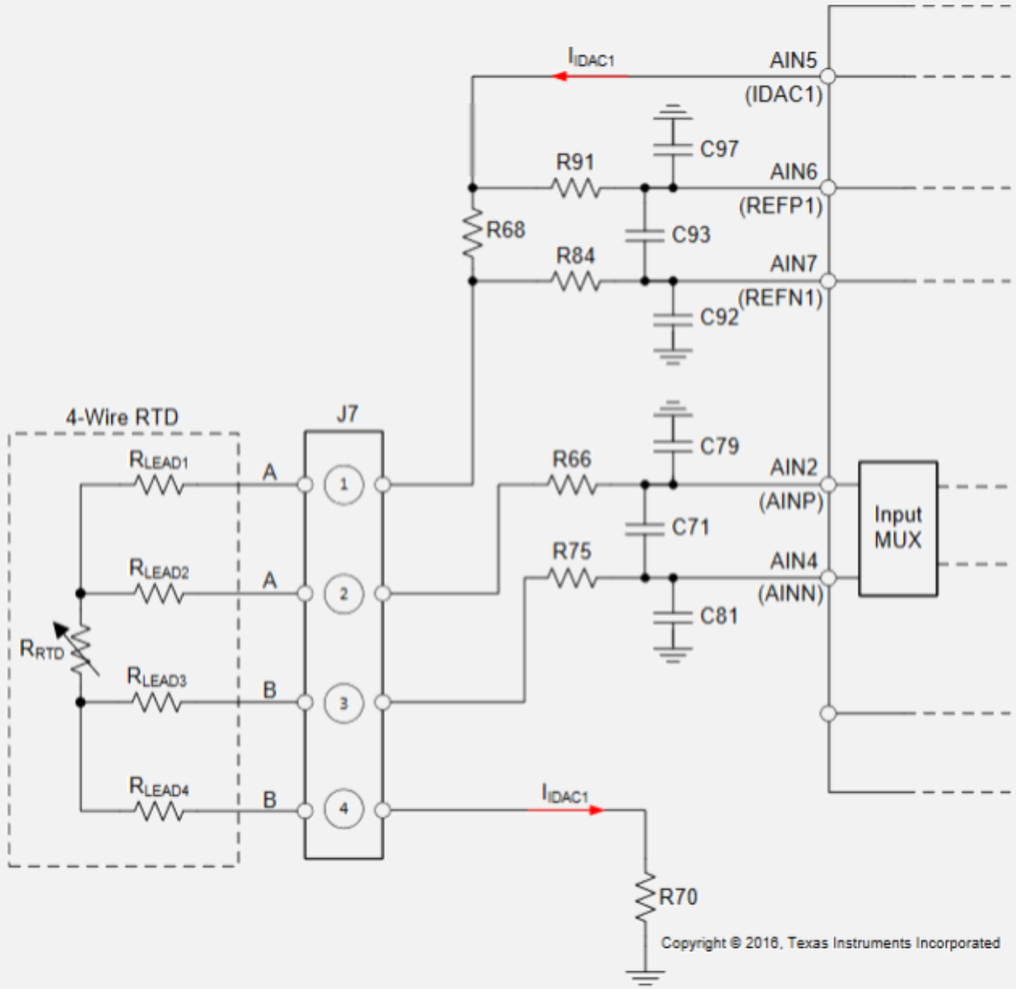
Typical Block Diagram: 4-wire RTD Inputs

4-Wire RTD Block Diagram



Circuit Notes

- 4 terminal input
- High-side reference (low-side is possible as well)
- One excitation current required
- Inherent lead wire compensation
- R_{REF} is typically largest source of error

Key ADC Specs

- Differential VREF inputs
- 1x current source
- Low-noise
- Integrated gain stage

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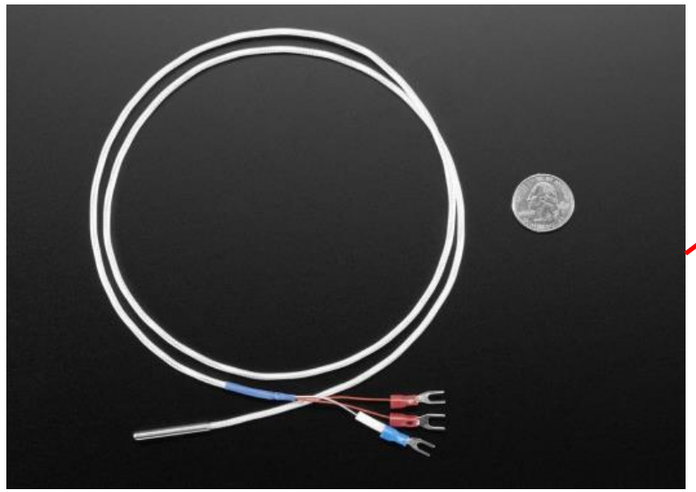
Common 3-wire RTD Measurement without Protection

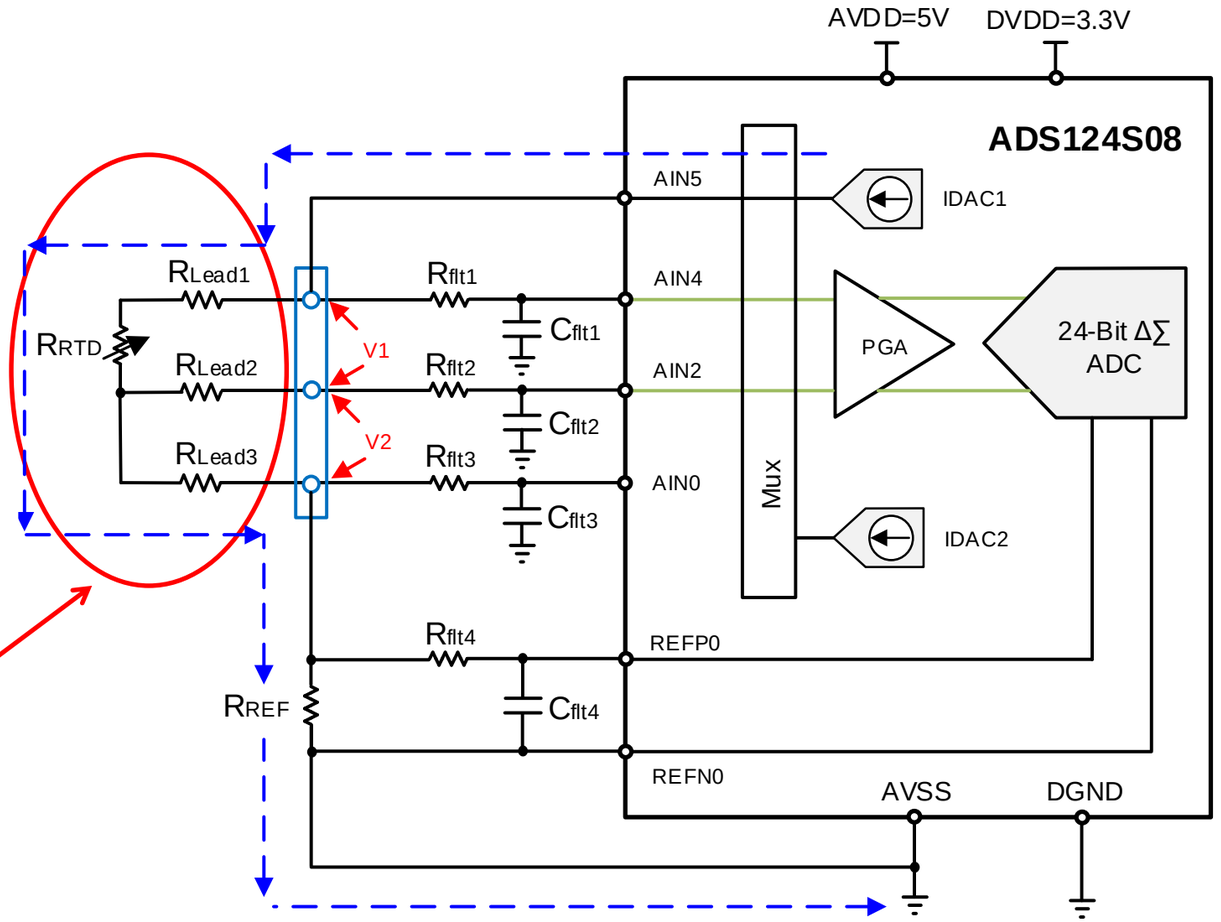
- **Ratiometric Measurement**:

  IDAC noise and drift are cancelled.

- **Lead Wire Resistance Cancellation**:
  - ✓ Lead resistance is related to length, material and cross-sectional-area of the conductor.
  - ✓ One IDAC needs two measurements.
- **Two IDACs need current chopping to minimize the effect of mismatched current sources**.



Note: 1-meter PT100 RTD sensor from Adafruit.

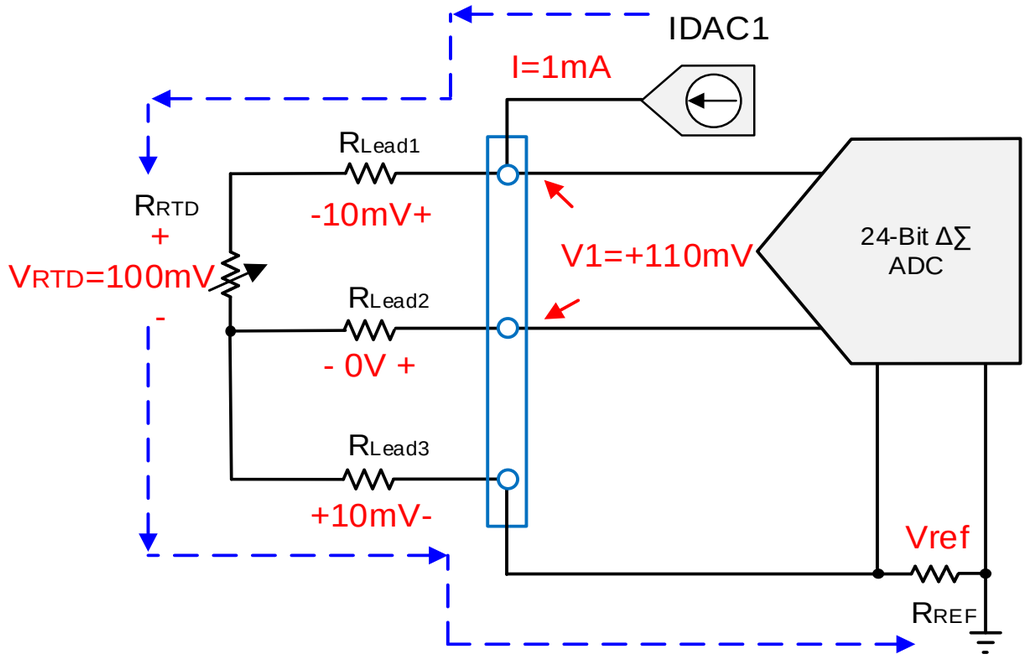


3-Wire RTD, Low-Side Reference Measurement Circuit With One IDAC Current Source (Common-mode capacitor not shown)

Why do we need Two measurements

Two measurements by taking difference between V_1 and V_2:

- Cancel lead wire resistance.
- Cancel the offset of ADC.
- Low side reference requires two measurements.
- High side reference measurement only requires one measurement, however the resistor selections (R_{RTD}, R_{ref} and R_{bias}) and IDAC current are limited by compliance voltage.



Note: R_{RTD} =100Ω, R_{Lead1} = R_{Lead2} = R_{Lead3} = 10Ω

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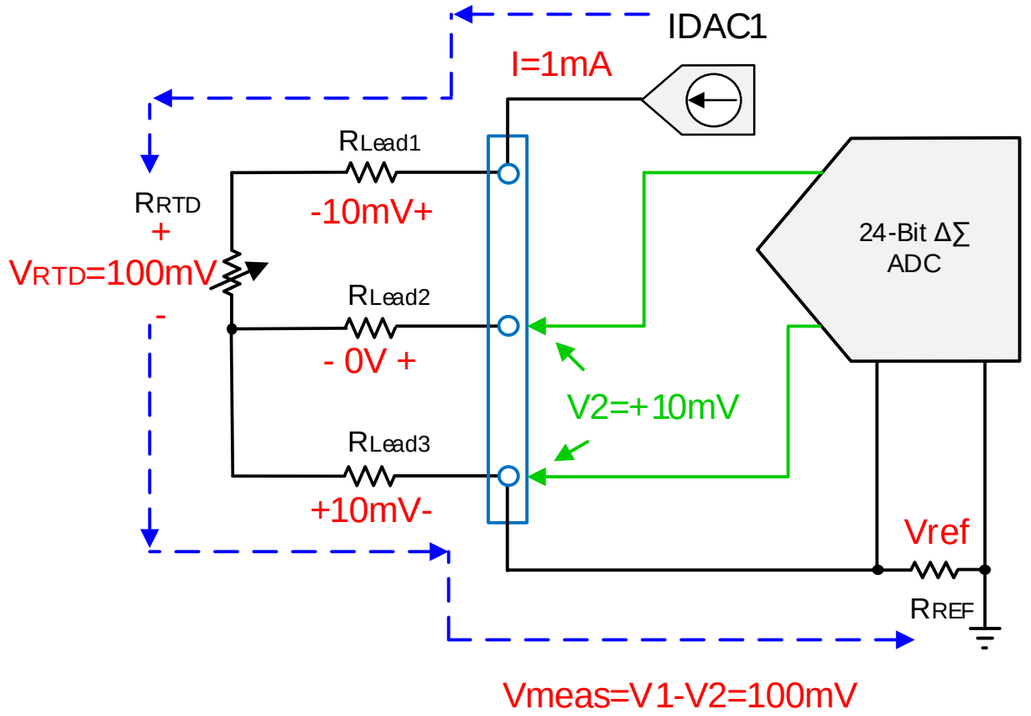

Note: R_{RTD} =100Ω, R_{Lead1} = R_{Lead2} = R_{Lead3} = 10Ω

Thanks for your time!
Please try the quiz.

Questions: Protecting RTD input Delta-Sigma

1. (T/F) The two wire RTD configuration uses multiple current sources to cancel lead resistance error.
   a. True.
   b. False.

2. (T/F) To achieve lead wire error cancelation, a three wire configuration must have equal resistance in each lead.
   a. True
   b. False.

Questions: Protecting RTD input Delta-Sigma

3. What does PT-100 stand for?
   a. Prime Temperature 100^{o}C.
   b. Part tolerance 100Ω
   c. Specific manufacture model number for high temperature RTD.
   d. Platinum RTD that is 100Ω at 0^{o}C.
   e. Copper RTD that is 100Ω at room temperature.

Thanks for your time!