PCB Trace as a Wave Guide

TI Precision Labs – ADCs

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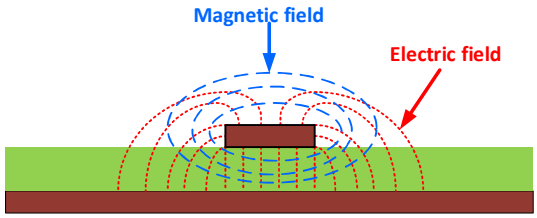
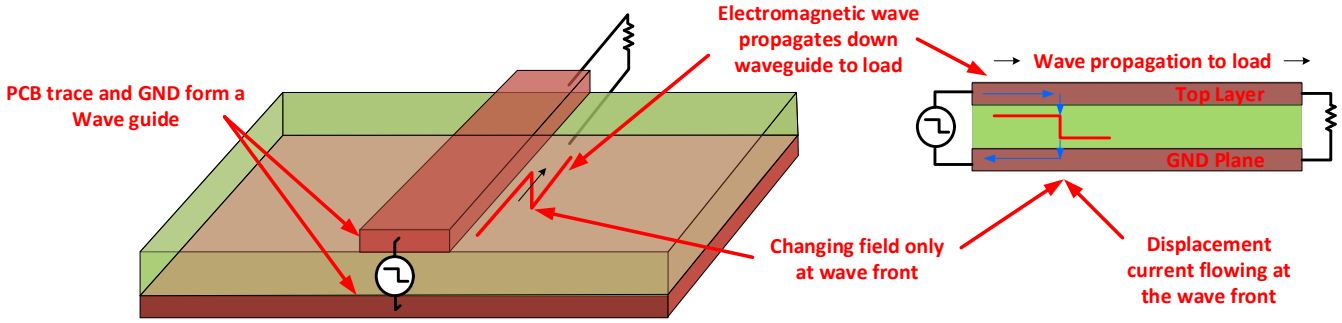
Hello, and welcome to the TI Precision Lab video covering how a PCB trace acts as a wave guide. This is part of a larger series on PCB layout for good EMC. This series is specifically intended to cover mixed signal designs where the digital signals are less than 100 MHz and clock rise times are greater than 1 ns. This video looks at how return current flows relative to the signal trace. The video describes the problem with ground plane discontinuities, and also describes the best way to use vias to transition layers and minimize EMI. Lets start by considering a PCB trace as a wave guide.

Think of your PCB trace as a wave guide



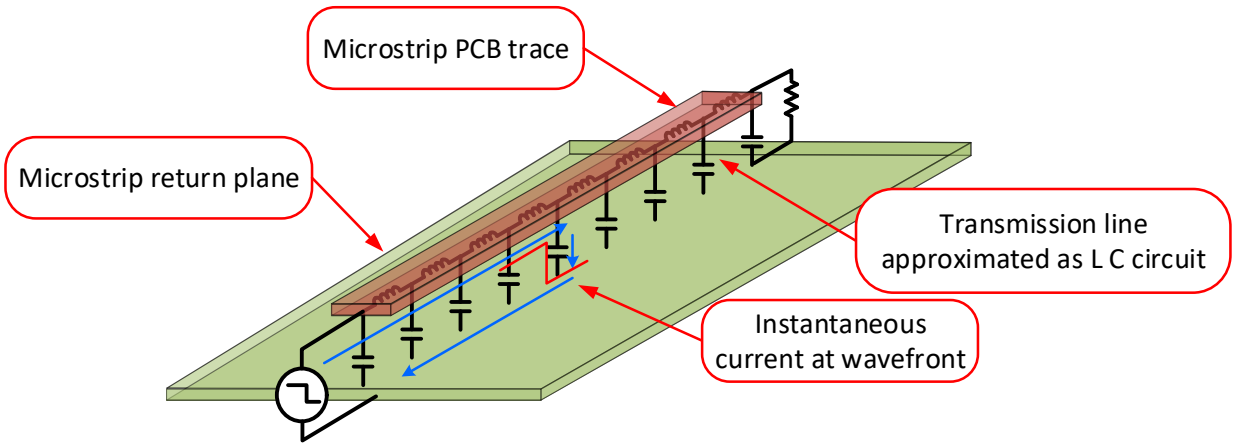
Signal Propagation

The signal propagates by displacement current $1.8 \cdot 10^8$ m/s. The conduction current travels at 0.01m/s



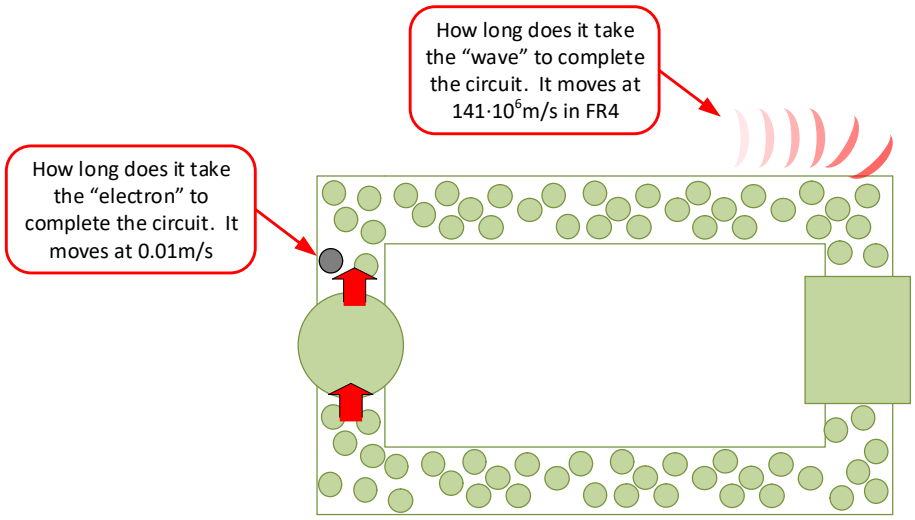
This slide shows how a voltage step propagates down a PCB trace. In this example, we show a trace separated from a ground return plane by PC board dielectric material. As the signal propagates down the trace, a changing electric and magnetic field follow the wave front. The electromagnetic wave propagates at a very fast rate of 1.8×10^8 m/s, whereas the actual conduction of electrons from the positive terminal to the negative terminal happens at a very slow rate of 0.01 m/s. The key point here is that an electromagnetic wave is traveling through the PC Board dielectric and is being guided by the trace on the top and the ground return plane on the bottom. Think about this wave guide as we step through today's material.

Transmission line view of signal propagation



Another way of looking at the same circuit is to consider the transmission line as a series of LC Circuits. As the wavefront progresses down the PCB trace, the capacitor and inductor will charge to steady state. An instantaneous current will be seen at the wavefront, but before and after the wavefront the LC circuit will be at steady state. This is really just another way of looking at the same circuit shown in the last slide. Remember this wave front is traveling at a very fast rate but conduction current is moving slowly. We will look at this closely in the next slide.

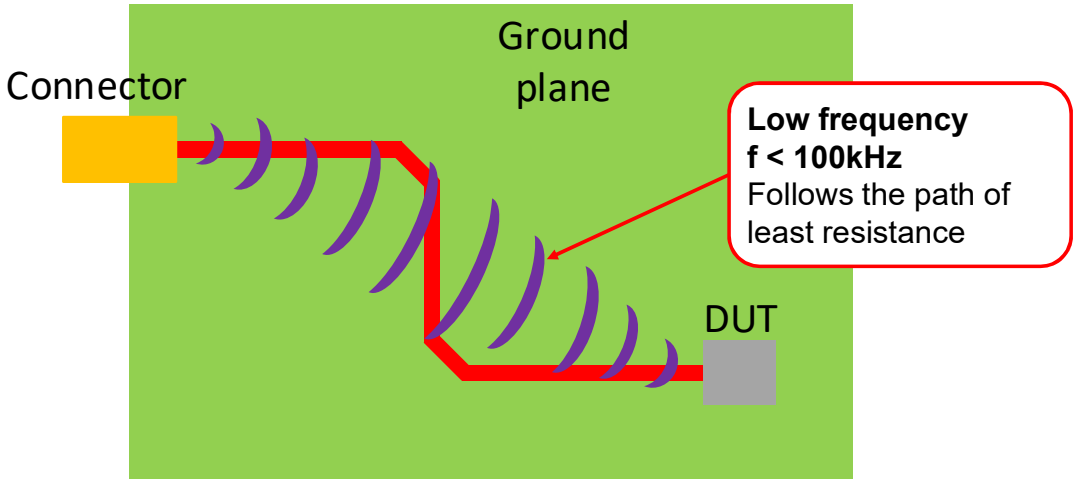
Displacement current vs. conduction current



- **Think of signals propagating as electromagnetic waves.**
- **Not as electron flow.**

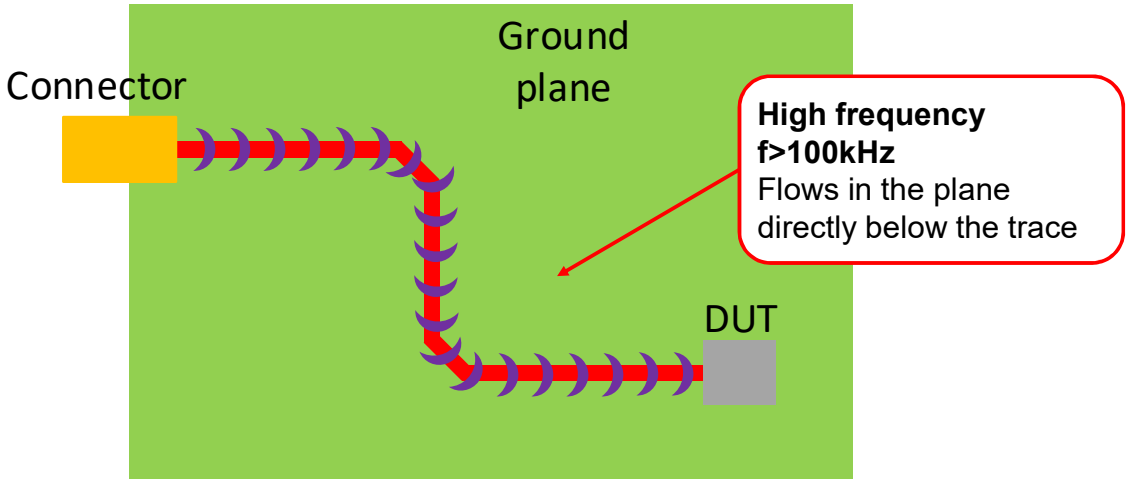
This slide is meant to illustrate the difference between conduction current and displacement current. It shows a simple circuit with a voltage source, wire, and load. Conduction current is the travel of an electron from the positive terminal of the voltage source, through the load to the negative terminal of a voltage source. This occurs at a very slow rate of .01 m/s. The displacement current, on the other hand, travels at a very high rate of 141×10^6 m/s in FR4 PCB material. Think of displacement current as a chain reaction of electron collisions starting at the source and traveling through the load back to the negative terminal of the source. As an as an analogy, consider a hose filled with water. When you turn on the water faucet, water will instantly come out of the other end of the hose. A chain reaction of water molecule collisions starts at the faucet, continues through the hose, and forces water out of the end. It may take some time for the water from the faucet to reach the end of the hose, but water will squirt out the hose the instant the faucet is turned on. Propagation of electromagnetic waves and displacement current happen in a similar manor. The wave front and displacement current move quickly but the conduction current is very slow.

Return current in high vs low frequency

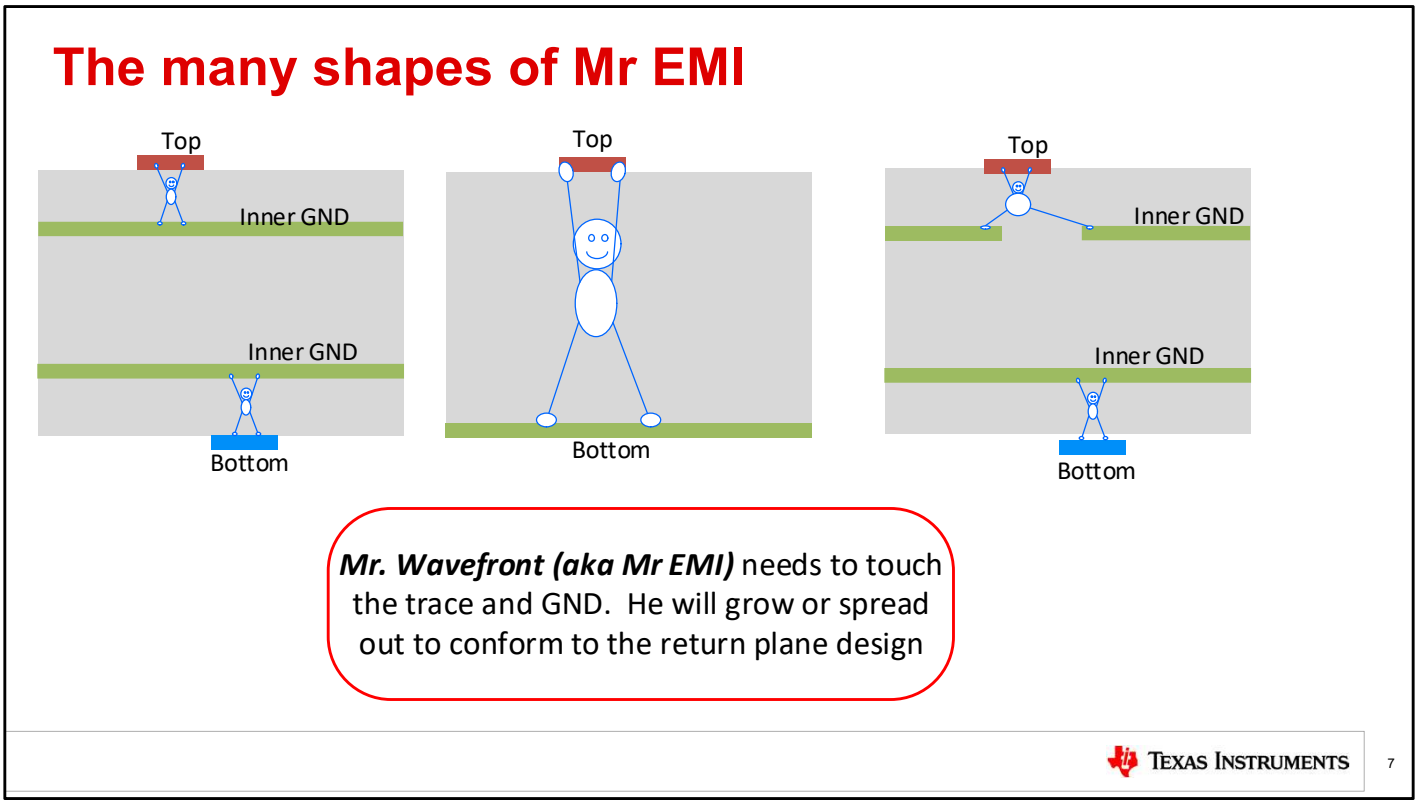


Now let's discuss how return current flows in a PCB ground plane relative to the top layer signal trace for low frequency signals. The figure shown here is the top layer of a printed circuit board where the signal applied to the connector travels across the red trace on the top of the PCB to the DUT. **[Click]** For low frequency signals the return current in the ground plane will spread across the board and follows the path of least resistance. In this case, "low frequency" means signals less than 100kHz.

Return current in high vs low frequency

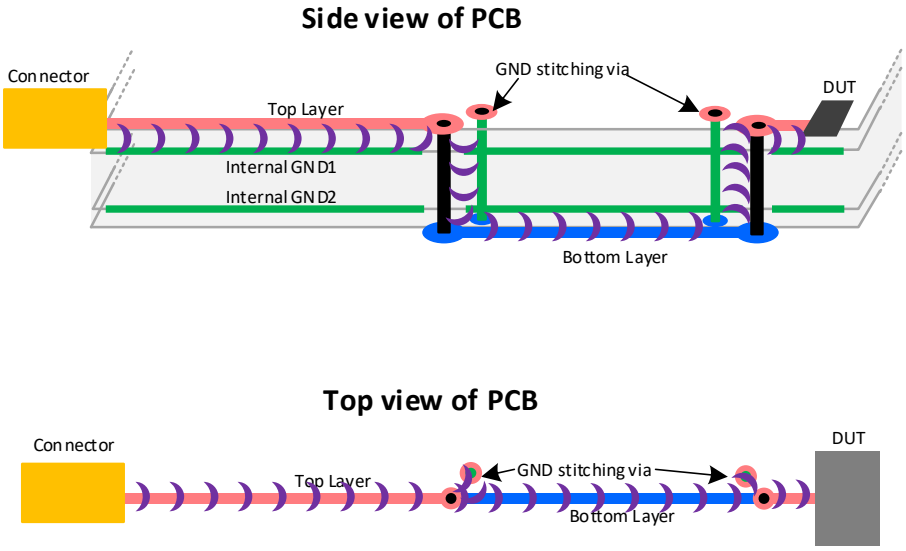


For signals above 100kHz, the return current will flow directly beneath the signal trace. [Click] This is a very useful and important electrical characteristic, because it means that the return currents for high frequency signals that are physically separated from each will not mix. When the return current of two signals mix this will cause interference or crosstalk between the signals. Later we will look at the details on how PCB spacing impacts crosstalk.



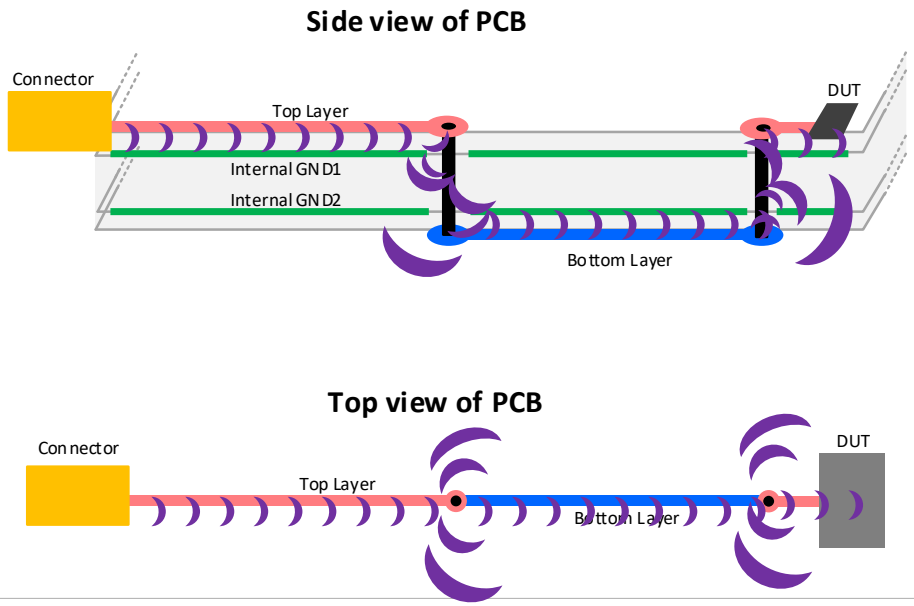
A silly analogy that helps explain how the wavefront beneath a signal trace changes in size is “Mr EMI”. Mr. EMI is the wavefront between the top layer and the ground return plane. Mr. EMI conforms to the size of this wave guide, so if the PCB trace is located close to a ground return plane, the size of the wavefront will be small. On the other hand, if the distance between the signal and return path is large Mr. EMI will grow large. Also, if there are gaps in the return path Mr. EMI will stretch to conform to the return path. Mr. EMI is not your friend, so keep him as small as possible. I know this is a little silly, but I hope it helps you visualize how different PCB geometries can change the size of the wavefront.

A well designed “wave guide” style PCB design



Now let’s look at how a signal travel across a printed circuit board when the signal transitions with vias between the top and bottom layer. Notice that this example layout uses an unusual stackup with two internal GND planes. It turns out that this is a very good stackup for low EMI. We will cover this in detail later. Now let’s will look at a well designed example using vias to transition layers, then we will look at a poorly designed example. **[Click]** Think of the signal layer and ground return paths as a wave guide where the wave travels. When the signal transitions from the top layer to the bottom layer the ground return needs to transition from internal ground 1 to internal ground 2. It makes transition using the stitching via as a vertical wave guide from the top to bottom. The entire signal path in this example has a good continuous wave guide for the signal to travel. Now lets look at the same circuit done the wrong way.

PCB design without GND stitching



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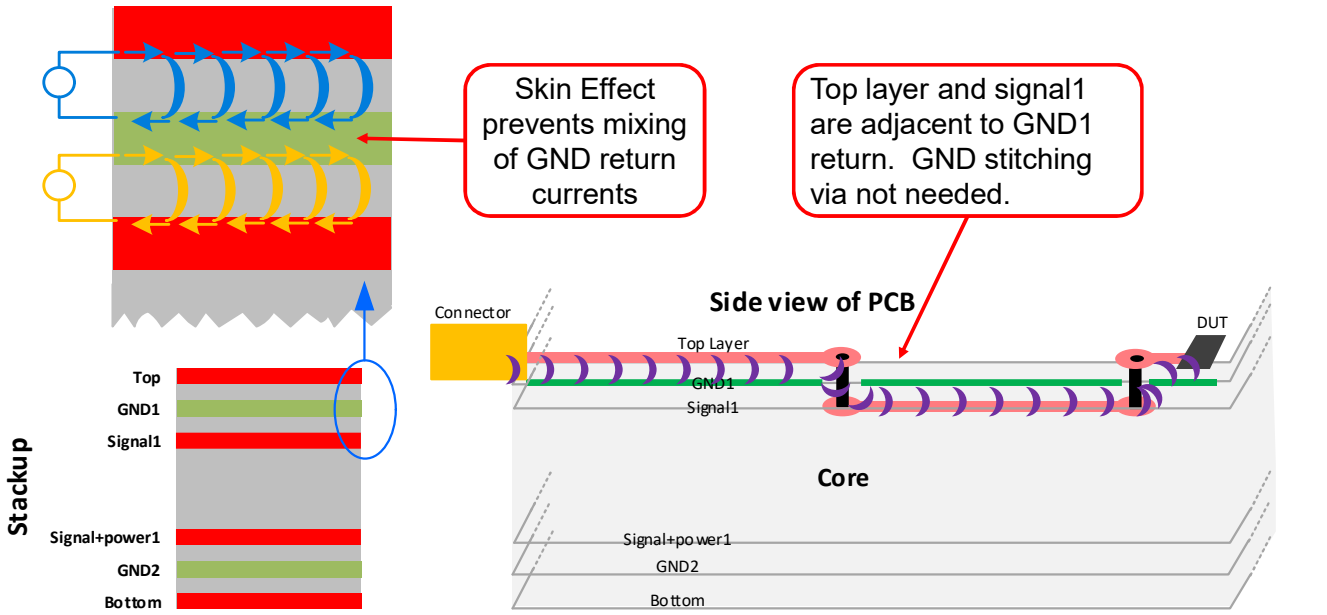
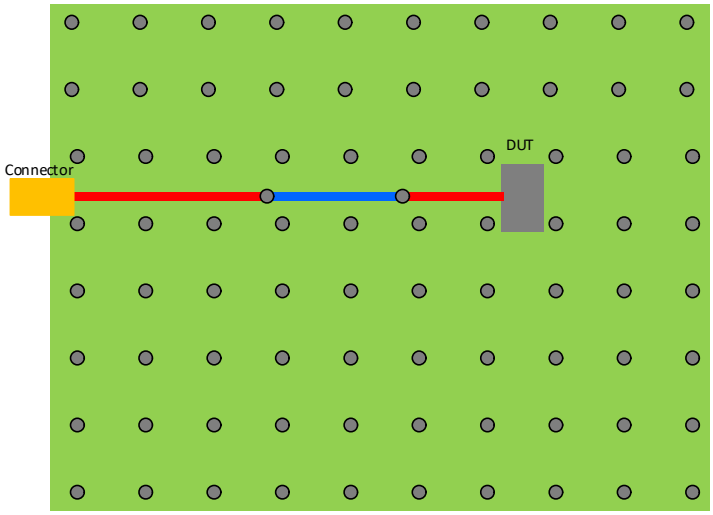
Here we have the same circuit without the stitching vias. In this case, the signal transitions from the top layer to the bottom layer without a vertical wave guide to contain the wavefront. Thus, you will see RF emissions at the via transition point. You may be thinking that your system has only a 50 MHz clock, so how can we get high frequency emissions. Don't forget the Fourier series for the square wave showed frequency content into the gigahertz, and the waveform rise time determines how much high frequency content you will have. The point of the slide is to emphasize the importance of using stitching vias to provide a continuous wave guide for signals to transition between layers.

Signals above and below GND on multi-layer board



Here's a six layer board example for via transition from the top layer to inner signal one. This type of configuration has a nice advantage in that it does not require stitching vias. [click] The ground one inner plane acts a return path for both the top layer and inner signal one. It also acts a vertical wave guide for the wavefront transitioning between layers. Note that because of the skin affect ground return currents on the top and bottom of the ground return will not mix with each other. The skin effect is a phenomenon where high frequency currents only travel on the outside of conductors.

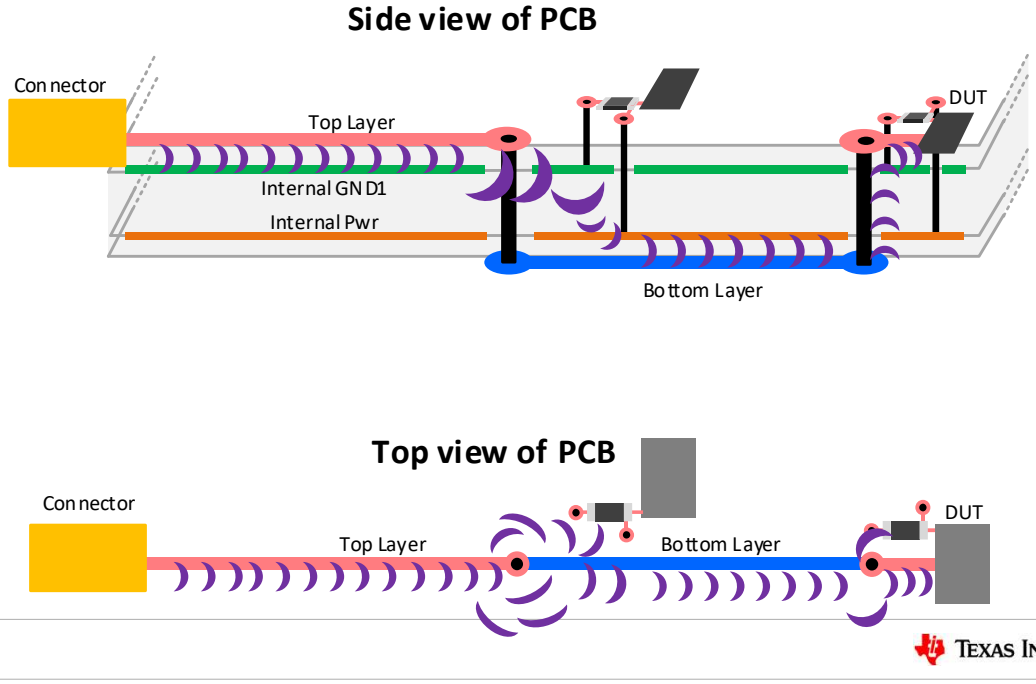
Distributed Via distributed array approach



Need to switch reference layers at first via. No near by AC path between power and GND

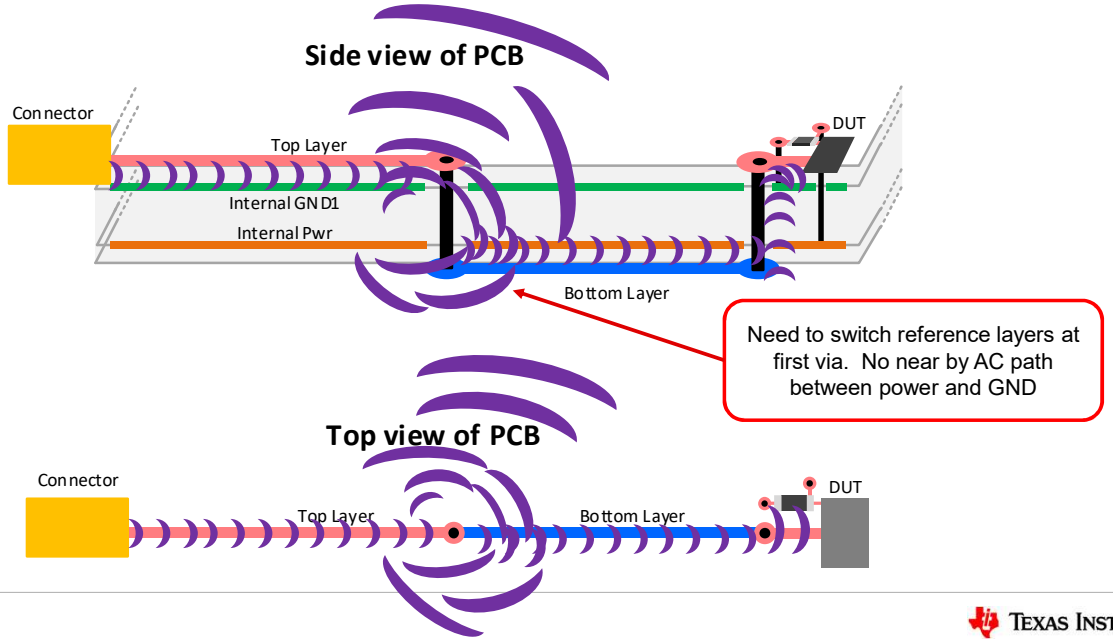
One approach to connecting internal ground planes together, and also connecting top and bottom fill to ground is to use a distributed array of stitching vias. Many printed circuit board layout software programs provide an automatic method for creating this distributed ray array. The spacing between the vias can be set to be a tenth of the wavelength for the maximum applied frequency.

Transition return layer with local stitching capacitor



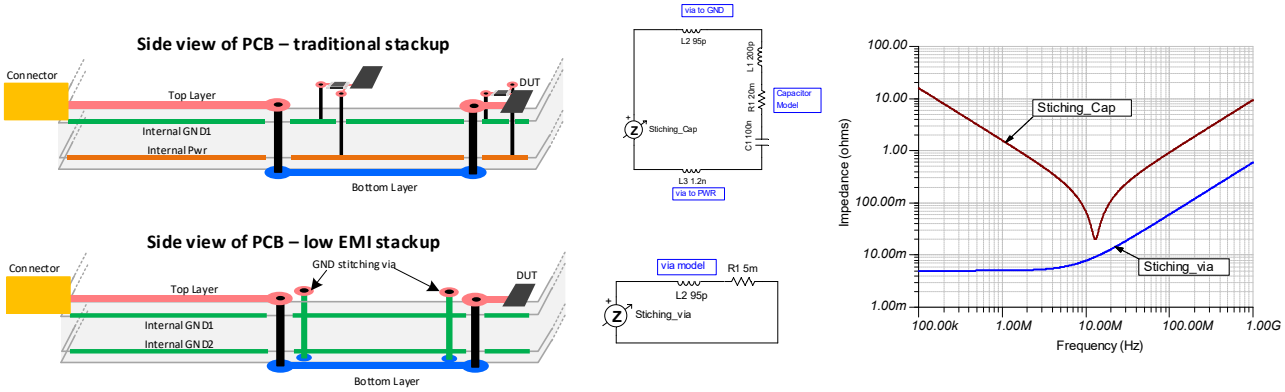
This side shows a more common PC Board stack up where there is an internal ground plane as well as an internal power plane. This is a more common stack up then the previous example with two ground planes. However this can be a little bit more challenging to it to achieve good EMI characteristics performance. **[click]** It's interesting to note that signal return current will flow in the closest adjacent plane. This is true regardless of whether the plane is a power plane or a ground plane. So in this example when the signal transitions from the top layer to the bottom layer, the return path needs to transition from internal ground1 to the internal power plane. One problem here is that you cannot have a stitching via from ground to power as you would short ground to power. Instead the return current must transition through a stitching capacitor. In many cases the stitching capacitor will simply be there decoupling capacitor closest to the via transitioning between layers. In this case you can see that the signal transitions between the top and bottom layer with minimal RF emissions.

Transition return layer without local stitching capacitor



The slide is the same design as in the previous slide, but no stitching capacitors are used. When transitioning from the top layer to the bottom layer there is no good path for the return signal to transition from internal ground to internal power. **[click]** This can lead to RF emissions when transitioning layers. This problem can be avoided through sufficient use of stitching or decoupling capacitors.

Is the stitching capacitor as good as a stitching via?

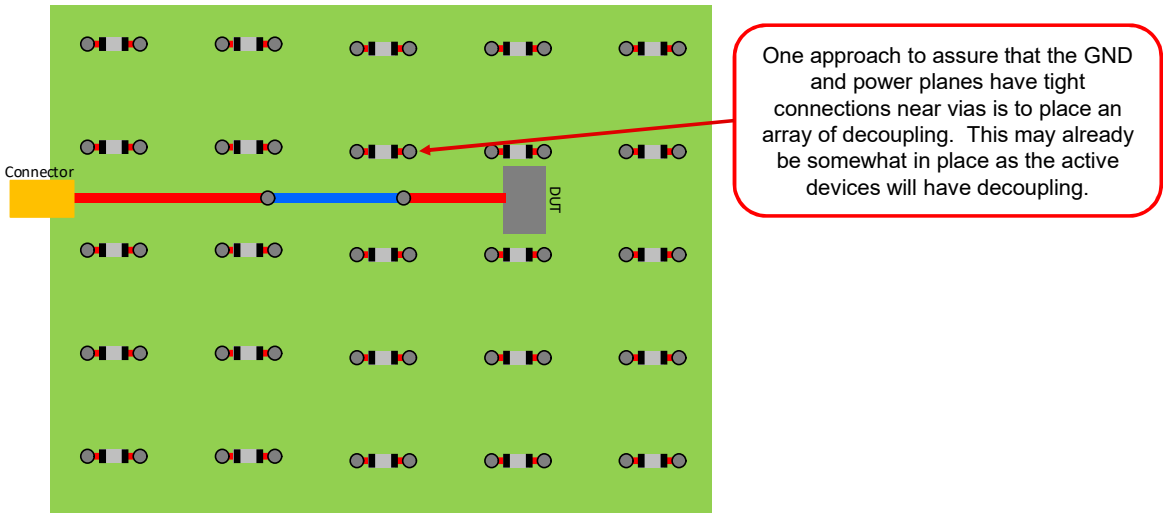


The stitching capacitor has a inductance from a via to GND, a via to PWR, and the ESL of the capacitor. The stitching via only has the inductance of the via.

One question you may ask is whether the stitching capacitors are as effective as stitching vias for connecting two planes together. The short answer is that the stitching capacitors will generally will not be as effective at high frequencies as the stitching vias. The reason is that The stitching capacitor will require two via and a capacitor. The capacitor and both via will have inductance that limit the effectiveness of this AC connection between the two planes. The stitching via will also have inductance but it will be less than the stitching capacitor and it's two associated via. Also, stitching via are small and virtually free of cost whereas the capacitor will take up PCB space and cost and complexity to the design. However, in general the

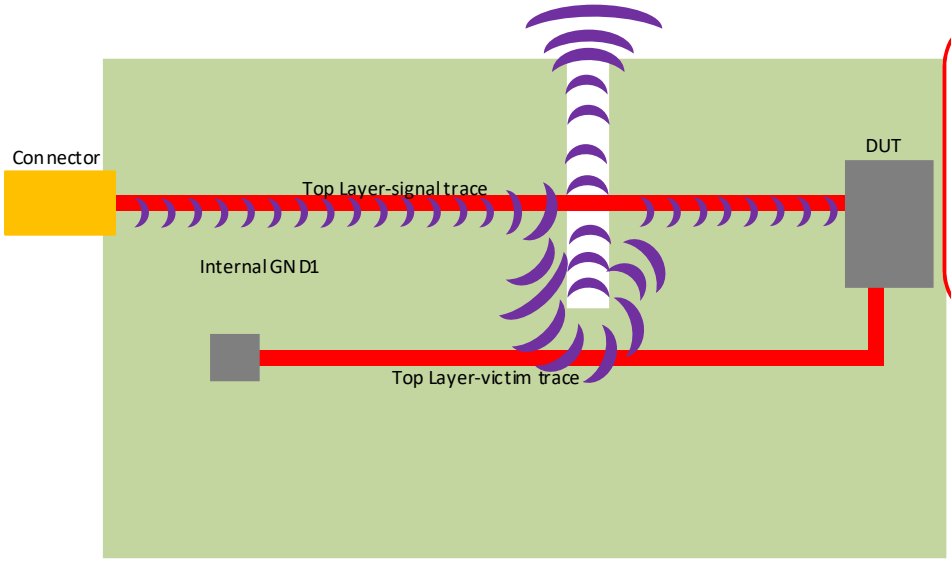
stitching capacitors are decoupling capacitors which are required in any case.

Distributed decoupling distributed array approach



Some PCB designers will used a distributed array of stitching or decoupling capacitors similar to the via array discussed previously. I think it makes more sense to strategically locate the capacitors where they are needed. We will focus on the importance of local decoupling later in this presentation.

Slot in GND plane causes RF emissions

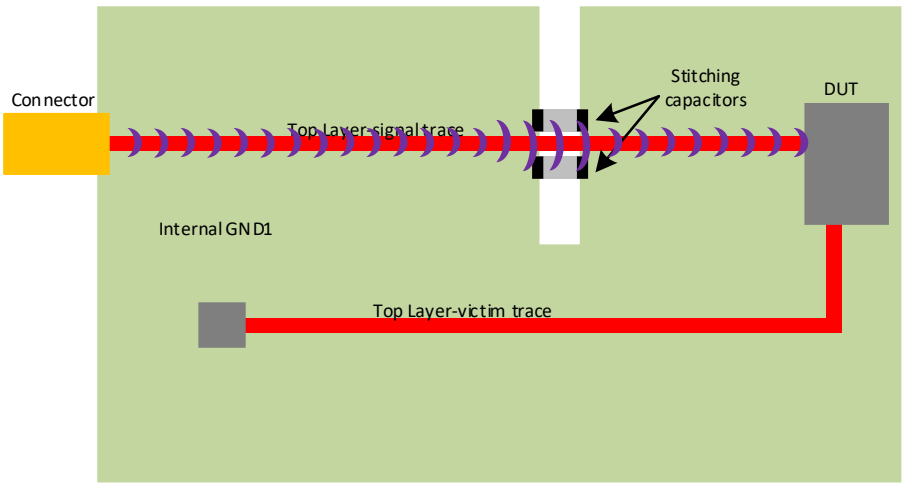


Problem with Slot in return path

- Return current needs to find a new path when the return plane has a discontinuity
- Some current travels around the slot and causes crosstalk in adjacent "victim" trace.
- Slot acts like an antenna and transmits RF off board and onto adjacent circuits.

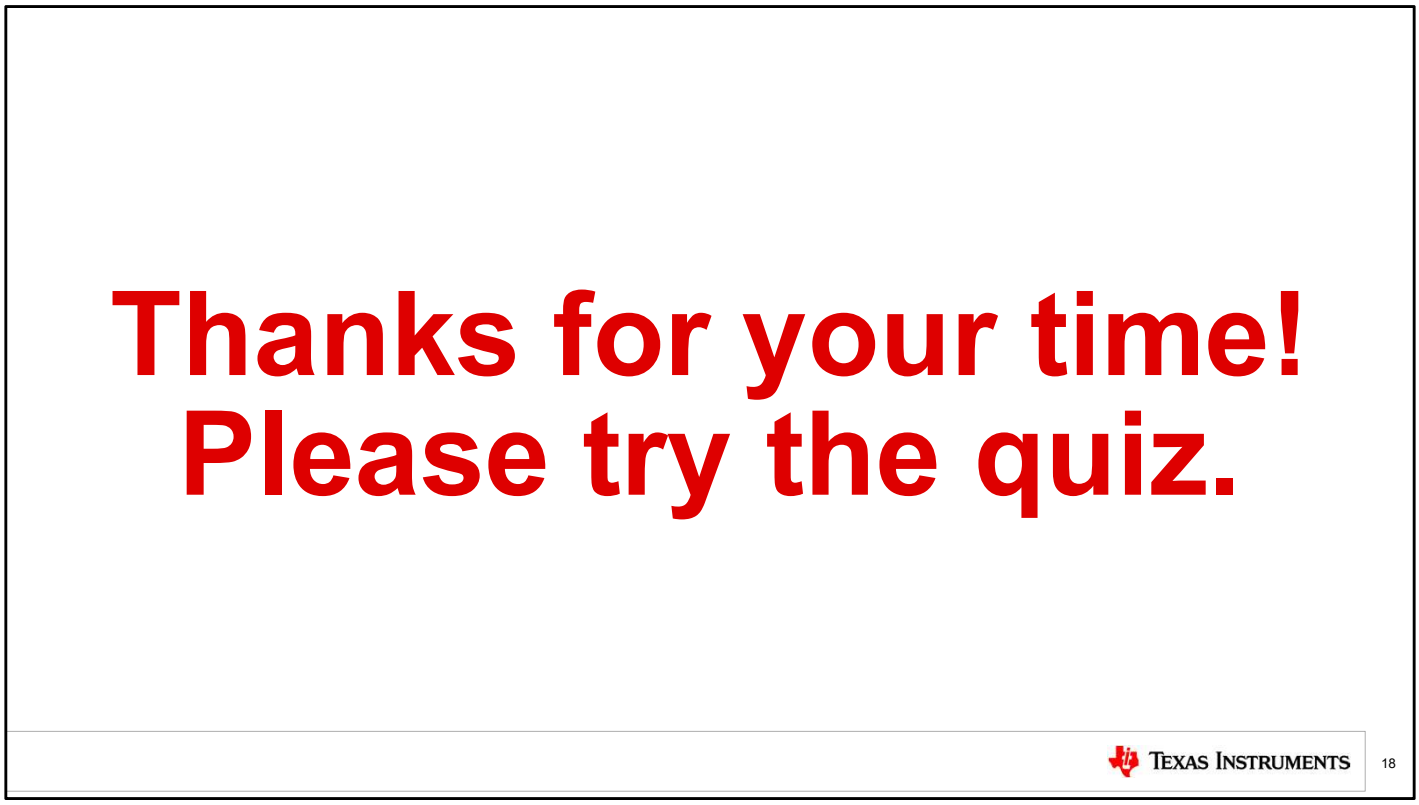
Previously we mentioned that for high frequency signals the return current will travel on the ground plane directly beneath the trace. This requires a continuous ground plane. If there's a slot or discontinuity in the return path, the ground return current will have to find a different path. [click] This creates emissions RF emissions. The example shown here will emit RF signals from the board as well as interfere with the victim trace shown. The emissions caused by slots in the PCB can be very significant and this issue is one of the leading causes for system level EMC problems.

Stitching capacitors



Fix issue associated with slot
- Best fix is to eliminate slot
- Another possible fix is to "stitch" the GND plane adjacent to the signal trace with capacitors.

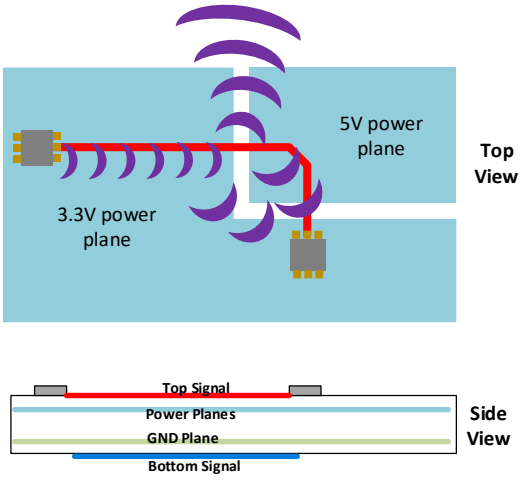
Of course, the best practice is to avoid the slot in the ground plane. In some cases this may not be practical. One way to minimize the impact of a discontinuity in the return path is to use stitching capacitors, or a ground bridge adjacent to the trace. [click] In this example, you can see that the return current transitions from the ground plane to the top layer stitching capacitors to travel over the gap in the ground plane.



That concludes this video – thank you for watching! Please try the quiz to check your understanding of this video's content.

Quiz: Introduction PCB Design for Good EMC

1. In the PCB layout below, a signal trace is driven above 5V and 3.3V power planes. Are there any potential EMI issues with this design?
   a) No issues with this PCB design. Return current will flow in the ground plane.
   b) The return current will flow in the adjacent power planes, but the power plane is split so high frequency return current will not be able to stay under the signal trace causing emissions.



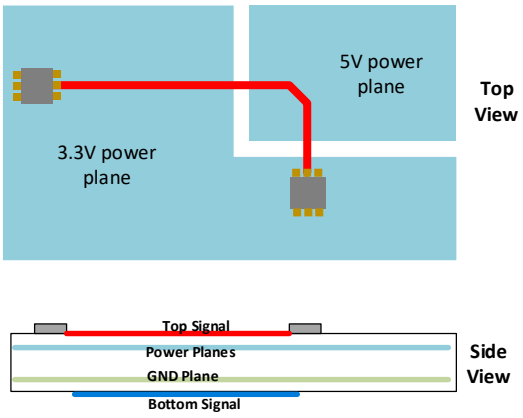
Question 1, In the PCB layout below, a signal trace is driven above 5V and 3.3V power planes. Are there any potential EMI issues with this design?

The correct answer is “b”, The return current will flow in the adjacent power planes, but the power plane is split so high frequency return current will not be able to stay under the signal trace causing emissions. [click] The animated wave front shows the return

current has no obvious path so RF emissions happen and the return current spreads across wider regions of the board.

Quiz: Introduction PCB Design for Good EMC

2. In the PCB layout below, what are some approaches that could be used to improve EMI performance?
   a) The trace routing could be adjusted so that it stays above the 3.3V power plane only and does not cross over the gap to the 5V plane.
   b) The ground plane could be moved so that it is directly adjacent to the top signal layer. Thus, the top signal will have a continuous return path.
   c) Stitching capacitors could be used to tie the two planes together from an AC perspective and bridge the return gap.
   d) All of the above.

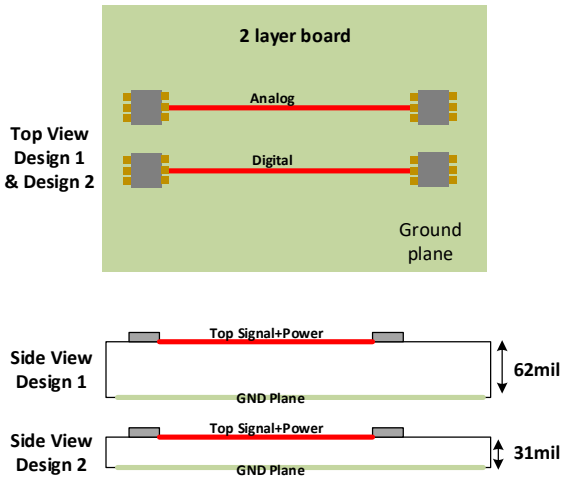


Question 2, In the PCB layout below, what are some approaches that could be used to improve EMI performance?

The correct answer is “d”, All of the above. Probably the easiest solution is to simply re-rout the trace so that the return current has a continuous path on the 3.3V plane. Another approach is to make sure that the signal trace is always adjacent to a solid GND plane, so changing the stackup so that GND is beneath the top signal will work. Finally providing a connection with a stitching capacitor between the planes is a possible approach to connect the two planes from an AC perspective.

Quiz: Introduction PCB Design for Good EMC

3. For the two circuit boards below, an analog signal trace is placed near a digital signals trace. The layout is the same for both PCB. The only difference is the PCB thickness. Which layout will minimize the interference between digital and analog?
   a) Design 1
   b) Design 2
   c) They are the same from a crosstalk perspective.



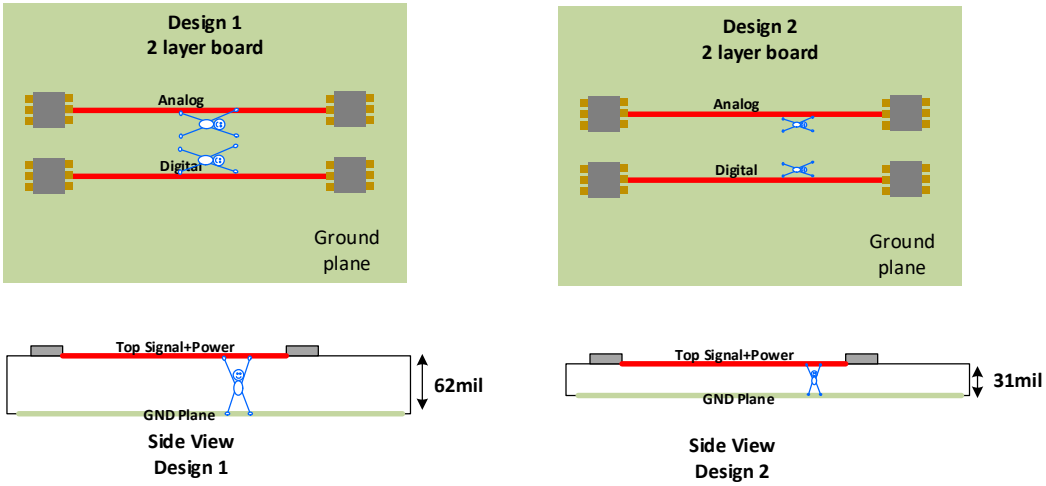
Question 3, For the two circuit boards below, an analog signal trace is placed near a digital signals trace. The layout is the same for both PCB. The only difference is the PCB thickness. Which layout will minimize the interference between digital and analog?

The correct answer is “b”, Design 2. The thick dielectric provides room for the return current to spread out. Let’s take a look at the Mr EMI analogy on the next slide.

Quiz: Introduction PCB Design for Good EMC

3. For the two circuit boards below, an analog signal trace is placed near a digital signals trace. The layout is the same for both PCB. The only difference is the PCB thickness. Which layout will minimize the interference between digital and analog?

Remember Mr. EMI!



Here you can see that Mr. EMI has more room to spread out for the thicker dialectric. Thus the fields for design 1 overlap but on design 2 the fields are much smaller and are separate from each other. This means that the crosstalk is lower for design 2 than 1.

That’s all for todays video. Thanks for watching.