Crosstalk on PCB Layouts

TI Precision Labs – ADCs

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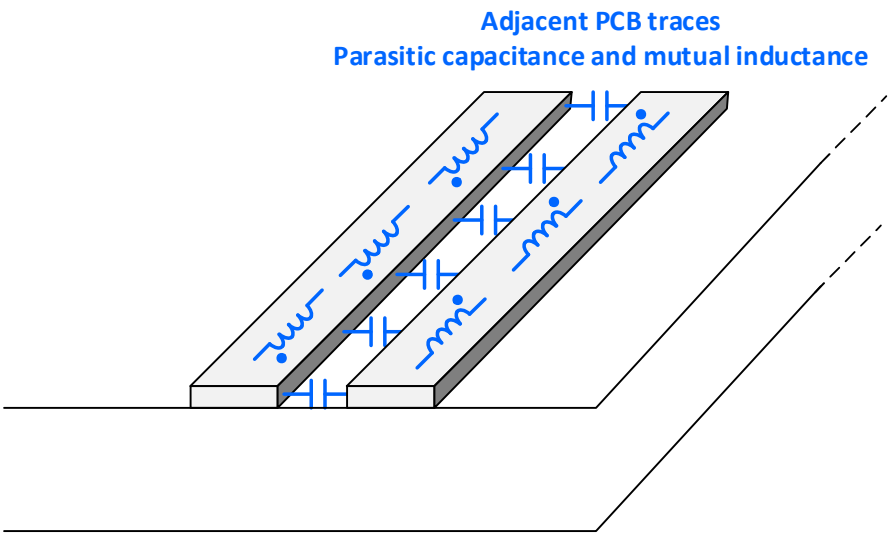
Texas Instruments

Hello, and welcome to the TI Precision Lab video covering crosstalk on PCB layouts. This is part of a larger series on PCB layout for good EMC. This series is specifically intended to cover mixed signal designs where the digital signals are less than 100 MHz and clock rise times are greater than 1 ns. This video looks at factors influencing crosstalk between two PCB traces, and provides measured results. The video also covers how ground pour can impact crosstalk. Finally, split versus solid ground plane is covered. Lets start by considering how PCB trace geometry influences the crosstalk between two traces.

Factors Impacting Crosstalk



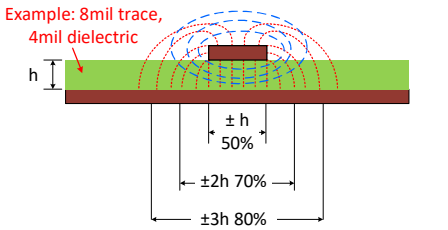
Factors impacting crosstalk

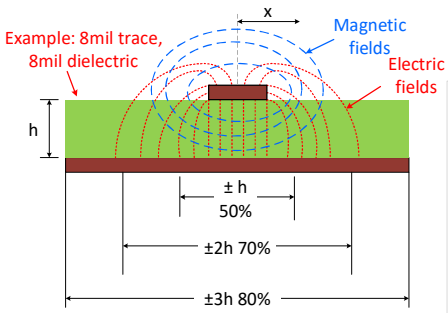
- **Trace spacing:** closer gives more inductive and capacitive coupling, so more crosstalk
- **Trace length:** longer means more coupling so more crosstalk
- **Faster rise time:** edge will induce a stronger crosstalk
- **Thicker PCB dielectric:** spreads out the fields more so more
- **Discontinuities in GND:** causes return currents to mix increasing crosstalk
- **GND Pour**: can decrease crosstalk if properly grounded, but can increases crosstalk if insufficient stitching vias are used

Crosstalk between two adjacent traces is a common problem. The parasitic capacitance between the traces will allow the signal on one trace to interfere with another. The closer two traces are the greater the parasitic capacitance and the greater the coupling. Also, longer traces will have more parasitic capacitance and will have greater coupling. Signals a fast rise time will introduce more crosstalk. A greater distance between the trace and its associated ground return path will cause the return currents to spread out further and mix together causing crosstalk. As we have seen before, discontinuities in the ground path can cause RF emissions which will lead to crosstalk. Finally, ground pour between traces can reduce crosstalk if the

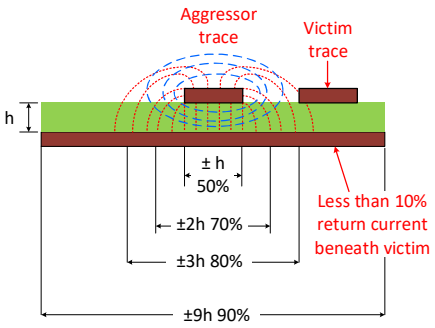
pour is properly grounded with stitching via. On the other hand, if the ground pour is not sufficiently grounded it can act as an antenna and make crosstalk worse.

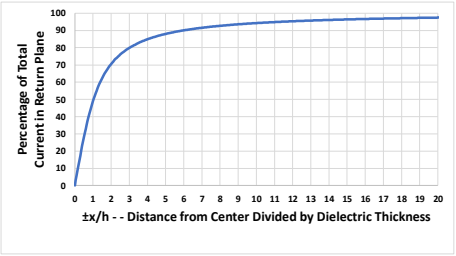
Crosstalk vs height





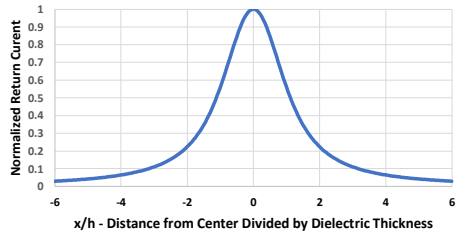
Reference: Ott, Henry W. (2009) *Electromagnetic Compatibility Engineering*





Distribution of Return Current Below a Trace

- Return current distribution is dependent on dielectric thickness
- For thin dielectrics the current will mostly be under the trace
- For thick dielectrics (e.g. 2 layer board) the current will spread further on the return plane
- A small percentage will be far from the trace (sensitive analog)
- The current follows this distribution above a few hundred kilohertz



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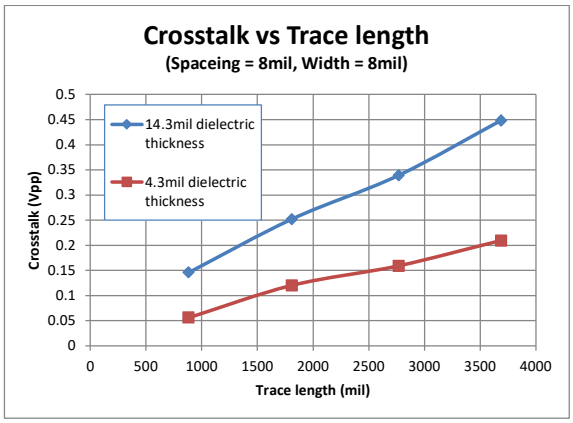
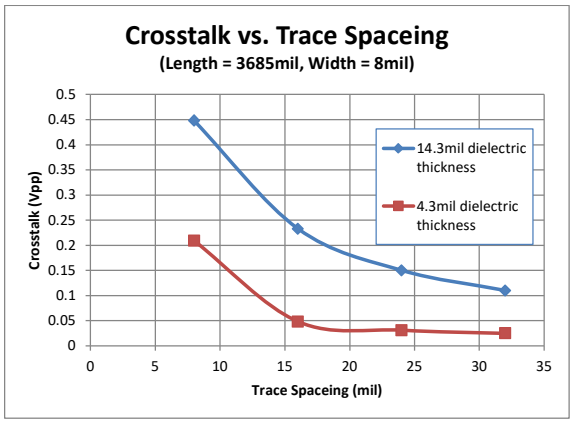
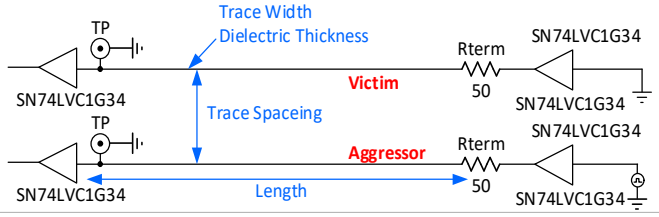
When a signal is applied to a PCB trace, a magnetic field will surround the trace and an electric field will run from the trace to the ground return plane. The return current will travel beneath the trace for frequencies above 100kHz. This slide shows how wide the return currents will spread out in the return path beneath the trace. The return current will spread out more when the height of the trace above the plane is increased. This is because increasing the height, or dielectric thickness, allows the field more room to spread out. Note that overlapping of the ground currents will cause crosstalk. The graph at the right shows the current distribution beneath a trace. You can see that the majority of the current is directly

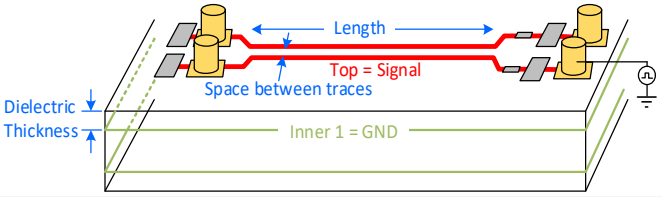
beneath the trace, but some small current density will exist far from the trace. The graph to the left is the integral of the current density plot. From this plot you can see that 70% of the current will flow under +/-2 time the height of the trace. The PCB examples show the electric field an 8 mil trace with a 4 mil thick dialectic and a 8 mil dielectric. These figures emphasize how changing the dielectric thickness, or height, causes the electric field and associated return current to spread out. Finally, the PCB example in the center shows how crosstalk can occur when the field from one trace overlaps the other trace. Based on the current distribution, you may adjust your trace spacing minimize overlap of return currents. In reality though, the crosstalk is a function of both trace length as well as the spacing between the traces, so trace separation is more important for long parallel traces than it is for short traces.

Measured Crosstalk vs Length, Spacing, & Thickness









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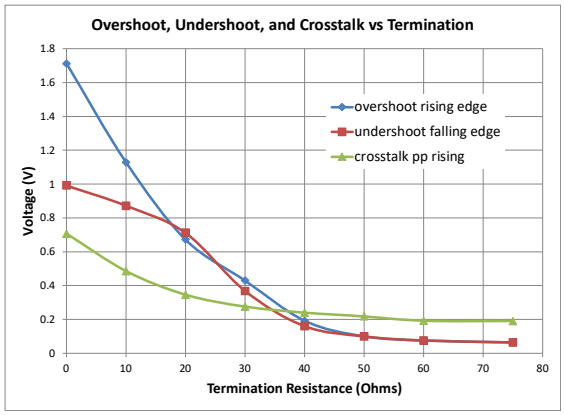
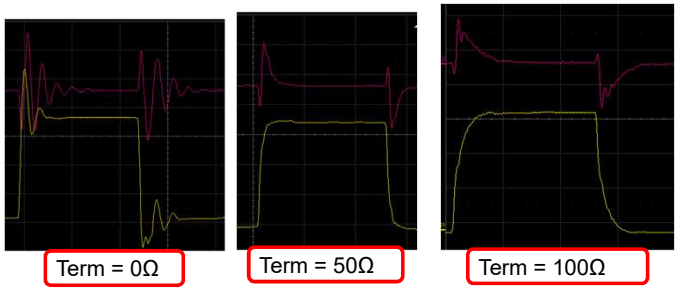
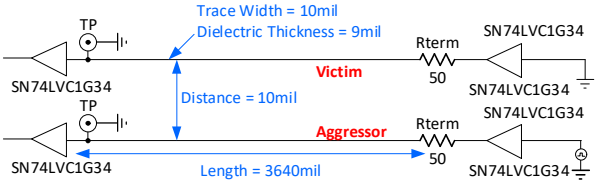
This slide shows measured crosstalk results for different trace spacing, length, and dielectric thinness. For the test a 3.3V 10MHz square wave with a 2ns rise time was applied to the aggressor trace, and the victim trace was driven by a logic low. The signal is routed on the top layer and the ground plane is directly adjacent to the signal layer. The two dielectric thicknesses used are the minimum and maximum prepreg thicknesses available for most PCB processes. The graph on the left shows how increasing the trace length will increase crosstalk. Also, notice that decreasing the dielectric thickness significantly reduced crosstalk. The crosstalk is 0.45Vpp for the 3700mil long trace with the 14mil dielectric thickness, but only 0.2Vpp for the 4.3mil

dielectric. The graph on the right shows how crosstalk is impacted by trace spacing. The tightest spacing used in this experiment is 8mil spacing between two 8mil traces. This is the minimum trace spacing for many low cost PCB process. Tighter spacing can be achieved but at higher cost. For 8 mil spacing on a 3700mil long trace, the crosstalk is about 0.45V for thick dielectric and 0.2V for thin dielectric. Doubling the spacing significantly decreases crosstalk. In fact for the thin dielectric, increasing the spacing further seems to have little to no impact on crosstalk. The crosstalk for a thicker dielectric continues to decrease all the way to a spacing of 32mil.

Measured: Overshoot vs Termination





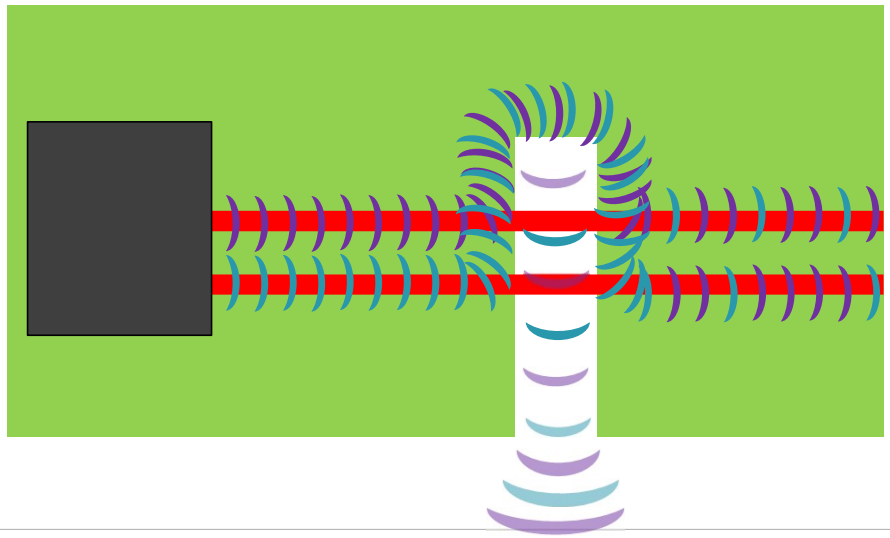


Overshoot and Crosstalk vs Termination

- The input signal is 3.3Vpp
- Overshoot ranges from 1.7V to 0.05V depending on the termination
- Crosstalk ranges from 0.7V to 0.2V
- Results for specific geometry: length = 3640mil, Space =10mil, Dielectric thickness = 9mil, FR4 Dielectric
- Results will be different for different geometry

This slide was previously covered in the impedance matching section. We review it here because a impedance mismatches can greatly impact crosstalk. The crosstalk ranges from 0.2Vpp to 0.7Vpp depending on the termination used. For termination impedances less than 20 ohms there is a lot of overshoot which translates to crosstalk.

Slot causes return currents to mix: Crosstalk



- Slot in Return Path Causes Return Currents to mix
- Slot also causes RF emissions

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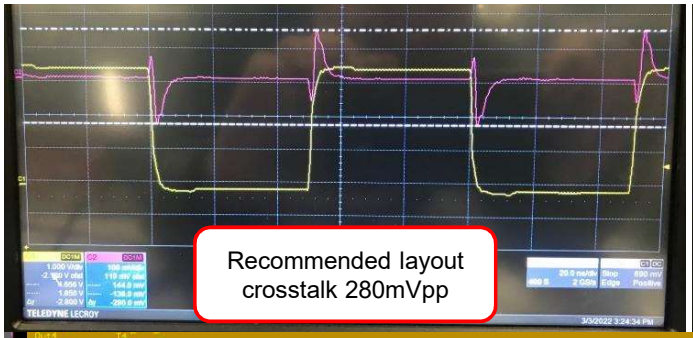
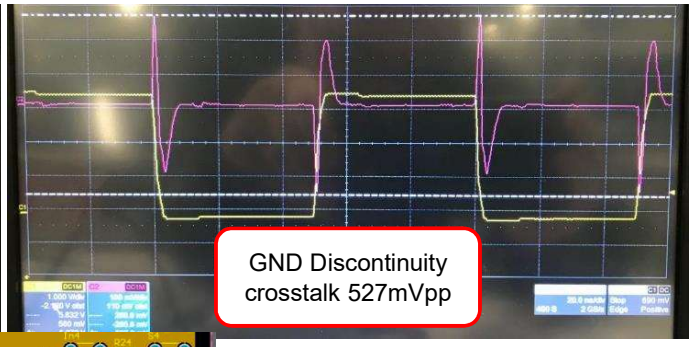
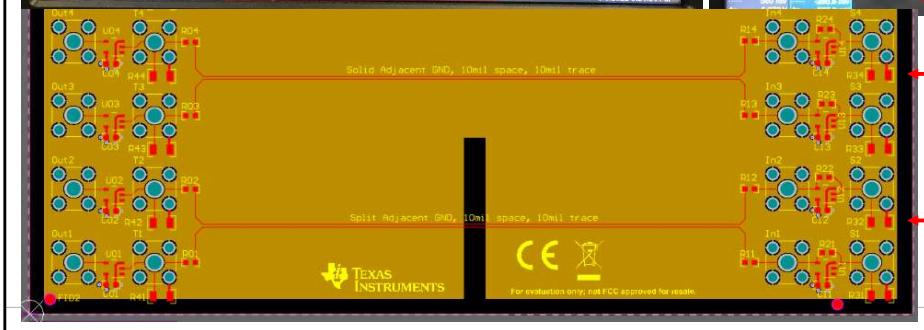
A slot or discontinuity in the return path is one of the most common reasons for crosstalk. In this picture you can see that the return currents will travel beneath the individual traces. These currents are separated enough from each other to minimize crosstalk. However when the signals pass over the ground return slot, they will mix together causing crosstalk and RF emissions. Let's look at some measured results!

Crosstalk with and without GND discontinuity







Recommended layout: 10mil traces, 10mil space, solid adjacent GND, 9mil diametric thickness

GND Discontinuity: 10mil traces, 10mil space, slot adjacent GND, 9mil diametric thickness

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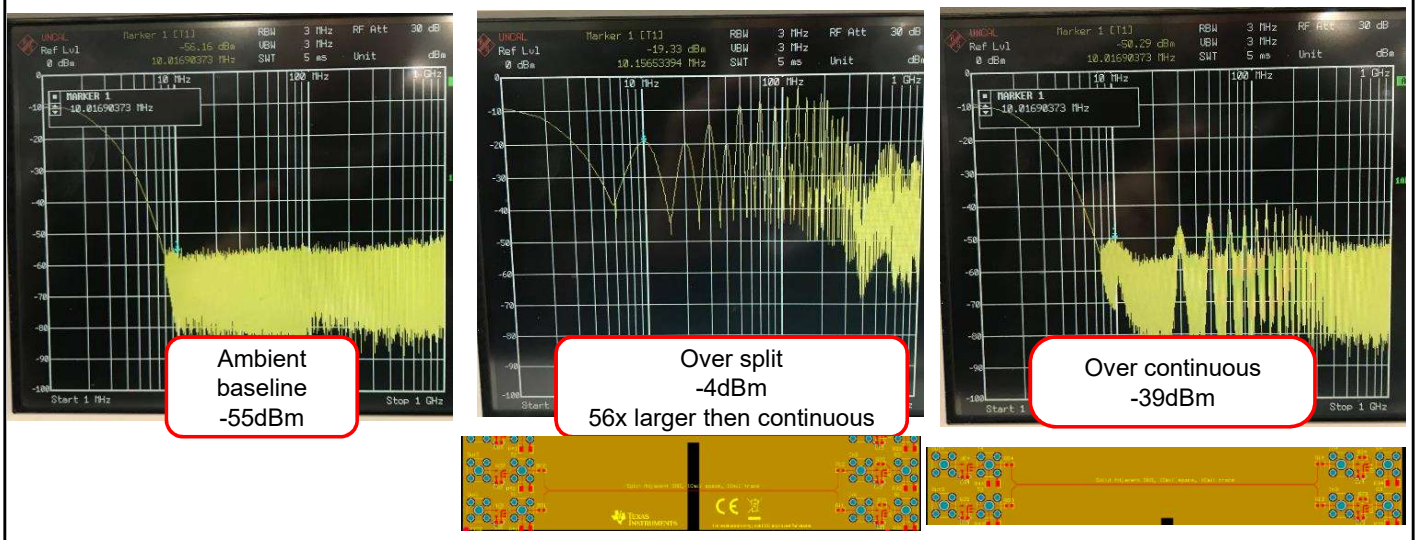
This slide shows two different experimental results. For the first experiment a 10MHz signal is driven on a line adjacent to line driven by ground. In this case both lines are above a solid ground return path. The second experiment is the same as the first experiment except that the signals travel over a discontinuity in the ground return path. The crosstalk with the solid return path was 280mVpp whereas the crosstalk with the discontinuity in ground was 527mVpp. Thus, the poor grounding almost doubled the crosstalk. Let's look at hoe RF emissions are impacted.

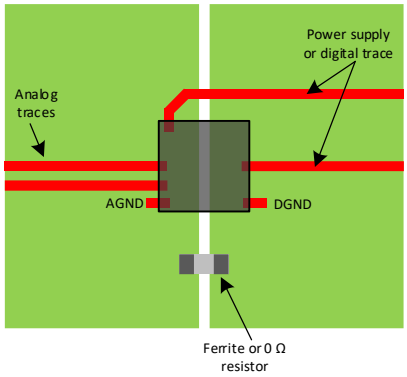
Split in GND vs Continuous GND



This slide shows the ambient noise floor, the RF emissions over the ground discontinuity, and the RF emissions over a continuous ground. The RF emissions for the circuit with a ground discontinuity were 56 times larger than for a continuous ground plane. This measurement helps illustrate why discontinuities in the ground return path are a leading cause of EMI issues.

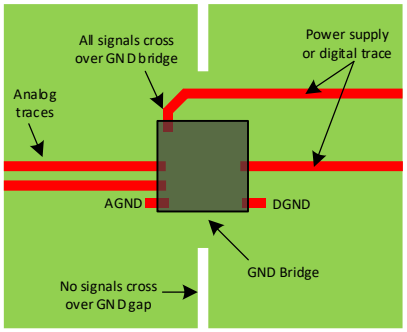
Split plane?

Worst Grounding Design Choice



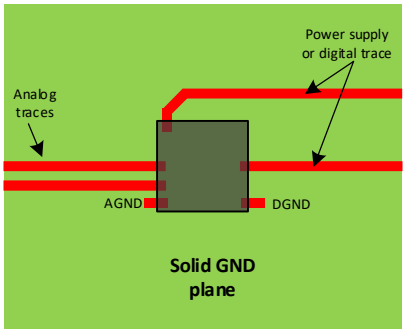
Digital communications errors likely. Significant RF emissions. Ferrite is worse than zero ohm.

Better Grounding Design Choice



Minimal issues as long as traces cross over bridge. Slots may act as antenna. Separate planes form dipole antenna.

Best Grounding Design Choice

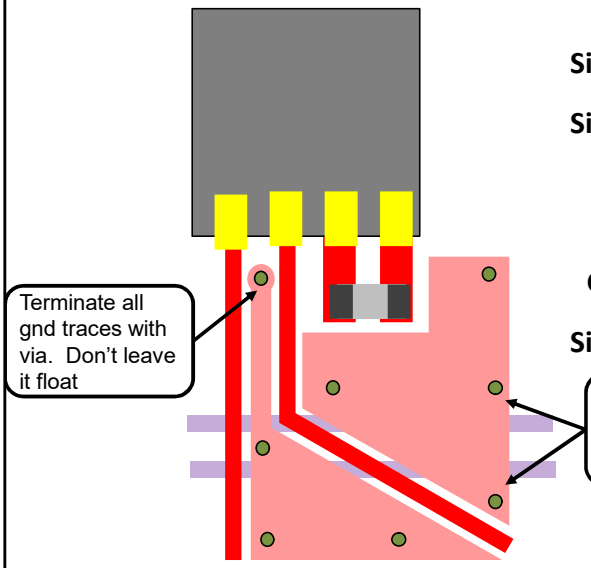


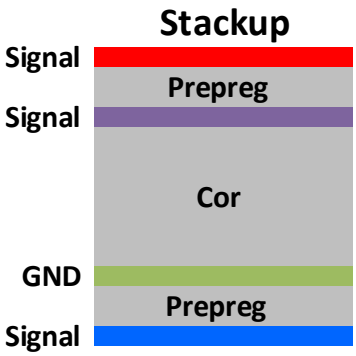
Best performance for both analog and digital.

This slide coverers another common PCB layout error. Some engineers will create a separate analog and digital ground plane in order to avoid corrupting the sensitive analog with crosstalk noise from the communications digital. Frequently, the two GND planes are connected together at one point near the ADC with a zero ohm resistor, inductor, or a ferrite. This approach was widely promoted as a good idea 30 years ago. It turns out that this is generally not a good approach. Signals that traverse the split will have large RF emissions and frequently have poor analog performance. Using an inductor or ferrite can generate large transient voltages when switching currents pass from digital to analog ground and this can cause data

errors and may even damage the device. For engineers who really want to use a split a better approach is the use a ground bridge as shown in the center drawing. The ground bridge needs to be wide enough to allow any digital traces to pass over the bridge and not over a split in the ground. The best grounding choice is to simply use a solid plane and to make sure to keep the physical distance of the digital and other noisy signals away from the analog. The process of physically segmenting different signal types to different sections of the PCB is called floor planning, and a good floor plan is a much better approach to minimize coupling of digital into analog then a split plane.

To pour or not to pour … That is the question





GND pour acts as GND return for adjacent traces. No plane in this example stackup.

Ground pour considerations:

- If signal layer is adjacent to GND plane pour may not be needed.
- Pour may be helpful for 1 or 2 layer boards to provide good GND return when a plane is not available
- Never pour a copper without vias to GND
- Place vias every 1/10 wavelength of maximum expected frequency.
- Estimate the maximum frequency for a square wave using the rise time $fc = 1/(\pi t_r)$
- Lack of GND via can translate pour area into antenna

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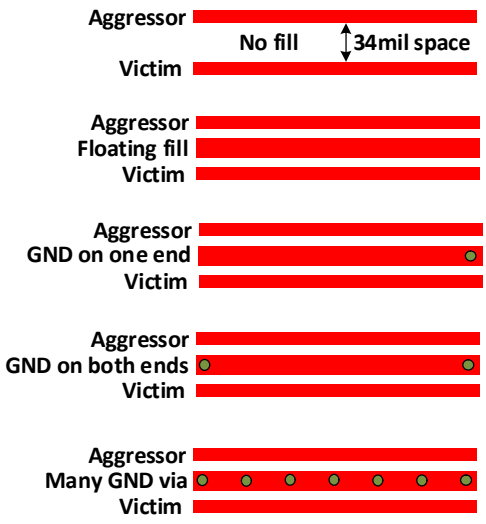
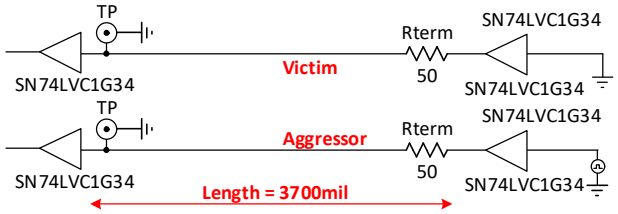
A common practice used to minimize coupling between traces is to use ground pour between the traces. The idea is that the signals will couple into the adjacent ground pour rather than into each other. Ground pour can be effective if it is well tied to other ground planes with vias, but it can make things worse if it is not. In the picture shown the ground pour is connected to the ground plane with many vias. Ideally, the spaceing between vias will be at most one tenth wavelength, and all edges of a pour should have a via. Any long ground fingers need vias on their end. To find the maximum frequency for square waves applied, use the RF bandwidth equation where the frequency is calculated as $1/_{/(\pi t_r)}$. Using insufficient vias or having

floating copper can make the pour act like an antenna which can actually increase crosstalk and cause RF emissions.

Crosstalk with and without GND pour



- Pour with vias on both ends had minimal crosstalk.
- Pour with via on one end showed large crosstalk and a resonance.
- Floating copper had large crosstalk.



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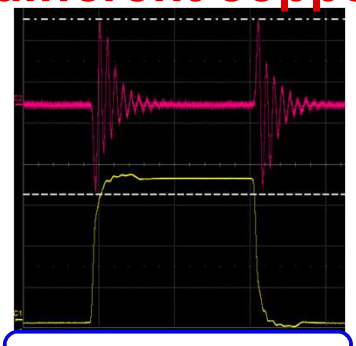
To prove the importance of using stitching vias on ground poor, I did multiple experiments. For each experiment the circuit and layout was the same except for the different cooper fills were used. First, the fill was eliminated and the space between the traces was 34 mils, and the length was 3700mil. For the no fill configuration 40mVpp of crosstalk was measured. Adding floating copper between the traces made the crosstalk increase to 60mVpp. Grounding the copper pour on one end made the crosstalk increase to 86mVpp and created a resonant ringing effect. Using grounding both ends of the pour with stitching vias showed good performance and the crosstalk was negligible. The rule of thumb for copper pour is that it

should have stitching vias in tenth wavelength intervals, so grounding both ends may not always work well. If you plan on using ground pours, I would be careful to use sufficient via so that you don't end up creating an inadvertent antenna.

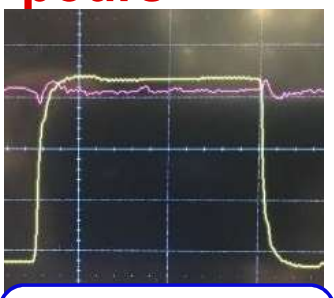
Measured: Crosstalk for different copper pours

No pour
Crosstalk ≈ 41mVpp

Floating pour
Crosstalk ≈ 60mVpp

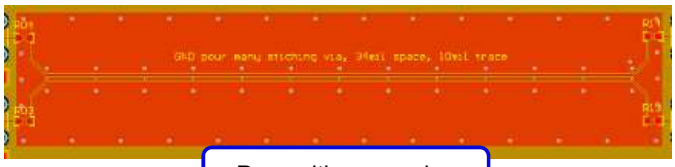


Pour grounded at one end
Crosstalk ≈ 85mVpp



Pour with minimal GND via and pour with many via looks the same
Crosstalk ≈ 4mVpp

No pour



Pour with many vias

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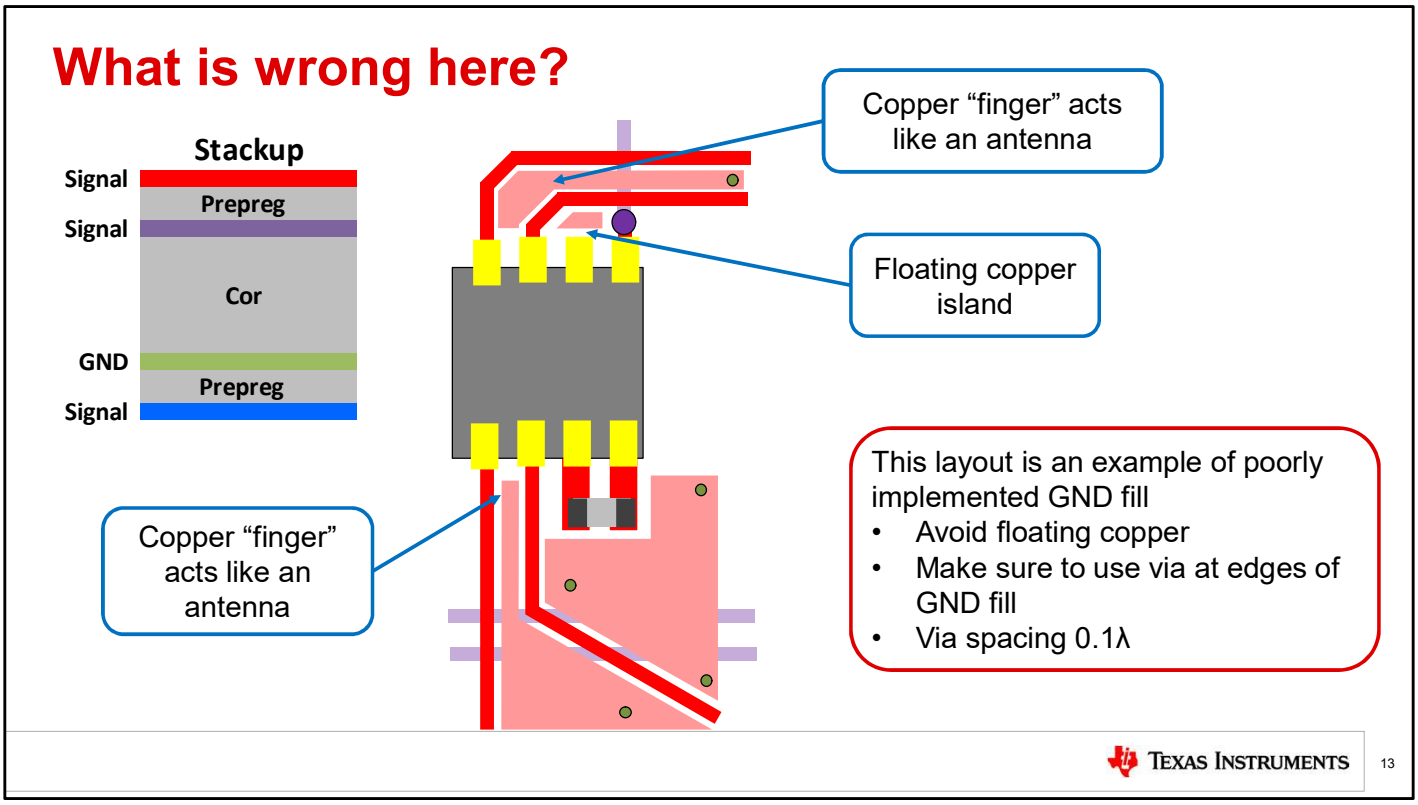
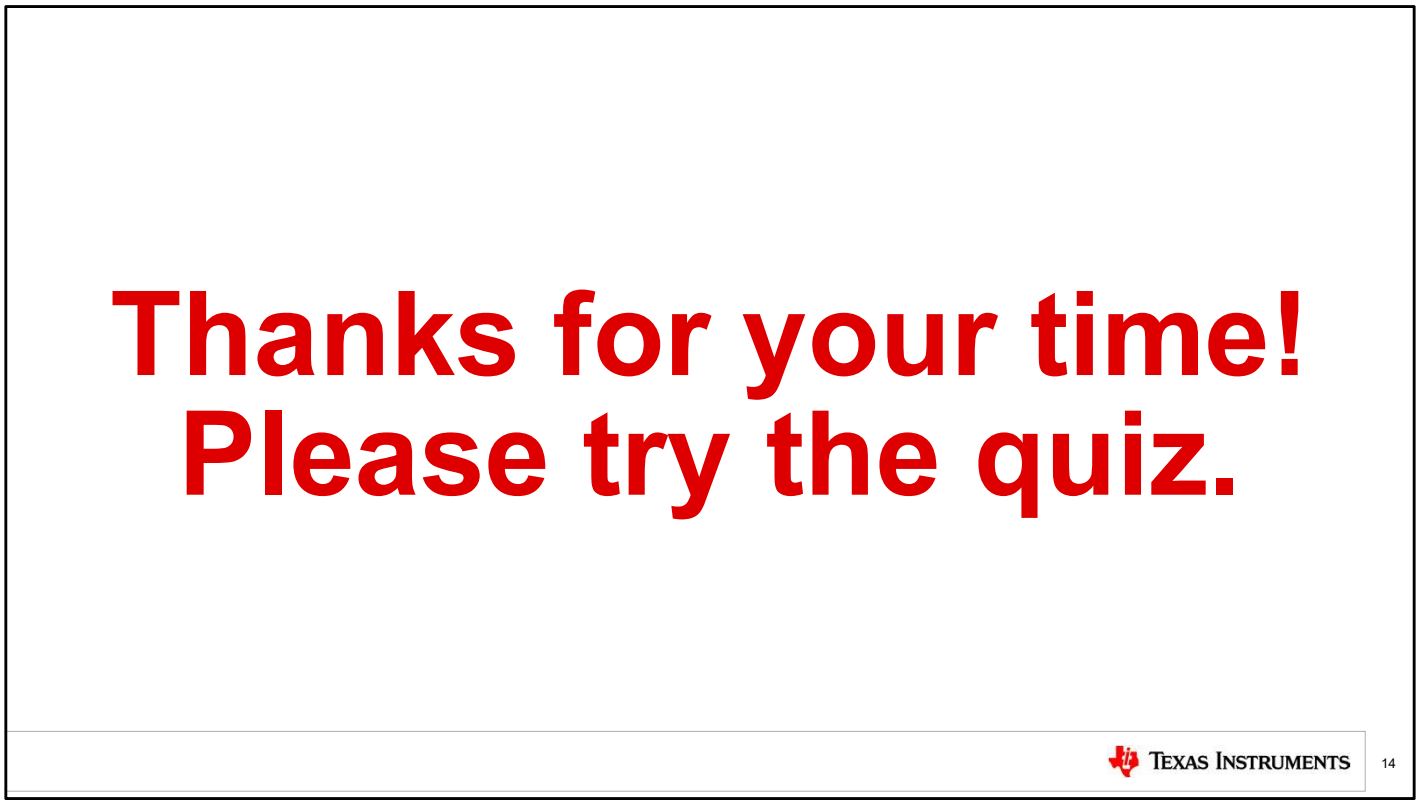
This slide summarizes the measured results for the ground fil experiments discussed on the previous slide. The layouts at the bottom show the example with no pour and a ground pour with many vias. The same circuitry and PCB layout geometry are used for each experiment except the pour is changed. The oscilloscope waveforms show the 3.3V 10MHz square wave applied to the aggressor trace in yellow and the crosstalk is shown on the red trace. The range on the red trace is 20mV/division for all measurements. Moving from left to right you can see that the circuit without pour has about 41mVpp of noise whereas the circuit with floating pour has significantly worse crosstalk at 60mVpp. When the fill is only grounded on

one end it acts as an antenna and has crosstalk of 85mVpp with a resonant oscillations. When a ground pour is used with two vias on the ends of the fill between the trace you get nearly zero crosstalk. Adding many via to the ground fill doesn't have a significant impact on crosstalk and it looks very similar to the case with minimal vias. Please do not conclude based on this experiment that you should use minimal ground vias. The recommendation is to space the via in tenth wavelength increments for the maximum frequency content expected on the board. Rembert, the maximum frequency is set by the rise time of your digital signal and is calculated as $1/_{/(\pi t_r)}$.



This slide shows a similar layout to what was previously shown for using copper pour. However, this example has a few issues that will cause crosstalk and RF emissions. Can you find them? [click] One issue is that some of the copper fill does not have a via at the end of the trace. These copper fingers will act as an antenna for RF emissions and will increase the crosstalk. Another issue is that there is a floating island of copper. A key point here is that it would be much better to avoid using the copper pour than to have the improperly grounded pour shown here.



That concludes this video – thank you for watching! Please try the quiz to check your understanding of this video's content.

Quiz: Introduction PCB Design for Good EMC

1. Which factor does ***not*** impact the crosstalk between two PCB traces?
   a) Rise time of applied signal.
   b) Trace copper thickness
   c) Trace length.
   d) Trace separation.
   e) PCB dielectric thickness.

2. (True/False) Ground pour can actually make crosstalk worse if it is not done correctly.
   a) True
   b) False

Question 1, Which factor does ***not*** impact the crosstalk between two PCB traces?

The correct answer is “b”, Trace copper thickness. Signal rise time, trace length, trace separation, and PCB dielectric thickness all significantly impact crosstalk.

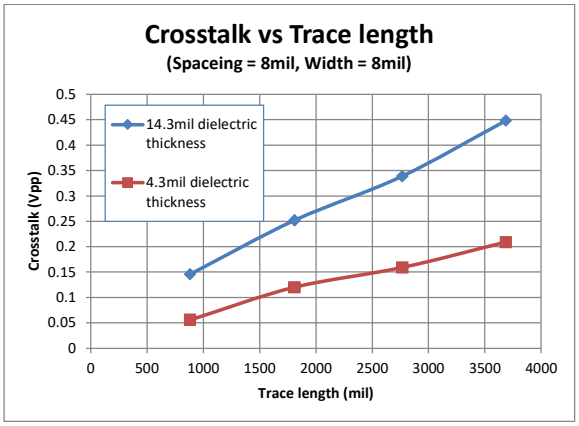
Question 2, true or false. Ground pour can actually make crosstalk worse if it is not done correctly.

The correct answer is a, true. If the pour is not well connected to ground with many via it can actually cause worse crosstalk and potential

resonances. The via should be at all ends of the pour and should be ideally be spaced in a maximum of 1/10 th wavelength increments.

Quiz: Introduction PCB Design for Good EMC

3. Using the graph below, what peak-to-peak crosstalk would be seen on a 3000 mil trace, with a 9 mil dielectric thickness. For this example trace spacing is 8mil, and trace width is 8mil.
   a) 0.15Vpp
   b) 0.25Vpp
   c) 0.35Vpp
   d) 0.45Vpp



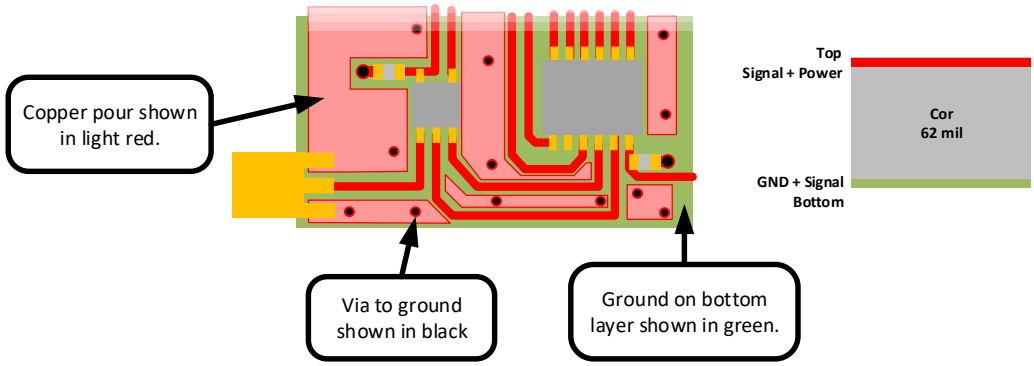
Question 3, Using the graph below, what peak-to-peak crosstalk would be seen on a 3000 mil trace, with a 9 mil dielectric thickness. For this example trace spacing is 8mil, and trace width is 8mil.

The correct answer is “b”, 0.25Vpp. In this case you have to interpolate between the two curves. At a 3000 mil trace length the 4.3mil dielectric had a crosstalk of about 0.17Vpp and the 14.3mil dielectric had a crosstalk of 0.36Vpp. Interpolating between the two gives approximately 0.25Vpp for a 9mil dielectric. Of

course, this is just an estimate but it does give a general idea of what kind of crosstalk to expect.

Quiz: Introduction PCB Design for Good EMC

4. What is a potential issue with the PCB layout below?
   a) The ground plane is separated from power by a large distance
   b) The copper pour has floating sections that will act as an antenna
   c) All of the above.
   d) None of the above.



Question 4, What is a potential issue with the PCB layout below?

The correct answer is “c”, All of the above. One general issue with all two layer boards is that the top and bottom layer are separated by a large distance. This will increase crosstalk. Of course, in some cases cost requirements necessitate the use of a two layer board and you have to tolerate the degraded performance. Another issue is that the copper pour is not optimally grounded. One trace in

particular has a finger that is grounded on one end and will act as an antenna.

That’s all for todays video. Thanks for watching.