# Simplifying board layout for ethernet applications using retimers and redrivers

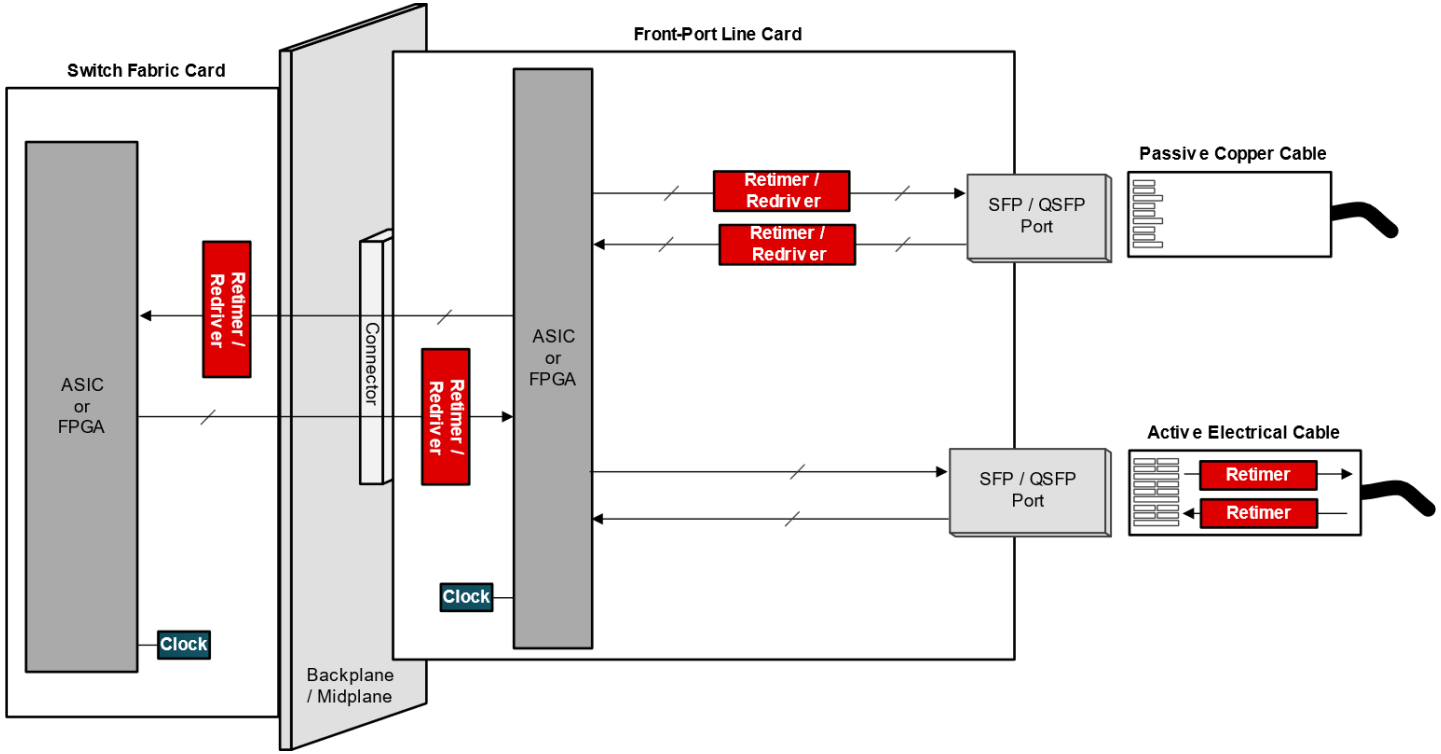
## TI Precision Labs – Ethernet

**Presented by Lucas Wolter**

**Prepared by Lucas Wolter**

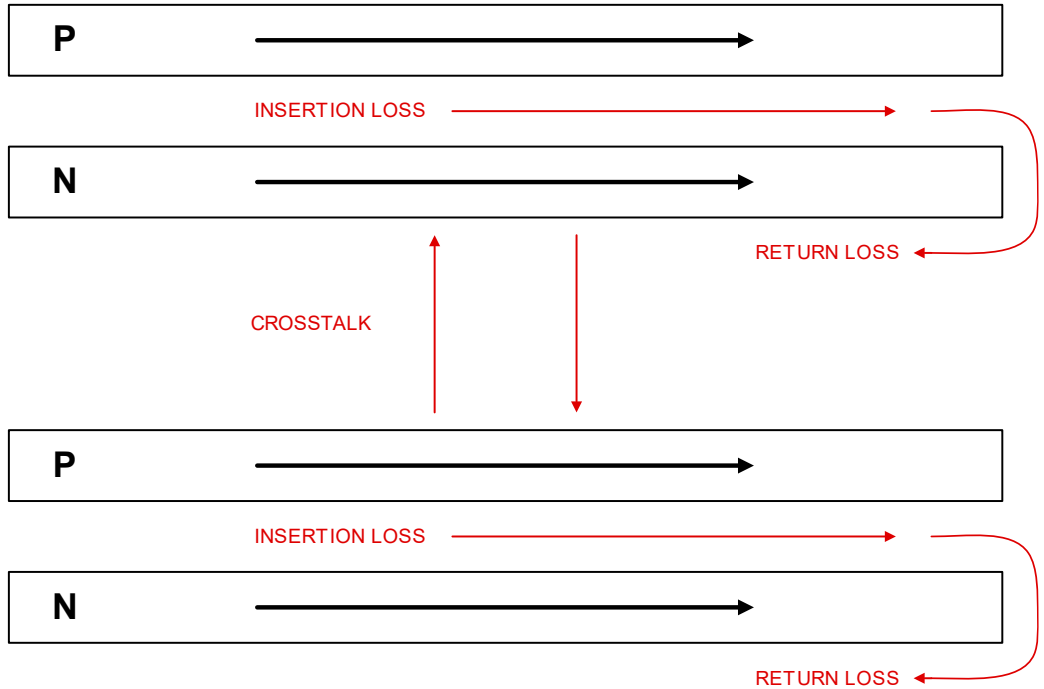
# Introduction

- Optimized board layout is critical to maintain good signal integrity at high transmission speeds.
  - TI offers ethernet retimers/redrivers that support data rates of 10 Gbps, 25-28 Gbps, and 56 Gbps (PAM-4 signaling).



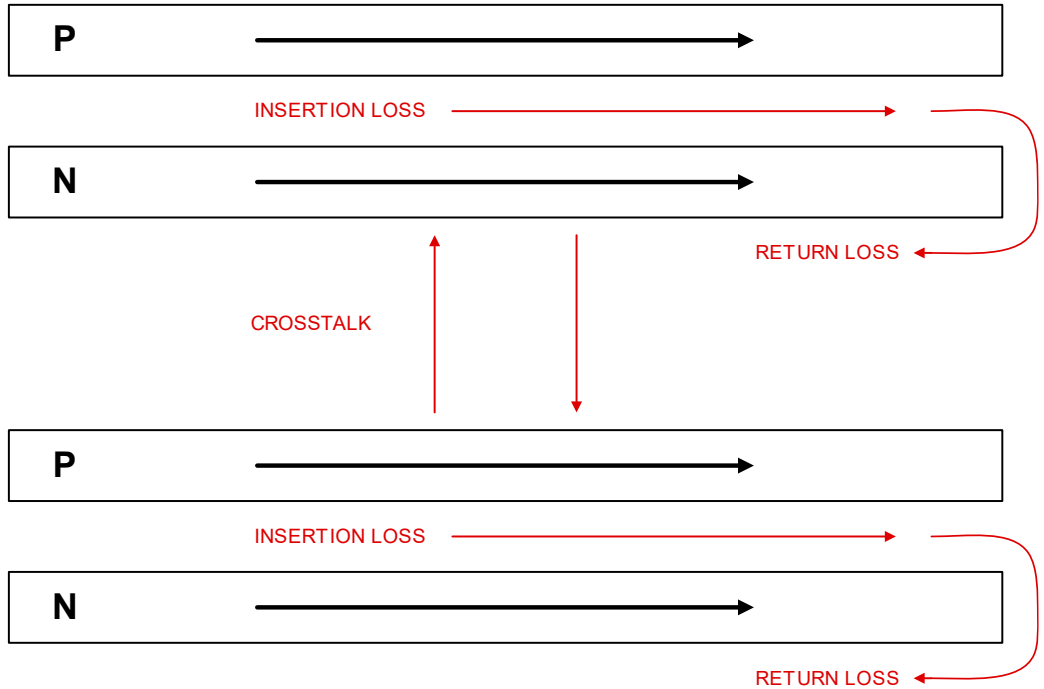
# High-speed layout considerations

- 3 measurements to consider on high-speed traces:
  - Insertion loss
  - Return loss (reflections)
  - Crosstalk



# High-speed layout considerations

- 3 measurements to consider on high-speed traces:
  - Insertion loss ← PCB material frequency versus loss properties
  - Return loss (reflections) ← Characteristic trace impedance
  - Crosstalk ← Channel design considerations



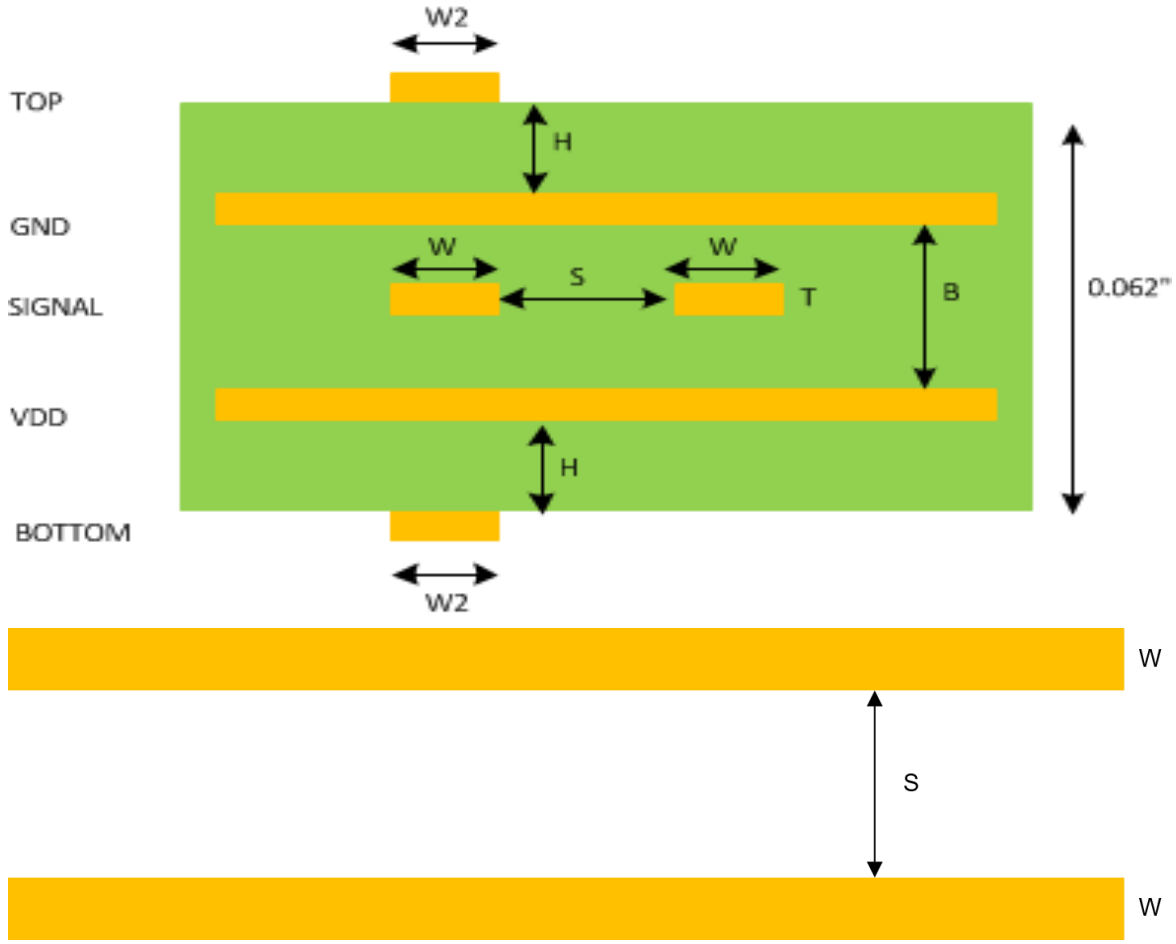
# PCB material selection

- Materials with lower dielectric constants ($\varepsilon_r$) and loss tangents ($D_f$) are typically better suited for high speed layout.
- On 28 GBd device EVMs, TI used Megtron 6.  We have observed good high speed performance with this material selection.

| Material Name | $\varepsilon_r$ | $D_f$ | 1” IL at 8 GHz | 1” IL at 16 GHz |
|---|---|---|---|---|
| Megtron 6 | 3.4 | 0.002 | 0.189 | 0.336 |
| Roger | 3.48 | 0.0037 | 0.251 | 0.411 |
| GETEK | 4.1 | 0.011 | 0.548 | 1.017 |
| Nelco 4000-6 | 4.0 | 0.012 | 0.578 | 1.078 |
| FR4 | 4.4 | 0.014 | 0.686 | 1.289 |

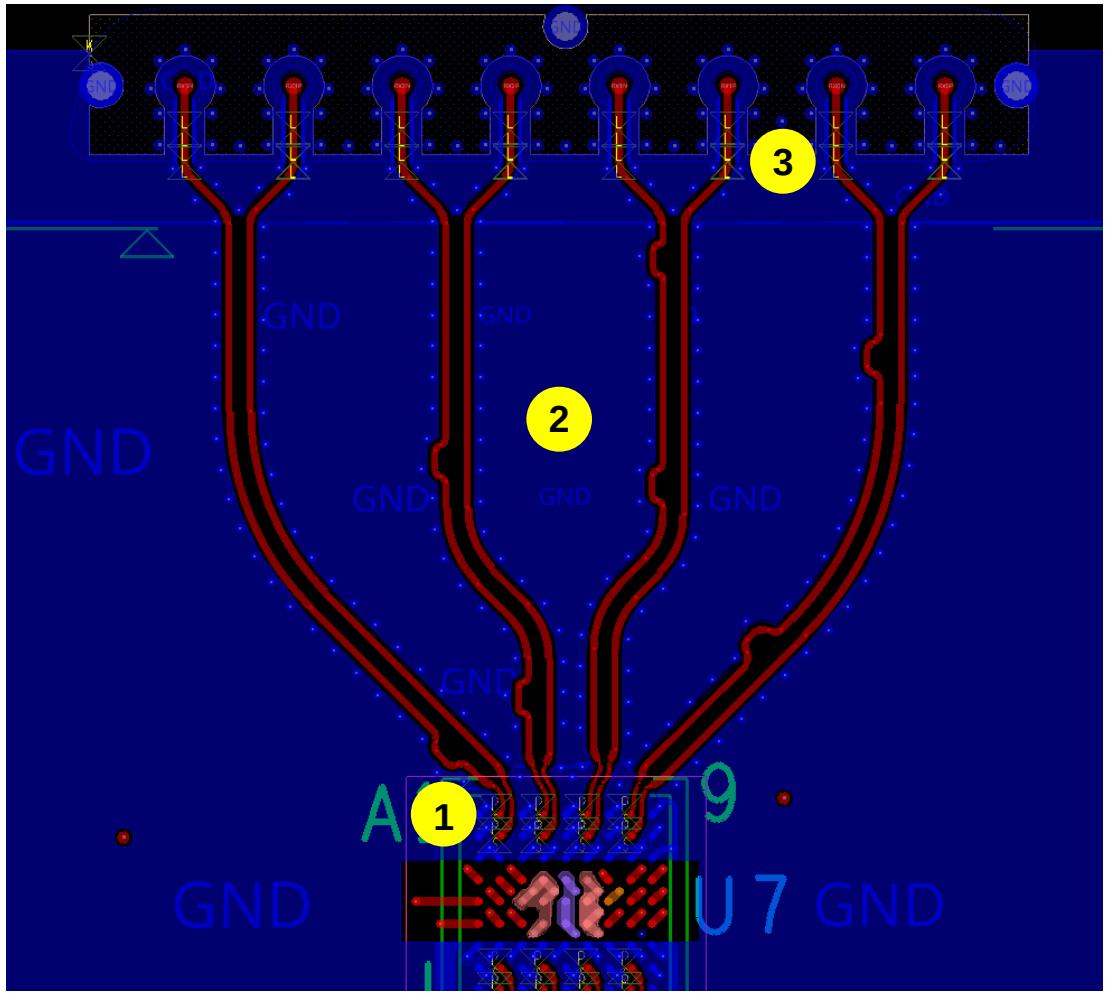
# High-speed trace impedance

- Traces should have a characteristic differential impedance ($Z_0$) of **100 Ω**.
  - This requirement should be strictly followed
  - Accomplished by impedance matching the P and N traces of each differential pair
- Trace impedance is determined by several factors:
  - Trace width
  - Trace spacing
  - Reference plane height
  - PCB material properties



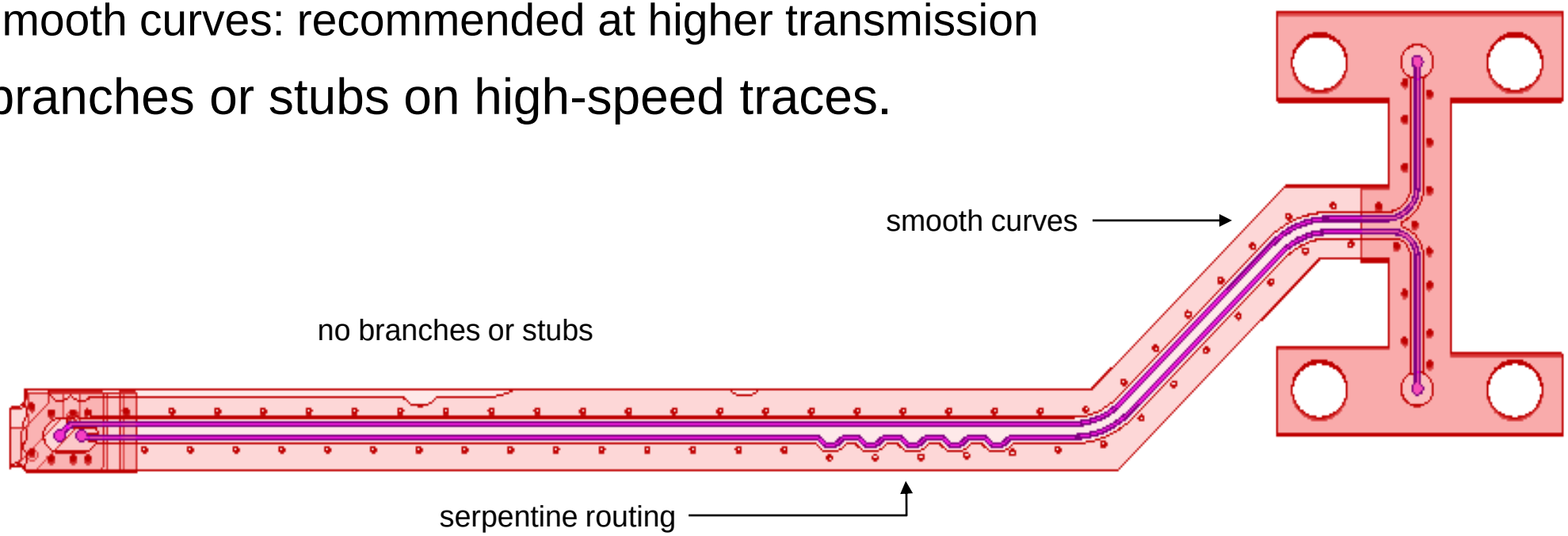
# High-speed trace impedance

- Trace dimensions should be considered in 3 separate areas
  1. Near retimer/redriver
  2. Along traces
  3. At connector
- 100 Ω differential impedance should be maintained in all sections



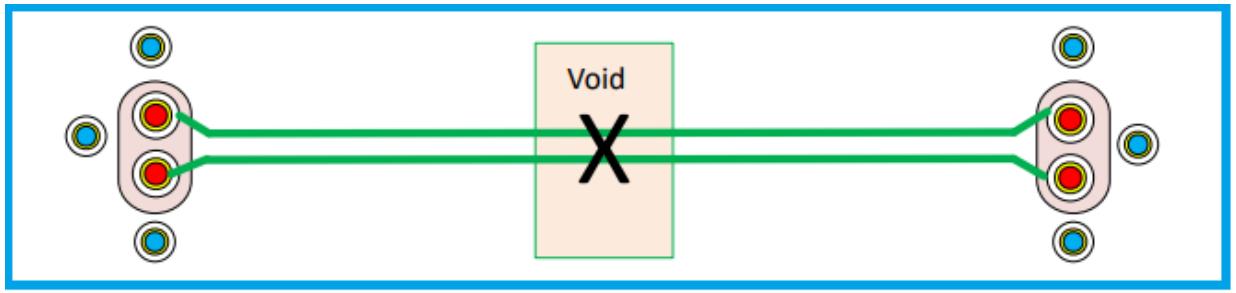
# Best practices to maintain trace impedance

- Match the trace lengths of each differential pair.
  - Use serpentine routing if needed
- Avoid sharp corners.
  - 135º straight edges: acceptable for 10 Gbps transmission
  - Smooth curves: recommended at higher transmission
- No branches or stubs on high-speed traces.

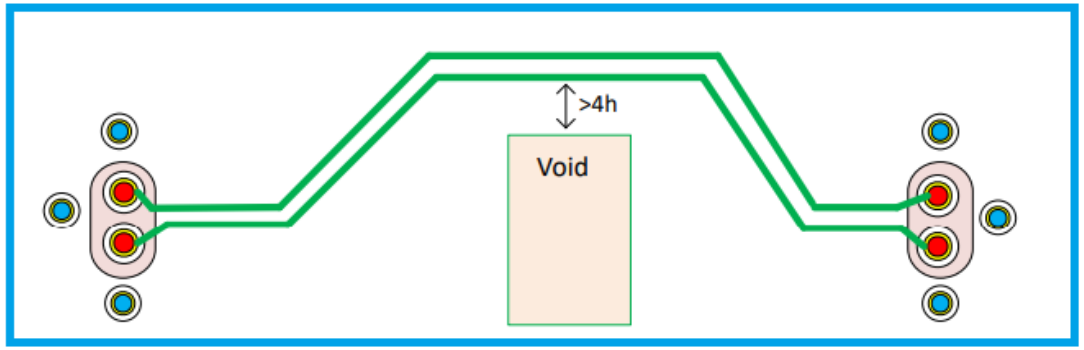


# Best practices to maintain trace impedance

- Continuous ground plane surrounding high-speed traces
  - On the same layer
  - 1 layer below
  - Avoid routing over any ground plane discontinuities
- Avoid using vias on high-speed traces as much as possible



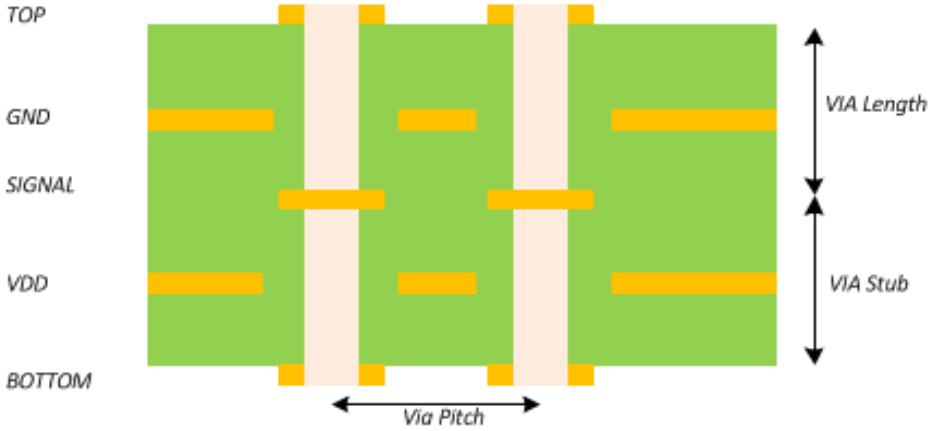

Incorrect Plane Void Routing

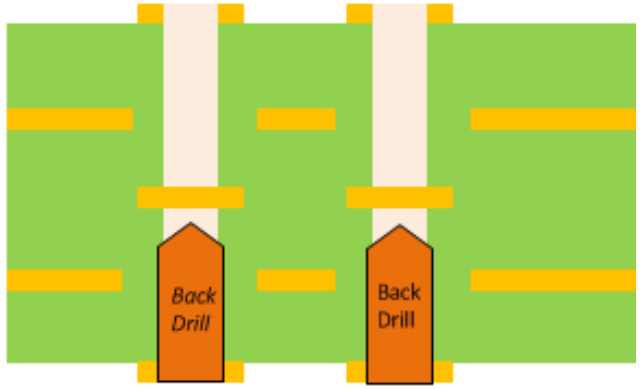


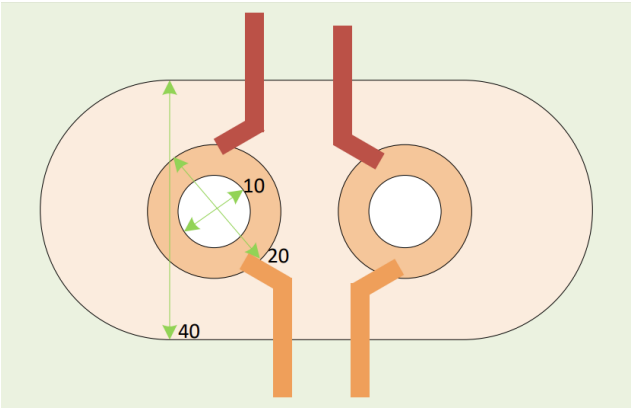

Correct Plane Voiding

# Via recommendations

- Clear the surrounding area of vias on every layer of the PCB.
- Stagger adjacent vias. Do not align adjacent vias vertically or horizontally.
- For via dimensions, follow the 10/20/40 drill/pad/anti-pad rule.
- Place the signal layer close to the bottom of the board to avoid via stubs.
  - Consider back-drilling or blind vias

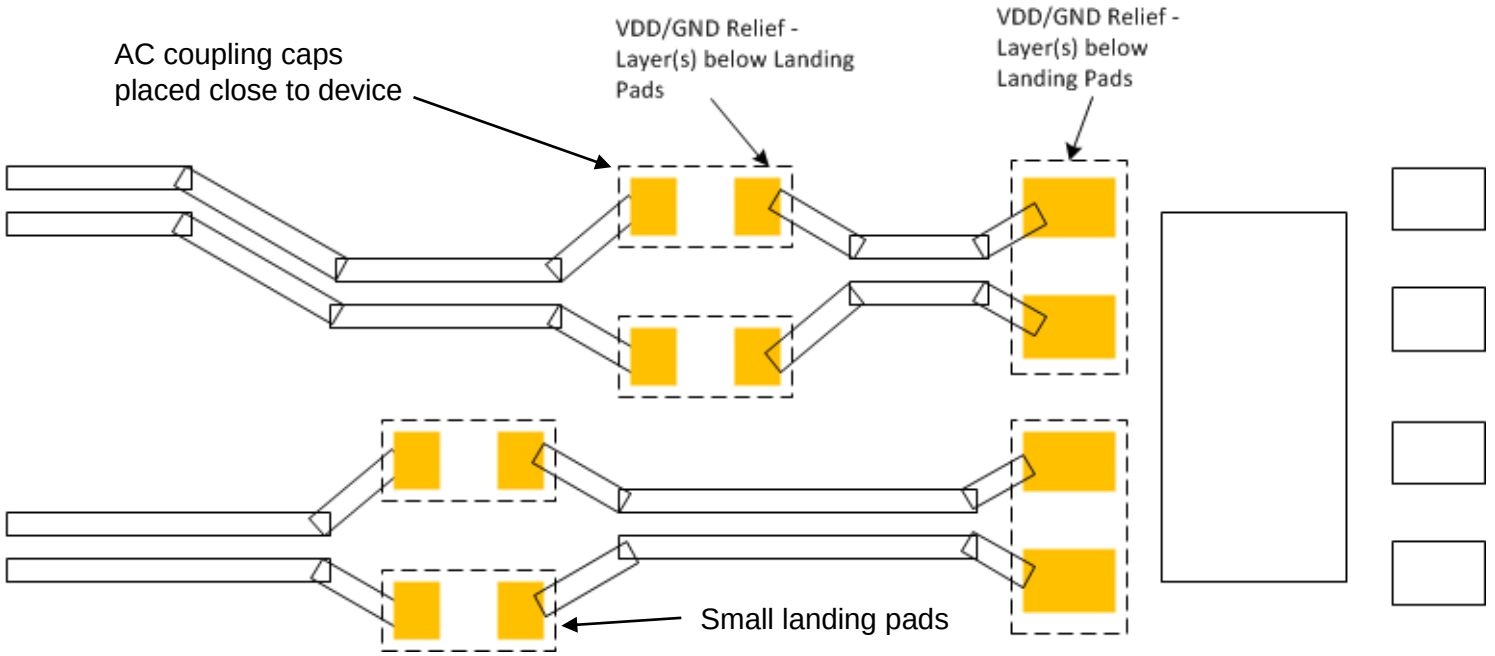


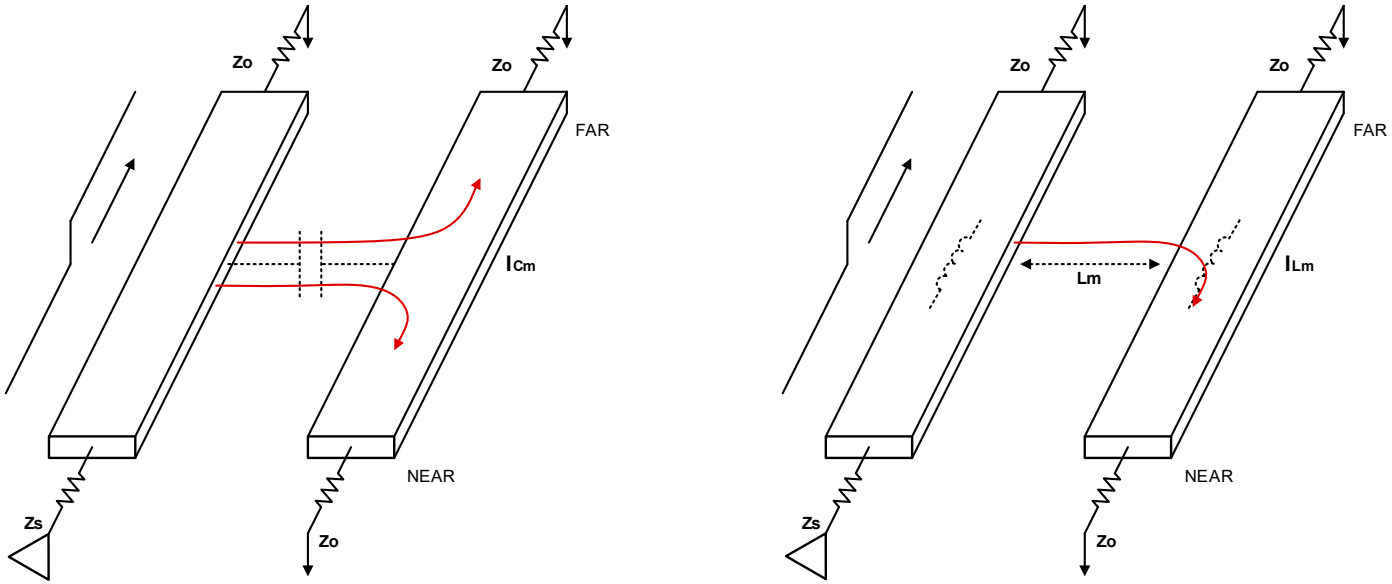
# AC coupling capacitor recommendations

- Retimer/Redriver RX: place AC coupling caps close to device
- Retimer/Redriver TX: place AC coupling caps close to connector
- Use small component size (0402 or smaller)
- Remove the ground plane directly below AC coupling caps and pin landing pads



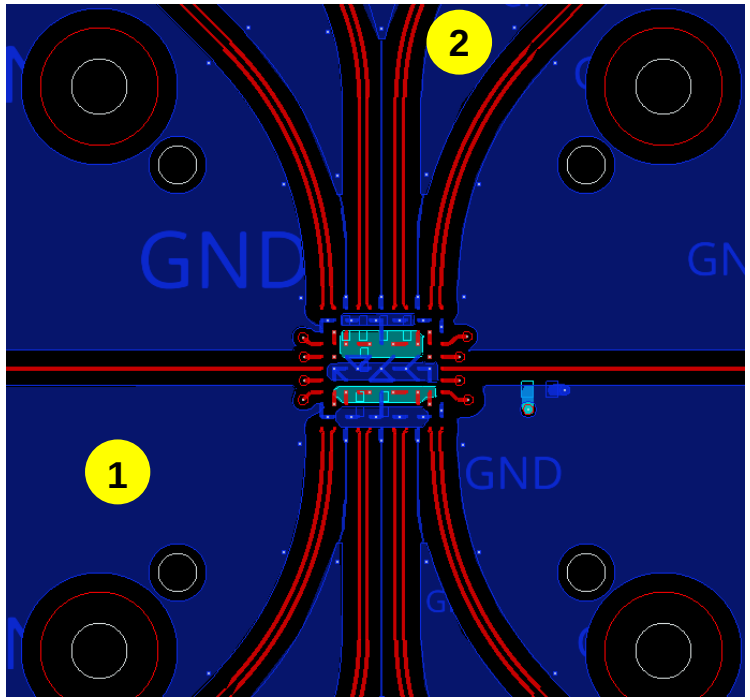
# Crosstalk recommendations

- Avoid placing power planes next to or directly below high-speed traces.
  - Could cause power-to-signal crosstalk
- Avoid placing differential pairs too close or directly below each other.
  - Could cause signal-to-signal crosstalk
  - If 1 layer below is required, orient traces orthogonally

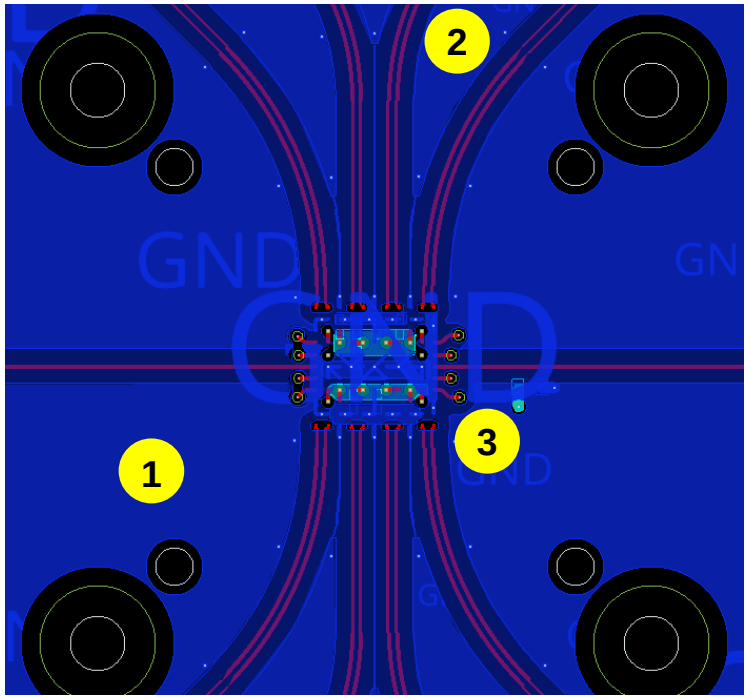


# Example layout

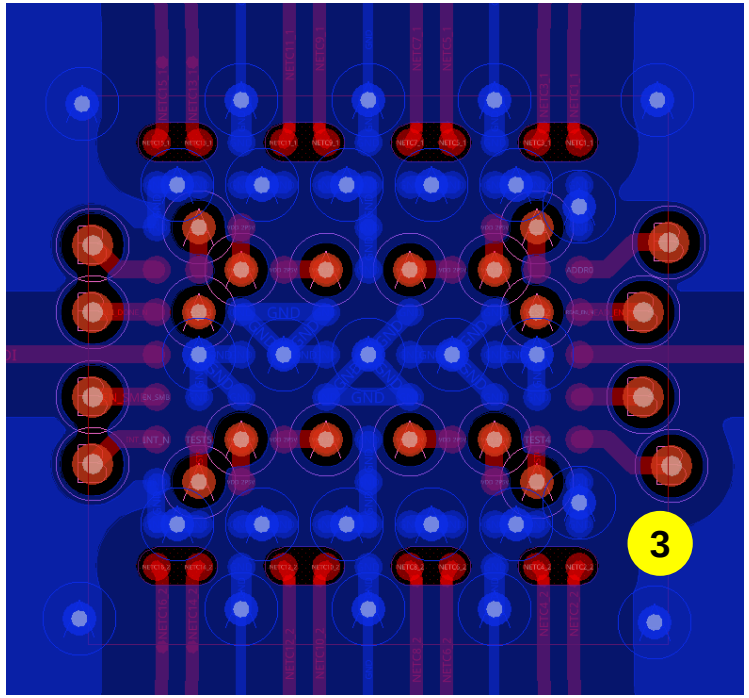
1. High speed traces are referenced to continuous ground plane.
2. High speed traces do not have sharp bends.
3. BGA pads have anti-pads in layer 2 in order to maintain $Z_0$.




Top Layer (Layer 1)



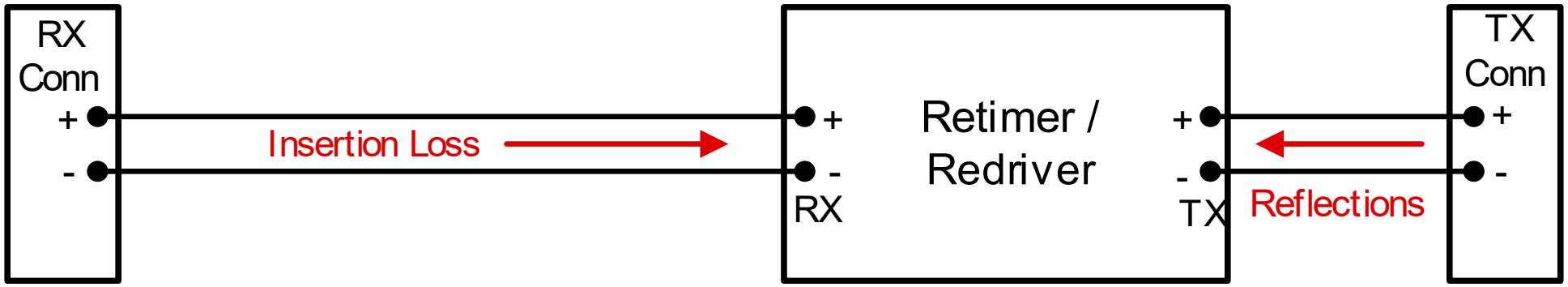

Layer 1 and Layer 2




Layer 1 and Layer 2 (Zoomed In)

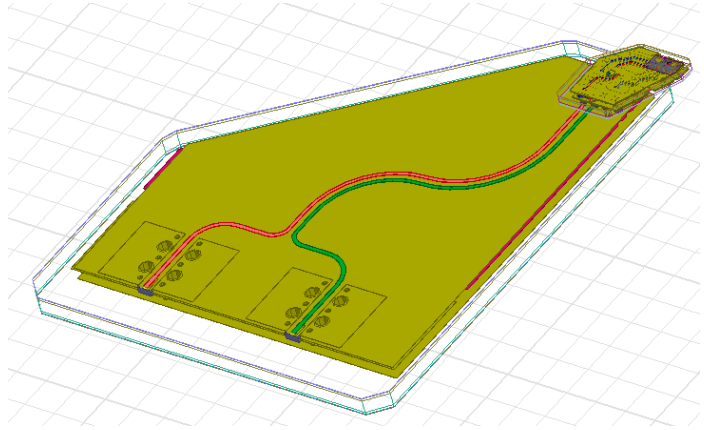
# Signal conditioner placement considerations

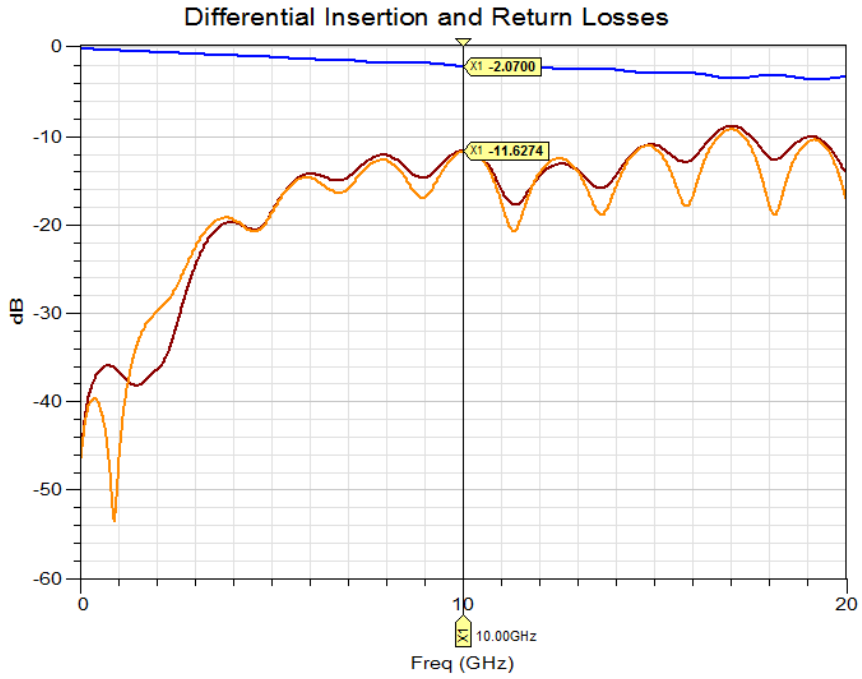
- Designers should consider insertion loss, reflections from connectors, and over-equalization when choosing where to place retimers/redrivers.
  - Close to TX connector: preferred to have more insertion loss on the input to the retimer/redriver
  - Not too close: minimum insertion loss of 2-3dB on the output of the retimer/redriver



# Layout simulation

- PCB simulation software can be used to verify high-speed layout design.
- These tools can typically report characteristic impedance, return loss, insertion loss, and crosstalk.
  - Ansys Siwave (2D simulation)
  - Ansys HFSS (3D simulation)
  - Keysight Momentum (3D simulation)
- 3D simulation preferred for greater accuracy.





To find more ethernet technical resources and search products, visit **ti.com/interface/ethernet/overview.html.**

# High-speed connector selection

- High speed connectors play an important role in signal integrity.
- In order to evaluate a connector, several criteria should be considered:
  - Is the connector designed for this application? Should not use SFP+ connector in SFP56 application.
  - What is the connector bandwidth?  Typically, a bandwidth of 2-3x the Nyquist frequency of the signal is recommended.
  - Can the manufacturer recommend an anti-pad for layout? Layout around a connector is critical in order to maintain characteristic impedance and avoid unwanted reflections. Simulation can be done to evaluate high speed performance.

- Mock presentation timing: ~9:40