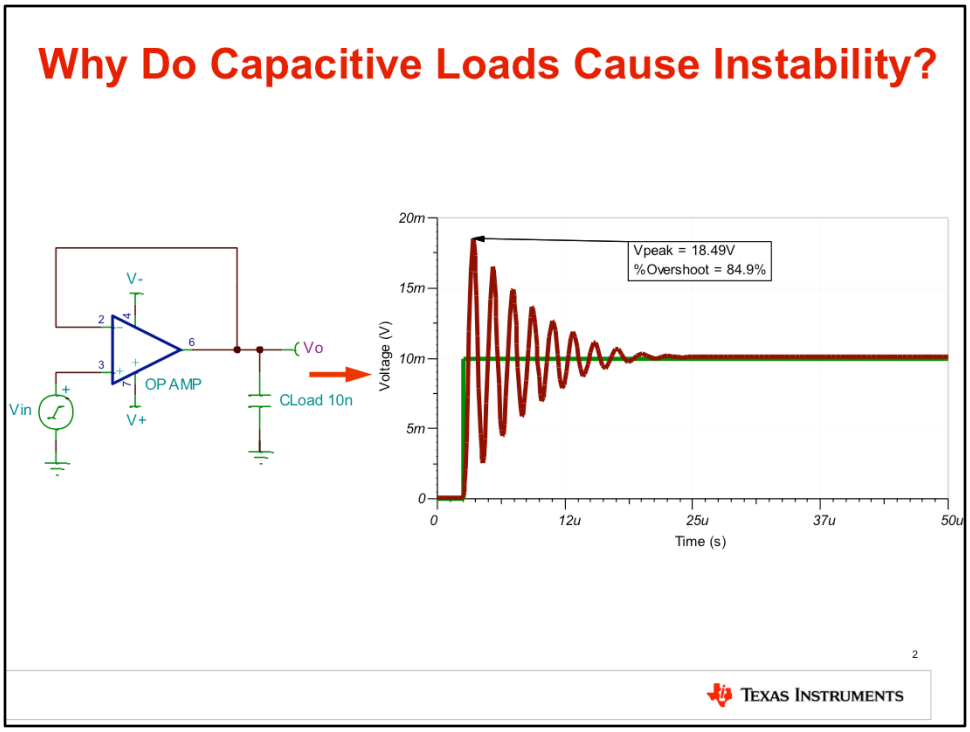
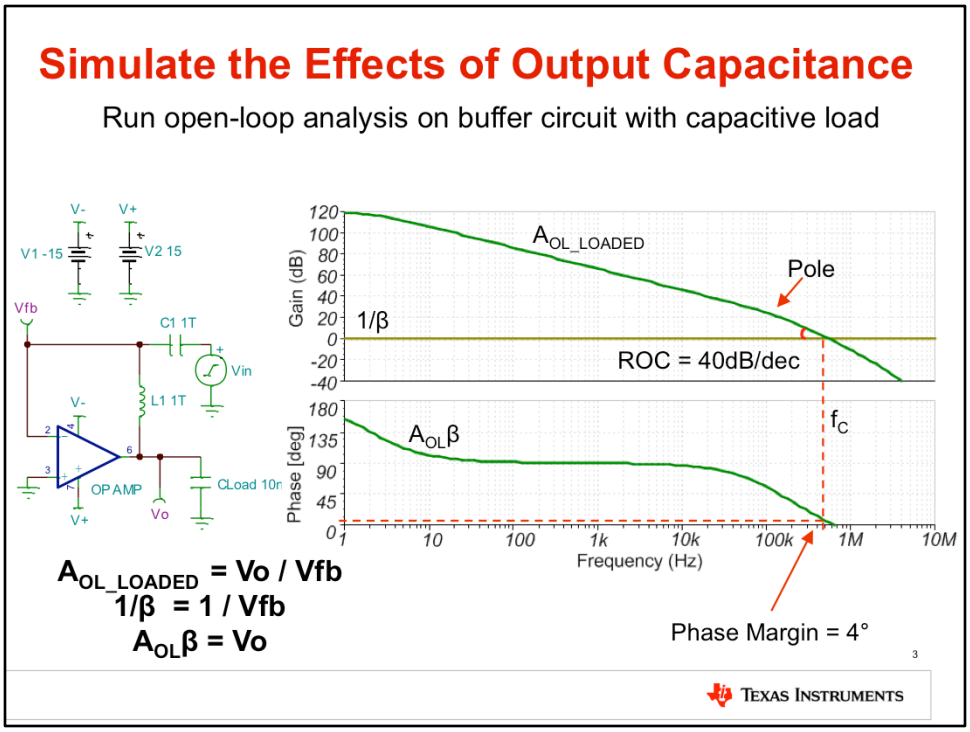
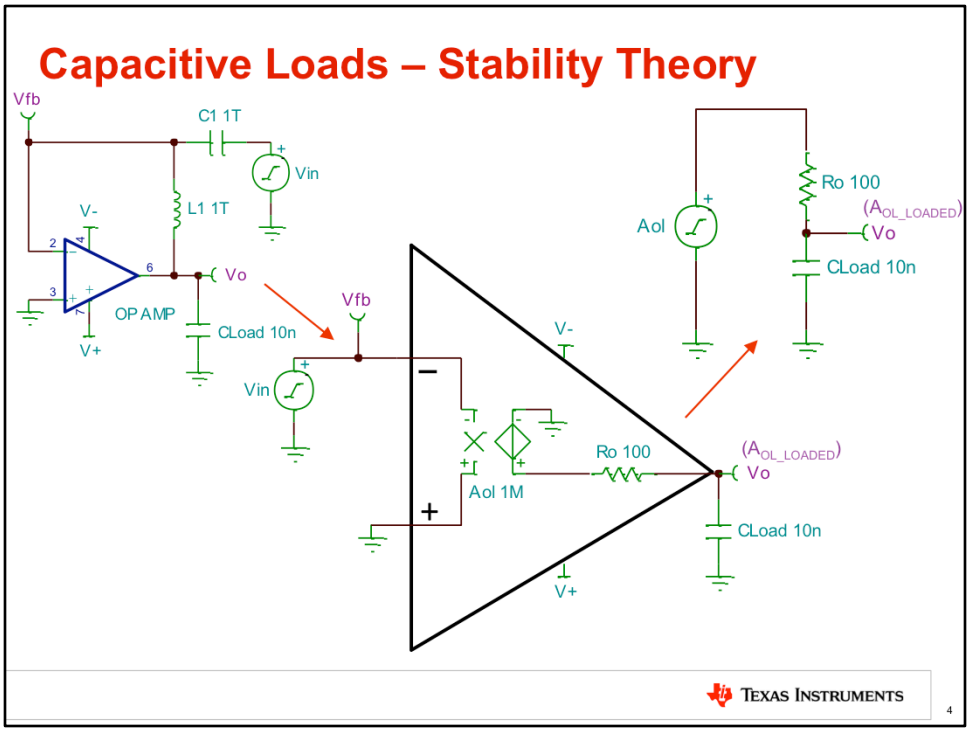
Hello, and welcome to part five of the TI Precision Labs on op amp stability. The previous videos discussed the concepts involved in basic stability theory, as well as how to test and simulate for stability issues in SPICE and on the bench. This video will discuss why capacitive loads cause stability issues and will present the first capacitive load compensation technique using an isolation resistor.



Part 1 of the stability series discussed that the most common cause of stability issues in amplifier circuits is capacitance on the output. Some common circuits that frequently have large capacitive loads are voltage reference buffers, cable/shield drive circuits, and MOSFET drive circuits. In the case of the MOSFET and cable or shield drive circuits the capacitive load is not always immediately apparent, so be sure to examine if the output is connected to anything with parasitic capacitance.

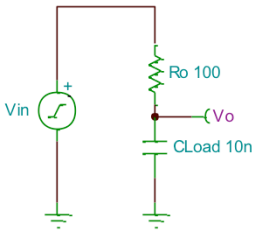


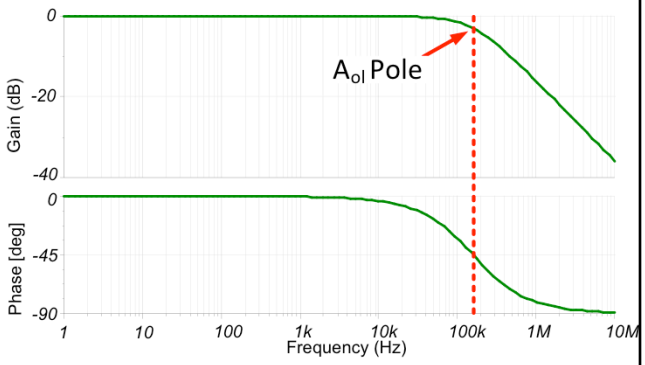
Now that we know how to generate the open-loop curves of an op amp circuit, we can simulate the effects with a capacitive load to determine the issue. As the results show, the 10nF capacitive load results in a pole in the Aol curve which degrades the Aol*ß phase to only 4 degrees at fc. Let's examine why this happens.



If we take a look at a simplified representation of the open-loop circuit, we see that the input signal passes through the Aol gain block and then the series open-loop output impedance, Ro, before reaching the op amp output, Vo. With a capacitor from Cload to GND on the output, the op amp Aol curve is loaded by the RC voltage divider formed from Ro and Cload.

Capacitive Loads – Stability Theory





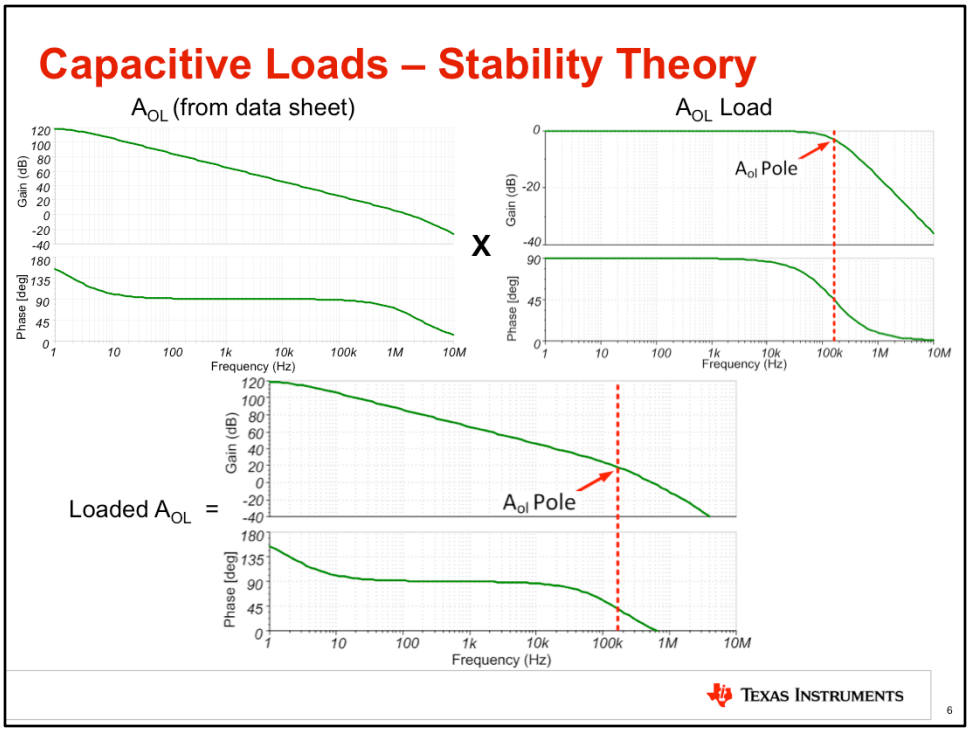
Transfer Function: $V_{out}/V_{in}(s) = 1/(1 + s * Ro * C_{LOAD})$

Pole Equation: $f_{POLE} = 1/(2 * \pi * Ro * C_{LOAD})$

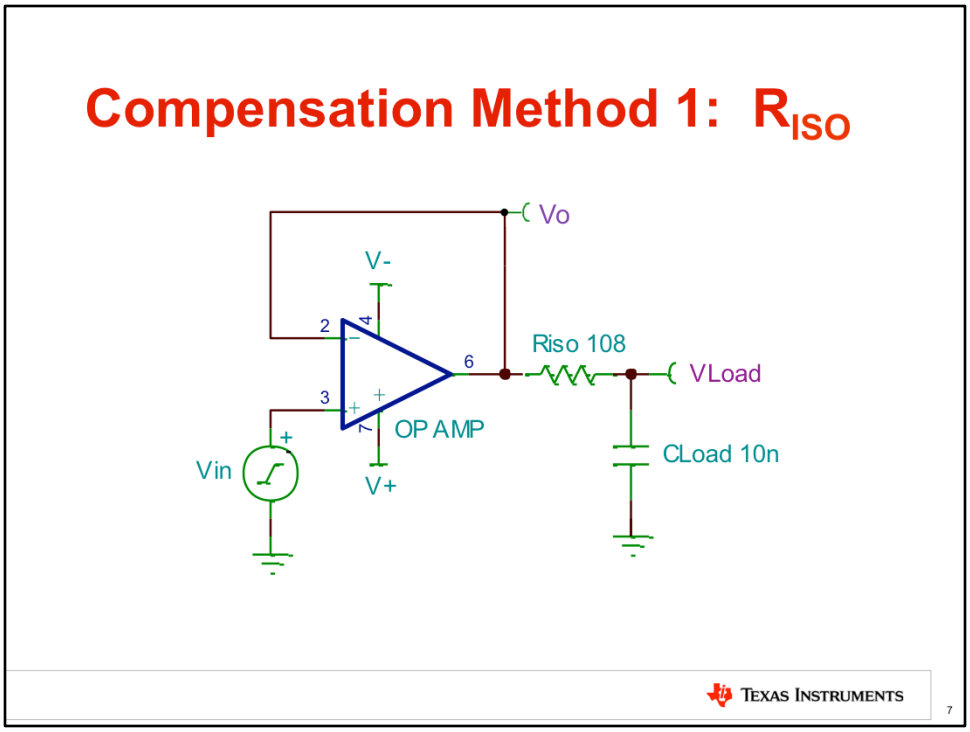
Texas Instruments

5

To understand the effects of the output load, the AC transfer function of the equivalent Ro + CLoad circuit has been plotted here. The pole location can be calculated from the transfer function and is shown at the bottom of the slide.

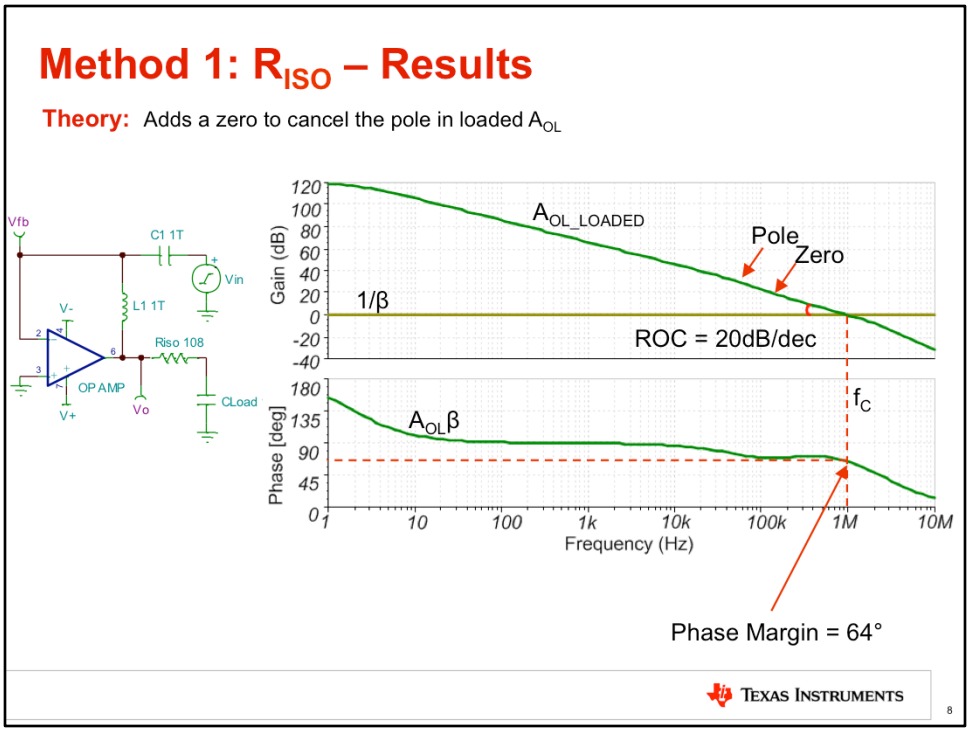


If the original op amp Aol curve and the Aol load curve are combined, the result is the loaded Aol curve shown on the bottom. The Aol pole from the interaction of Ro and Cload causes the Aol curve to change to a -40dB / decade slope and reduces the unity-gain phase margin.

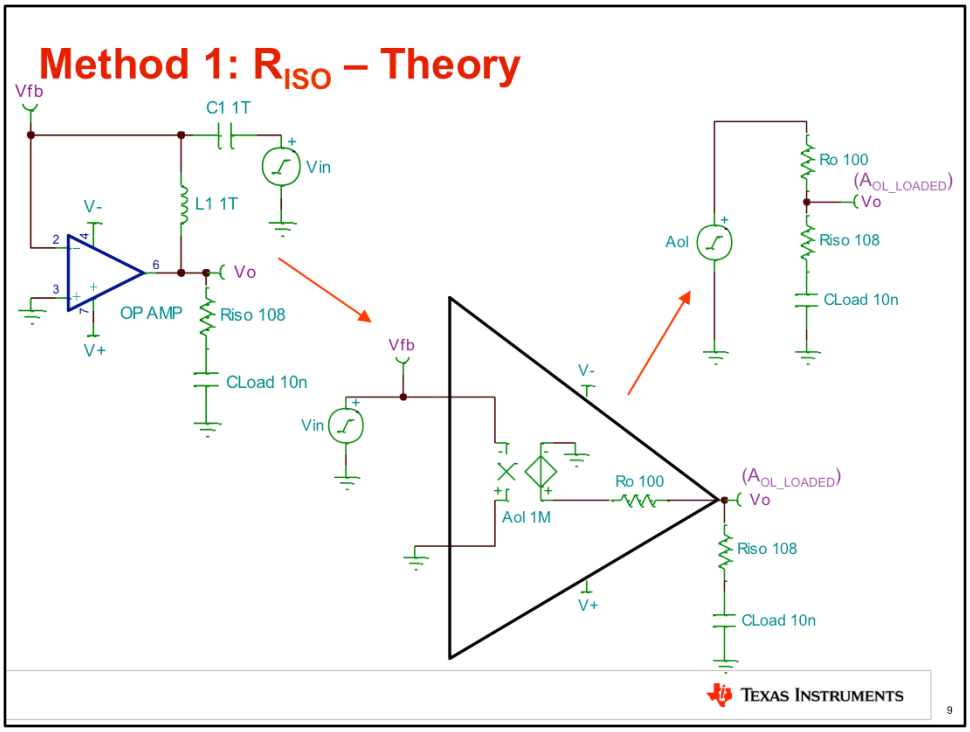


Now that we understand how a capacitive load contributes to circuit instability, we can introduce our first compensation technique, known as the Riso method.

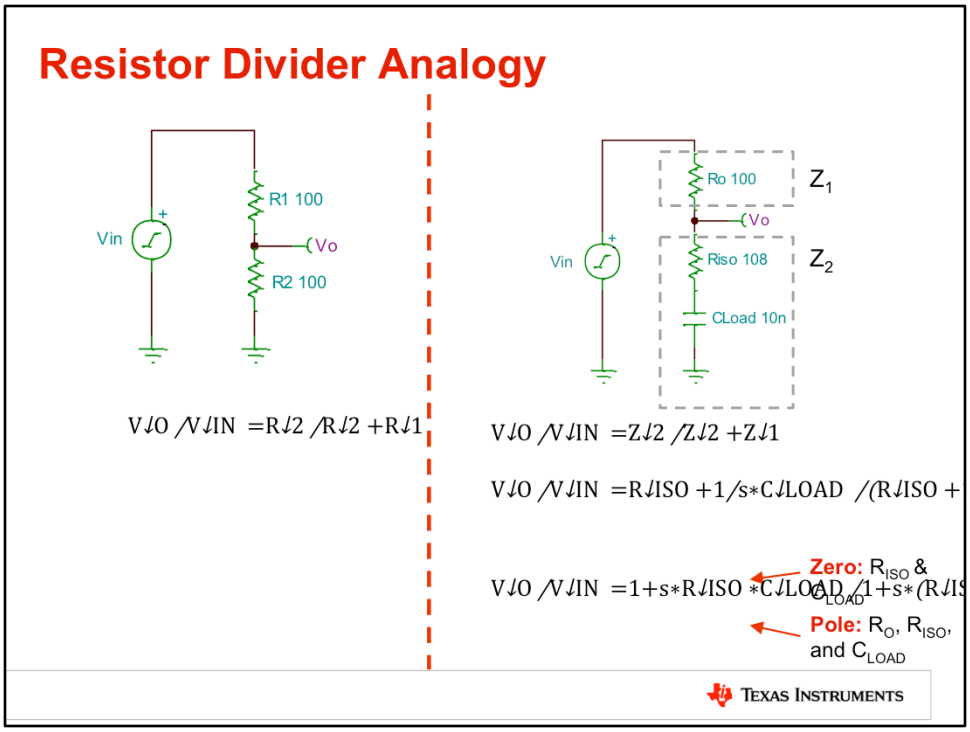
The Riso method compensates the circuit by adding a zero to cancel the pole from the output impedance and capacitive load.



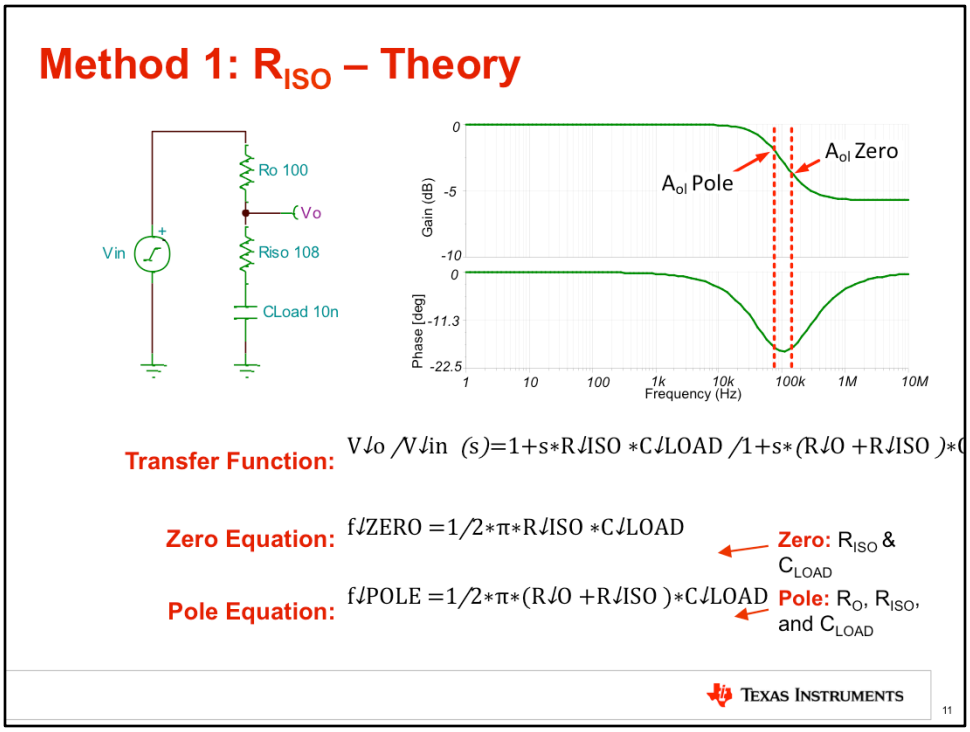
Looking at the open-loop results from the “Riso” compensation method, a zero can be seen cancelling the pole from Riso and Cload. This results in a return to a 20dB/ decade Aol slope and significantly improved phase margin.



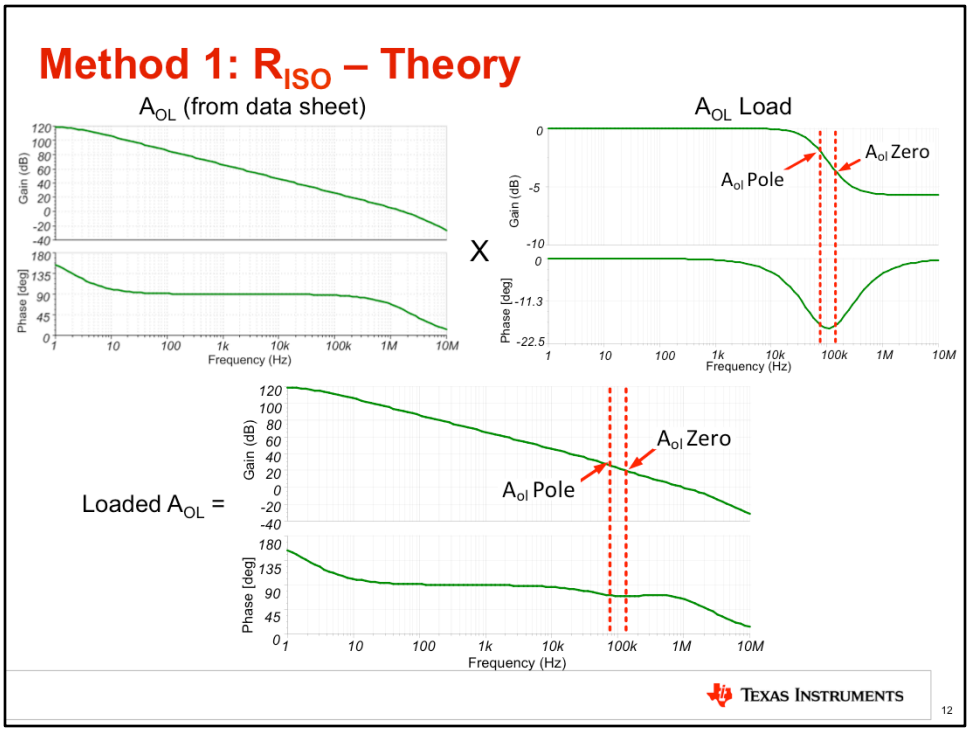
We can examine the open-loop Riso circuit the same way we examined the capacitive load circuit. Once again the Aol is loaded by an impedance divider, but this time both Riso and Cload are on the bottom side of the divider and Ro is on the top side of the divider.



We can compare the Aol Load to a classic resistive voltage divider. Remember, the transfer function of a voltage divider is equal to the impedance of the bottom leg divided by the sum of both the top and bottom impedances. The same applies to the circuit with Ro, Riso, and Cload, as shown on the right. Ro makes up Z1, the impedance of the top leg, while the series combination of Riso and Cload make up Z2, the impedance of the bottom leg. The transfer function can be simplified to the form shown at the bottom-right. The numerator shows a zero dependent only on Riso and Cload, both external circuit components, while the denominator shows a pole dependent on Ro, Riso, and Cload.



The resulting Laplace transfer function for this circuit is shown here. Again, with a single “s” term in both the numerator and denominator it is clear that there is now both a pole and a zero in the transfer function. The equations for the pole and zero frequency can be calculated from the transfer function. Plotting the ac transfer function, you can see that the positive phase shift from the zero cancels the negative phase shift from the pole, causing a net phase shift of zero degrees.



Adding the Aol and Aol load curves together as before, we can again see that the zero added by Riso cancels the pole in the Aol curve and restores the unity-gain phase margin to an acceptable level for stability.

Method 1: R_{ISO} – Design

Design Steps:

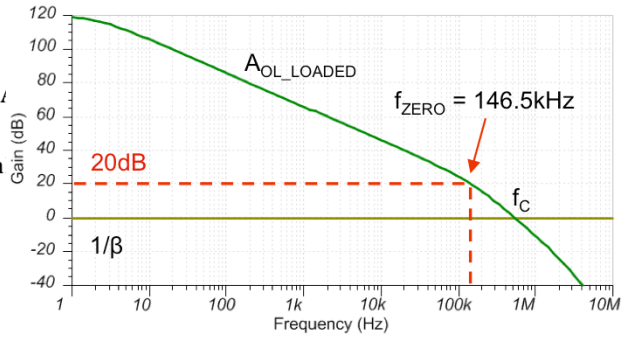
1.) Find the zero frequency, f_{ZERO}, where A_{OL_Loaded} = 20 dB
2.) Calculate Riso to set the zero at f_{ZERO}
This will yield between 60° and 90° degrees of phase margin

R_{ISO} Equation:

$$R_{ISO} = 1/2*\pi*f_{ZERO}*C_{LOAD}$$

$$R_{ISO} = 1/2*\pi*146.5kHz*10n$$

$$R_{ISO} = \mathbf{108\Omega}$$



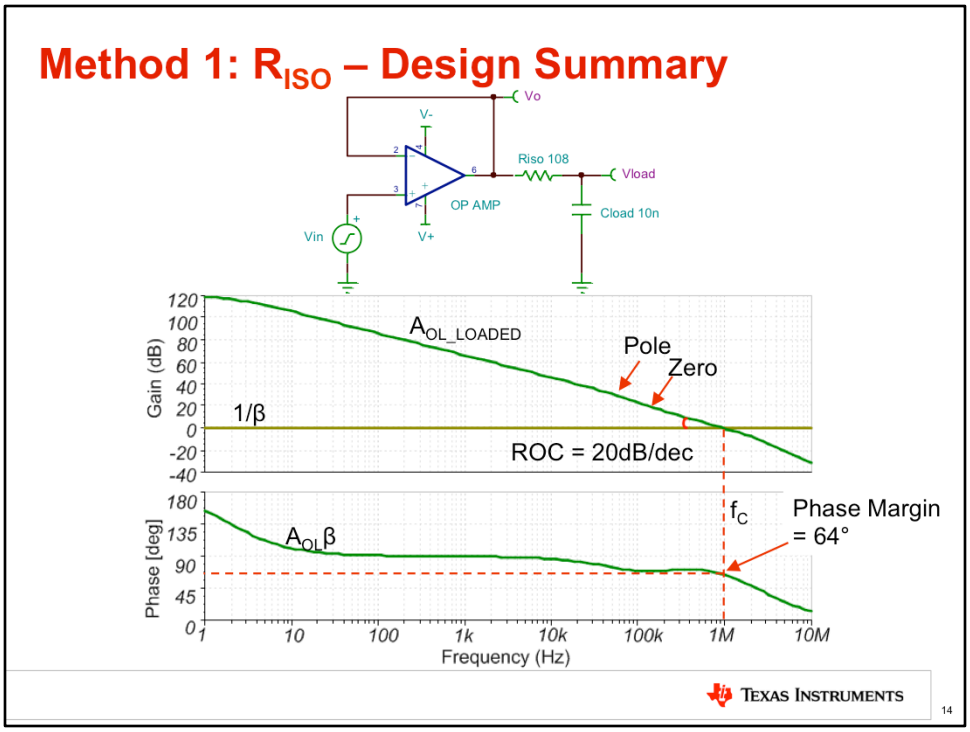
Texas Instruments

13

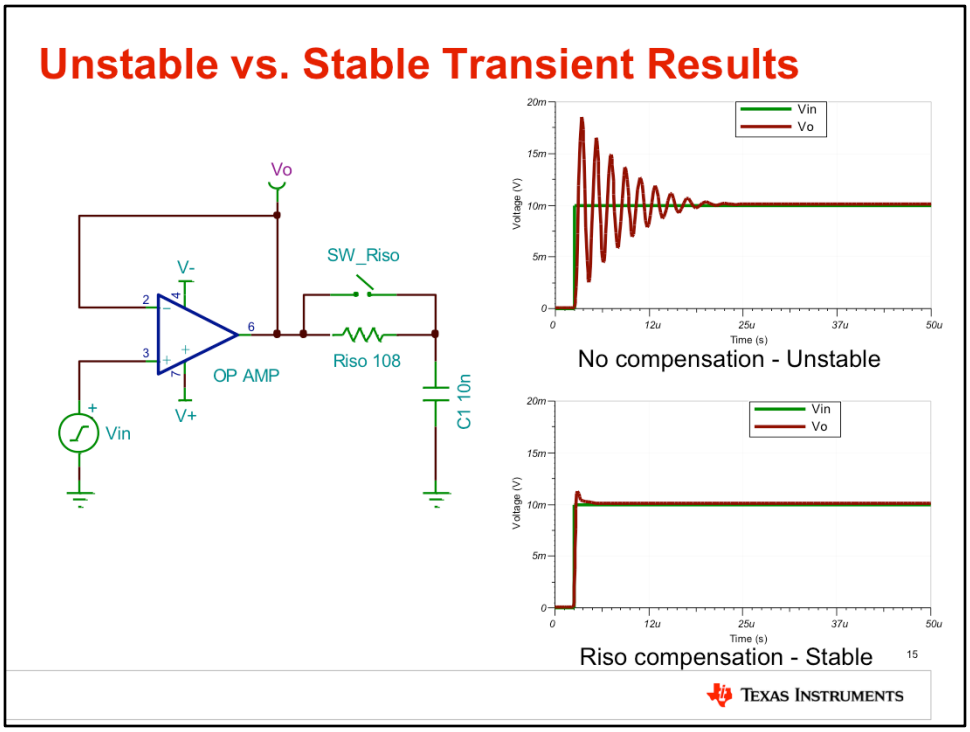
To design the Riso circuit for a phase margin above 60 degrees, first find the frequency where the Loaded Aol curve is equal to 20dB, f(zero).

Then, to calculate the value of Riso, use the equations shown on the left and plug in the values for Cload and f(zero). An Riso value of 108 ohms is the result in this case.

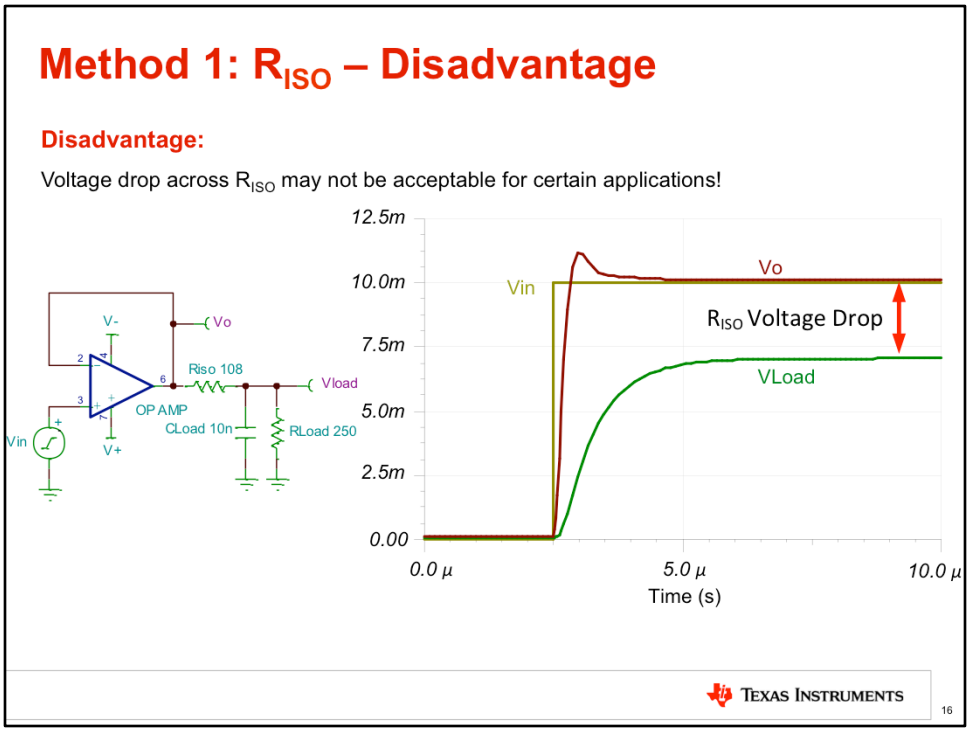
These steps will result in a phase margin between 60 and 90 degrees of phase margin depending on the op amp unity-gain phase margin and location of the Aol pole.



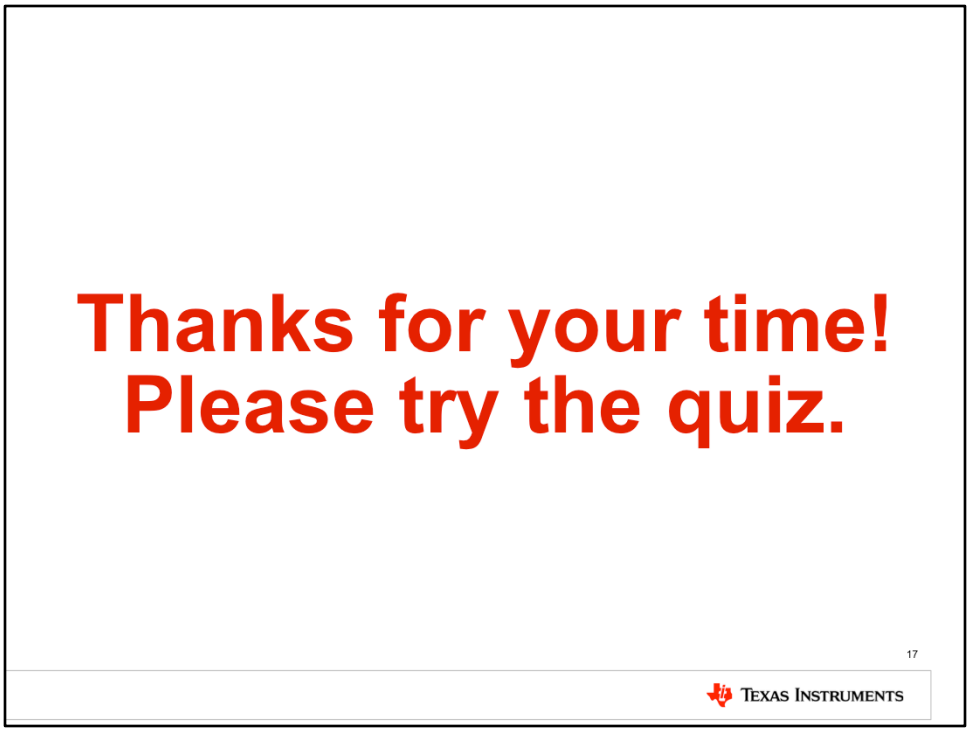
In summary, find the frequency where the loaded Aol curve equals 20dB and set the zero to that frequency by calculating the proper Riso value. While the theory behind this is not shown here, if the zero frequency ends up greater than ~1.5 decades from the pole, the Riso value should be increased to prevent the Aol*ß phase from dipping too low in the loop. If Riso is equal to at least Ro/34, then the zero will be within 1.5 decades of the pole. If the circuit is not required to deliver larger output currents then consider increasing Riso to be equal to or larger than Ro and the circuit will be stable under basically all capacitive loads.



Comparing the transient response of the circuit both with and without Riso compensation, we can see the significant improvement by using Riso. Without Riso, the output of the circuit shows heavy overshoot and ringing.



While the Riso circuit is both simple to implement and design, it has a big disadvantage in precision circuits. The voltage drop from Riso is dependent on the output current or output load, and may be significant compared to the desired signal. As shown here, a 10mV signal has over 3mV (30%) of error due to a 250Ω output load.



In summary, this video discussed the theory behind why capacitive loads cause stability issues and presented a simple method to compensate for the capacitive load by placing a resistor between the amplifier output and capacitive load.

The next video will present a second capacitive load compensation technique that fixes the dc errors caused by the Riso circuit.

Thank you for your time! Please try the quiz to check your understanding of this video's content.

Stability 5

Multiple Choice Quiz

TI Precision Labs – Op Amps

Quiz: Stability 5

1. (T/F) Placing capacitive loads on the output of an op amp will generally cause stability issues.

a. True
b. False

2. The output capacitance causes issues because it interacts with the amplifier's:

a. Open-Loop Gain
b. Input Offset Voltage
c. Open-Loop Output Impedance
d. Feedback network

3. Output capacitance results in an additional _____ which degrades the phase margin.

a. pole in the Aol curve
b. zero in the Aol curve
c. pole-zero pair in the Aol curve

Quiz: Stability 5

4. (T/F) The Riso compensation technique works by adding a zero to cancel the Aol pole from the capacitive load.

a. True
b. False

5. (T/F) The frequency of the zero in the Riso compensation method is based on the values of:

a. Riso, Ro, Cload
b. Riso, Cload
c. Ro, Cload

6. (T/F) DC voltage errors due to the voltage drop across Riso are a disadvantage to the Riso compensation method.

a. True
b. False

Stability 5

Multiple Choice Quiz: Solutions

TI Precision Labs – Op Amps

Quiz: Stability 5

1. (T/F) Placing capacitive loads on the output of an op amp will generally cause stability issues.

a. True
b. False

2. The output capacitance causes issues because it interacts with the amplifier's:

a. Open-Loop Gain
b. Input Offset Voltage
c. Open-Loop Output Impedance
d. Feedback network

3. Output capacitance results in an additional _____ which degrades the phase margin.

a. pole in the Aol curve
b. zero in the Aol curve
c. pole-zero pair in the Aol curve

Quiz: Stability 5

4. (T/F) The Riso compensation technique works by adding a zero to cancel the Aol pole from the capacitive load.

a. True
b. False

5. (T/F) The frequency of the zero in the Riso compensation method is based on the values of:

a. Riso, Ro, Cload
b. Riso, Cload
c. Ro, Cload

6. (T/F) DC voltage errors due to the voltage drop across Riso are a disadvantage to the Riso compensation method.

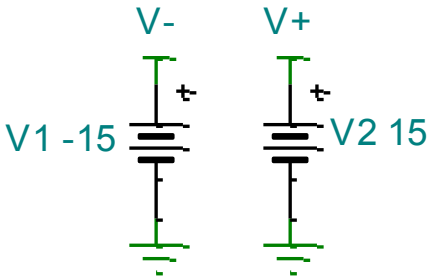
a. True
b. False

Stability 5

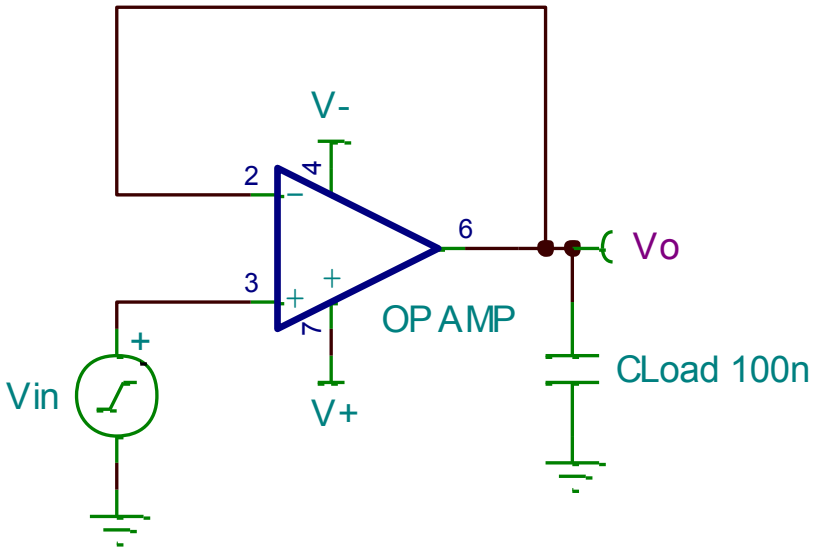
Exercises

TI Precision Labs – Op Amps

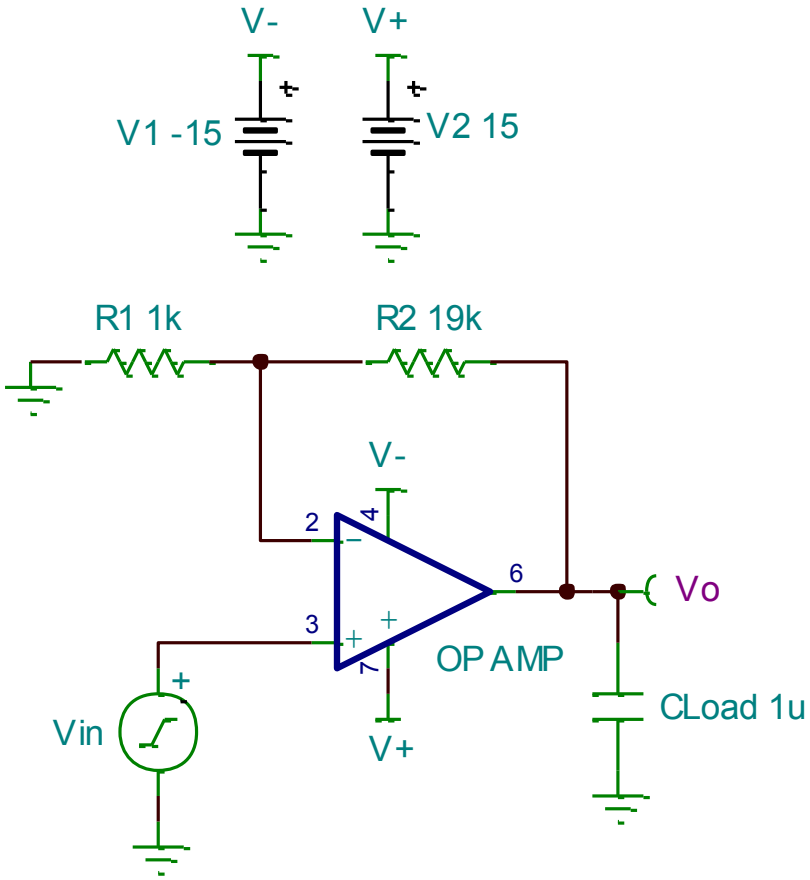
1. **Compensate the amplifier circuit using an R_{ISO} resistor so the final circuit has at least 60° of phase margin.**



1335 - Stability 5 - Problem 1.TSC



2. Compensate the amplifier circuit using an R_{ISO} resistor so the final circuit has at least 60° of phase margin.



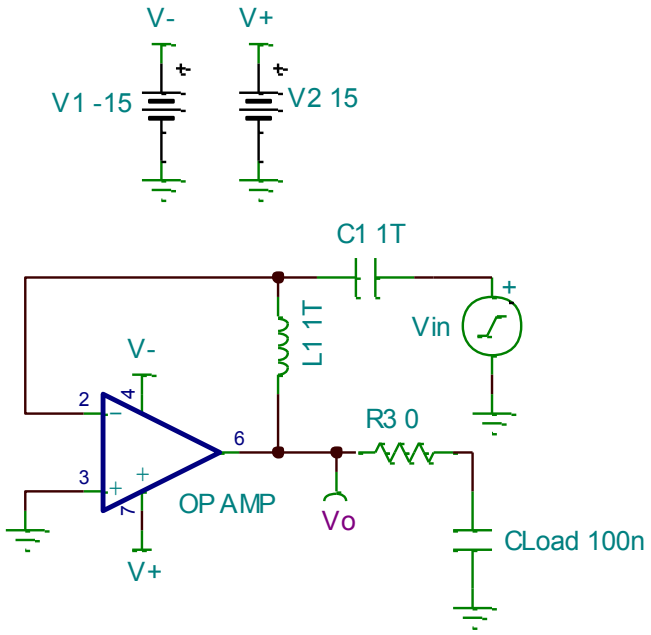
1335 - Stability 5 - Problem 2.TSC

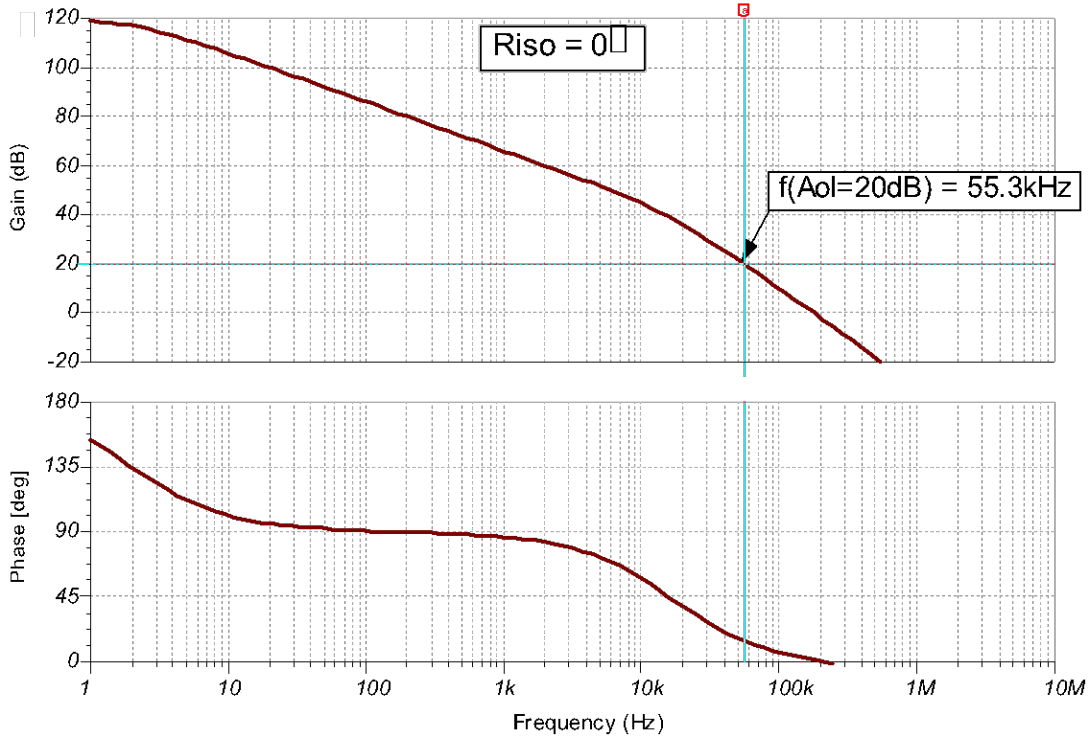
Stability 5

Solutions

TI Precision Labs – Op Amps

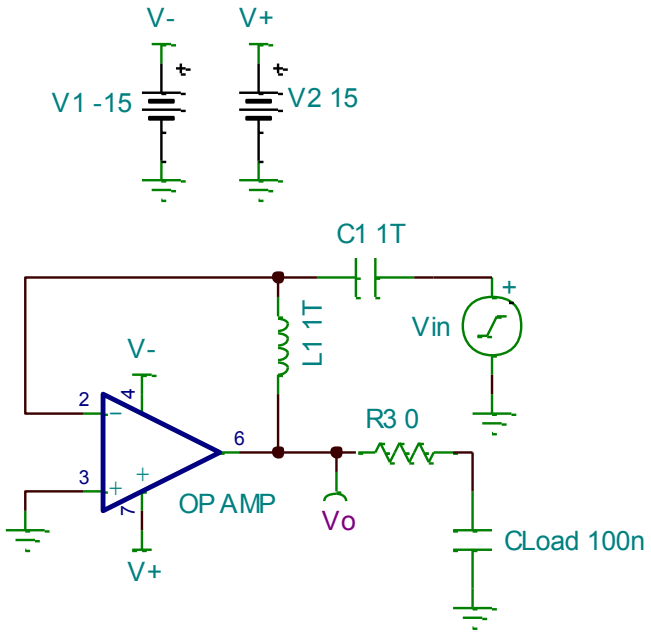
1. Compensate the amplifier circuit using an R_{ISO} resistor so the final circuit has at least 60° of phase margin.

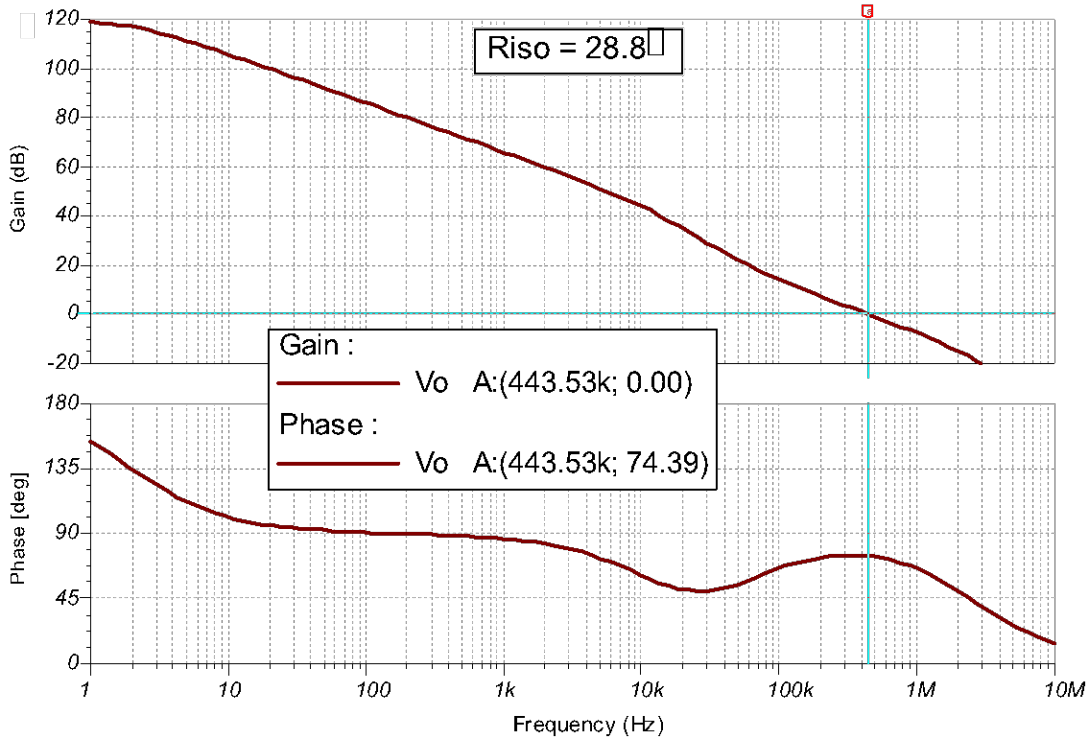




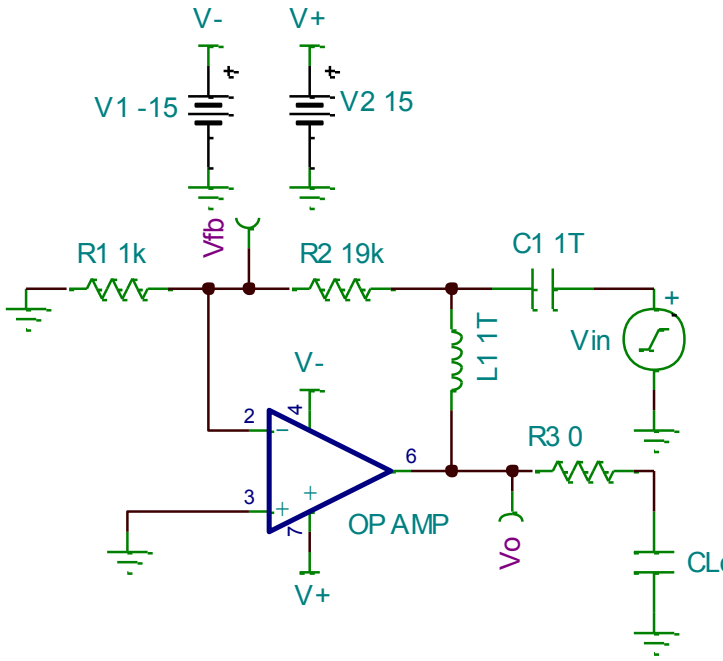
1335 - Stability 5 - Problem 1 - Solution.TSC

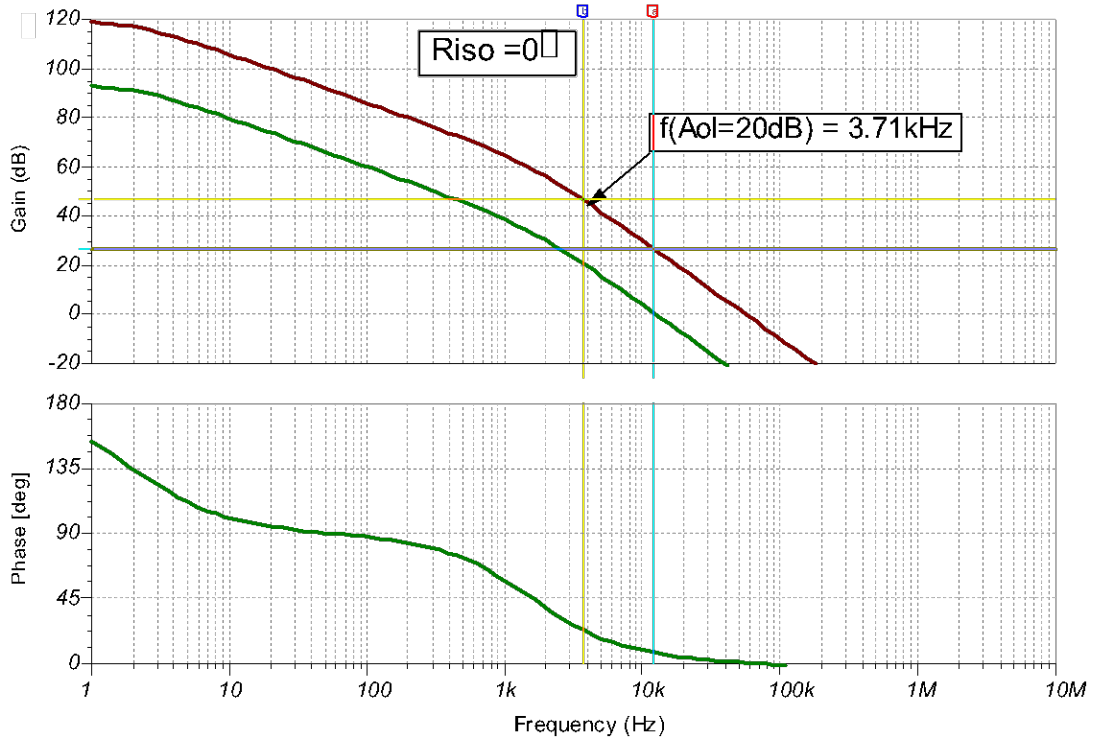
1. **Simulate the percent overshoot and ac gain peaking for the following circuit. Based on these indirect measurements, what is the Aolβ phase margin?**





2. Compensate the amplifier circuit using an R_{ISO} resistor so the final circuit has at least 60° of phase margin.





1335 - Stability 5 - Problem 2 - Solution.TSC

2. Compensate the amplifier circuit using an R_{ISO} resistor so the final circuit has at least 60° of phase margin.