



Stability – 3
TIPL 1333
TI Precision Labs – Op Amps

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Prerequisites: Op Amp Bandwidth 1 – 3
(TIPL1221 – TIPL1223)

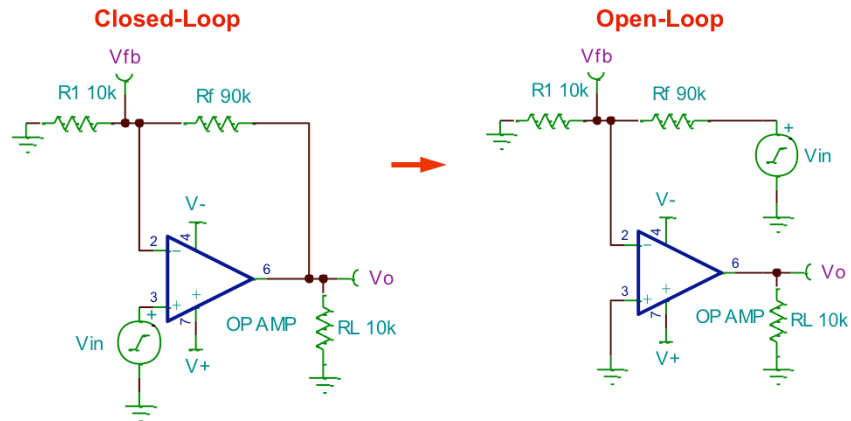
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Hello, and welcome to part three of the TI Precision Labs on op amp stability. The previous videos discussed the type of issues that op amp stability can cause in production systems, how to identify issues in the lab, and a review of Bode plots and stability theory.

This video will explain how to perform open-loop SPICE simulations to obtain the rate of closure and phase margin of op amp circuits. Please be sure you've completed the lectures and problem sections for Op-Amp Bandwidth one through three before proceeding.

Simulating Open-Loop Circuits

We need an open-loop circuit (no feedback) to generate open-loop gain (A_{OL}), $1/\beta$, and loop gain ($A_{OL}\beta$) curves



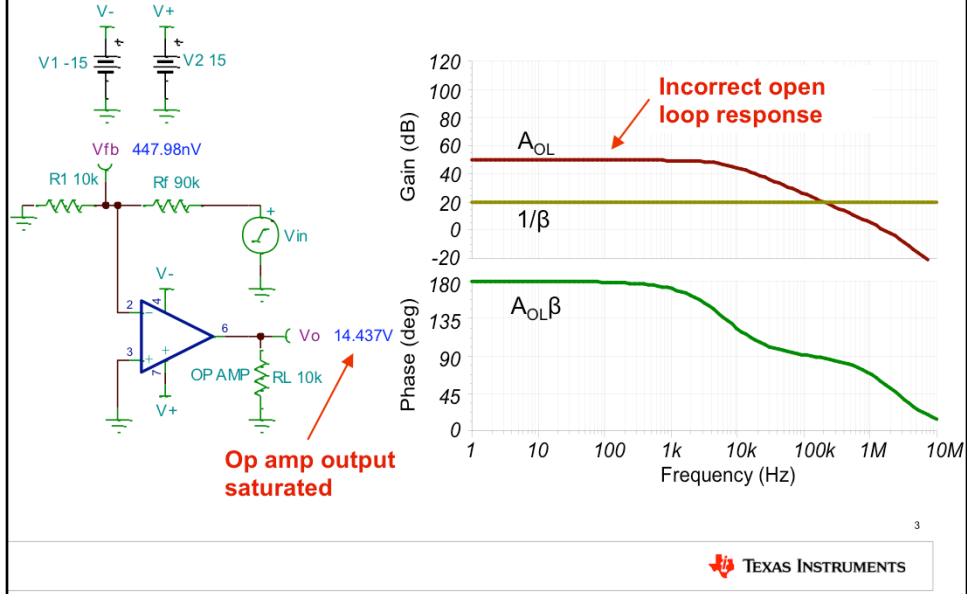
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The A_{ol} , $1/\beta$, and $A_{ol}\beta$ curves required for rate of closure and phase margin measurements can not be obtained from a circuit in a standard closed-loop configuration. To generate these curves, the feedback loop of the amplifier needs to be opened up, or “broken”. Then, a small signal source is used to excite the high-impedance side of where the loop was broken. Measurements can then be taken at the op amp inverting input (V_{fb}) and output (V_o), which will be used to derive the desired curves.

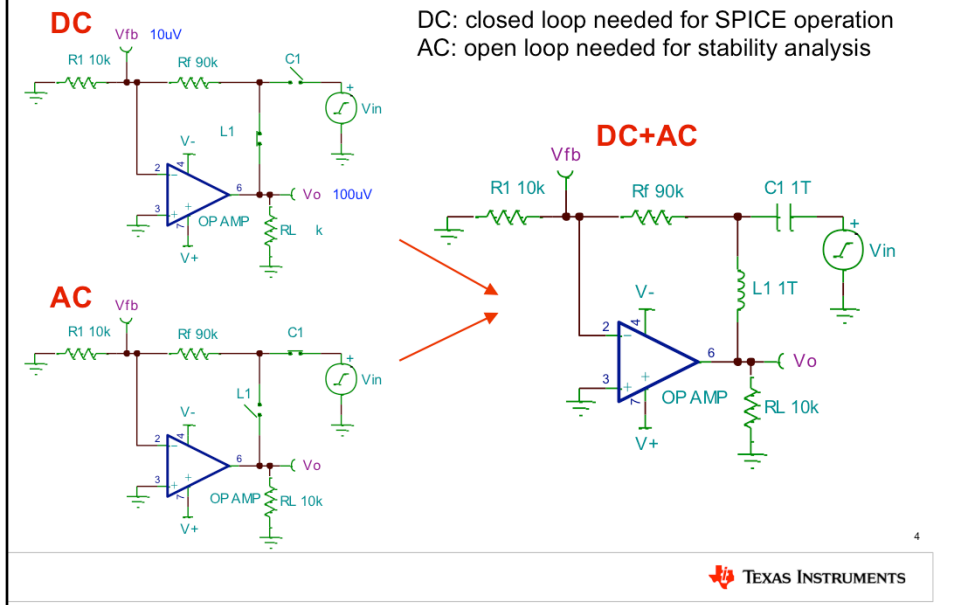
Simulating Open-Loop Circuits

No DC biasing produces erroneous results!



However, simply breaking the feedback loop of a circuit will not produce correct simulation results! Without a proper dc bias, the output will saturate to one rail or the other, reducing the performance of the output stage. As shown here, the op-amp output is near the positive rail, resulting in erroneous A_{OL} and $A_{OL}\beta$ curves.

Simulating Open-Loop Circuits



To properly generate the open-loop curves in SPICE, the circuit being simulated must have a closed loop feedback path at dc while being open for all ac frequencies.

The circuit at the top left shows the desired dc circuit with the L1 switch closed and C1 switch open. A closed loop circuit at dc allows the output to be properly biased to a recommended dc operating point, commonly mid-supply.

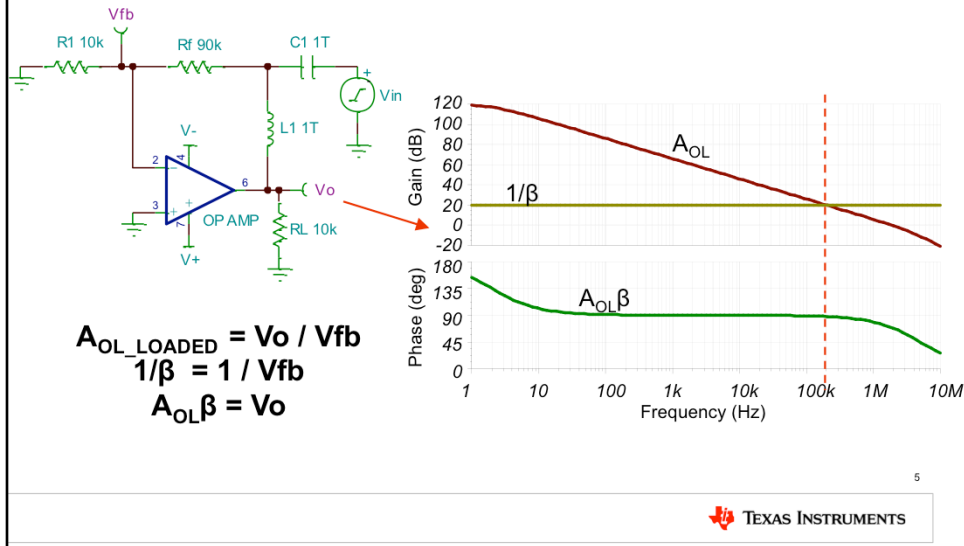
The circuit at the bottom left shows the desired ac circuit with the L1 switch open and C1 switch closed. With the loop open for ac frequencies, the ac stimulus can be applied to generate the open-loop curves.

Thankfully, there's a straightforward way to create a circuit that meets both the dc and ac criteria using the ideal properties of SPICE components. Switch L1 is replaced with a 1Tera-Henry inductor, and switch C1 is replaced with a 1Tera-Farad capacitor.

At dc, L1 is a short and C1 is an open-circuit, providing a proper dc operating point. For all ac frequencies, L1 is an open-circuit and C1 is a short resulting in the proper open-loop ac connections.

Standard Open-Loop SPICE Configuration

Standard circuit breaks the feedback loop between the output and the feedback elements



Therefore, here is the recommended standard open-loop SPICE circuit configuration for op amp circuits. The feedback loop is broken between the op amp output and the feedback elements. The ac signal source is injected into the feedback network and measurements are taken at the output, V_o , and feedback node, V_{fb} .

With the feedback loop broken as shown, the equations for generating the desired curves are as follows:

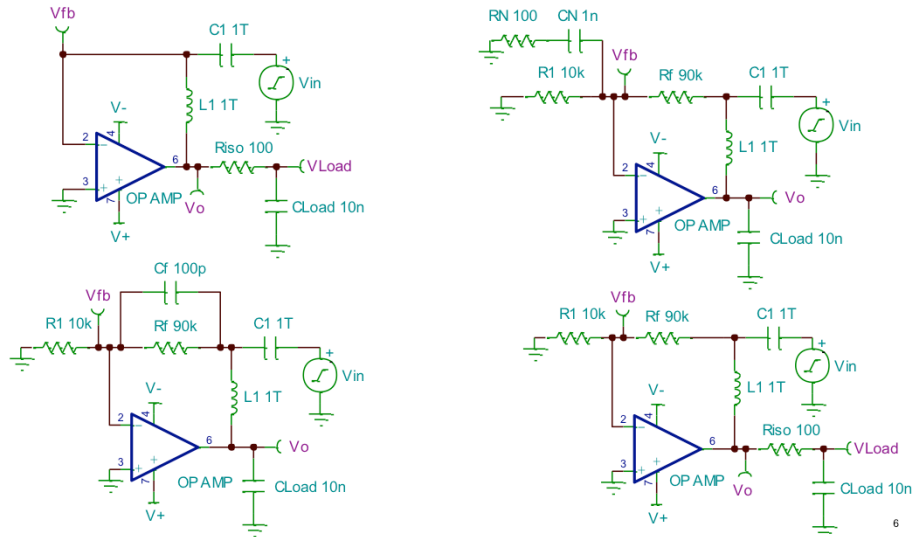
$$A_{ol_loaded} = V_o/V_{fb}$$

$$1/\beta = 1/V_{fb}$$

$$A_{ol} \cdot \beta = V_o$$

Example Open-Loop SPICE Circuits

Common op-amp circuits using standard configuration for open-loop simulation



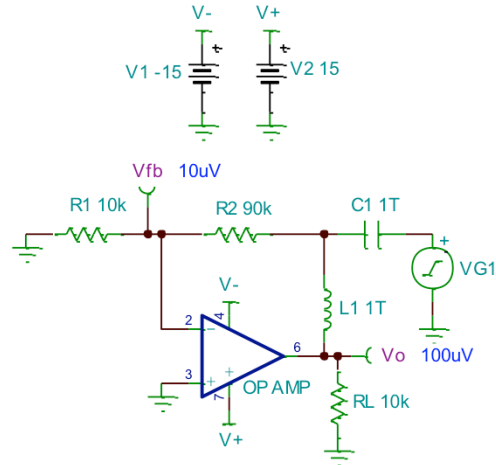
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Several example circuits ready for open-loop simulation are shown here. They can be used for review if there is confusion regarding where to break the loop in many standard circuit configurations.


Note that for proper stability analysis, any output loading must remain directly on the output of the op amp and should not be placed on the other side of the inductor. Doing so would remove the effects the output loads have on the op amp output.

Check DC Operating Point

Click **Analysis** → **DC Analysis** → **Calculate Nodal Voltages**



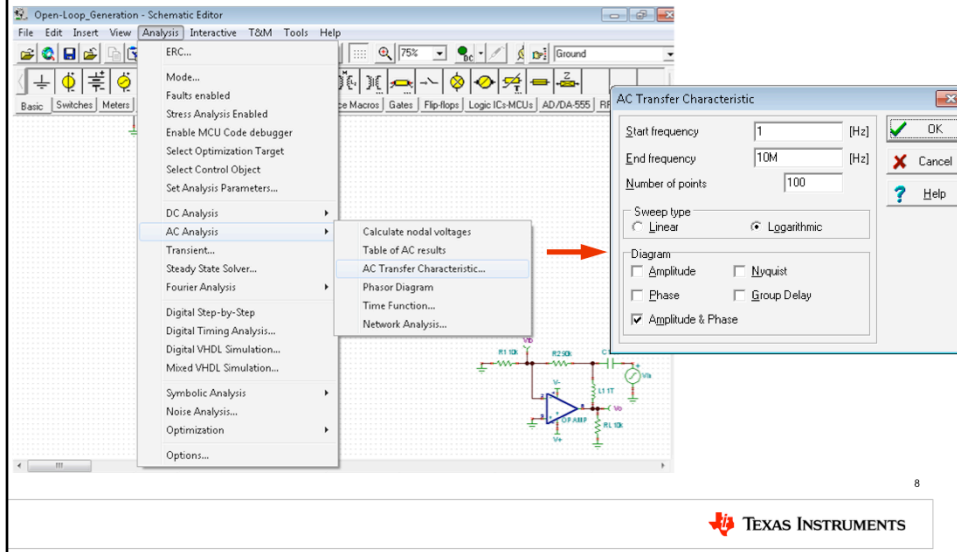
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Before checking the ac behavior of the circuit, a quick check of the dc operating point should be performed. Simply click Analysis, DC Analysis, Calculate Nodal Voltages to do this. Vfb should show the input offset voltage, or Vos, of the op amp, while Vo will show Vos multiplied by the closed-loop gain.

Generating Open-Loop Curves

Run an AC transfer characteristic analysis over the appropriate frequency range:
Click **Analysis** → **AC Analysis** → **AC Transfer Characteristic**

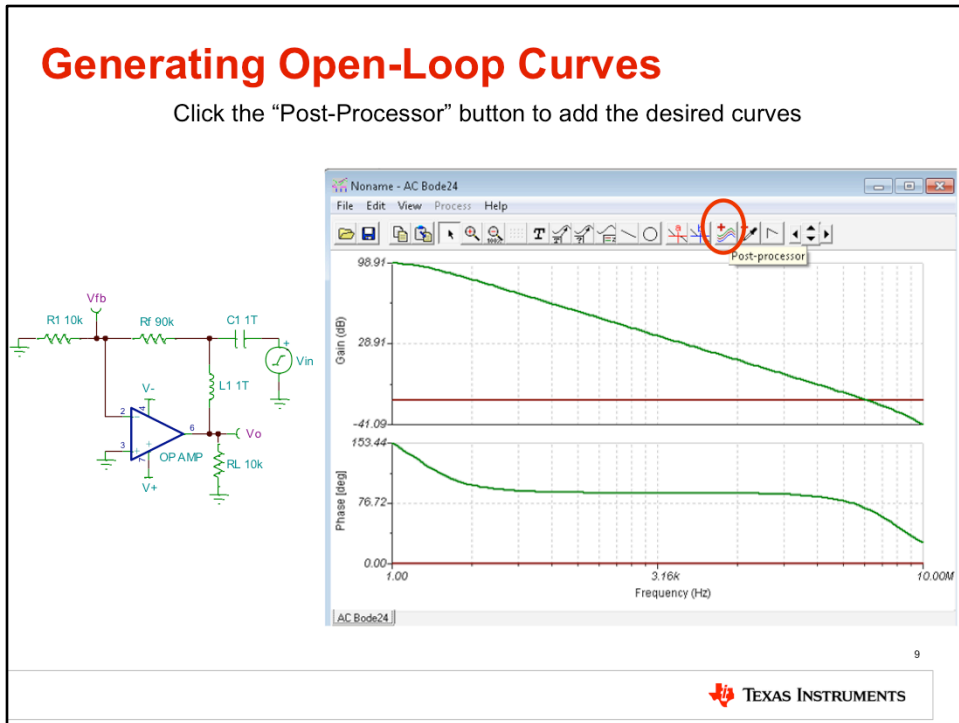


Once you've verified the dc operating point of the circuit, perform an ac transfer characteristic analysis over the op-amp bandwidth. Click Analysis, AC Analysis, AC Transfer Characteristic to do this.

Set the start and end frequencies and then press "OK".

Generating Open-Loop Curves

Click the "Post-Processor" button to add the desired curves

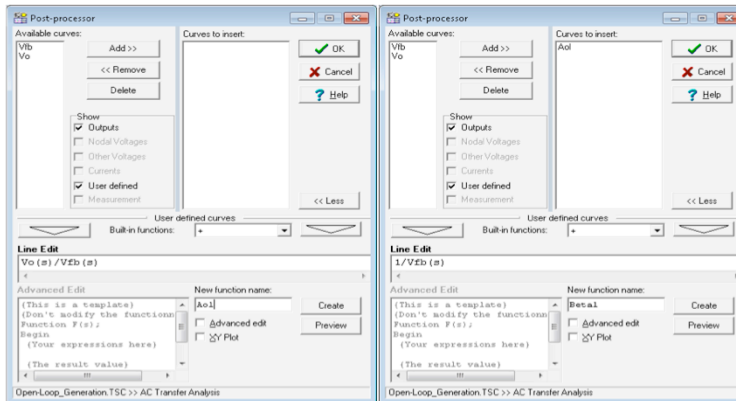


The results for the Vo and Vfb probes will be displayed after the simulation is complete. To add the desired curves for open-loop analysis, click the post-processor button in the result window.

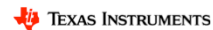
Generating Open-Loop Curves

Click the “Post-Processor” button to add the desired curves

$$A_{OL_LOADED} = V_o / V_{fb}$$
$$1/\beta = 1 / V_{fb}$$
$$A_{OL}\beta = V_o$$



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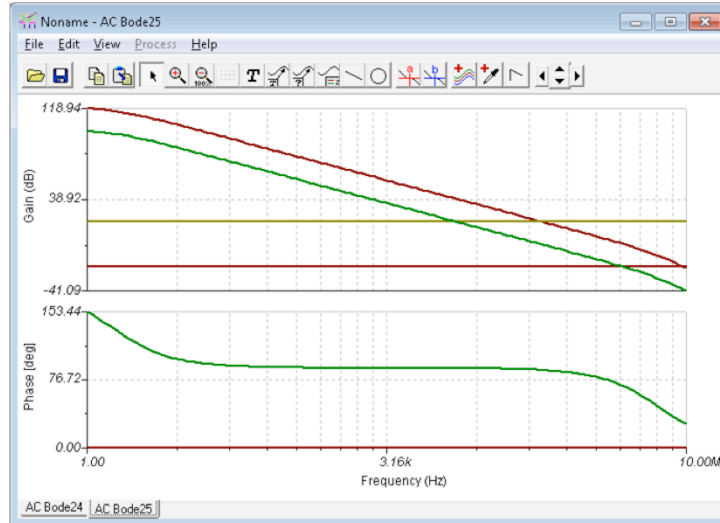


Write the proper equations for Aol and $1/\beta$ in the line editor, name them, and then create the curves. A new curve can be added for $A_{ol}\beta$, but since it equals “Vo” which is already displayed, this is not necessary.

Please note, the editor will not allow the entry in the “New Function Name” box to begin with a number or have special characters. Therefore “1/Beta”, or “1Beta” are not allowed. We recommend to use “Beta1” for the 1/Beta curve name.

Generating Open-Loop Curves

Unformatted results with all curves:



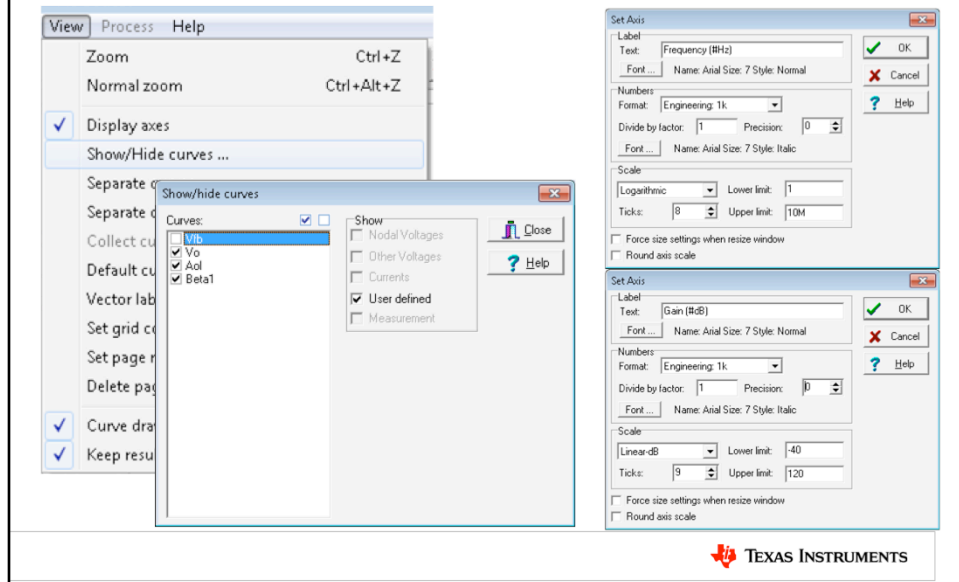
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Here's what the results will look like with the new curves added. The next steps will format the results to make them easier to view.

Generating Open-Loop Curves

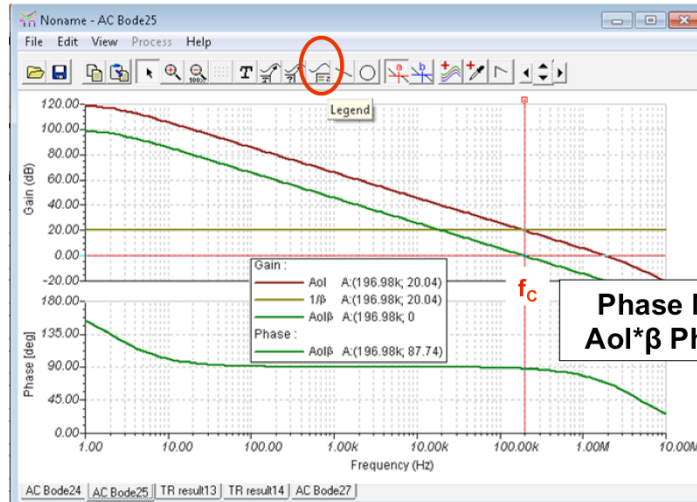
Remove undesired curves and format axis for easier viewing:



Click View, then Show/Hide curves. Select only the curves Vo, Aol, and Beta1. Then, double-click the x-axis and y-axis to bring up the “Set Axis” window. Change the x-axis to a logarithmic scale, 8 ticks, lower limit 1Hz, upper limit 10MHz. Change the y-axis to a linear-in-dB scale, 9 ticks, lower limit -40dB, upper limit 120dB.

Generating Open-Loop Curves

Use a cursor to determine the frequency where $Aol\beta = 0\text{dB}$, f_c , and place legend to show corresponding magnitudes and phases



Phase Margin =
 $Aol\beta$ Phase @ f_c

The final step is to measure the phase margin on the curves. First, place a cursor on the $Aol\beta$ curve and then type "0" into the "Y:" text box to set the cursor to the f_c frequency. Then either place a second cursor on the $Aol\beta$ curve to directly measure the $Aol\beta$ phase or as shown here, click the "Legend" button and place it on the screen which will display the magnitude and phase of all of the visible curves at f_c . The phase margin is the phase of $Aol\beta$ at f_c , which is 87.7 degrees in this example.

The easiest method is to place a cursor on the $Aol\beta$ curve and then type "0" into the "y:" text box to set the cursor to the f_c frequency. Then click the "Legend" button and place it on the screen which will display the magnitude and phase of the curves at f_c . The phase margin is the phase of $Aol\beta$ at f_c , which is 87.7 degrees in this example.

**Thanks for your time!
Please try the quiz.**

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In summary, this video described the methods to break the loop of standard op amp circuits and perform open-loop ac analysis. The next video will review indirect methods to test for op amp stability, including transient and ac transfer function measurements and simulations.

Thank you for time! Please try the quiz to check your understanding of this video's content.

Stability 3

Multiple Choice Quiz

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Quiz: Stability 3

1. (T/F) An open-loop circuit is required to generate the A_{ol} , $1/\beta$ and $A_{ol} \cdot \beta$ curves.
 - a. True
 - b. False

2. (T/F) The DC operating point of a circuit will not affect open-loop simulation results.
 - a. True
 - b. False

3. (T/F) Once the feedback loop is broken, a small-signal source is injected into the:
 - a. Low Impedance node
 - b. High Impedance node
 - c. Power Supply

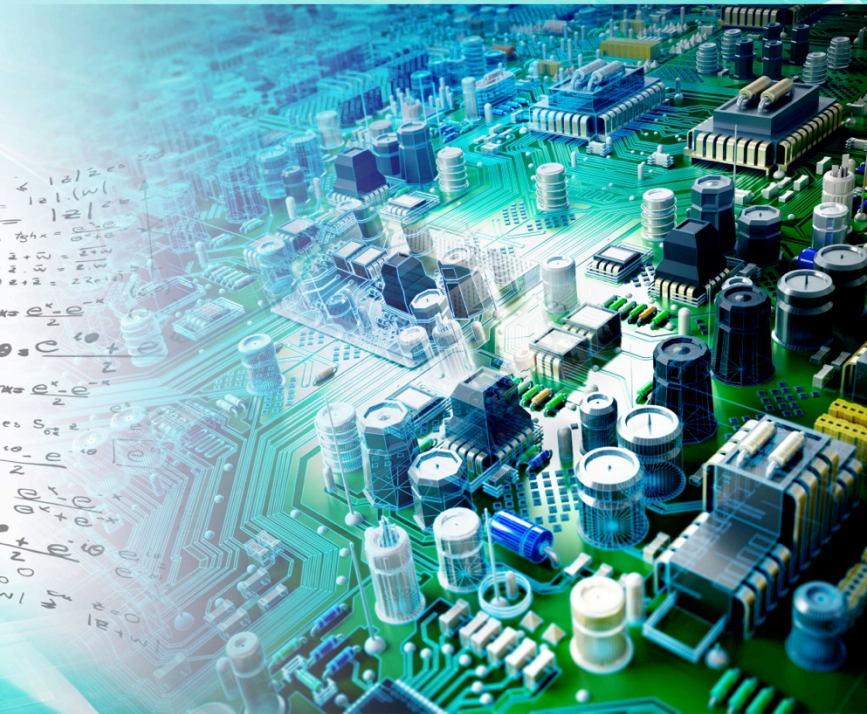
Quiz: Stability 3

- 4. For proper open-loop simulation the simulation circuit must be:**
- a. Open-loop for dc and open-loop for ac frequencies
 - b. Open-loop for dc and closed-loop for ac frequencies
 - c. Closed-loop for dc and closed-loop for ac frequencies
 - d. Closed-loop for dc and open-loop for ac frequencies

Stability 3

Multiple Choice Quiz: Solutions

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Quiz: Stability 3

1. (T/F) An open-loop circuit is required to generate the A_{ol} , $1/\beta$ and $A_{ol} \cdot \beta$ curves.

- a. True
- b. False

2. (T/F) The DC operating point of a circuit will not affect open-loop simulation results.

- a. True
- b. False

3. (T/F) Once the feedback loop is broken, a small-signal source is injected into the:

- a. Low Impedance node
- b. High Impedance node
- c. Power Supply

Quiz: Stability 3

4. For proper open-loop simulation the simulation circuit must be:

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- d. Closed-loop for dc and open-loop for ac frequencies**

Stability 3

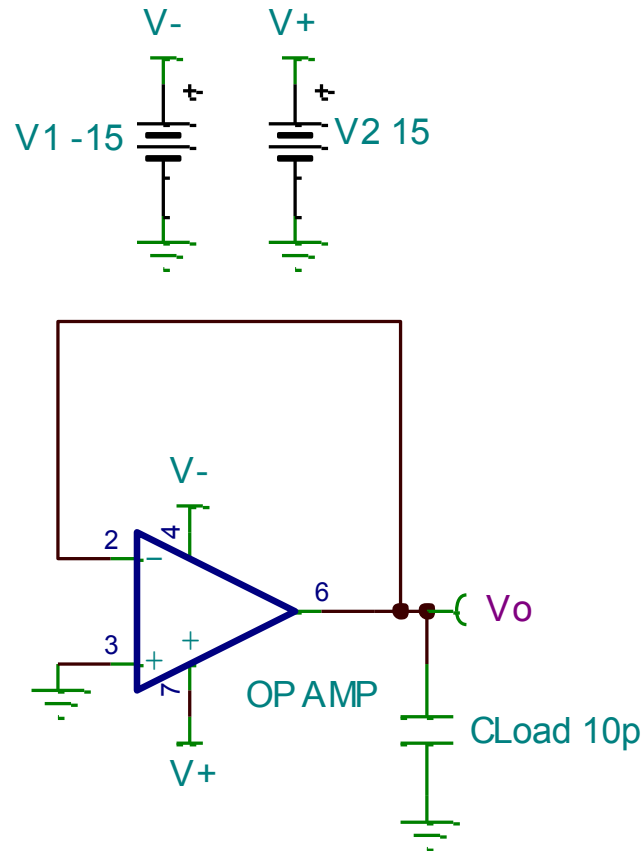
Exercises

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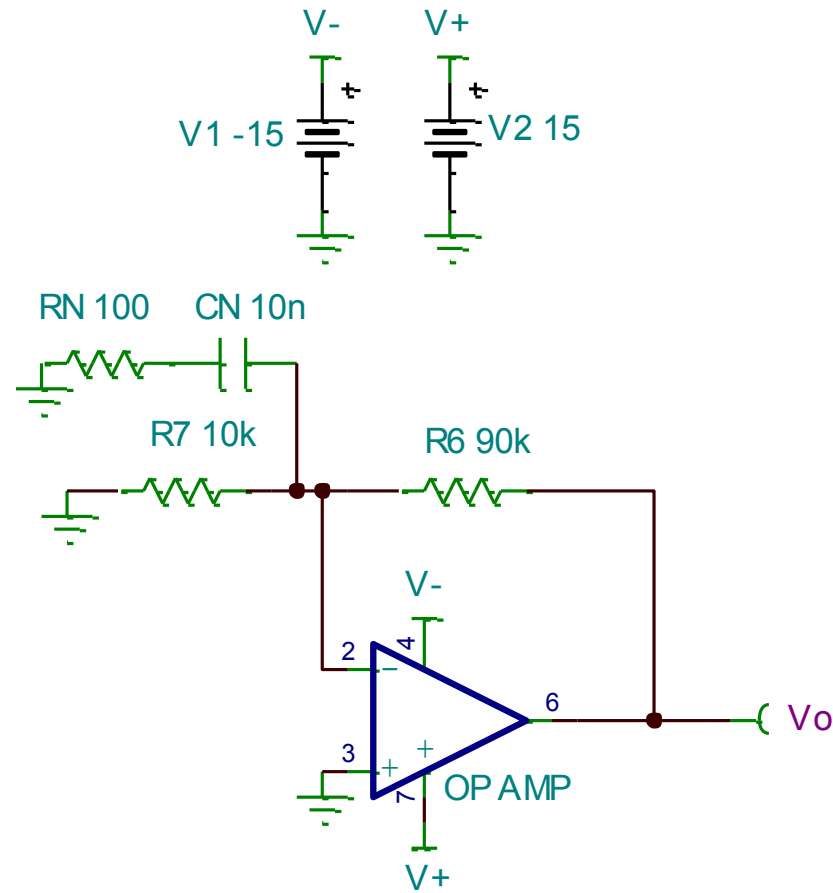
1. Simulate the Loop-Gain ($A_{ol}\beta$) Phase Margin for the circuit below with the following capacitive loads:

- a.) 10pF
- b.) 100pF
- c.) 1nF



1333 - Stability 3 - Problem 1.TSC

2. Simulate the Loop-Gain ($A_oI\beta$) Phase Margin for the circuit below.



1333 - Stability 3 - Problem 2.TSC

Stability 3

Solutions

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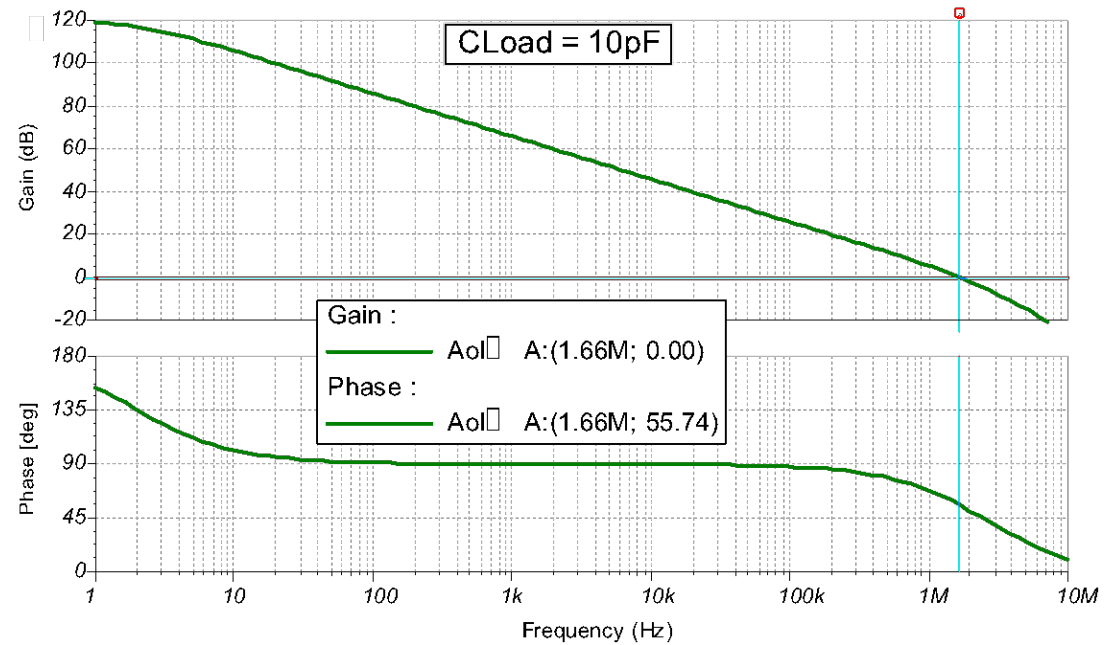
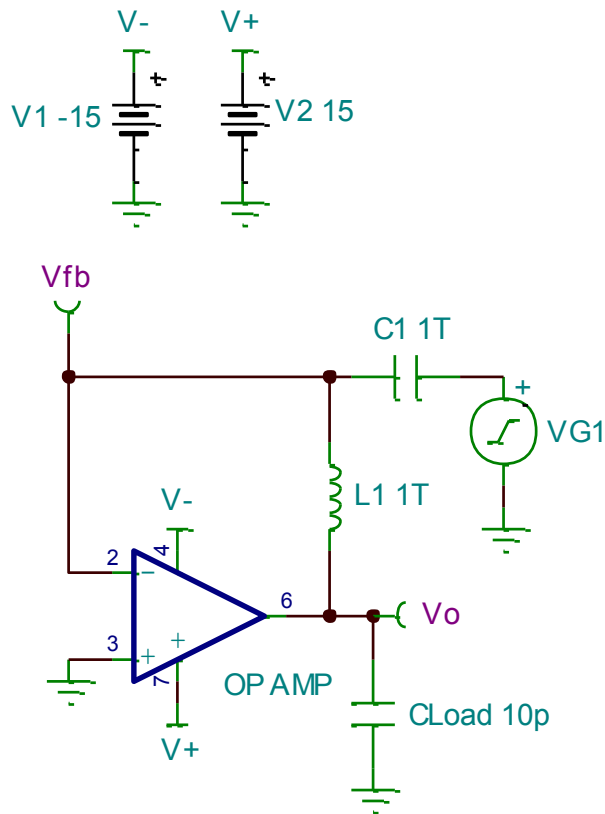


1. Simulate the Loop-Gain ($Aol\beta$) Phase Margin for the circuit below with the following capacitive loads:

- a.) 10pF **55.7°**
- b.) 100pF **50.5°**
- c.) 1nF **21.5°**

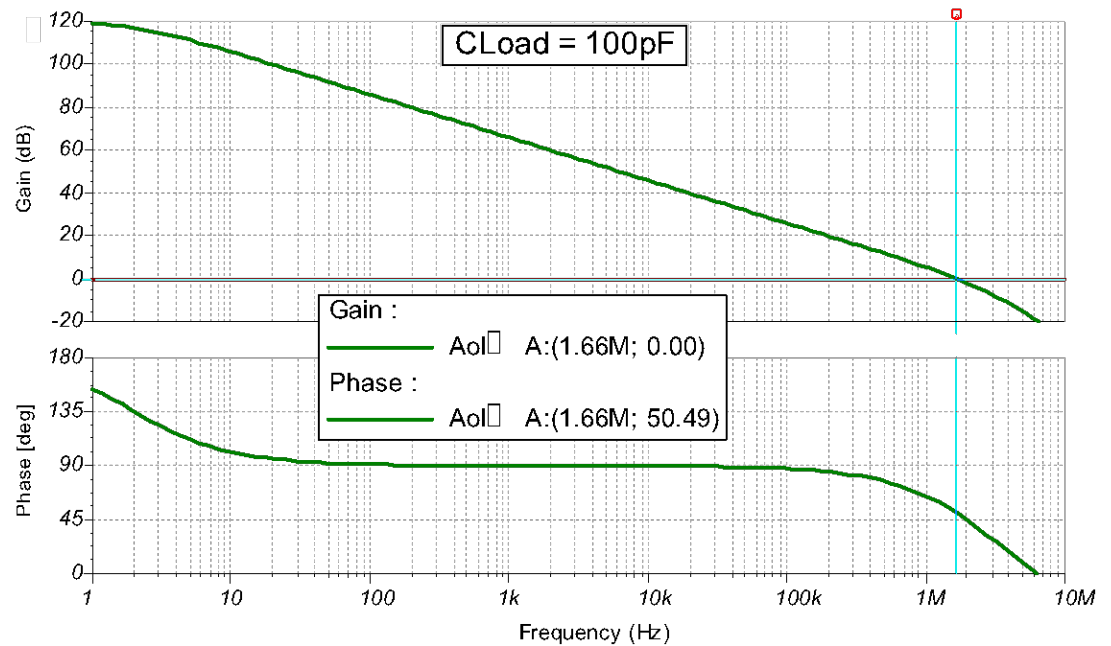
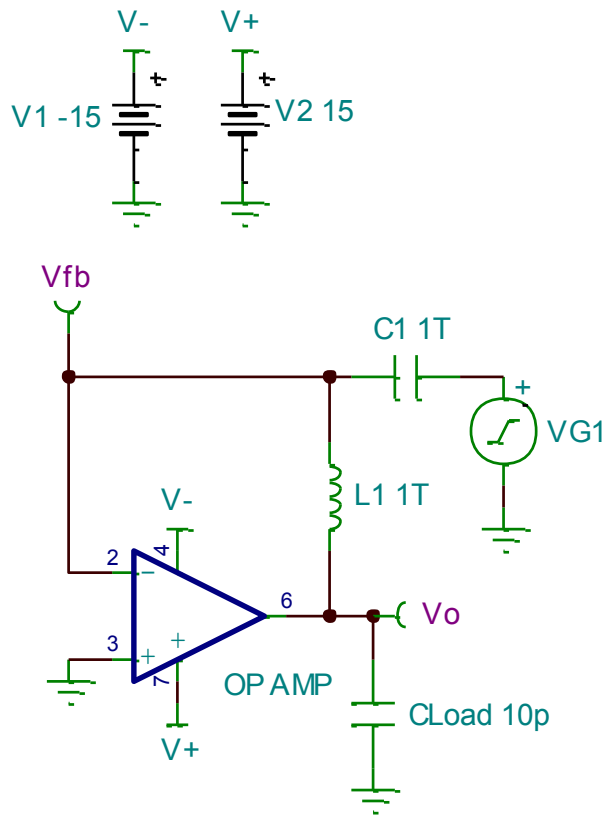


1333 - Stability 3 - Problem 1 -Solution.TSC



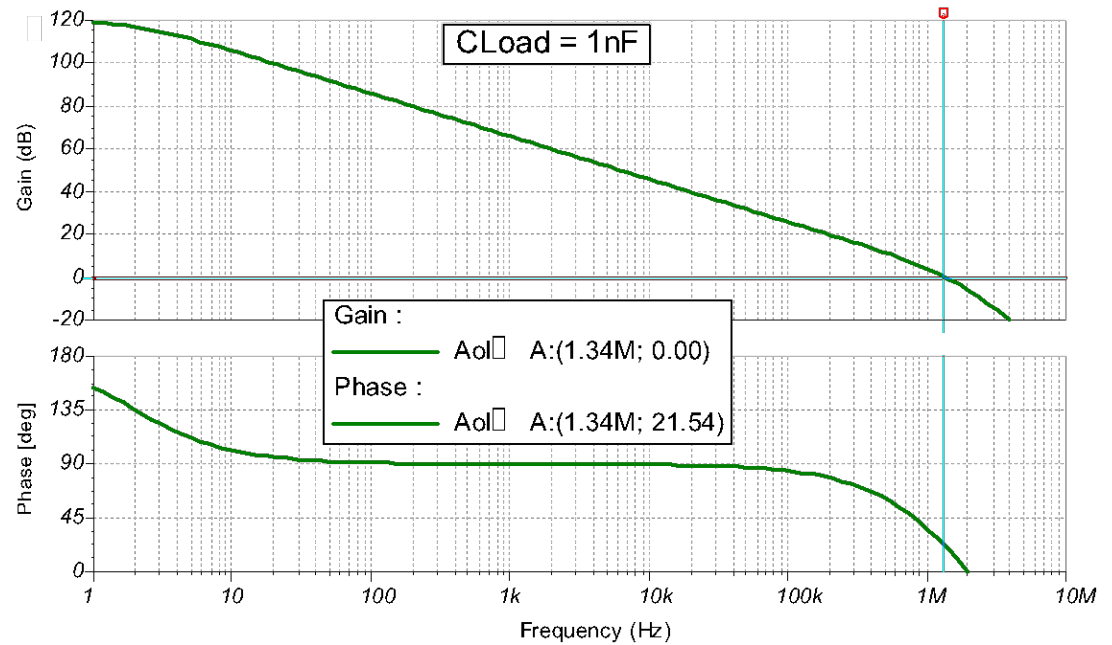
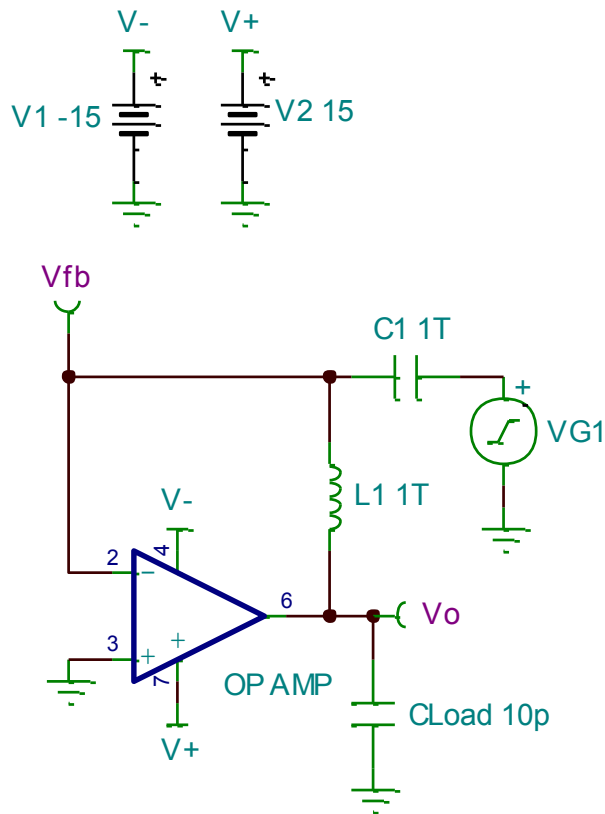
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- a.) 10pF **55.7°**
- b.) 100pF **50.5°**
- c.) **1nF** **21.5°**



2. Simulate the Loop-Gain ($Aol\beta$) Phase Margin for the circuit below.

Phase Margin = 11.8°



1333 - Stability 3 - Problem 2 -Solution.TSC

