

Introduction to SAR ADC Component Selection

TIPL 4401

TI Precision Labs – ADCs

Created by Art Kay

Presented by Peggy Liska

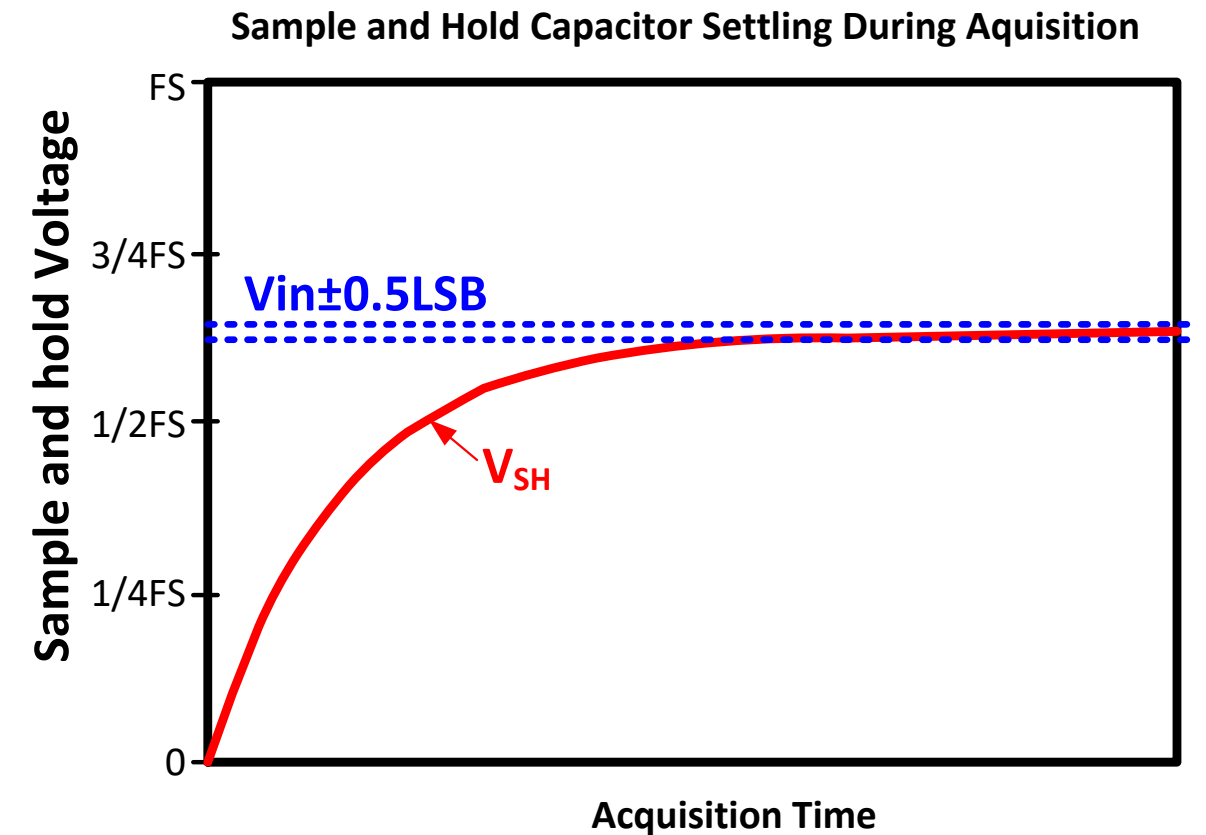
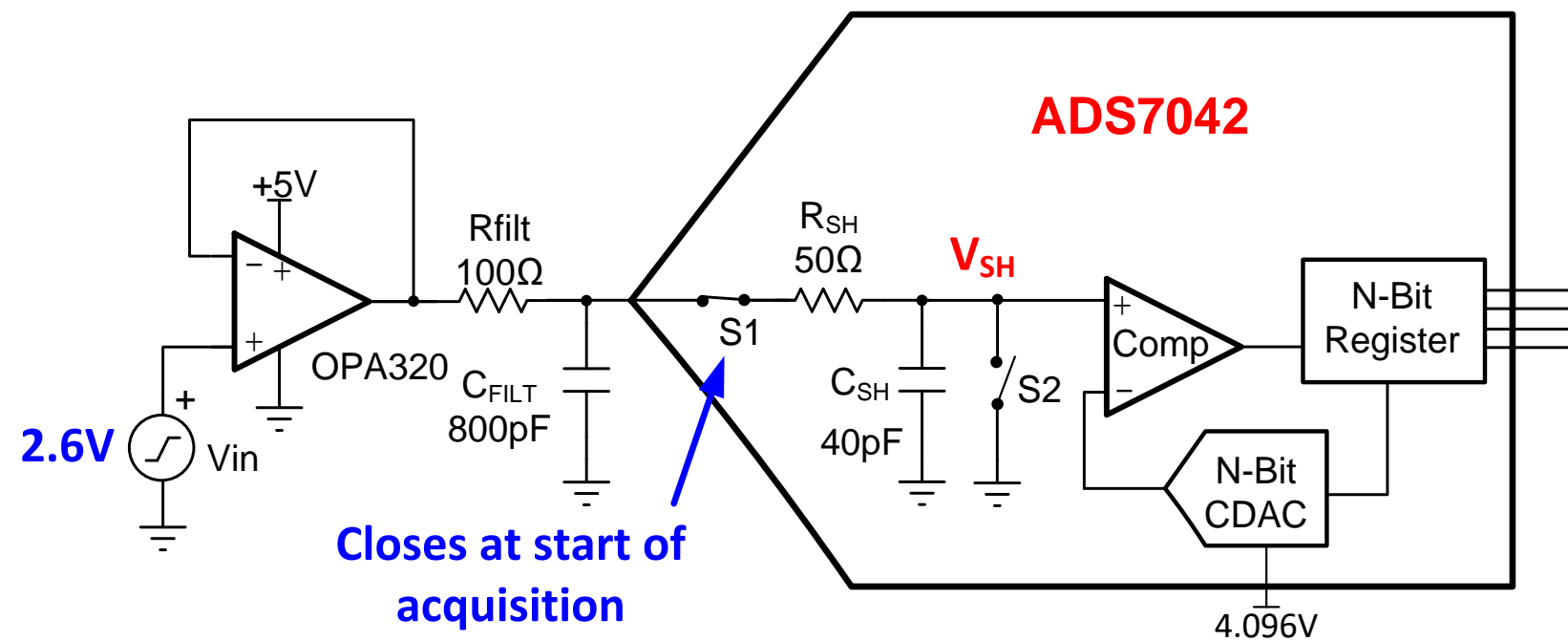
Agenda – Next several videos

1. SAR Operation Overview
2. Select the data converter
3. Use the Calculator to find amplifier and RC filter
4. Find the Op Amp
5. Verify the Op Amp Model
6. Building the SAR Model
7. Refine the Rfilt and Cfilt values
8. Final simulations
9. Measured Results
10. SAR Drive Calculator Algorithm

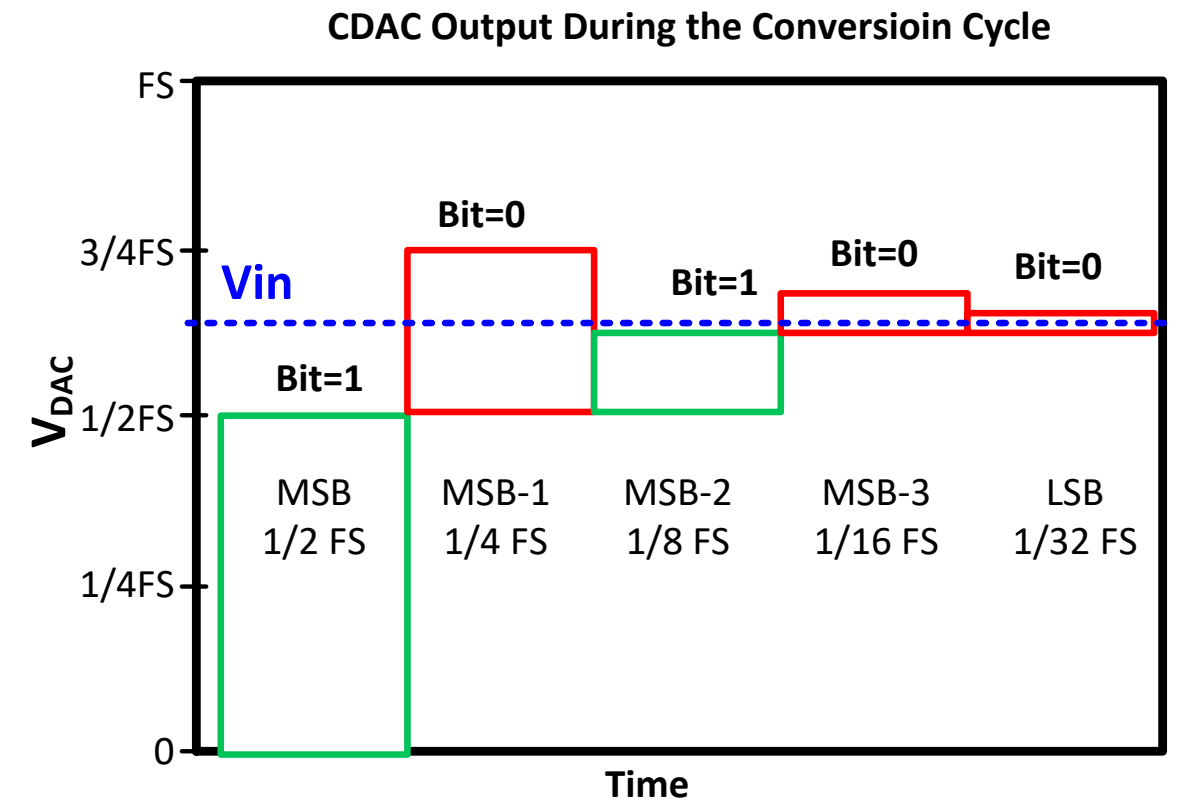
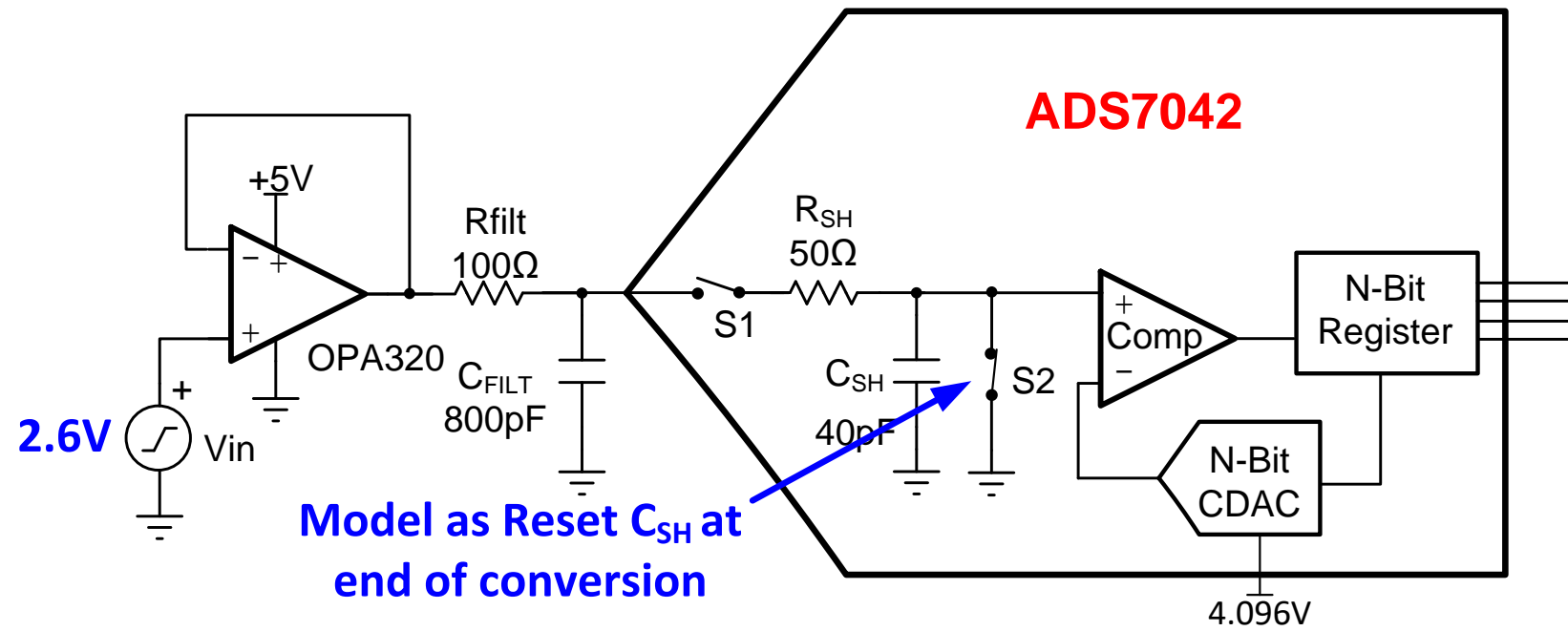
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Acquisition phase

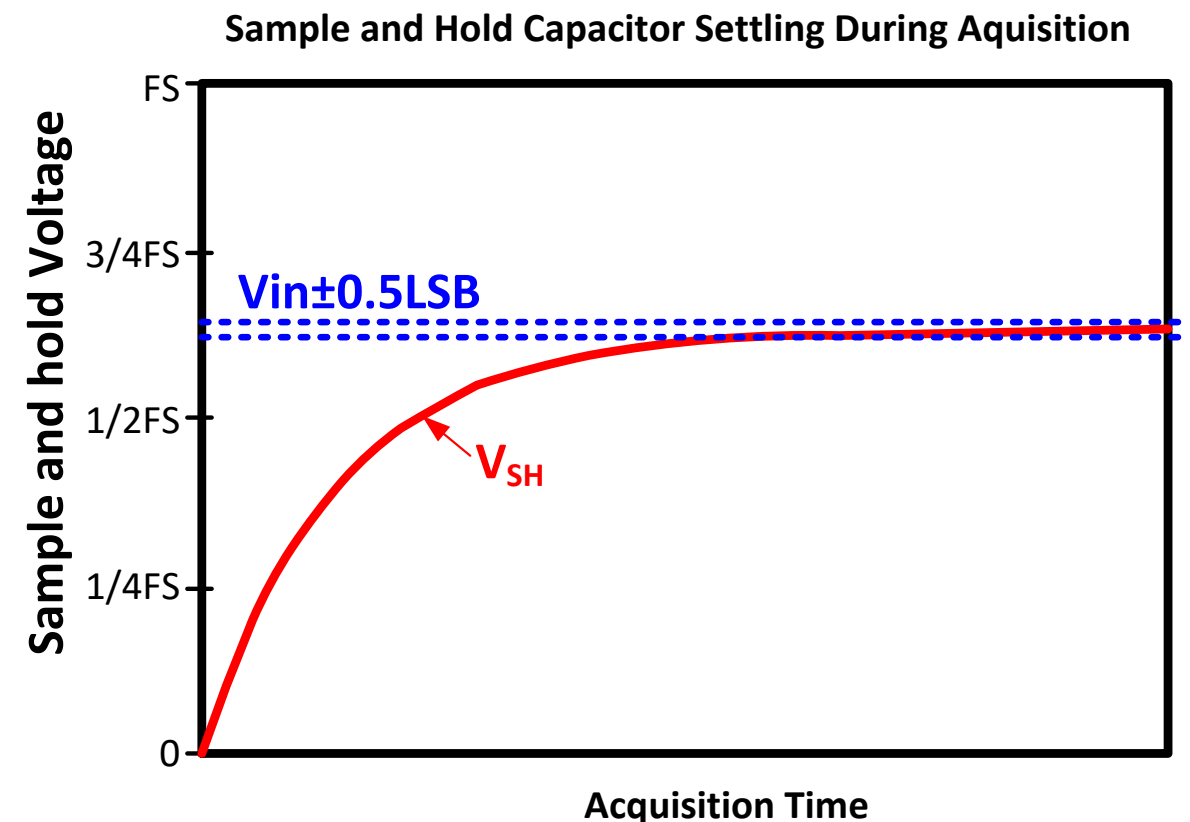
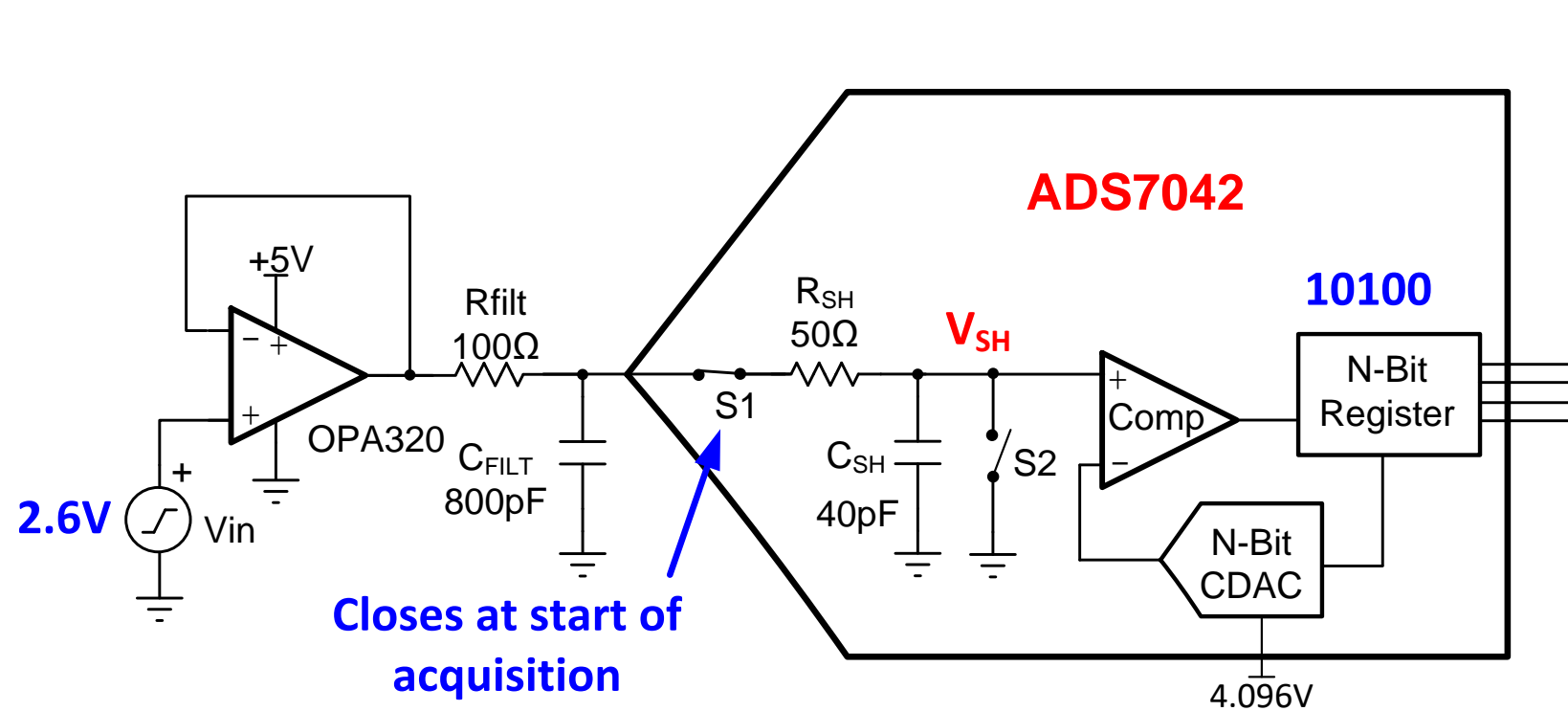


Conversion Phase

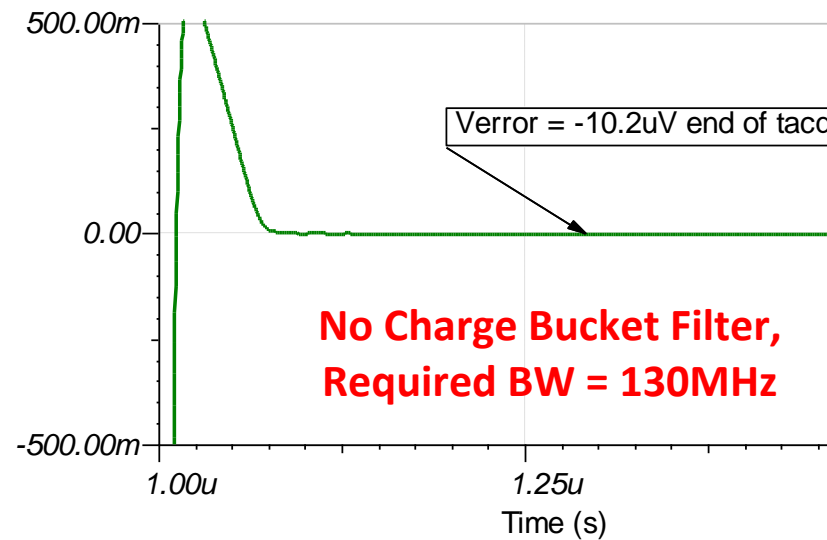
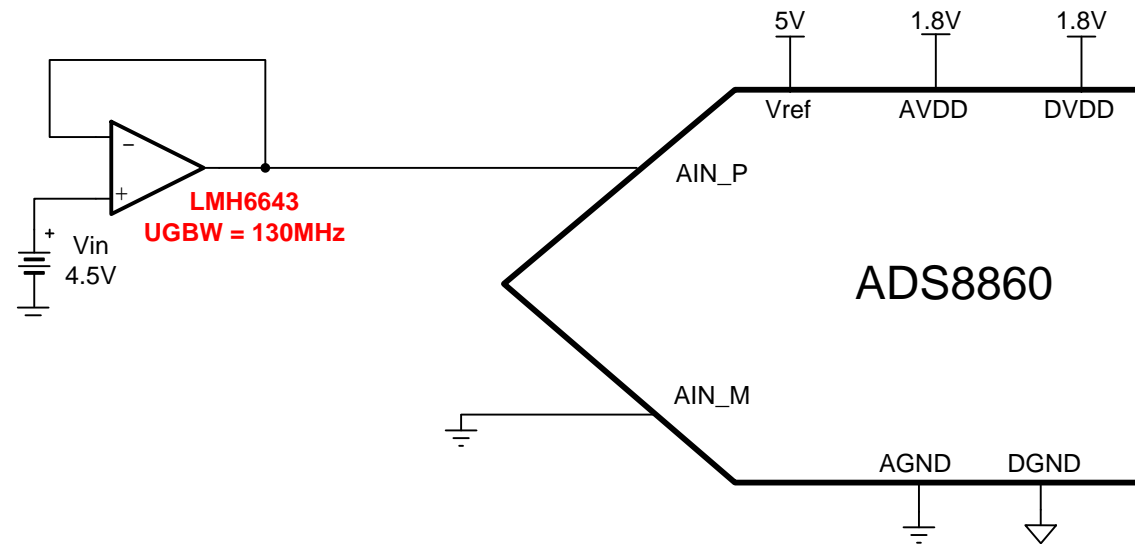


Overall Objective

- Find R_{filt} and C_{filt} charge bucket filter that will optimize settling
- Find amplifier with bandwidth sufficient for settling
- Achieve final settling of 0.5LSB or better at end of t_{acq}

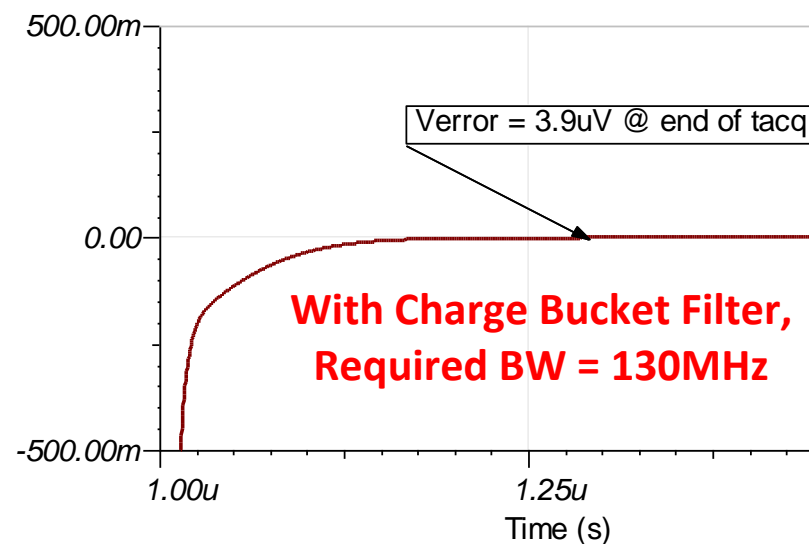
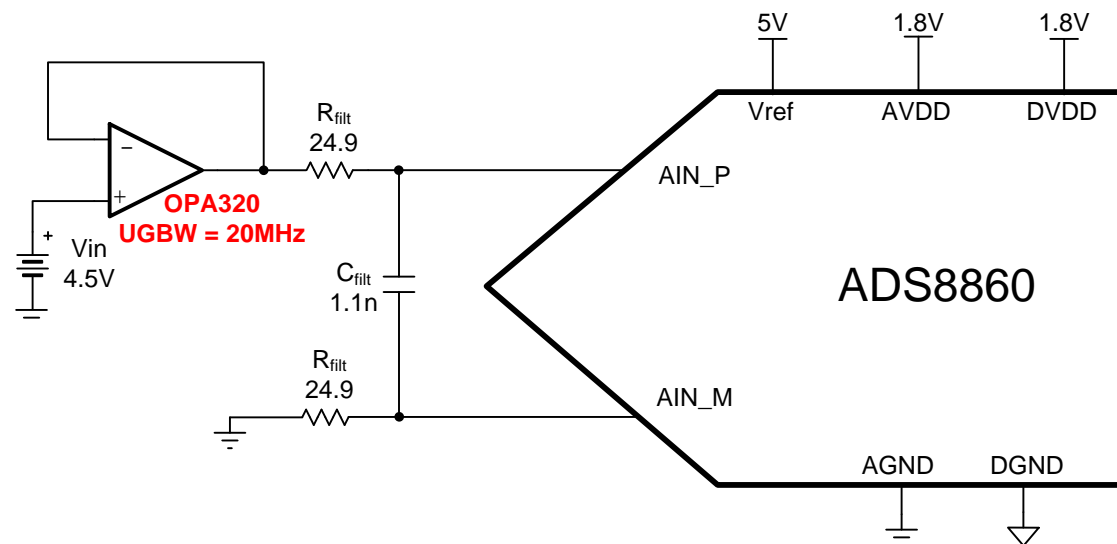


Is the charge bucket filter required?



Advantage of low BW Amp

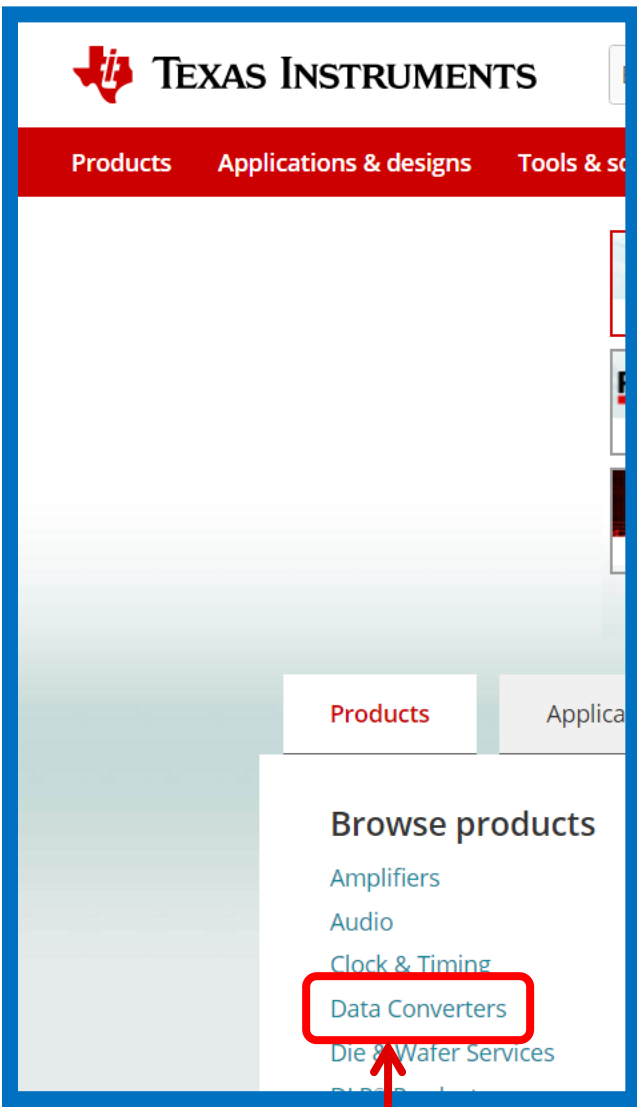
- Lower Iq
- Better Vos, Ib
- Lower cost
- Less sensitive to stability issues



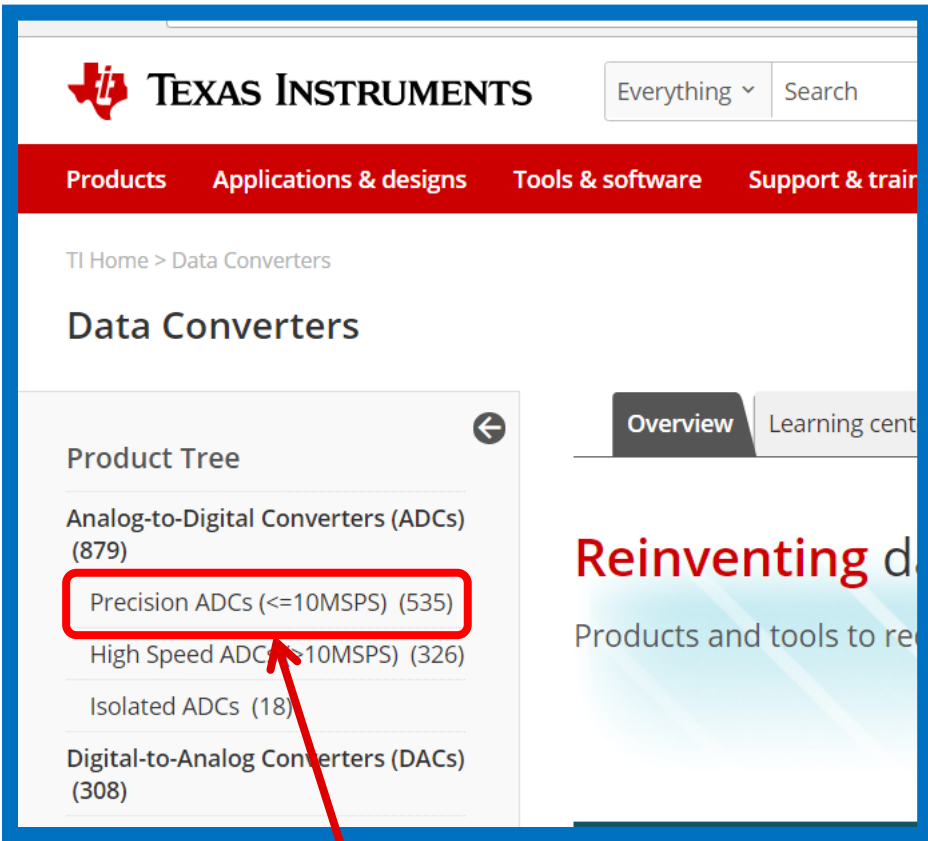
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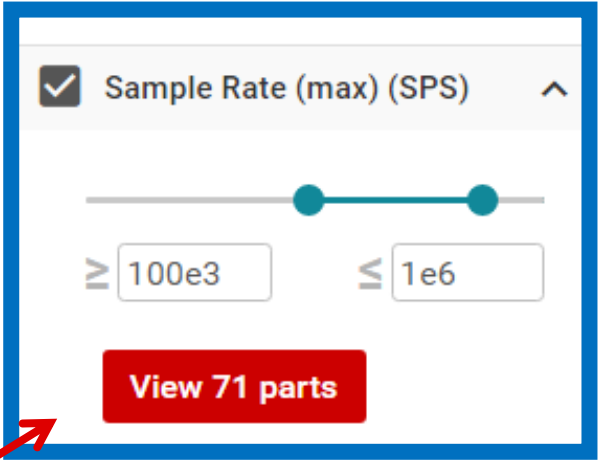
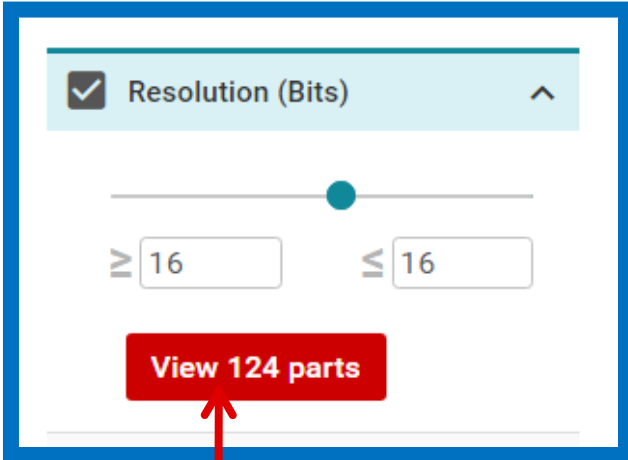
Find the data converter



Select Data Converters



Select "Precision ADC"
Operational Amplifiers (Op Amps)
535 different choices!



Continue to refine selection

Design Goal:
#Bits = 16
100kSPS < Sample Rate <1MSPS
Single Ended Input
5V input range
SPI interface

Find the data converter

Input Channels

≥ 1 ≤ 1

View 42 parts

Input Range (Max) (V)

≥ 0.0195 ≤ 5

View 17 parts

Interface

- Byte-wide
- I2C
- Microwire (Serial I/O)
- Parallel
- QSPI
- SPI
- Serial

View 11 parts

Input Type

OR

- Differential
- Pseudo-Differential
- Single-Ended

View 4 parts

Continue to refine selection

4 matching parts out of 535 total parts

Compare	Part Number	Resolution (Bits)	Sample Rate (max) (SPS)	# Input Channels	Multi-Channel Configuration	Input Range (Min) (V)	Input Range (Max) (V)	Interface	Integrated Features	Analog Voltage AVDD (Min) (V)	Analog Voltage AVDD (Max) (V)	Architecture	Rating	Operating Temperature Range (C)	Package Group
<input type="checkbox"/>	ADS8866 - 16-Bit, 100-kSPS, Serial Interface, microPower, Miniature, Single-Ended Input, SAR Analog-to-Digital	16	100kSPS	1	N/A	0	5	SPI	Daisy-Chainable, Oscillator	2.7	3.6	SAR	Catalog	-40 to 85	VSSOP, VSON
<input type="checkbox"/>	ADS8864 - 16-Bit, 400-kSPS, Serial Interface, microPower, Miniature, Single-Ended Input, SAR ADC	16	400kSPS	1	N/A	0	5	SPI	Daisy-Chainable, Oscillator	2.7	3.6	SAR	Catalog	-40 to 85	VSON, VSSOP
<input type="checkbox"/>	ADS8862 - 16-Bit, 680-kSPS, Serial Interface, uPower, Miniature, Single-Ended, Differential Input SAR ADC	16	680kSPS	1	N/A	0	5	SPI	Daisy-Chainable, Oscillator	2.7	3.6	SAR	Catalog	-40 to 85	VSON, VSSOP
<input type="checkbox"/>	ADS8860 - 16 bit 1 MSPS, Serial, Pseudo-Differential Input, Micro Power, Miniature, SAR ADC	16	1MSPS	1	N/A	0	5	SPI	Daisy-Chainable, Oscillator	2.7	3.6	SAR	Catalog	-40 to 85	VSON, VSSOP

ADS8860
Choose the data converter with the highest sample rate from this group

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Information needed from the data sheet

Full Scale Range (FSR)	The range of voltage that is applied to the converter for valid conversions. Typically this is V_{ref} or a multiple of V_{ref} .
Resolution	The number of bits used to represent the digital equivalent of the equivalent analog signal. In this example we use a 16 bit converter that has 2^{16} or 65536 codes.
C_{sh}	Sample and Hold capacitance. Sometimes called C_{in} . Typically between 10pF and 100pF.
R_{sh}	On-resistance for sample and hold switch. Typically between 10 ohms and 100 ohms. Normally, this information is in the data sheet equivalent circuit.
t_{acq}	Acquisition time. This is duration that the sample and hold switch is closed. A longer acquisition time makes it easier to settle. The data sheet provides a minimum acquisition time that corresponds to the maximum throughput (samples / second).

Example: Full Scale Range, Resolution, C_{sh} , R_{sh}

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Full-scale input span ⁽¹⁾	AINP – AINN	0		V_{REF}	V
Operating input range ⁽¹⁾	AINP	-0.1		$V_{REF} + 0.1$	V
	AINN	-0.1		+ 0.1	V
C_I Input capacitance	AINP and AINN terminal to GND		59		pF
Input leakage current	During acquisition for dc input		5		nA
SYSTEM PERFORMANCE					
Resolution			16		Bits

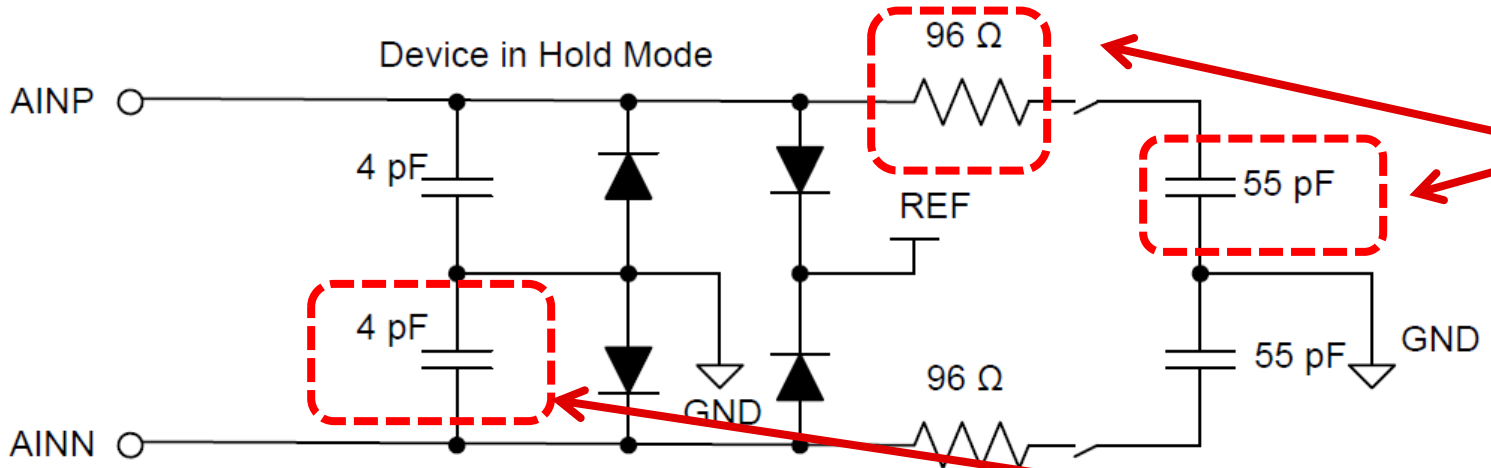


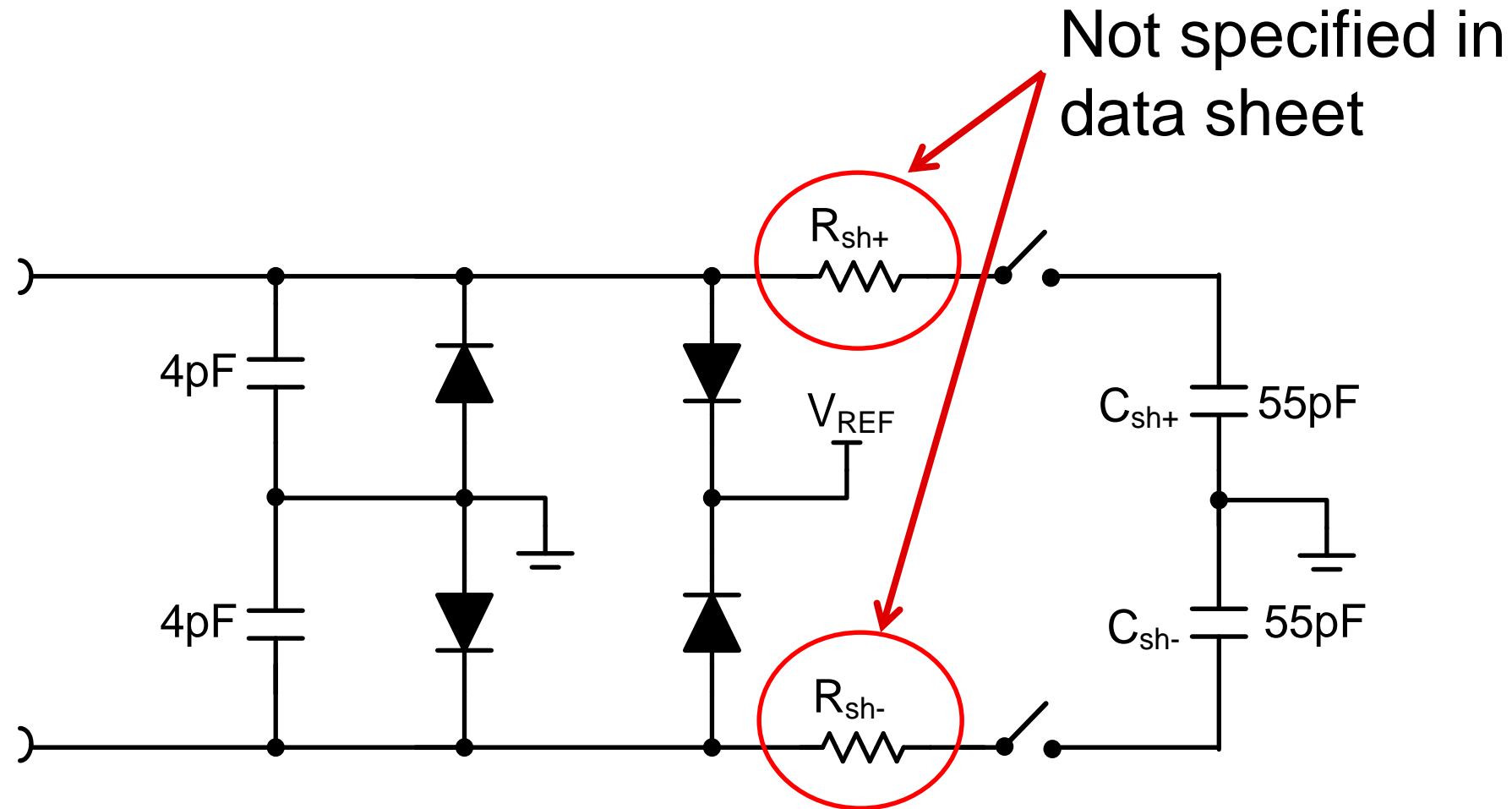
Figure 45. Input Sampling Stage Equivalent Circuit

C_{sh} and R_{sh} can usually be found in the equivalent circuit.

Note: C_I from the table
 $C_I = 55pF + 4pF$

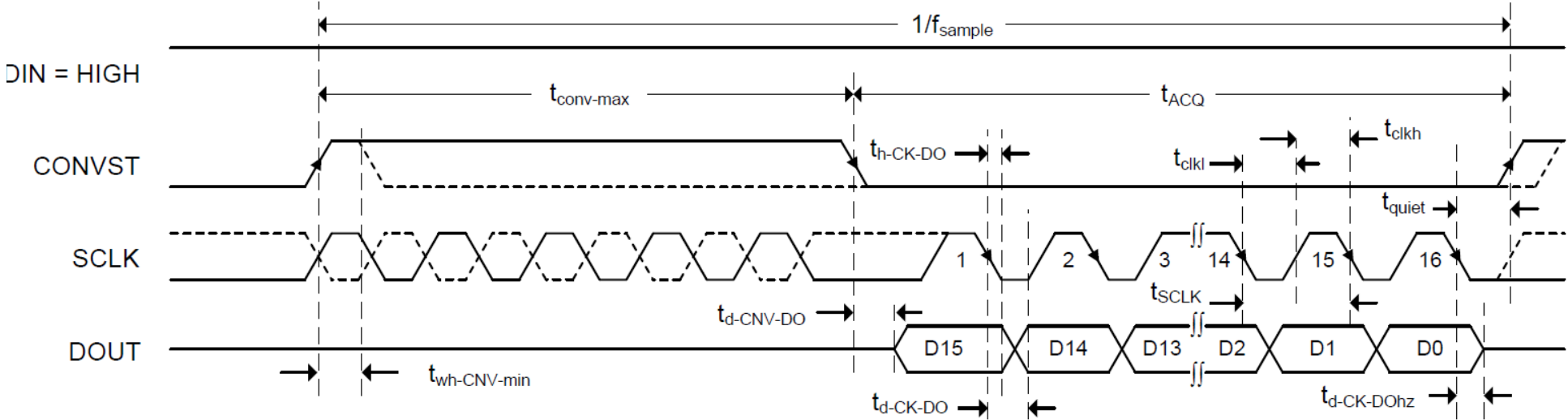
Full Scale Range and resolution

If the data sheet doesn't provide R_{sh}



$$R_{sh} \approx \frac{t_{acq_min}}{100 \cdot C_{sh}}$$
$$R_{sh} \approx \frac{290ns}{100 \cdot 55pF} = 53\Omega$$

For our example: acquisition time



Conversion time set by internal clock. The maximum time for conversion is 710ns.

PARAMETER		MIN	TYP	MAX	UNIT
t_{ACQ}	Acquisition time	290			ns
t_{conv}	Conversion time	500		710	ns

We are running at maximum throughput (1MHz)
 $1/f_{\text{sample}} = t_{\text{conv-max}} + t_{\text{acq-min}} = 710\text{ns} + 290\text{ns} = 1\mu\text{s}$, or $f_{\text{sample}} = 1\text{MHz}$

For cases where you aren't running at maximum throughput (e.g. 500kHz)
 $t_{\text{acq}} = 1/f_{\text{sample}} - t_{\text{conv-max}} = (1/500\text{kHz}) - 710\text{ns} = 1290\text{ns}$

Run the “ADC SAR Drive” tool: ADS8860 Example

1. Enter the information from the ADS8860 Data Sheet.

2. Results will be used in the simulation

Single Ended #2: Includes Ground Sense (Negative Input)

Agenda – next video...

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Thanks for your time!
Please try the quiz.

Quiz: Introduction to SAR ADC Component Selection

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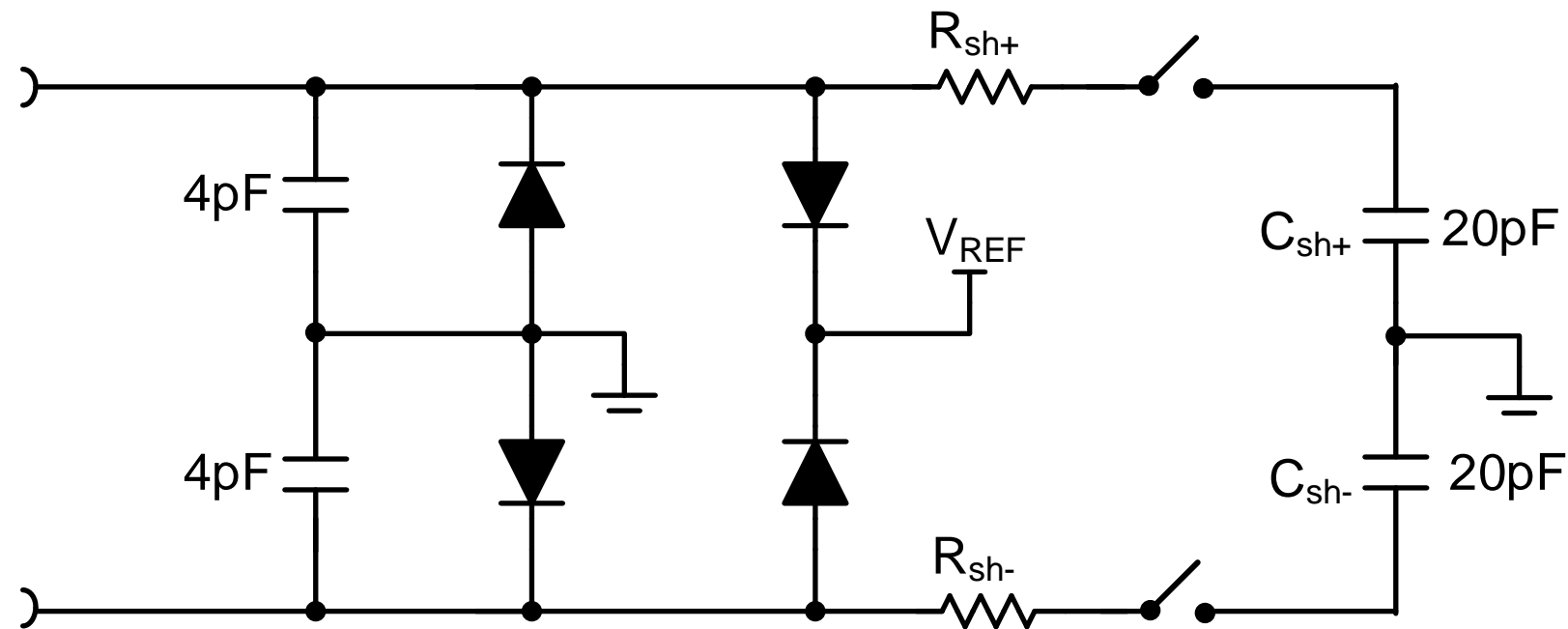
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1. The SAR data converter throughput is set by the _____.
 - a) Acquisition and communications phase.
 - b) Reference and conversion phase.
 - c) Acquisition and conversion phase.
 - d) None of the above.

2. SAR data converters with short acquisition time will need a driver amplifier with _____.
 - a) High bandwidth.
 - b) High slew rate.
 - c) Good output swing.
 - d) Low noise.

Quiz: Introduction to SAR ADC Component Selection

3. The data sheet for the input circuit below does not specify R_{sh} . What is a good estimate for R_{sh} ? Assume $t_{acq_min} = 150\text{ns}$.
- a) 25 ohms.
 - b) 50 ohms.
 - c) 75 ohms.
 - d) 100 ohms.



Quiz: Introduction to SAR ADC Component Selection

4. Use the calculator to find an amplifier and RC range for a converter with the following specifications: ADS7056, Single Ended, 14 bit, 2.5Msps, $t_{acq_min} = 95\text{ns}$, FSR = 3.3V, and $C_{sh} = 16\text{pF}$.

Solutions

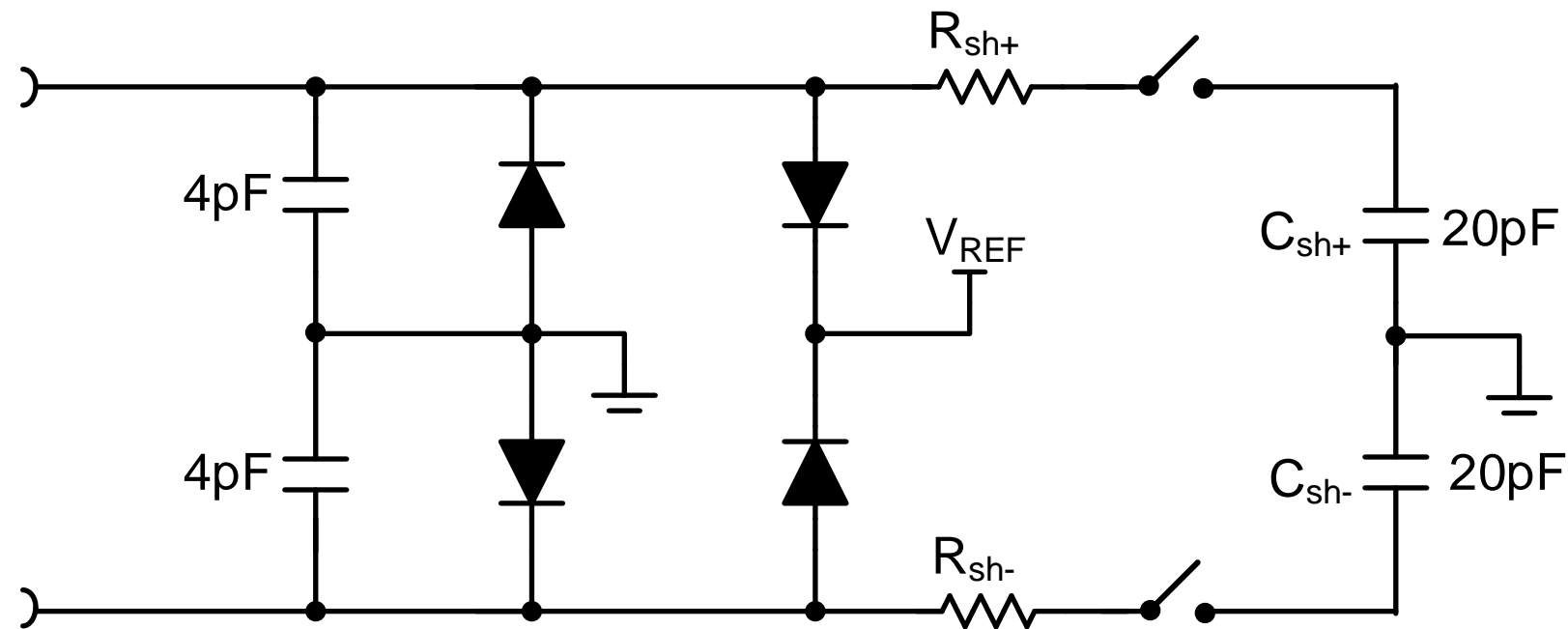
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The screenshot shows the 'Analog Engineer's Calculator' interface. On the left, a tree view shows 'Data Converters' > 'ADC SAR Drive' selected. The main window is divided into a 'Select the Calculator' pane and a 'Calculator' pane. The 'Calculator' pane has the following settings:

- Select Type: Single Ended #2
- Resolution: 14
- Csh: 16p F
- Full Scale Range: 3.3 V
- Acquisition Time: 95n s
- Rfilt/2 Min: 5.2 Ohm
- Cfilt: 330p F
- Rfilt/2 Max: 41.7 Ohm
- Optional Cmin: 160p F
- Gain Bandwidth: 47.7M Hz
- Optional Cmax: 470p F
- Max Error Target: 100.7u V

Buttons for 'OK' and 'Help' are at the bottom. To the right, a circuit diagram shows an op-amp with a +5V supply. The non-inverting input is connected to V_{in} . The inverting input is connected to a network of resistors ($R_{filt/2}$), capacitors (C_{FILT}), and switches ($S1, S2, S3, S4$) leading to sampling capacitors (C_{SH+}, C_{SH-}) and resistors (R_{SH+}, R_{SH-}). The sampling capacitors are connected to the ADC's V_{sh+} and V_{sh-} pins. Below the diagram, the text reads: 'Single Ended #2: Includes Ground Sense (Negative Input)'.