Decoupling capacitors

TI Precision Labs – ADCs

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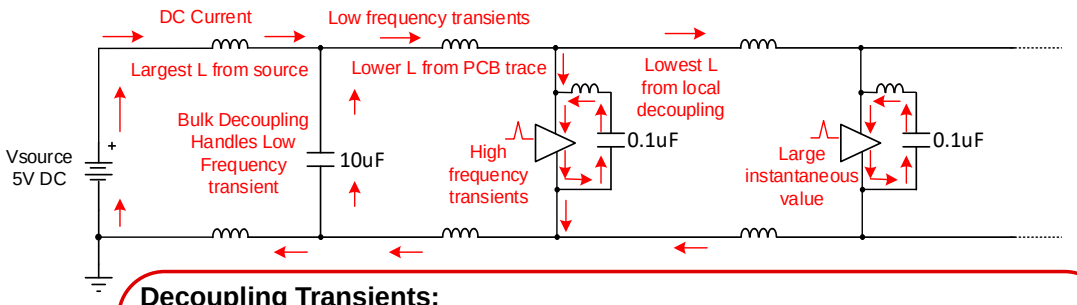
Texas Instruments

Hello, and welcome to the TI Precision Lab video covering decoupling capacitors. This is part of a larger series on PCB layout for good EMC. This series is specifically intended to cover mixed signal designs where the digital signals are less than 100 MHz and clock rise times are greater than 1 ns. This video looks at factors impacting the impedance of the decoupling network, such as PCB trace length, via selection, and capacitor parasitics. The video also covers how current flows relative to the decoupling network and associated power and ground planes. Let's start by looking at the decoupling network from a transient and AC impedance perspective.

Decoupling from a Transient Perspective



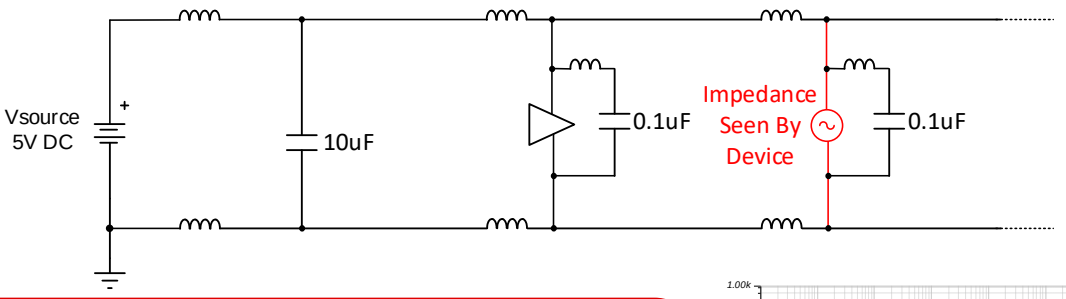
Decoupling Transients:

- Local decoupling provides high frequency transient current
- Instantaneous transient current from device can be high
- Bulk decoupling provides low frequency current
- The source has highest inductance, PCB power traces have lower inductance, and local decoupling has lowest inductance
- Decoupling minimizes noise local to device and minimizes the impact on other devices sharing the power bus

One way to understand how decoupling works is to think of the decoupling network using a transient analysis. The decoupling network has bulk and local decoupling capacitors. Local decoupling capacitors provide high frequency transient current for device power supplies of devices as needed. The instantaneous supply current on digital circuits and switching analog circuits can be quite high. To provide this transient current, the path connecting the local decoupling capacitor to the power and ground pin of a device needs to have the lowest possible inductance. The local decoupling will provide many short transients and the bulk decoupling is a larger capacitor that helps recharge the local decoupling in between transients.

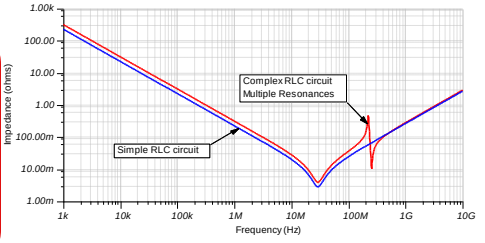
Generally one bulk decoupling capacitor can supply multiple devices and is placed at the power supply entry for the board. Normally the bulk decoupling is sized to be at least 10 times the sum of all the local decoupling. A commonly used bulk capacitor is 10uF and a common local decoupling is 0.1uF or 1uF. The inductance between the power source and bulk decoupling is generally higher than the inductance between the bulk capacitor and the devices, and the inductance between the local decoupling and the device is the lowest. By providing the high frequency transient current the local decoupling minimizes the variation of the local devices power supply voltage. Furthermore, the local decoupling prevents the transient current demand from disrupting the power supply bus and other devices.

Decoupling from an AC Impedance Perspective



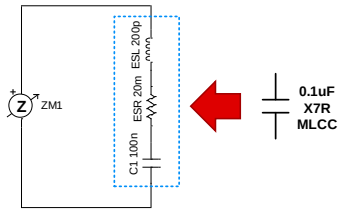
Impedance Seen by Device:

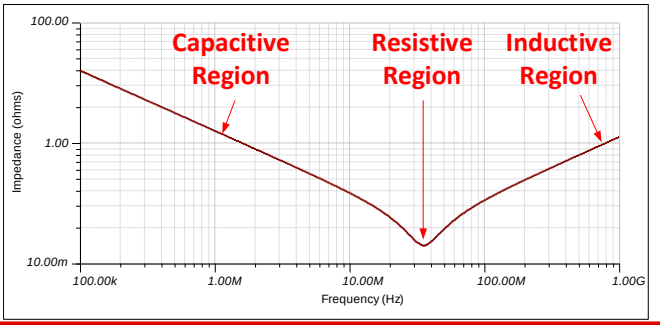
- High impedance at DC
- *Ideally* would have zero impedance at high frequency to short out high frequency transients
- Practical decoupling will be low at high frequency but will begin to increase from parasitic inductance.
- Practical decoupling may have multiple resonant peaks



A different way of looking at decoupling is to consider the AC impedance seen by the device power supply terminals. Ideally this impedance would be high at DC and low at high frequencies to effectively short out power supply transients. From a practical perspective the impedance of the decoupling network will decrease to low levels at high frequency then start to increase again from parasitic inductance. The process of optimizing decoupling is to minimize this parasitic inductance. Also, some decoupling impedance networks will have multiple resonant peaks that can introduce noise problems. We will look at all this in detail.

Model of a practical capacitor



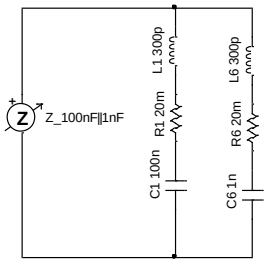


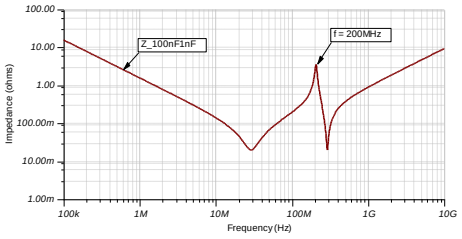
Practical impedance of Capacitor:

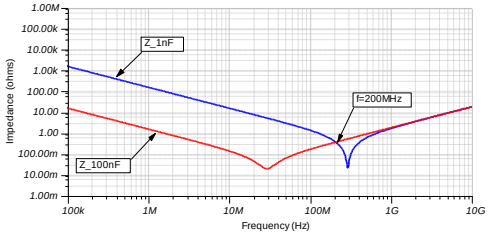
- ESR – parasitic resistance of capacitor
- ESL – parasitic inductance of capacitor
- Practical capacitor acts like capacitor at low frequency and like an inductor at high frequency
- Values shown in this example are typical for a X7R decoupling capacitor
- More accurate models provided by capacitor manufacture.

To understand decoupling it is important to understand a practical model for a capacitor. An ideal capacitor would have capacitor reactance that would always decrease at higher frequency. A real-world capacitor as parasitic resistance called ESR and parasitic inductance called ESL. The impedance of the practical capacitor will decrease until it reaches the ESR limit, than begin to increase because of the ESL. The example shown here is a typical X7R capacitor which is frequently used for decoupling. More sophisticated models are generally provided by the capacitor manufacture.

Resonance from Different Decoupling Capacitors







Don't use two different capacitor values for "better" high frequency bypass

- The practice of using two different parallel capacitors was developed 1970's for through-hole capacitors. It doesn't apply to modern surface mount ceramic
- ESL is relatively independent of capacitance value
  - e.g. ESL for a 100pF, 1000pF, and 10,000pF (25V, 0603, X7R) is approximately the same (ESL ≈ 200pH GRM033R71E103ME14, GRM033R71E102ME14, GRM033R71E101ME14)
- Using two different parallel capacitors can create a resonance

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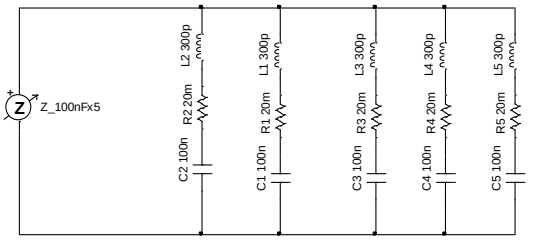
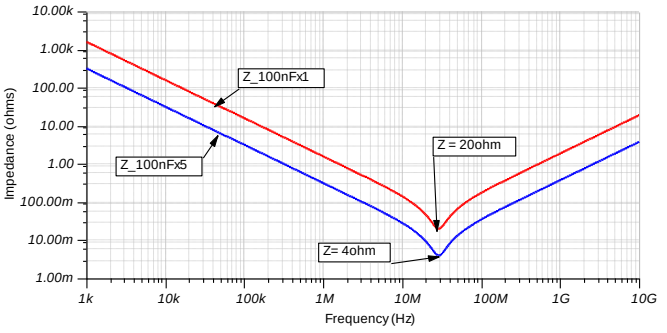
One commonly use decoupling method is to use multiple different values in parallel for decoupling. For example a 100nF and 1nF may be used in parallel. The idea is that the smaller capacitor will have lower ESL and will provide a lower impedance at high frequencies. This idea was probably correct years ago when through-hole components were popular, but modern surface mount ceramic capacitors will have similar ESL for different capacitance values. For example, a the ESL for a 25V 0603 X7R capacitor is relatively the same for a 100pF, 1000pF and 10,000pF capacitor. For the sample part numbers in the slide the ESL was about 200pH for all of the different capacitors. Using the outdated approach of putting different

capacitors in parallel can actually cause problems. In the circuit above a 1nF and 100nF capacitor are placed in parallel. If you look at the impedance curve for each capacitor, you can see that when these curves are combined they create a resonant peak in the impedance at 200MHz. This resonant peak can cause noise to peak at this frequency on the power supply rail. Thus, in general, it is best to use the same value and type of decoupling for all devices on the power rail to avoid resonances. Finally, using multiple capacitors when one is sufficient waists board space and adds cost.

Multiple Same Value Decoupling





Using Multiple Same Type / Value Decoupling Capacitors

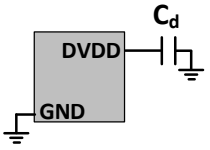
- Total impedance is divided by the number of capacitors
  - The example shows five capacitors in parallel ($Z_{total} = Z_c/5$)
- No resonance in impedance -- all capacitors are the same

This slide shows the preferred method of using the same value of decoupling across the supply rail. Note that impedance of equal capacitors will divided by the number of capacitors, so in this example the total impedance is divided by five. Also note that this example doesn't have any strange resonant peaks from the different value capacitors.

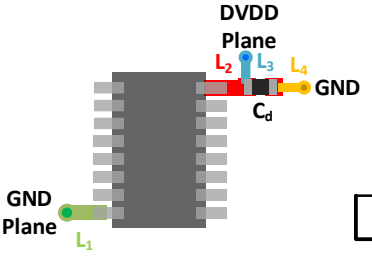
PCB Design for good decoupling

- **Main objective:** reduce the parasitic inductances from traces and vias.
- Use short wide traces or polygons
- Use multiple vias (or larger via) for plane connections if possible
- Thin dielectric spacing between top layer and plane reduce via inductance
- Use low ESL capacitor

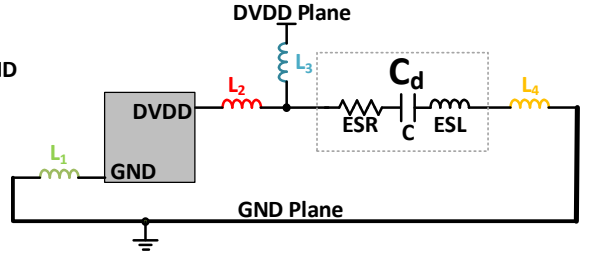
Schematic Design



Layout



Circuit including parasitics



This slide shows decoupling from a practical layout perspective. Note that the capacitor, traces, and via all have inductance. In most designs the ground and power will be on an internal plane so the capacitor is connected to power and ground using via. The capacitor is then connected to the device rail with a short thick trace. To minimize the inductance of any via connecting to ground it is useful to have a thin dielectric thickness between the signal layer and ground. Also, using multiple vias will reduce the inductance further. One question you may ask is how high does the inductance of the via and trace compare to the ESL of the decoupling capacitor?

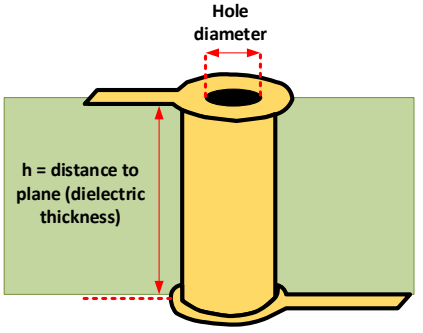
via inductance

Via inductance		
Drill hole (mil)	h - Distance to Plane (mil)	Inductance - FR4
12	9	0.0959nH
12	62	1.26782nH
16	9	0.08273nH
16	62	1.17729nH
20	9	0.07253nH
20	62	1.10706nH

Note 1: 9 mil is typical pre-preg thickness, 62 mil is typical two layer board thickness.
Note 2: 12 mil is typical minimum drilled via hole size.

Via Inductance

- Reducing dielectric thickness (h) significantly reduces inductance
- Using larger vias also helps incrementally
- Multiple vias are parallel inductors, so two similar vias will cut the inductance in half



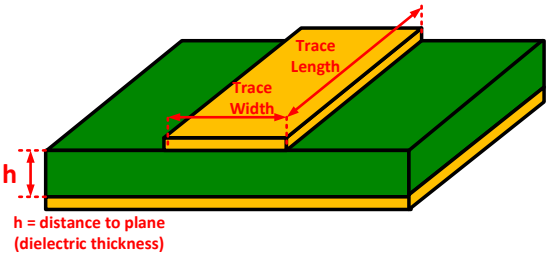
This chart shows the inductance for 12mil through 20mil vias. The inductance is shown for a thin 9mil dielectric and a thick 62mil dielectric. For a 12mil via the inductance is more than 10 times greater for the thick dielectric. Thus, dielectric thickness or the height of the via has a significant impact on it's inductance. Comparing a 12mil via to a 20mil via you don't see a very large improvement for the large via. Rather than using a large via, it is much better to use multiple parallel via as the inductance will divide by the number of via.

Trace inductance

Trace inductance			
Length (mil)	Width (mil)	h - Distance to Plane (mil)	Inductance
100	8	9	0.9814n
100	8	62	1.960n
100	12	9	0.8065n
100	12	62	1.785n
100	20	9	0.5735n
100	20	62	1.552n
1000	20	9	5.735n
1000	20	62	15.52n

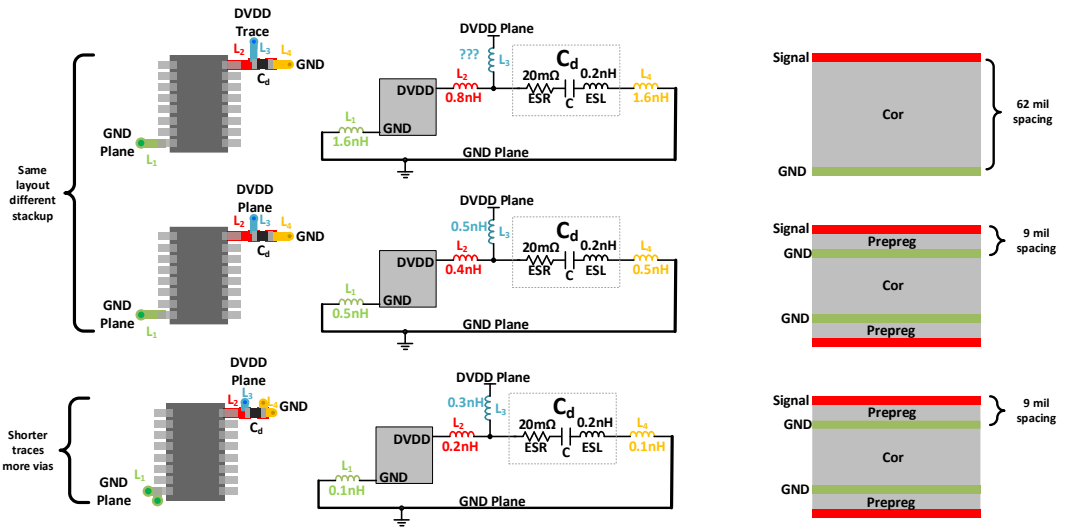
Trace Inductance

- Increasing width decreases inductance
- Decreasing the length decreases inductance
- Reducing dielectric thickness reduces inductance



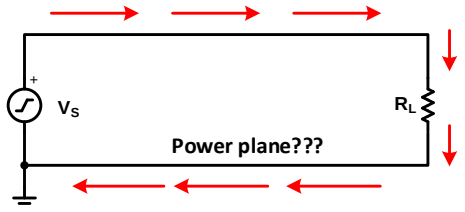
This slide shows trace inductance versus width, length, and dielectric thickness. In this case doubling the width cuts the inductance in half. Likewise, reducing the length will also proportionately reduce the inductance. Reducing the dielectric thickness will also reduce inductance but not substantially. The lengths and widths given in the table are typical for what is connected to decoupling capacitors. The typical ESL of a decoupling capacitor is on the order of 200nH, so the table shows that the trace inductance can easily be a dominant factor.

Comparison of parasitic inductance and ESL



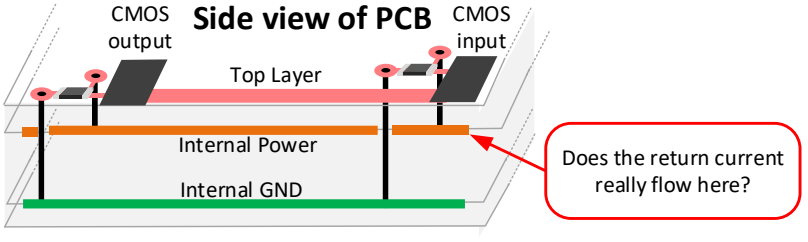
This slide shows three example layouts. The first layout uses a two layer board. The two layer board has a thick 62 mil dielectric so any via have a lot of inductance. Furthermore, the trace connecting between the capacitor and DVDD is long and thin. Notice that the parasitic inductances from the trace and via are large compared to the capacitors ESL. The example layer uses a four layer board. This helps minimize the via and trace inductance. The last example sues shorter traces and multiple via. In this case the trace and via impedances are now more in line with the ESL of the capacitor.

Can return current flow through the power plane?



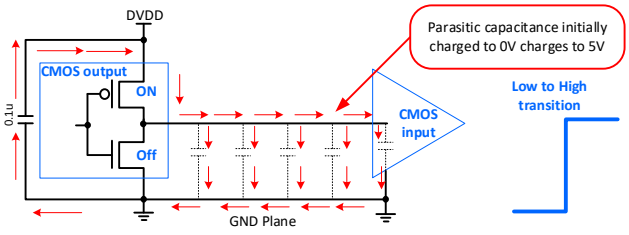
Can return current flow through the power plane?

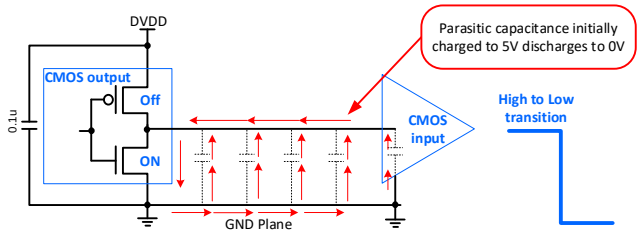
- I seems counter intuitive that return current can flow through the power plane, but it can.
- The next two slides will show how current flows in the GND or power plane for a CMOS gate depending on which plane is adjacent to the signal path.



One of the assertions made throughout this presentient is that return current will flow in the plane adjacent to the signal trace regardless if this plane is a power plane or a ground plane. This seems counter initiative when you think about a traditional circuit with a signal source, load, and ground. In the next few slides we will see how decoupling and return current flow, and how the PCB stackup impacts the current flow.

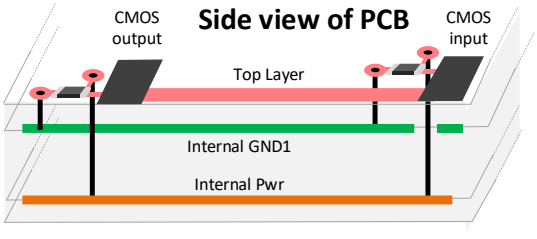
Decoupling: How does current flow in GND plane?





Current flow for adjacent GND Plane for microstrip

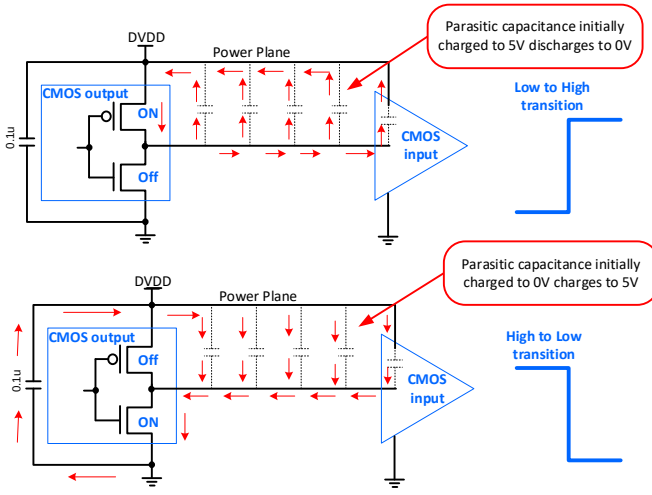
- **Low to high transition**: decoupling capacitor supplies transient current to charge parasitic capacitance of bus and CMOS input.
- **High to Low transition**: parasitic capacitance of bus discharge through the CMOS output



First, let's look at how return current flows when the signal trace is directly adjacent to a ground plane. In this case, the signal has a distributed parasitic capacitance with the ground plane. When the gate transitions its logic state, the parasitic capacitances will need to be charged or discharged depending the direction of the logic transition. Before the gate makes a low to high transition, the parasitic capacitances are all discharged to zero volts initially. At the time of the transition, the top transistor is turned on and the bottom one is turned off. At this time the parasitic capacitors will charge to DVDD. Note that the current is drawn from the decoupling capacitor to supply this sharp transient current. Before a high to low

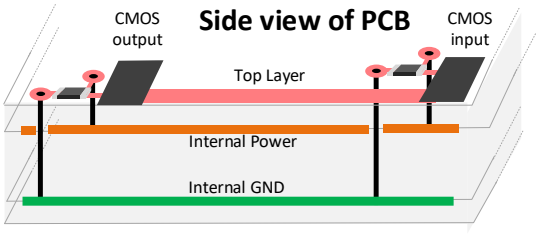
transition, the parasitic capacitors are initially charged to DVDD and will discharge through the bottom transistor. Note at this time the decoupling capacitor and power supply do not provide any current. Finally, note that for both transitions, the return current flows in the ground plane for this configuration.

Decoupling: How does current flow in power plane?



Current flow for adjacent power Plane for microstrip

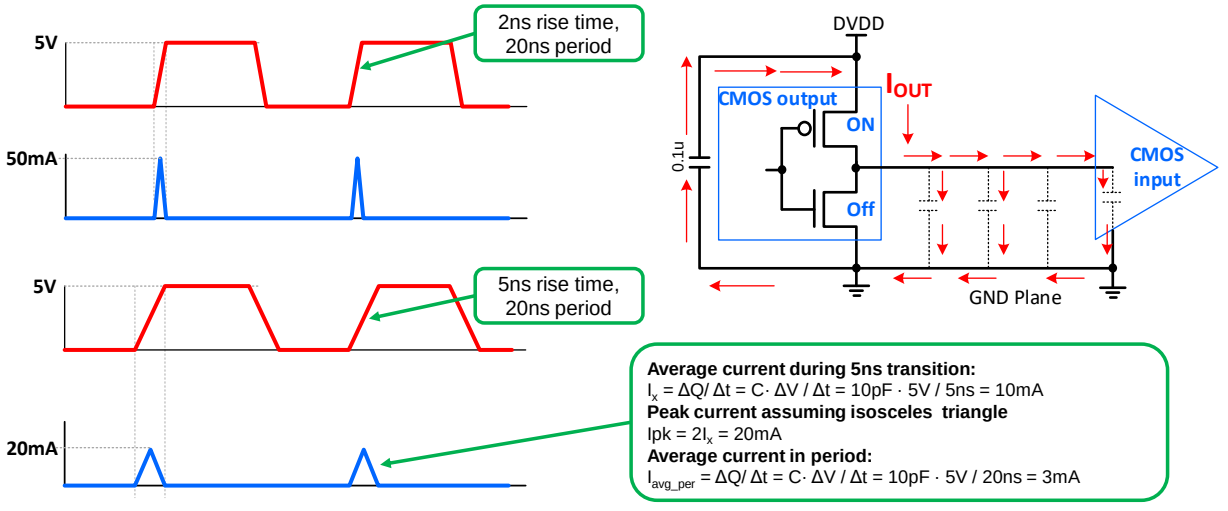
- **Low to high transition**: parasitic capacitance of bus discharge through the CMOS output
- **High to Low transition**: decoupling capacitor supplies transient current to charge parasitic capacitance of bus and CMOS input.



Now let's look at the case where a power plane is beneath the signal trace. In this case, the parasitic capacitance connects from the signal trace to the power plane. Again, transitioning the logic output of the gate will cause this parasitic to charge and discharge. When transitioning from low to high the parasitic capacitors are initially charged to DVDD and need to discharge to zero volts. This discharge happens when the top transistor turns on. Note that the decoupling capacitor and supply do not provide any current at this time. When transitioning from high to low, the capacitor will need to be charged from zero volts to DVDD. In this case the decoupling capacitor and DVDD supply will provide the current needed to

charge the parasitic capacitance. Notice for this example that the return current flows in the power plane. The key points of the last two slides is to show that the decoupling only provides current on one of the logic transitions and also to show how return current can flow through a power plane. Now let's look at how much current is drawn during logic transitions.

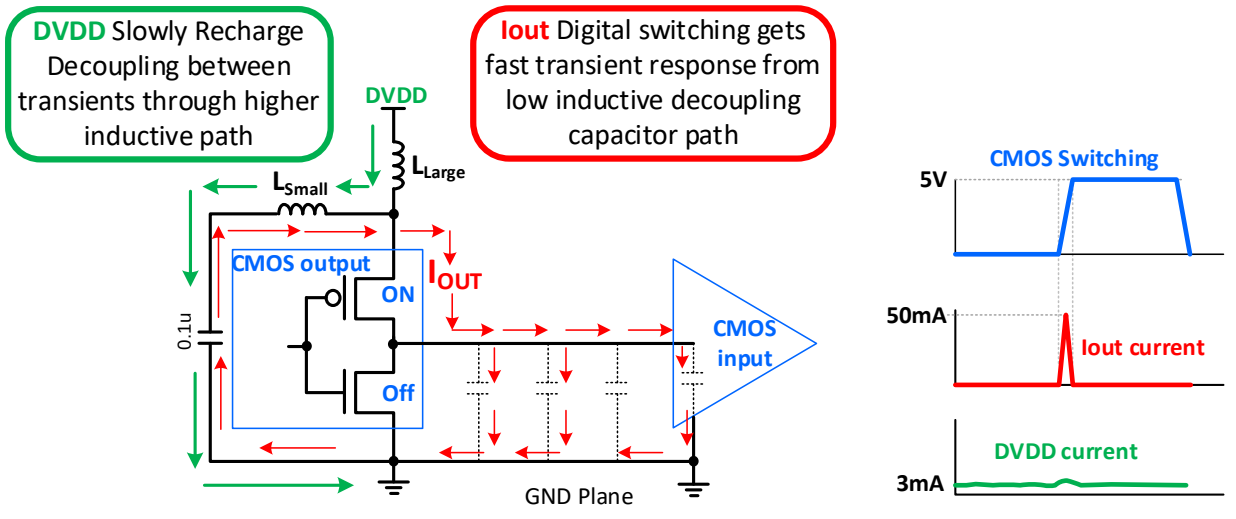
How much current does the decoupling deliver?



The schematic shown here shows the current flow for a low to high transition where the signal trace is above an adjacent ground plane. The CMOS gate needs to provide current to charge up the parasitic capacitors connected from the signal trace to ground. The amount current required relates to the size of the parasitic capacitor. The size of the capacitor relates to the PCB trace dimensions. Long traces will have large parasitic capacitances. A typical traces capacitance for a medium length trace is 10pF. For a 5ns rise time, the parasitic capacitance need to be fully charged in 5ns. Current is defined as the change in charge over time and charge is defined as C*V, so the average current is C*V/time. For this example 10pF * 5V / 5ns gives an

average current of 10mA during the transient event. The peak current can be estimated as two times the average current by assuming the transient has the wave shape of an isosceles triangle. In this case the peak current is approximately 20mA. The overall average current during the period of the square wave can be determined by dividing the charge in charge by the entire period of the square wave. In this case the waveform period is 20ns, and the average current across the period is calculated as 3mA. For proper decoupling consider that the 3mA average current is provided by the bulk decoupling over the 20ns period and the 20mA peak current is provided by the local decoupling during the 5ns transient. Note that doing the same calculation for a 2ns rise time causes the peak current to increase to 50mA but the average current in the period is still 3mA.

The supply doesn't provide the transient current



This slide reiterates that the large rapid transient current is provided by the local decoupling. Proper layout with wide traces and multiple via provide a low inductance connection between the local decoupling and the device power supply. Transient happens over a short time period of a few nano-seconds. The average current to recharge the local decoupling happens over a much longer time. The lower frequency average current is provided by the bulk capacitance and power supply. Since the frequency of the average current is much lower than the transient current the power supply connection may have more inductance than the local decoupling path.

Thanks for your time! Please try the quiz.

That concludes this video – thank you for watching! Please try the quiz to check your understanding of this video's content.

Quiz: Decoupling capacitors

1. (True/False) Using a large and small value decoupling capacitor is a good way to improve decoupling because the small value decoupling capacitor will be optimal for high frequency. For example, connecting a 0.1uF and a 0.001uF capacitor in parallel is a good combination for better high frequency decoupling.
   a) True
   b) False

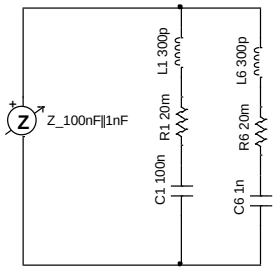
Question 1, (True/False) Using a large and small value decoupling capacitor is a good way to improve decoupling because the small value decoupling capacitor will be optimal for high frequency. For example, a 0.1uF and a 0.001uF in parallel is a good combination for better high frequency decoupling.

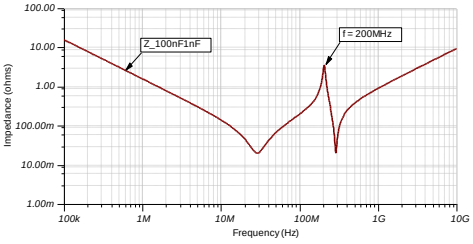
Quiz: Decoupling capacitors

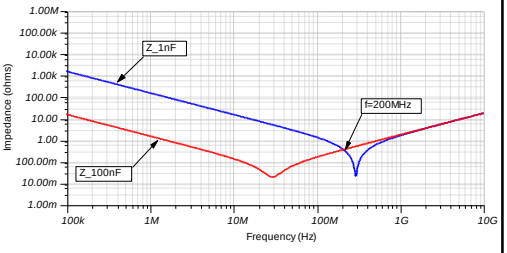
1. (True/False) Using a large and small value decoupling capacitor is a good way to improve decoupling because the small value decoupling capacitor will be optimal for high frequency. For example, connecting a 0.1uF and a 0.001uF capacitor in parallel is a good combination for better high frequency decoupling.

   a) True

   b) False







The correct answer is “b”, false. Most modern ceramic capacitors with similar package size will have similar ESL. In the past, lower value capacitors would have a correspondingly low ESL, so using low value capacitors for high frequency decoupling was common practice However, the ESL on modern surface mount ceramic capacitors is no longer closely connected to the capacitance value. Furthermore, the combination of two different capacitors in parallel can have a combined impedance with a resonant peak which can increase noise at that frequency.

Quiz: Decoupling capacitors

2. (True/False) For low inductance, it is better to place multiple small via than one large one. For example, two 12mil via would have lower inductance than one 20mil via.
   a) True
   b) False

3. (True/False) The thickness of the dielectric between the decoupling capacitor and ground plane will impact the decoupling effectiveness.
   a) True
   b) False

Question 2, (True/False) For low inductance, it is better to place multiple small via than one large one. For example, two 12mil via would have lower inductance than one 20mil via.

The correct answer is “a”, True. The for a 62mil board thickness, the inductance of a 12mil via is 1.27nH and the inductance of a 20mil is 1.11nH. Placing two

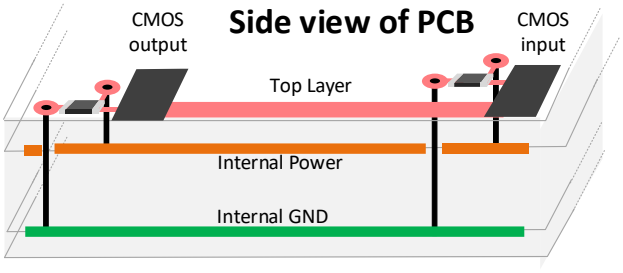
12mil in parallel will cut the inductance in half from 1.27nH to 0.64nH.

Question 3, (True/False) The thickness of the dielectric between the decoupling capacitor and ground plane will impact the decoupling effectiveness.

The correct answer is “a”, true. A thin board means that the vias are short and low inductance. This will reduce the impedance of the decoupling network and make it more effective.

Quiz: Decoupling capacitors

4. (True/False) For the layout below, when a signal is being transmitted from the CMOS output to the input, the return current will flow in the ground plane (GND).
   a) True
   b) False



Question 4, (True/False) For the layout below, when a signal is being transmitted from the CMOS output to the input, the return current will flow in the ground plane (GND).

The correct answer is “b”, False. The return current will always travel in the plane adjacent to the signal trace. In this example the power plane is adjacent to the signal trace so the return current will flow in the power plane.

Thanks for your time!

That’s all for todays video. Thanks for watching.