ADC3664-SP Radiation-Hardness-Assured 14-Bit, Dual Channel, 1 to 125MSPS, Low Latency, Low Noise, Ultra-low Power, Analog-to-Digital Converter (ADC)

1 Features

- Screening and radiation performance
  - QMLV screening and reliability assurance
  - Total ionizing dose (TID): 300krad (Si)
  - Single event latch-up (SEL): 75MeV-cm^2/mg
- Ambient temperature range: -55°C to 105°C
- Dual Channel ADC
- 14-bit 125MSPS
- Noise floor: -156.9dBFS/Hz
- Low power consumption: 100mW/ch
- Latency: 2 clock cycles
- Clock rate versus voltage reference:
  - External reference: 1MSPS to 125MSPS
  - Internal reference: 100MSPS to 125MSPS
- 14-Bit, no missing codes
- Input bandwidth: 200MHz (-3dB)
- INL: ±2.6LSB; DNL: ±0.9LSB
- Optional digital down converter (DDC):
  - Real or complex decimation
  - Decimation by 2, 4, 8, 16, and 32
  - 32-bit NCO
- Serial LVDS (SLVDS) interface (2-, 1-, and 1/2-wire)
- Spectral performance (F_{IN} = 5MHz):
  - SNR: 77.5dBFS
  - SFDR: 84dBc HD2, HD3
  - Non HD23: 91dBc

2 Applications

- Optical imaging payload
- Radar imaging payload
- Satellite communication payloads

3 Description

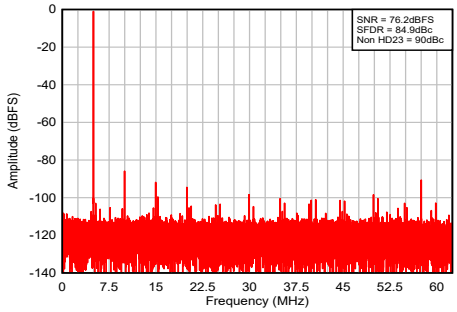
The ADC3664-SP is a low latency, low noise, and ultra low power, 14-bit, 125MSPS, high-speed dual channel ADC. Designed for best noise performance, the device delivers a noise spectral density of –156.9dBFS/Hz combined with excellent linearity and dynamic range. The ADC3664-SP offers DC precision together with IF sampling support to enable the design of a wide range of applications. The low latency architecture (as low as 1 clock cycle latency) and high sample rate also enable high speed control loops. The ADC consumes only 100mW/ch at 125MSPS and the power consumption scales well with sampling rate.

The device uses a serial LVDS (SLVDS) interface to output the data which minimizes the number of digital interconnects. The device also integrates a digital down converter (DDC) to help reduce the data rate and lower system power consumption. The device is pin-to-pin compatible with the 18-bit, 65MSPS ADC3683-SP. It comes in a 64-pin CFP package (10.9mm x 10.9mm) and supports a temperature range from –55°C to +105°C.

Device Information

PART NUMBER	GRADE	PACKAGE(1)
5962F2320501VXC	Radiation hardness assured QML-V	10.9mm x 10.9mm 64-pin Ceramic Flat Pack (HBP)
ADC3664HBP/EM(2)	Engineering model, for non-flight prototype work	

(1) For more information, see Section 12.
(2) These units are intended for engineering evaluation only. They are not put through a compliant flow (so there is no burn-in, only 25°C testing, etc.). Additionally, these units are not suitable for qualification, production, radiation testing, or flight use. The parts are not warranted for performance over temperature or operating life.



Single Tone Spectrum, F_s = 125MSPS, F_{in} = 5MHz

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4 Pin Configuration and Functions

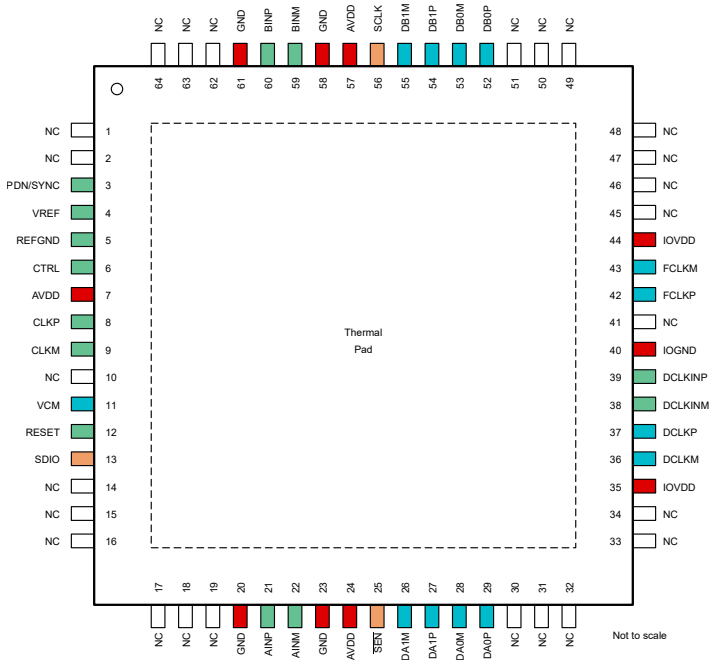


Figure 4-1. HBP Package, 64-Pin CFP (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
INPUT			
AINP	21	I	Positive analog input for ADC A.
AINM	22	I	Negative analog input for ADC A.
BINP	60	I	Positive analog input for ADC B.
BINM	59	I	Negative analog input for ADC B.
CLKP	8	I	Positive sampling clock input for ADCs A & B.
CLKM	9	I	Negative sampling clock input for ADCs A & B.
VREF	4	I	External, 1.6V, voltage reference input.
REFGND	5	I	Voltage reference ground. This pin allows close placement of the decoupling capacitors near the VREF input when using either the internal or external reference modes.
CTRL	6	I	This pin is used to configure the default sampling clock type and voltage reference source upon power up (see Section 7.5.1). There is an internal 100kΩ pull-up resistor to AVDD.
PDN/SYNC	3	I	Dual purpose, active high, pin. The pin can be configured to control the power down state of the device or as a synchronization input. The pin functionality can be configured via SPI (default function is PDN). This pin has an internal 21kΩ pull-down resistor.
RESET	12	I	Active high reset pin. This pin has an internal 21kΩ pull-down resistor.
DCLKINP	39	I	Positive input of the interface clock. This pin connects to DCLKINM through an internal 100Ω termination resistor.
DCLKINM	38	I	Negative input of the interface clock. This pin connects to DCLKINP through an internal 100Ω termination resistor.
OUTPUT			
DA0P	29	O	Positive output for interface lane A0.
DA0M	28	O	Negative output for interface lane A0.

Table 4-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
DA1P	27	O	Positive output for interface lane A1.
DA1M	26	O	Negative output for interface lane A1.
DB0P	52	O	Positive output for interface lane B0.
DB0M	53	O	Negative output for interface lane B0
DB1P	54	O	Positive output for interface lane B1.
DB1M	55	O	Negative output for interface lane B1.
DCLKP	37	O	Positive output of the interface clock.
DCLKM	36	O	Negative output of the interface clock.
FCLKP	42	O	Positive output of the interface frame clock.
FCLKM	43	O	Negative output of the interface frame clock.
VCM	11	O	Common-mode output voltage of the analog inputs (typically 0.95V).
SPI			
$\overline{SEN}$	25	I	Active low SPI enable. This pin has an internal 21kΩ pull-up resistor to AVDD.
SCLK	56	I	SPI clock input. This pin has an internal 21kΩ pull-down resistor.
SDIO	13	I/O	SPI data input or output. This pin has an internal 21kΩ pull-down resistor.
POWER			
AVDD	7, 24, 57	I	Analog supply input, 1.8V.
GND	20, 23, 58, 61	I	Ground supply input, 0V.
IOVDD	35, 44	I	Interface supply input, 1.8V.
IOGND	40	I	Interface ground supply input, 0V.
OTHER			
DAP	DAP	-	Die attached pad (thermal pad), connect to GND.
NC	1, 2, 10, 14, 15, 16, 17, 18, 19, 30, 31, 32, 33, 34, 41, 45, 46, 47, 48, 49, 50, 51, 62, 63, 64	-	No connect pins. Connect to ground or leave floating.(1)

(1) Thermal pad and top metal lid are connected to pin 17. Can be grounded or no connect.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage range, AVDD, IOVDD		–0.3	2.1	V
Supply voltage range, GND, IOGND, REFGND		–0.3	0.3	V
Voltage applied to input pins	AINP/M, BINP/M, CLKP/M, VREF, CTRL	–0.3	MIN(2.1, AVDD+0.3)	V
	PDN/SYNC, RESET, SCLK, $\overline{SEN}$, SDIO	–0.3	MIN(2.1, AVDD+0.3)	
	DCLKINP/M	–0.3	MIN(2.1, IOVDD+0.3)	
Junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage range	AVDD(1)	1.75	1.8	1.85	V
	IOVDD(1)	1.75	1.8	1.85	V
T_A	Operating free-air temperature	–55		105	°C
T_J	Operating junction temperature			105(2)	°C

(1) Measured with respect to GND.
(2) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.

5.4 Thermal Information

THERMAL METRIC(1)		ADC3664-SP HBP (CFP) 64 Pins	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	28.4	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	12.0	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	14.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	7.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.8	°C/W
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics - Power Consumption

Typical values are at T_A = 25°C, full temperature range is T_{MIN} = –55°C to T_{MAX} = 105°C, ADC sampling rate = 125MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8V, external 1.6V reference, and –1dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC3664-SP: 125MSPS						
I_{AVDD}	Analog supply current	Internal reference		72		mA
		External reference		66	82	
I_{IOVDD}	I/O supply current	2-wire		45	72	
P_{DIS}	Power dissipation	External reference, 2-wire		200	277	mW
I_{IOVDD}	I/O supply current	2-wire, 1/2-swing		45		mA
		4x real decimation, 1-wire		54		
		4x real decimation, 1/2-wire		55		
		16x real decimation, 1-wire		49		
		16x real decimation, 1/2-wire		49		
		4x complex decimation, 1-wire		58		
		16x complex decimation, 1-wire		51		
		16x complex decimation, 1/2-wire		51		
P_{DIS}	Power consumption in global power down mode	Default mask settings, internal reference		11		mW
		Default mask settings, external reference		13		

5.6 Electrical Characteristics - DC Specifications

Typical values are at T_A = 25°C, full temperature range is T_{MIN} = –55°C to T_{MAX} = 105°C, ADC sampling rate = 125MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8V, 1.6V external reference, and –1dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
No missing codes			14			bits
PSRR	Power supply rejection ratio	F_{IN} = 1MHz		35		dB
DNL	Differential nonlinearity	F_{IN} = 5MHz		±0.9	±0.97	LSB
INL	Integral nonlinearity	F_{IN} = 5MHz		±2.6	±9.5	LSB
V_{OS}	Input offset			±30	±50	LSB
V_{OS_DRIFT}	Offset drift			±0.06		LSB/°C
Error	Gain error and internal reference combined error	Both channels are powered up		±2		%FSR
	Gain error	Both channels are powered up		±1.8		%FSR
	Gain drift	External 1.6V reference		±57		ppm/°C
		Internal reference		106		ppm/°C
Transition noise				0.7		LSB
ADC ANALOG INPUT (AINP/M, BINP/M)						
FS	Input full scale	Differential		3.2		V_{pp}
V_{CM}	Input common-mode voltage			0.95		V
R_{IN}	Input resistance	Differential at DC		8		kΩ
C_{IN}	Input capacitance	Differential at DC		5.4		pF
V_{OCM}	Output common-mode voltage			0.95		V
BW	Analog input bandwidth (-3dB)			1.4		GHz
INTERNAL VOLTAGE REFERENCE						
V_{REF}	Internal reference voltage			1.6		V
V_{REF} output impedance				8		Ω
EXTERNAL VOLTAGE REFERENCE						
V_{REF}	External voltage reference			1.6		V
Input current				1		mA
Input impedance				5.3		kΩ
CLOCK INPUT (CLKP/M)						
Input clock frequency		External reference	1		125	MHz
		Internal reference	100		125	MHz
V_{ID}	Differential input voltage		0.5	1		V_{pp}
V_{CM}	Input common-mode voltage			0.9		V
R_{IN}	Single ended input resistance to common mode			5		kΩ
C_{IN}	Single ended input capacitance			1.5		pF
Clock duty cycle			45	50	60	%

5.6 Electrical Characteristics - DC Specifications (continued)

Typical values are at T_A = 25°C, full temperature range is T_{MIN} = –55°C to T_{MAX} = 105°C, ADC sampling rate = 125MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8V, 1.6V external reference, and –1dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, PDN, SCLK, $\overline{SEN}$, SDIO)						
V_{IH}	High level input voltage		1.5			V
V_{IL}	Low level input voltage				0.3	
I_{IH}	High level input current			90	150	uA
I_{IL}	Low level input current		-150	-90		uA
C_I	Input capacitance			1.5		pF
DIGITAL OUTPUT (SDOUT)						
V_{OH}	High level output voltage	I_{LOAD} = -400 uA	IOVDD – 0.1	IOVDD		V
V_{OL}	Low level output voltage	I_{LOAD} = 400 uA			0.1	
LVDS lane rate					1	Gbps
V_{ID}	DCLKIN differential input voltage		200	350		mV_{pp}
V_{CM}	DCLKIN input common-mode voltage		1.1	1.2	1.3	V
SLVDS INTERFACE						
V_{OD}	Differential output voltage		0.585	700	0.785	mV_{pp}
V_{CM}	Output common-mode voltage		0.85	1.0	1.15	V

5.7 Electrical Characteristics - AC Specifications

Typical values are at T_A = 25°C, full temperature range is T_{MIN} = –55°C to T_{MAX} = 105°C, ADC sampling rate = 125MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8V, 1.6V external reference, and –1dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NSD	Noise spectral density	F_{IN} = 5MHz, A_{IN} = -20dBFS		-156.9		dBFS/Hz
SNR	Signal to noise ratio	F_{IN} = 5MHz	70	77.5		dBFS
		F_{IN} = 5MHz, A_{IN} = -20dBFS		78.9		dBFS
		F_{IN} = 10MHz		77.6		
		F_{IN} = 40MHz		76.9		
		F_{IN} = 70MHz		75.5		
		F_{IN} = 100MHz		74.1		
SINAD	Signal to noise and distortion ratio	F_{IN} = 5 MHz		75.7		dBFS
		F_{IN} = 10MHz		74.2		
		F_{IN} = 40MHz		72.6		
		F_{IN} = 70MHz		71.3		
		F_{IN} = 100MHz		72.4		
ENOB	Effective number of bits	F_{IN} = 5MHz		12.6		bit
		F_{IN} = 10MHz		12.6		
		F_{IN} = 40MHz		12.5		
		F_{IN} = 70MHz		12.3		
		F_{IN} = 100MHz		12.0		
THD	Total harmonic distortion (first five harmonics)	F_{IN} = 5MHz	68	80		dBc
		F_{IN} = 10MHz		76		
		F_{IN} = 40 =MHz		74		
		F_{IN} = 70MHz		72		
		F_{IN} = 100MHz		76		
HD2	Second harmonic distortion	F_{IN} = 5MHz	72.5	84		dBc
		F_{IN} = 10MHz		78		
		F_{IN} = 40MHz		75		
		F_{IN} = 70MHz		77		
		F_{IN} = 100MHz		79		
HD3	Third harmonic distortion	F_{IN} = 5MHz	69.5	84		dBc
		F_{IN} = 10MHz		81		
		F_{IN} = 40MHz		88		
		F_{IN} = 70MHz		76		
		F_{IN} = 100MHz		81		
Non HD2,3	Spurious free dynamic range (excluding HD2 and HD3)	F_{IN} = 5MHz	77	92		dBFS
		F_{IN} = 10MHz		93		
		F_{IN} = 40MHz		89		
		F_{IN} = 70MHz		84		
		F_{IN} = 100MHz		86		
IMD3	Two tone inter-modulation distortion	F_1 = 10MHz, F_2 = 12MHz, A_{IN} = -7dBFS/tone		88		dBc

5.8 Timing Requirements

Typical values are at T_A = 25°C, MIN and MAX timing values are characterized over the full temperature range T_{MIN} = –55°C to T_{MAX} = 105°C and are NOT production tested, ADC sampling rate = 125MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8V, 1.6V external reference, and –1dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
ADC TIMING SPECIFICATIONS						
t_{AD}	Aperture delay			0.85		ns
t_A	Aperture jitter	Square wave clock with fast edges		250		fs
t_{ACQ}	Signal acquisition period, referenced to sampling clock falling edge			$-T_S/4$		Sampling clock period
t_{CONV}	Signal conversion period, referenced to sampling clock falling edge			6		ns
Wake up time	Time to valid data after coming out of power down	External 1.6V reference, differential clock			100	µs
$t_{S,SYNC}$	Setup time for SYNC input signal	Referenced to sampling clock rising edge	500			ps
$t_{H,SYNC}$	Hold time for SYNC input signal	Referenced to sampling clock rising edge	600			
ADC latency	Signal input to data output	1/2-wire SLVDS		1		Clock cycles
		1-wire SLVDS		1		
		2-wire SLVDS		2		
		Real decimation by 2		21		Output clock cycles
		Complex decimation by 2		22		
		Real or complex decimation by 4, 8, 16, 32		23		

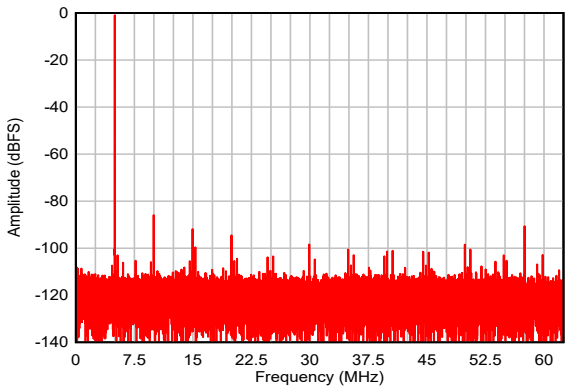
5.8 Timing Requirements (continued)

Typical values are at T_A = 25°C, MIN and MAX timing values are characterized over the full temperature range T_{MIN} = –55°C to T_{MAX} = 105°C and are NOT production tested, ADC sampling rate = 125MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8V, 1.6V external reference, and –1dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
INTERFACE TIMING: SERIAL LVDS INTERFACE						
t_{PD}	Propagation delay: sampling clock falling edge to DCLK rising edge	Delay between sampling clock falling edge to DCLKIN falling edge < 2.5ns. T_{DCLK} = DCLK period t_{CDCLK} = Sampling clock falling edge to DCLKIN falling edge	2 + T_{DCLK} + t_{CDCLK}	3 + T_{DCLK} + t_{CDCLK}	4 + T_{DCLK} + t_{CDCLK}	ns
		Delay between sampling clock falling edge to DCLKIN falling edge >= 2.5ns. T_{DCLK} = DCLK period t_{CDCLK} = Sampling clock falling edge to DCLKIN falling edge	2 + t_{CDCLK}	3 + t_{CDCLK}	4 + t_{CDCLK}	
t_{CD}	DCLK rising edge to output data delay	F_{out} = 65MSPS, data rate = 455MBPS, 2-wire	0	0.1	0.3	ns
		F_{out} = 125MSPS, data rate = 875MBPS, 2-wire	-0.2	0.1	0.3	
		F_{out} = 65MSPS, data rate = 910MBPS, 1-wire	0	0.1	0.3	
t_{DV}	Data valid	F_{out} = 65MSPS, data rate = 455MBPS, 2-wire	1.8	1.9	2	ns
		F_{out} = 125MSPS, data rate = 875MBPS, 2-wire	0.6	0.8	0.9	
		F_{out} = 65MSPS, data rate = 910MBPS, 1-wire	0.6	0.8	0.9	
SERIAL PROGRAMMING INTERFACE (SCLK, $\overline{SEN}$, SDIO) - INPUT						
$f_{CLK(SCLK)}$	Serial clock frequency				20	MHz
$t_{SU(\overline{SEN})}$	$\overline{SEN}$ to rising edge of SCLK				10	ns
$t_{H(\overline{SEN})}$	$\overline{SEN}$ from rising edge of SCLK				17	
$t_{SU(SDIO)}$	SDIO to rising edge of SCLK				17	
$t_{H(SDIO)}$	SDIO from rising edge of SCLK				10	
SERIAL PROGRAMMING INTERFACE (SDIO) - OUTPUT						
$t_{(OZD)}$	SDIO HiZ to LoZ				19	ns
$t_{(ODZ)}$	SDIO LoZ to HiZ				17	
$t_{(OD)}$	Falling edge of SCLK to SDIO data valid				19	

5.9 Typical Characteristics

Typical values at T_A = 25°C, ADC sampling rate = 125MSPS, A_{IN} = –1dBFS differential input, AVDD = IOVDD = 1.8V, external 1.6V voltage reference, unless otherwise noted.



SNR = 76.2dBFS, SFDR = 84.9dBc, Non HD23 = 90dBc

Figure 5-1. Single Tone Spectrum At F_{IN} = 5MHz

6 Parameter Measurement Information

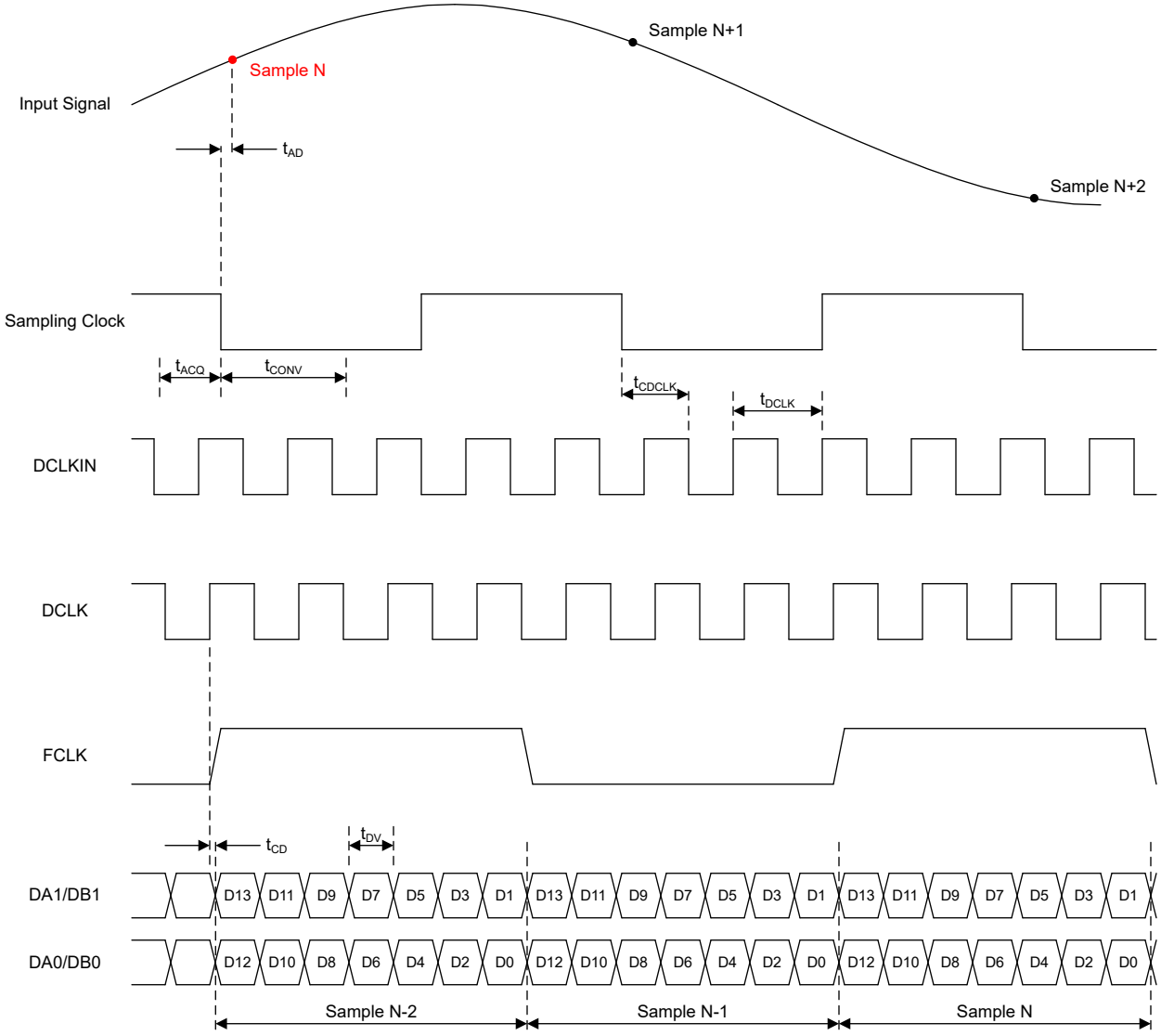


Figure 6-1. Timing diagram: 2-wire

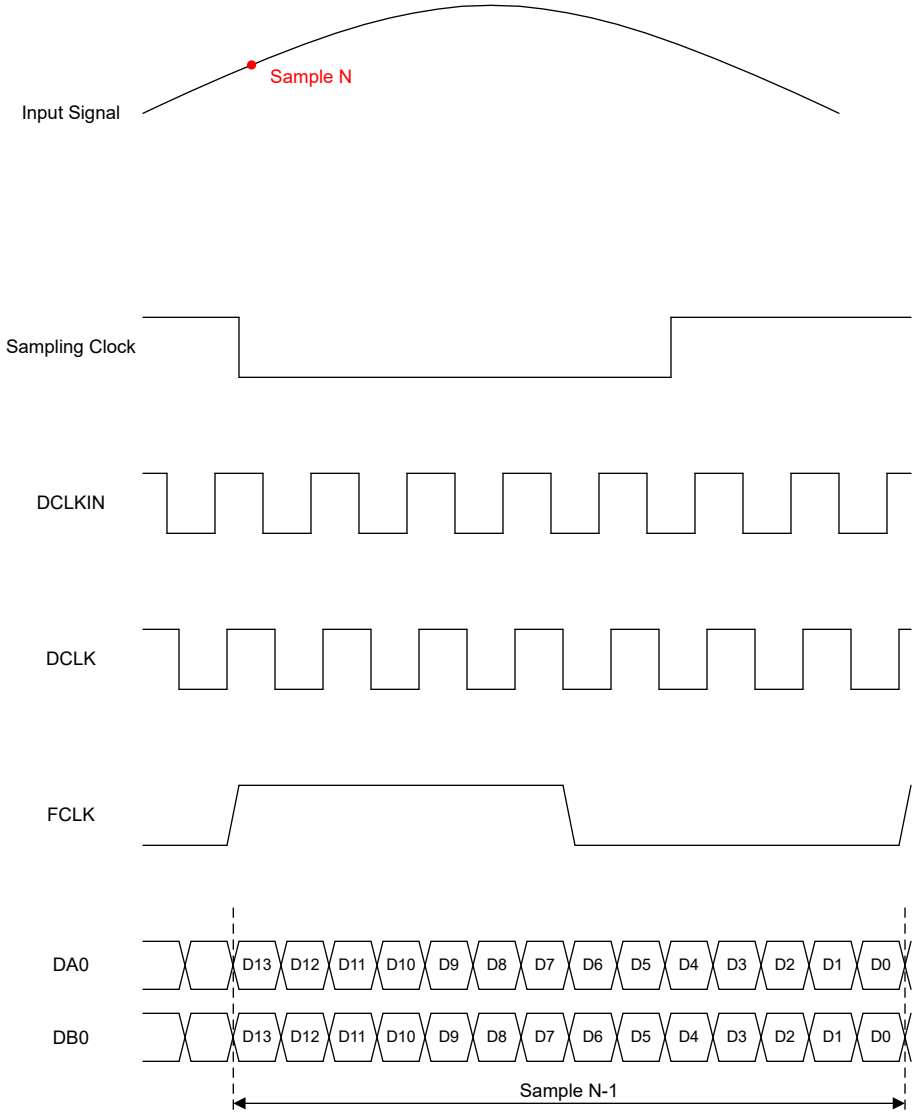


Figure 6-2. Timing diagram: 1-wire

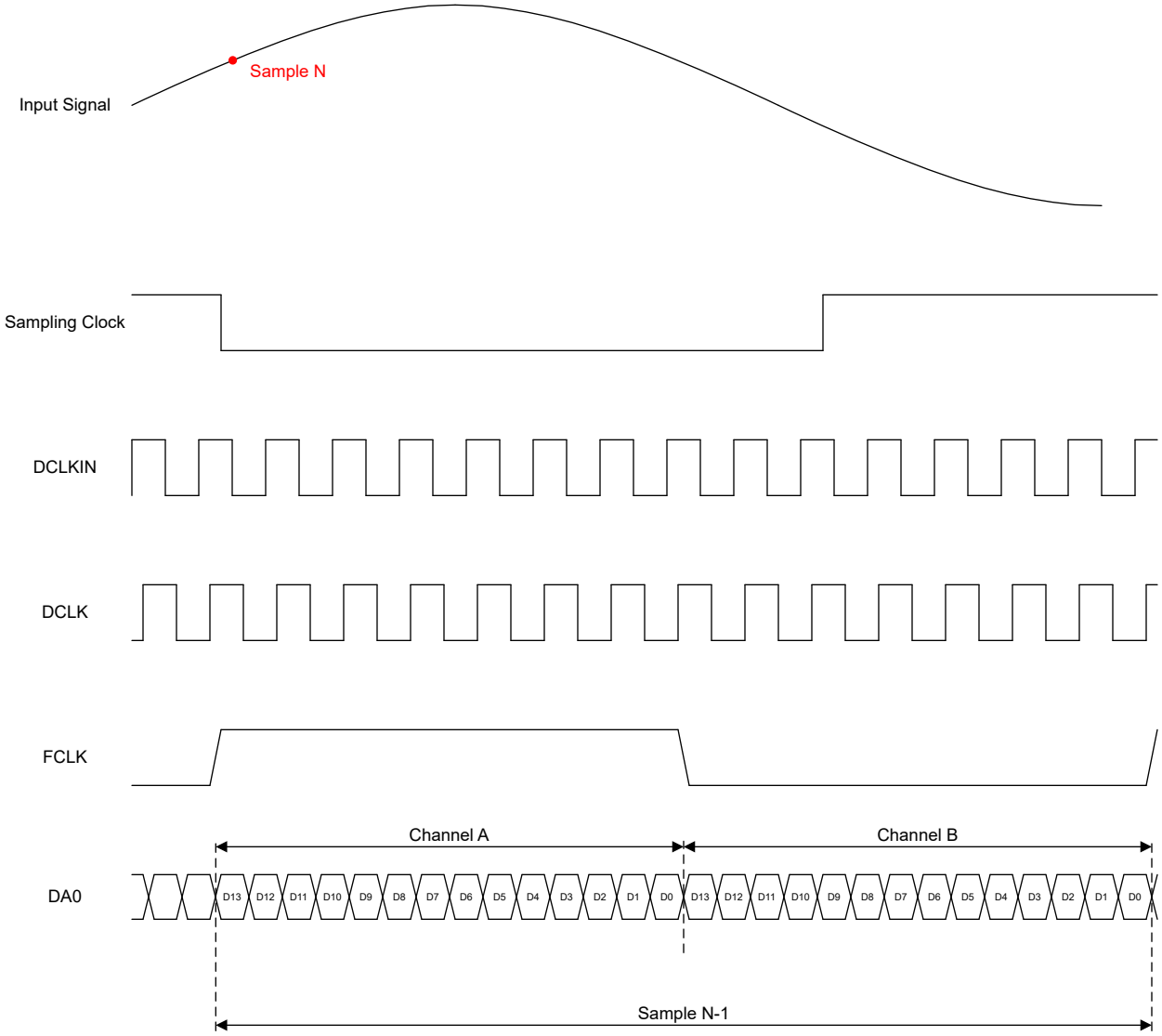


Figure 6-3. Timing diagram: 1/2-wire

7 Detailed Description

7.1 Overview

The ADC3664-SP is a low latency, low noise, and ultra low power 14-bit high-speed dual channel ADC with a max sampling rate of 125MSPS intended for use in space applications with mission profiles of total ionizing dose (TID) less than 300krad (Si) and single event latch-up (SEL) of less than 75MeV-cm^2/mg. The ADC has an internal reference option and supports the use of an external, high precision, 1.6V reference (see Section 7.3.3). Optionally, integrated programmable digital down converters (DDCs) enable output data rate reduction and channelization (see Section 7.3.5). The DDCs, if operated in a complex decimation mode, offer a 32-bit programmable NCO for complex mixing. The DDCs also support a real decimation mode with no mixing.

The ADC3664-SP uses a serial LVDS (SLVDS) interface to output the data which minimizes the number of digital interconnects (see Section 7.3.4.2). The SLVDS interface can be configured to one of the following modes: two LVDS lanes per channel (2-wire), one LVDS lane per channel (1-wire), or a single lane mode (1/2-wire) where both channels are multiplexed on the same LVDS lane. The device supports configurable output resolutions from 14-bit to 20-bit. Due to the inherent low latency ADC architecture, the digital output result is available after only one or two clock cycles depending on the output interface mode.

The ADC3664-SP is intended to be controlled through the Serial Peripheral Interface (SPI) by configuring registers (Section 7.5); however, the CTRL pin can also be used to configure the voltage reference source and sampling clock input type upon power up.

7.2 Functional Block Diagram

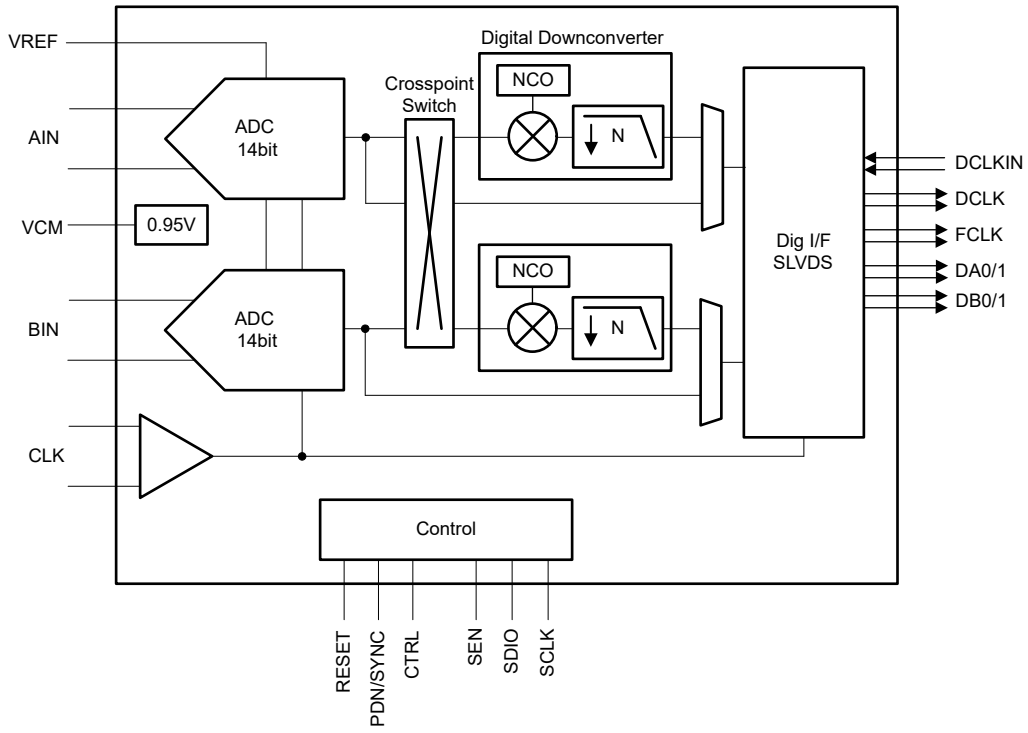


Figure 7-1. Simplified Block Diagram

7.3 Feature Description

7.3.1 Analog Input

The analog inputs of the ADC3664-SP are intended to be driven differentially. Both AC coupling and DC coupling of the analog inputs is supported. The analog inputs are designed for an input common-mode voltage of 0.95V which must be provided externally on each input pin. Figure 7-2 shows the analog input model of the ADCs. First, 8 switches are closed during acquisition for a period of t_{ACQ}. Then, all switches are open for a period of t_{CONV}. Finally, before the next acquisition period, the reset switch is closed for a period of t_{RST}.

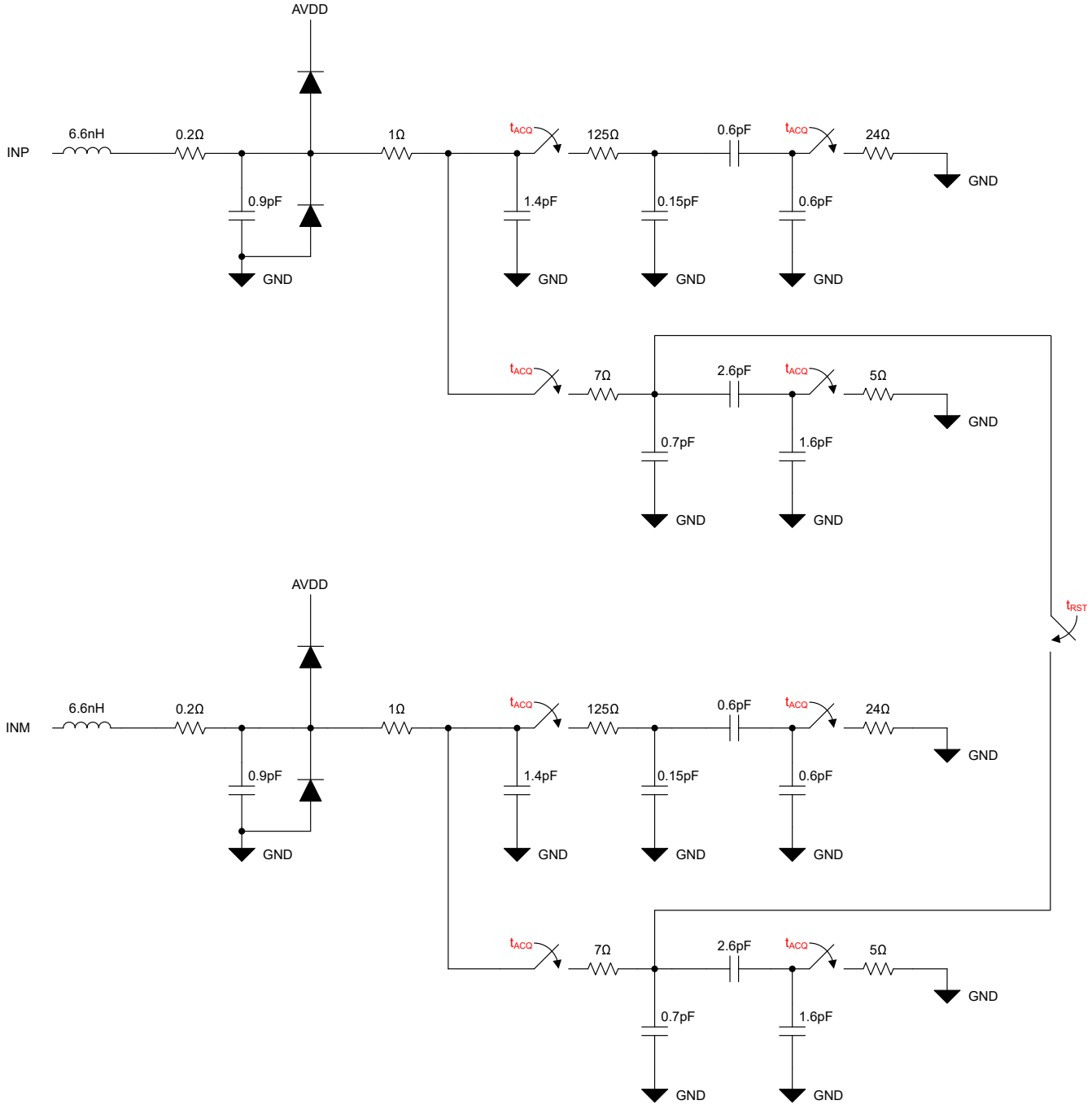


Figure 7-2. Analog Input Model

7.3.1.1 Analog Input Bandwidth

The -3dB bandwidth is approximately 200MHz. The ADC architecture limits the full power bandwidth to 65MHz; therefore, to avoid significantly degrading the ADC performance. The recommendation is that the input power is decreased linearly with increasing input frequency above 65MHz.

7.3.1.2 Analog Front End Design

The ADC3664-SP should be used with a passive filter to absorb the glitches on the input due to sampling. Additionally, a passive DC bias circuit is needed in AC-coupled applications which can be combined with a termination network.

7.3.1.2.1 Sampling Glitch Filter

The front end sampling glitch filter is designed to optimize the SNR and HD3 performance of the ADC. The filter performance is dependent on input frequency: therefore, the following filter designs are recommended for different input frequency ranges as shown in Figure 7-3 and Figure 7-4 (assuming a 50Ω source impedance).

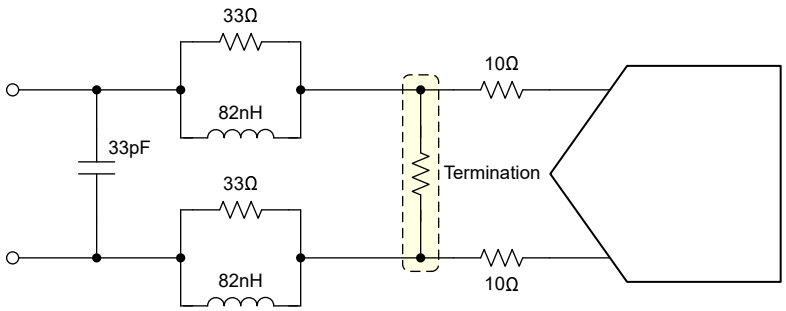


Figure 7-3. Sampling Glitch Filter for Input Frequencies from 0Hz to 60MHz

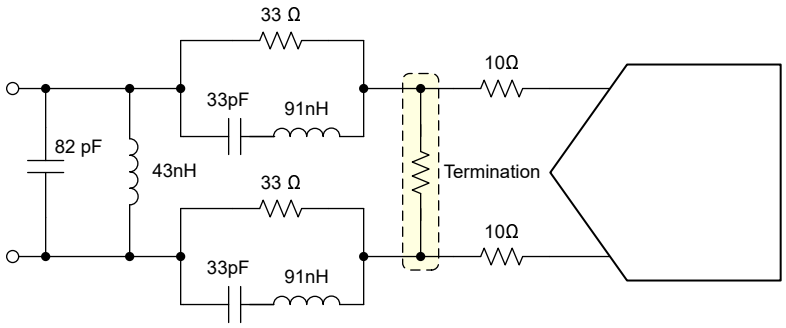


Figure 7-4. Sampling Glitch Filter for Input Frequencies from 60MHz to 120MHz

7.3.1.2.2 AC Coupling

The ADC3664-SP analog inputs require an external DC bias to the common-mode voltage (VCM) of the ADC when the input is AC coupled. An example AC coupled input network is shown in Figure 7-5.

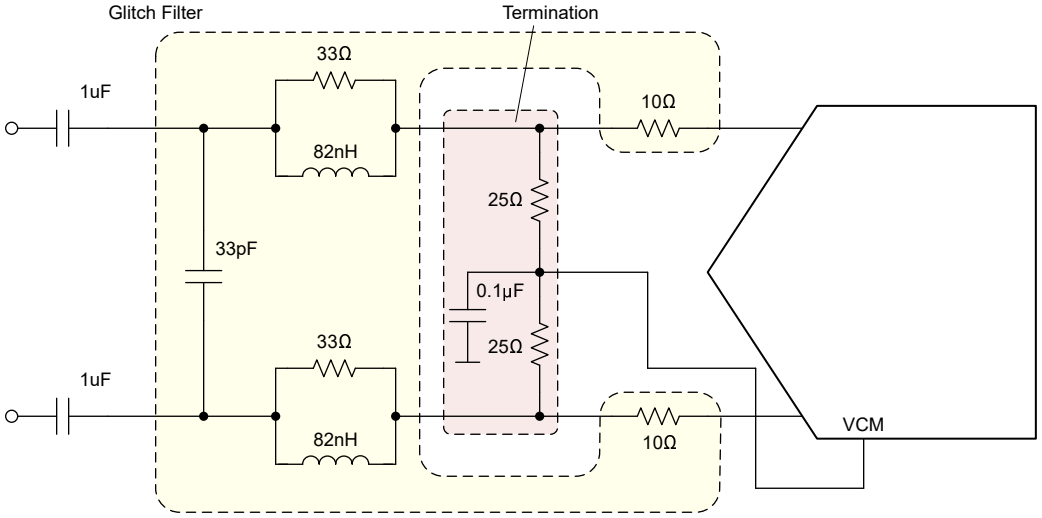


Figure 7-5. AC Coupled Input Network

7.3.1.2.3 DC Coupling

In DC coupled applications, the DC bias needs to be provided from the driver (typically a fully differential amplifier or FDA) using the VCM output of the ADC as shown in Figure 7-6.

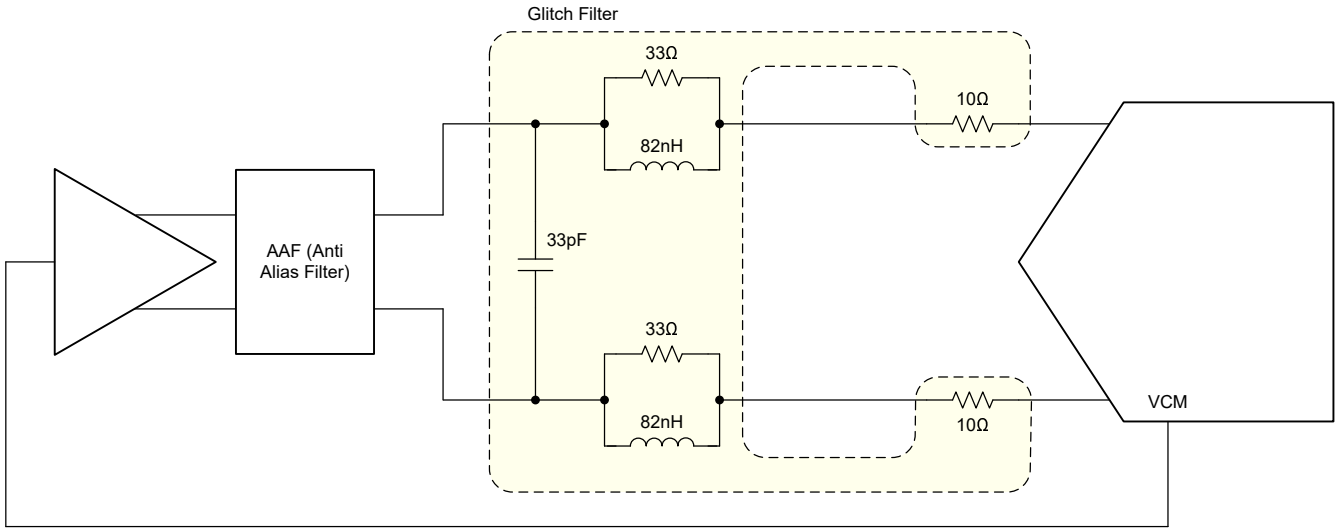


Figure 7-6. DC Coupled Input Network

7.3.2 Clock Input

To maximize the ADC3664-SP SNR performance, the external sampling clock should be a low jitter differential signal. The device provides the option to operate with a single-ended clock input to reduce the device power consumption and simplify system design at the expense of performance.

7.3.2.1 Differential Vs Single-ended Clock Input

The ADC3664-SP can be operated using a differential or a single-ended clock input where the single-ended clock input consumes less power at the expense of performance.

- Differential clock input mode: the clock input must be AC coupled externally. The ADC3664-SP has an internal DC bias.
- Single-ended clock input mode: this mode is configured either using SPI (D3 and D0 of 0x0E), or with the CTRL pin. In this mode, there is no internal clock biasing. The clock input needs to be DC coupled with a common-mode voltage of 0.9V. The unused clock input should be AC coupled to ground.

7.3.2.2 Signal Acquisition Time Adjust

The ADC3664-SP includes a register (D2 of 0x11) to power down an internal DLL which increases the signal acquisition time for sample rates below 30MSPS from 25% to 50% of the clock period. When powering down the DLL, the acquisition time tracks the clock duty cycle.

Table 7-1. Acquisition Time Vs DLL_PDN Setting

SAMPLING CLOCK F_S (MSPS)	DLL_PDN (D2 of 0x11)	ACQUISITION TIME (t_{ACQ})
> 30	0	T_S / 4
≤ 30	1	T_S / 2

7.3.3 Voltage Reference

The ADC3664-SP provides two different options for supplying the voltage reference to the ADCs. The first option is an internal 1.6V reference. The second option is an external 1.6V reference that can be directly connected to the VREF input for best performance. The reference noise can be filtered by connecting a 10µF and a 0.1µF ceramic bypass capacitor to the VREF pin irrespective of the reference source (internal or external).

Note

The voltage reference mode can be selected via SPI or by using the CTRL pin (Section 7.5.1). If the CTRL pin is not used for configuration, the CTRL pin should be connected to AVDD and the voltage reference may be selected via SPI.

7.3.3.1 Internal Voltage Reference

The ADC3664-SP has a 1.6V reference that may be used in the absence of an external reference. A 10µF decoupling capacitor and a 0.1µF decoupling capacitor should be connected between VREF and REFGND. The capacitors should be placed as close to the device pins as possible.

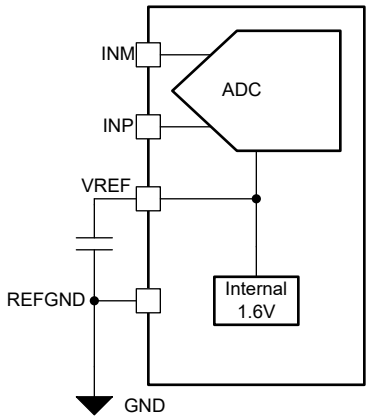


Figure 7-7. Internal Reference Mode

7.3.3.2 External Voltage Reference

For the highest accuracy and best drift performance, the ADC3664-SP reference voltage can be sourced externally. When using an external reference, the VREF pin can be directly connected to an external 1.6V reference. A 10µF decoupling capacitor and a 0.1µF decoupling capacitor should be connected between VREF and REFGND. The capacitors should be placed as close to the device pins as possible.

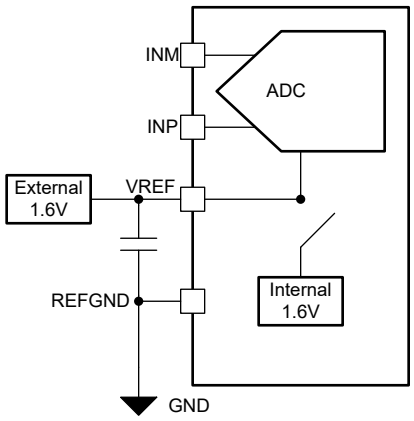


Figure 7-8. External Reference Mode

7.3.4 Digital Data Path & Interface

The ADC3664-SP uses a serial LVDS (SLVDS) interface to output the ADCs' data which minimizes the number of digital interconnects. The SLVDS interface can be configured to one of the following modes: two LVDS lanes per channel (2-wire), one LVDS lane per channel (1-wire), or a half-lane mode (1/2-wire) option where both channels are multiplexed on a single LVDS lane. The device supports configurable output resolutions from 14-bit to 20-bit.

The ADC3664-SP requires an external interface clock (DCLKIN). A delayed version of DCLKIN is used as the interface output clock (DCLK).

7.3.4.1 Data Path Overview

The ADC3664-SP offers a flexible set of digital signal processing (DSP) features (Figure 7-9) where all or a subset of the features can be used. The ADC cores provide an 14-bit output which can be passed to the digital down converters (DDCs) or directly provided to the digital interface. Since the ADC core offers very low latency, the DSP features have to be disabled (D2 of 0x24) for the lowest latency.

Before data is sent on the data lanes, the data first passes through a resolution selection block and then an output bit mapper. The resolution selector offers selection of output resolutions: 14-bit, 16-bit, 18-bit, or 20-bit. For 16-bit, 18-bit, and 20-bit output resolutions, if the DDCs are not used, then zeros are simply appended as LSBs. The output bit mapper maps each data bit to a position within the data stream for each active lane.

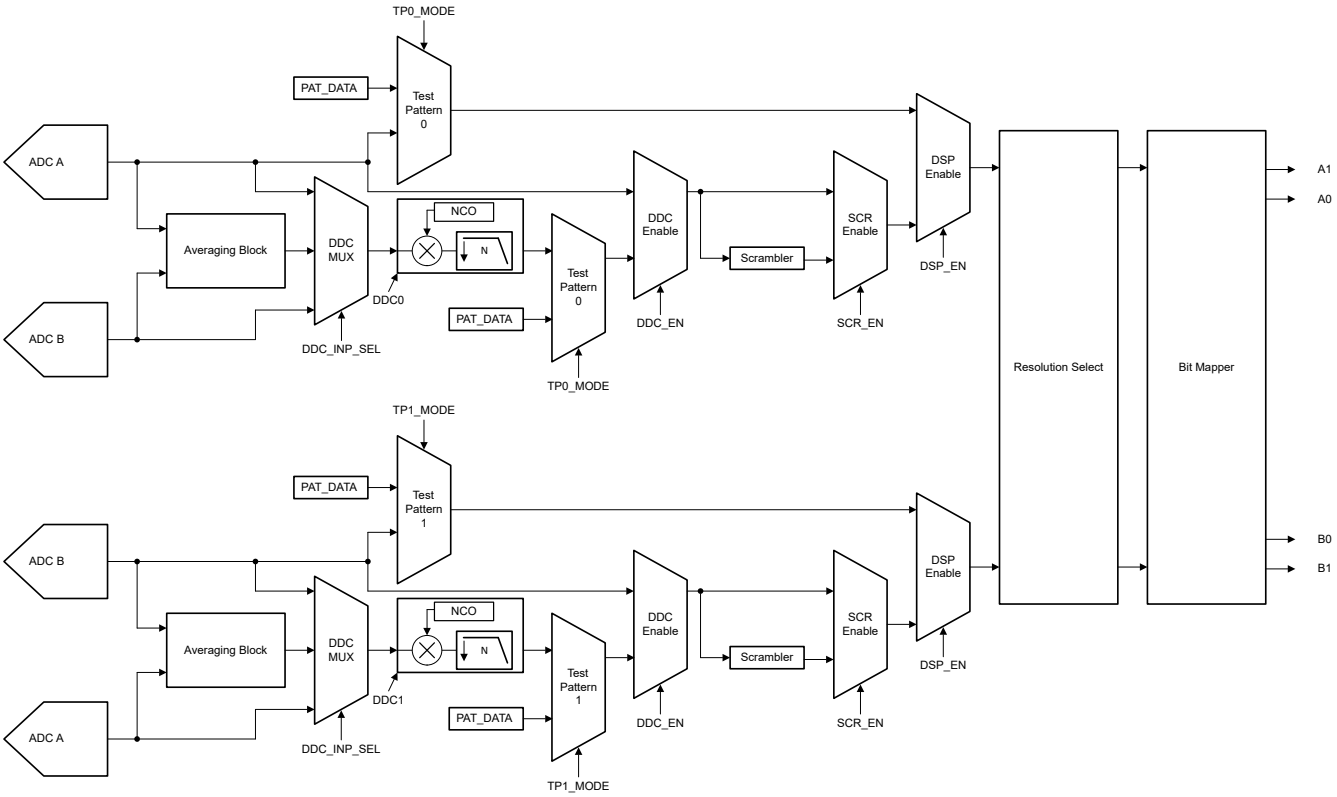


Figure 7-9. Digital Data Path Overview

7.3.4.2 Digital Interface

Table 7-2 provides an overview for the resulting serialization factor depending on output resolution and interface mode. The output serialization factor is internally adjusted based on the interface mode setting and resolution; however, the maximum SLVDS interface output data rate of 1Gbps can not be exceeded regardless of the interface settings. Note, the DCLKIN frequency needs to be adjusted accordingly as well. For example, changing the output resolution from 14-bit to 16-bit in 2-wire mode results in DCLKIN equaling F_S * 4 instead of F_S * 3.5.

The programming sequence for changing the output interface and/or resolution is shown in Section 7.5.3.

Note

When possible, interface modes that allow for an integer ratio between the DCLKIN frequency and the sample clock (CLK) frequency are recommended. This eases meeting the DCLKIN to CLK timing requirements described in Section 7.3.4.3.

Note

Since the ADC3664-SP SNR is very high, the LVDS outputs can potentially couple and degrade the SNR. Therefore, a half swing LVDS mode is provided to reduce the LVDS output swing and minimize coupling. When possible, enable half swing (D6 of 0x1A) to minimize degrading the ADC SNR.

Table 7-2. Digital Interface Modes

Output Resolution	Interface	Serialization Factor	FCLK	DCLKIN	DCLK	Data Rate
14-bit	2-Wire	7x	F_S/2	F_S* 3.5	F_S* 3.5	F_S* 7
	1-Wire	14x	F_S	F_S* 7	F_S* 7	F_S* 14
	1/2-Wire	28x	F_S	F_S* 14	F_S* 14	F_S* 28
16-bit	2-Wire	8x	F_S/2	F_S* 4	F_S* 4	F_S* 8
	1-Wire	16x	F_S	F_S* 8	F_S* 8	F_S* 16
	1/2-Wire	32x	F_S	F_S* 16	F_S* 16	F_S* 32
18-bit	2-Wire	9x	F_S/2	F_S* 4.5	F_S* 4.5	F_S* 9
	1-Wire	18x	F_S	F_S* 9	F_S* 9	F_S* 18
	1/2-Wire	36x	F_S	F_S* 18	F_S* 18	F_S* 36
20-bit	2-Wire	10x	F_S/2	F_S* 5	F_S* 5	F_S* 10
	1-Wire	20x	F_S	F_S* 10	F_S* 10	F_S* 20
	1/2-Wire	40x	F_S	F_S* 20	F_S* 20	F_S* 40

7.3.4.3 DCLKIN

DCLKIN is an external clock to the ADC3664-SP where a delayed version of this clock is used as the output interface clock (DCLK). DCLKIN can be configured for external or internal biasing to a 1.2V common-mode voltage via SPI (D5 of 0x244). DCLKIN also has an internal 100Ω termination resistor.

Note

DCLKIN can be a maximum of 500MHz which limits the LVDS lanes to a maximum of 1Gbps per lane as data is sent on both rising edge and falling edge of DCLK.

Given the low latency architecture of the ADC3664-SP, the relationship between the sample clock (CLK) and DCLKIN needs to be controlled. DCLKIN and CLK must be phase locked to the same reference frequency. The falling edges of CLK and DCLKIN need to be 2.5ns apart otherwise a timing violation occurs. If a timing violation is observed, an internal timing violation detection circuit adds a 1ns delay between CLK and DCLKIN. The effect of this detection circuit is observed as a change in the t_{PD} specification by one DCLK cycle.

7.3.4.4 Output Scrambler

The ADC3664-SP includes an optional output scrambler feature in 2-wire mode only. The scrambler can enabled by enabling the DSP features (D2 of 0x24) and enabling scrambling (D6 of 0x22). When enabled, each sample is split into two halves. Each half of the samples stream is scrambled independently. For example, if the samples stream is at an 18-bit resolution, the stream is divided into two halves consisting of bits D17-D9 & D8-D0. The two halves are fed into independent scrambling blocks where each input bit (x[k]) of each scrambler is XOR-ed with 2 previous bits (y[k-14] and y[k-15]) as shown in Figure 7-10. Since this is a self-synchronizing scrambler, the start up state of the scrambler can be ignored.

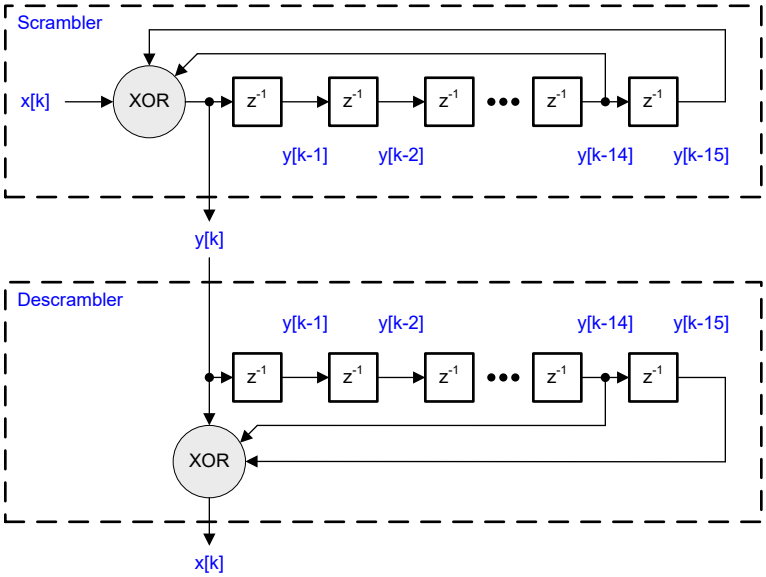


Figure 7-10. Scrambler and Descrambler Operation

Note

The sample streams fed into each scrambler are fed to the scrambler LSB first. Therefore, in the previous example, the sample stream half consisting of D8-D0 is provided to the scrambler with D0 first as x[k] followed by D1 as x[k+1] and so on.

For proper descrambling, the sample stream halves must be descrambled independently then the descrambled data can be used to reconstruct the samples. On the receiver side, the incoming serial data stream can be descrambled by XOR-ing each incoming bit (y[k]) with 2 previous bits (y[k-14] and y[k-15]).

Note

Since the scramblers are looking at the two halves of the sample stream, the output bit mapper needs to be configured such that each lane contains only one of the sample halves.

For example, in 2-wire and 18-bit mode, one lane carries the odd bits (D17, D15, D13, etc.) and one lane carries the even bits (D16, D14, D12, etc.). When scrambling is enabled, the bit mapper needs to be configured so that one lane carries bits D9-D17 and the other lane carries D0-D8 (LSB first for each lane). An example data flow diagram of scrambling an 18-bit sample stream is shown in Figure 7-11, where D17:D0 is the sample provided by the ADC after the resolution select block, the sample is split into D0-D8 and D9-D17 and fed into each scrambler (LSB first) and S0-S17 are the resultant scrambled bits.

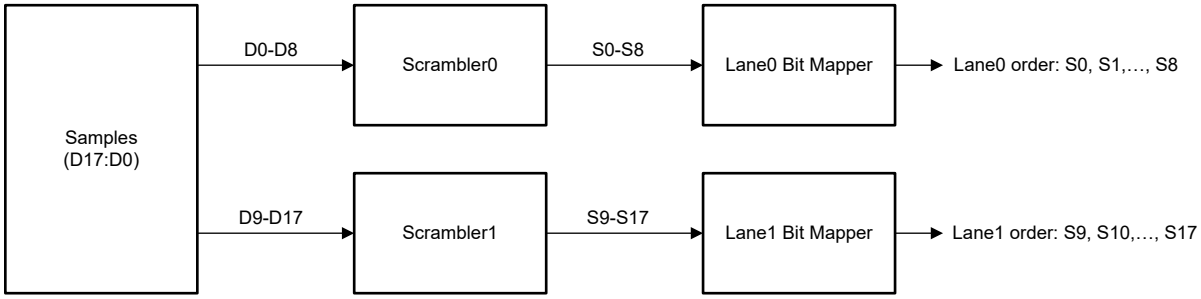


Figure 7-11. 18-bit Scrambling Example

7.3.4.5 Output Bit Mapper

The output bit mapper sits right before the physical output interface and dictates the transmitted bit order on each active lane. Each sample bit is uniquely identifiable by a value as shown in Table 7-3. Similarly, each bit position in each lane is also uniquely identifiable with each bit position having an independent register address. To map a specific bit to a specific bit position (and a specific lane), the value for the bit from the Table 7-3 needs to be written to the address corresponding to the desired bit position in the desired lane.

The ADC3664-SP supports a maximum output resolution of 20-bit; therefore, there are 20-bits that are uniquely identifiable per channel. In 2-wire mode, two samples are considered part of the same frame; therefore, there are two sets of 20-bits each, one for the previous sample and another for the current sample. Section 7.3.4.5.1, Section 7.3.4.5.2, and Section 7.3.4.5.3 provide the register addresses that correspond to each bit position in each lane for 2-wire, 1-wire, and 1/2-wire, respectively.

Table 7-3. Unique Bit Identifiers

BIT_ID	Channel A		Channel B	
	Previous sample (2w only)	Current sample	Previous sample (2w only)	Current sample
D19 (MSB)	0x2D	0x6D	0x29	0x69
D18	0x2C	0x6C	0x28	0x68
D17	0x27	0x67	0x23	0x63
D16	0x26	0x66	0x22	0x62
D15	0x25	0x65	0x21	0x61
D14	0x24	0x64	0x20	0x60
D13	0x1F	0x5F	0x1B	0x5B
D12	0x1E	0x5E	0x1A	0x5A
D11	0x1D	0x5D	0x19	0x59
D10	0x1C	0x5C	0x18	0x58
D9	0x17	0x57	0x13	0x53
D8	0x16	0x56	0x12	0x52
D7	0x15	0x55	0x11	0x51
D6	0x14	0x54	0x10	0x50
D5	0x0F	0x4F	0x0B	0x4B
D4	0x0E	0x4E	0x0A	0x4A
D3	0x0D	0x4D	0x09	0x49
D2	0x0C	0x4C	0x08	0x48
D1	0x07	0x47	0x03	0x43
D0 (LSB)	0x06	0x46	0x02	0x42

7.3.4.5.1 2-Wire Mode

In 2-wire mode, both the current sample and the previous sample columns of Table 7-3 are used. Furthermore, each BIT_ID for the current and previous sample in Table 7-3 needs to be mapped to a specific address which indicates the position of the bit in the respective lane. The address space order is different for 14-bit/18-bit resolutions and 16-bit/20-bit resolutions. The bit mapper address space is also different for each lane.

Note

Depending on the resolution, there can be unused addresses between samples which can be skipped. For example, going from 18-bit resolution to 14-bit, the addresses corresponding to the last two LSBs per lane can be ignored.

Figure 7-12 and Figure 7-13 show register addresses that correspond to the bit positions for each resolution setting and lane. The default values shown for each address are after configuring the ADC3664-SP into the 2-wire interface mode.

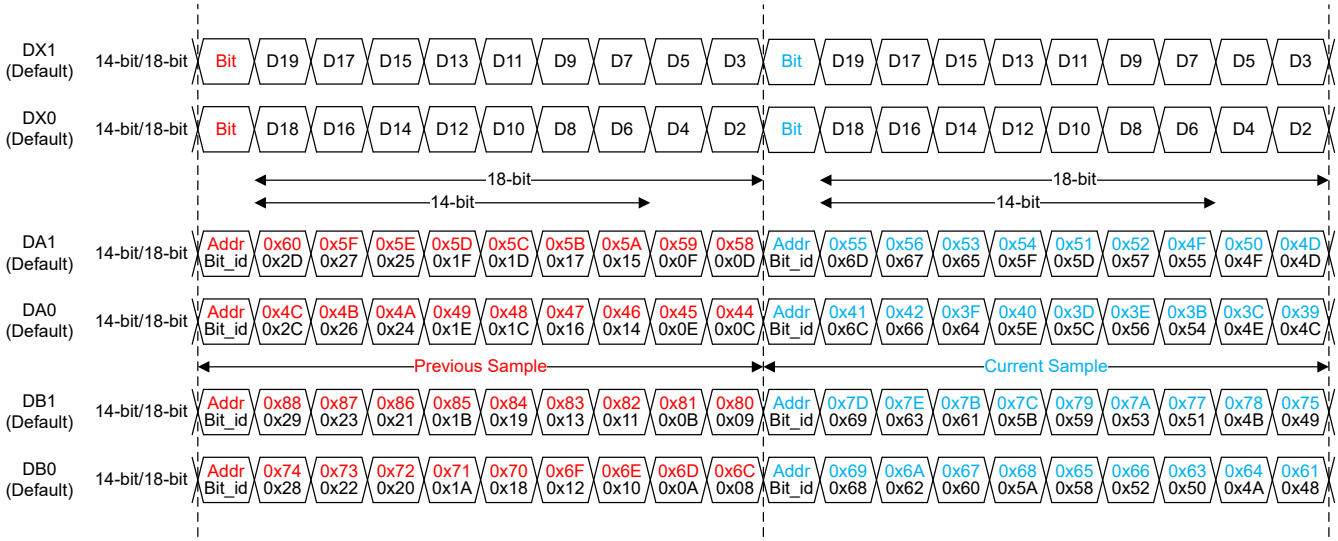


Figure 7-12. Default Bit Mapping for 2-wire, 14-bit/18-bit

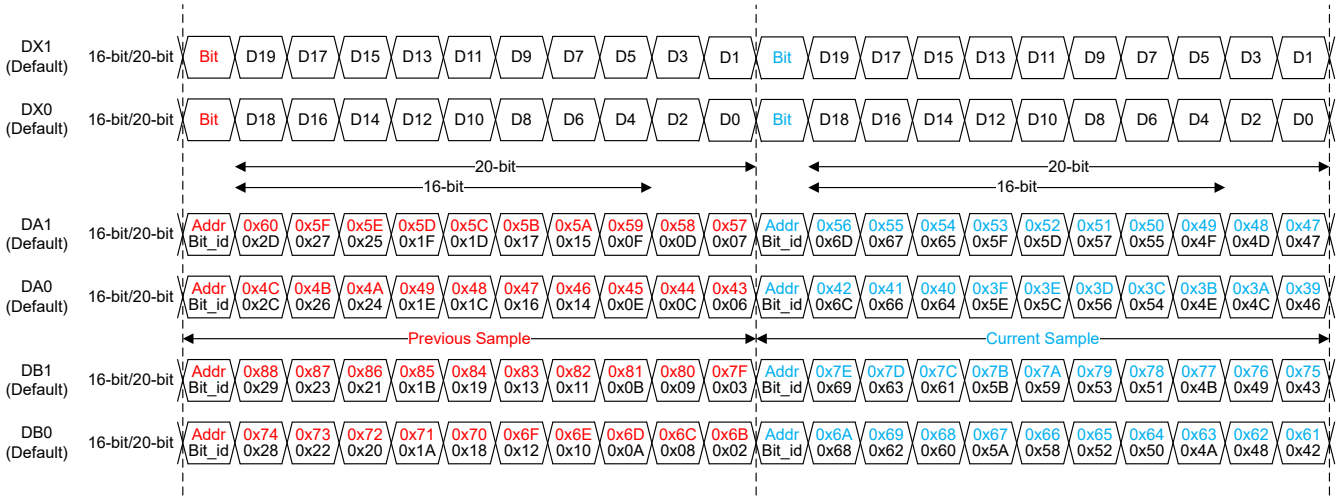


Figure 7-13. Default Bit Mapping for 2-wire, 16-bit/20-bit

Figure 7-14 shows how the bit mapper can be configured to support 16-bit scrambled output. The bit mapper is configured so that the top and bottom halves of the samples are sent on separate lanes and the bits are sent out LSB first as described in Section 7.3.4.4.

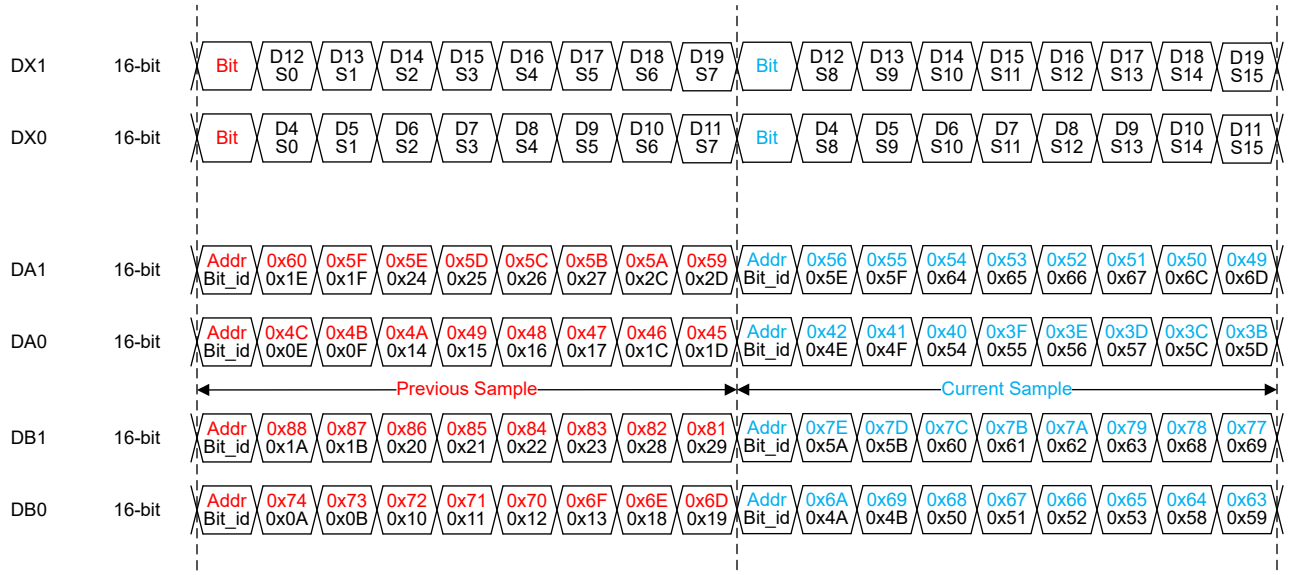


Figure 7-14. Example of Configuring the Bit Mapper for 16-bit Scrambled Output

7.3.4.5.2 1-Wire Mode

Figure 7-15 shows the register addresses that correspond to the bit positions for each resolution setting and lane used for 1-wire mode. The default values shown for each address are after configuring the ADC3664-SP into the 1-wire interface mode.

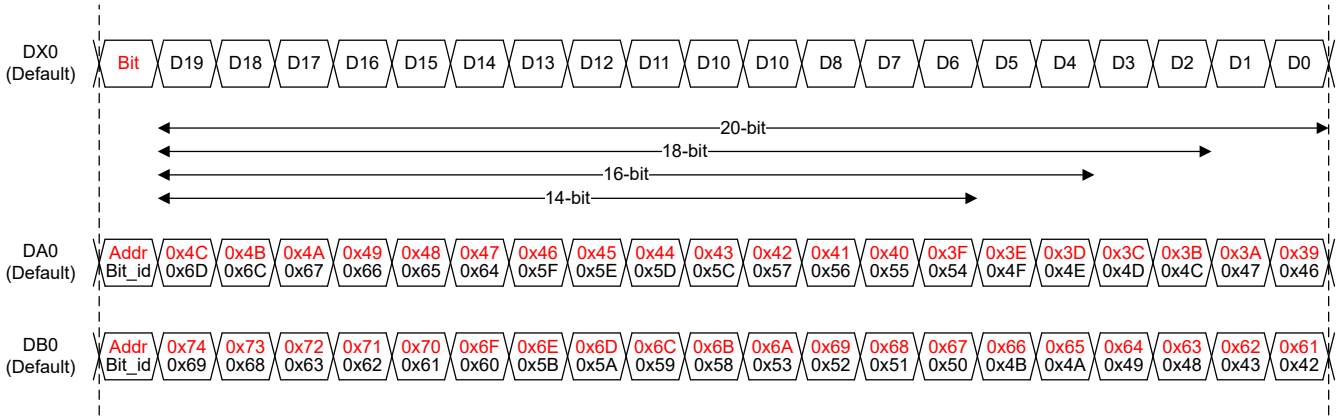


Figure 7-15. Default Bit Mapping for 1-wire

7.3.4.5.3 1/2-Wire Mode

In 1/2-wire mode, both channels multiplexed on the same lane and is provided only on lane DA0. Figure 7-16) shows the register addresses that correspond to the bit positions on the lane for each resolution setting in 1-wire mode. The default values shown for each address are after configuring the ADC3664-SP into the 1/2-wire interface mode.

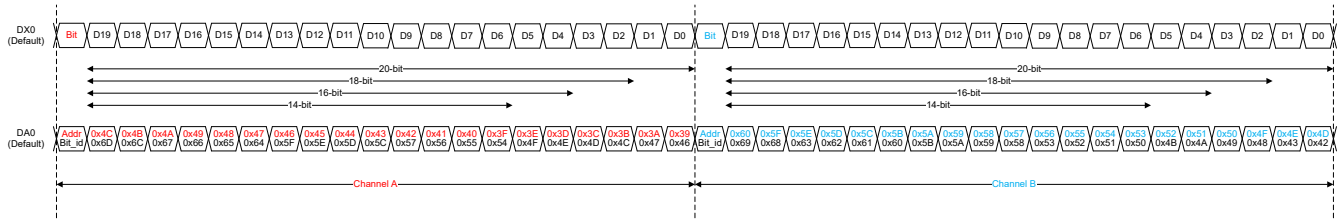


Figure 7-16. Default Bit Mapping for 1/2-wire

7.3.4.6 Output Data Format

The ADC3664-SP samples can be configured for either two's complement format (default) or offset binary via SPI (D2 of 0x8F and 0x92). Table 7-4 provides an overview for minimum and maximum output codes for the two formatting options based on resolution.

Table 7-4. Minimum and Maximum ADC Codes

	Two's Complement (default)				Offset Binary			
RESOLUTION (BIT)	**14**	**16**	**18**	**20**	**14**	**16**	**18**	**20**
$V_{IN,MAX}$	0x1FFF	0x7FFF	0x1FFFF	0x7FFFF	0x3FFF	0xFFFF	0x3FFFF	0xFFFFF
0	0x0000		0x00000		0x2000	0x8000	0x20000	0x80000
$V_{IN,MIN}$	0x2000	0x8000	0x20000	0x80000	0x0000		0x00000	

7.3.4.7 Test Pattern

Figure 7-9 shows the location of the test pattern blocks within the device. When the digital signal processing (DSP) features are disabled (D2 of 0x24), a test pattern block can be enabled to replace the ADC data. Similarly, when using the DDC, a test pattern is available to replace the DDC data.

Note

No test pattern block is available when the DSP features are enabled and the DDC is not used.

Each test pattern block has the capability to generate one of the following outputs:

- Ramp pattern with programmable step size set by PAT_DATA.
- Constant pattern with a programmable custom pattern set by PAT_DATA.

As shown in Figure 7-9, there are two test pattern blocks, test pattern 0 and test pattern 1. The test pattern mode for each block can be configured via D7:D5 and D4:D2 of 0x16. A shared set of data bits (PAT_DATA) is given to the test pattern blocks and this data is used as ramp pattern step size and/or the constant pattern. The PAT_DATA is an 18-bit value located across three different registers: D17:D16 in 0x16, D15:D8 in 0x15, and D7:D0 in 0x14. The PAT_DATA is MSB aligned. For example, if the device is configured for 14-bit resolution and constant pattern, only the top 14-bits of the PAT_DATA are used for the constant pattern. Additionally, in ramp mode, the test pattern counter operates at a 18-bit resolution; therefore, the ramp pattern step size must be configured based on the desired resolution and the step size at that resolution.

Note

When not using the test pattern in the DDC path. Only the top 14-bits of PAT_DATA are used. Therefore, for higher resolutions, zeros are appended as LSBs.

- The test pattern data must be configured to the following for a step size of one at each resolution:
  - 0x00001: 18-bit output resolution
  - 0x00004: 16-bit output resolution
  - 0x00010: 14-bit output resolution

7.3.5 Digital Down Converter

The ADC3664-SP includes an optional digital down converters (DDCs). The DDCs Supports real and complex decimation by 2, 4, 8, 16 and 32. Additionally, each DDC has a 32-bit numerically controlled oscillator (NCO) available in complex decimation.

Internally, the DDC data path operates at a 20-bit resolution to avoid any SNR degradation due to quantization. Depending on the configured resolution, the DDC output is truncated to the selected resolution prior to outputting the data on the digital interface.

Figure 7-17 shows a detailed view of the DDCs. The DDC MUX maps one of three different inputs to each DDC. By default, ADC A and ADC B are mapped to DDC0 and DDC1, respectively. However, the DDC MUX allows for one ADC to be mapped to both DDCs or the average of both ADCs to be mapped to each DDC.

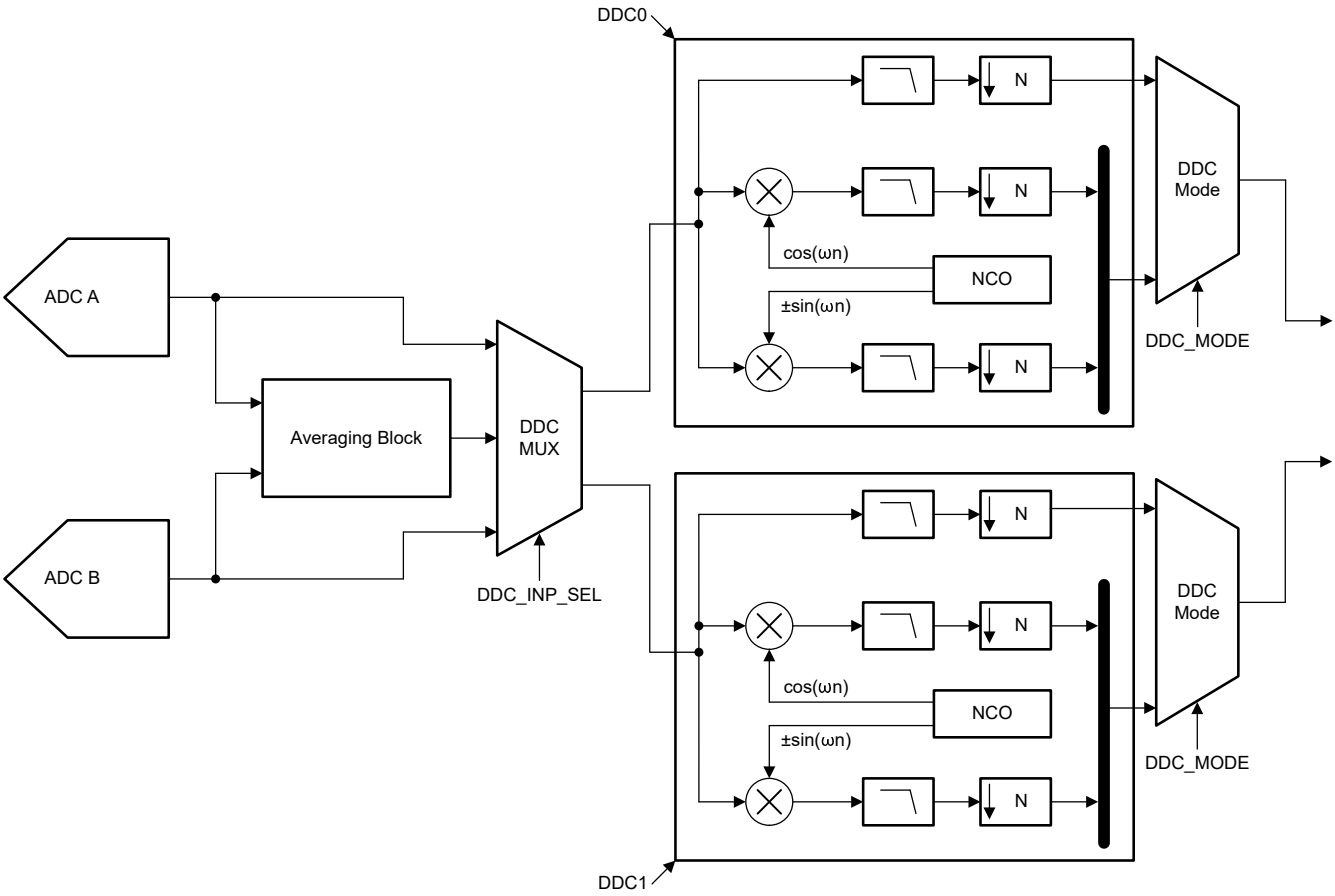


Figure 7-17. Digital Down Converter Overview

7.3.5.1 Decimation Operation

The complex decimation operation is illustrated with an example in Figure 7-18. First, the input signal (and the negative image) are frequency shifted by the NCO frequency as shown on the left side of the figure. Next, a digital filter is applied (centered around 0Hz) and the output data rate is decimated by 8 complex, In this example, the output data rate is complex of $F_{OUT} = F_S/8$ complex with a spectrum from $-F_S/16$ to $F_S/16$. During the complex mixing operation, the spectrum (signal and noise) is split into real and complex parts, and the amplitude is reduced by 6dB. To compensate for the amplitude reduction, there is a 6dB digital gain option in the decimation filter block that can be enabled via SPI.

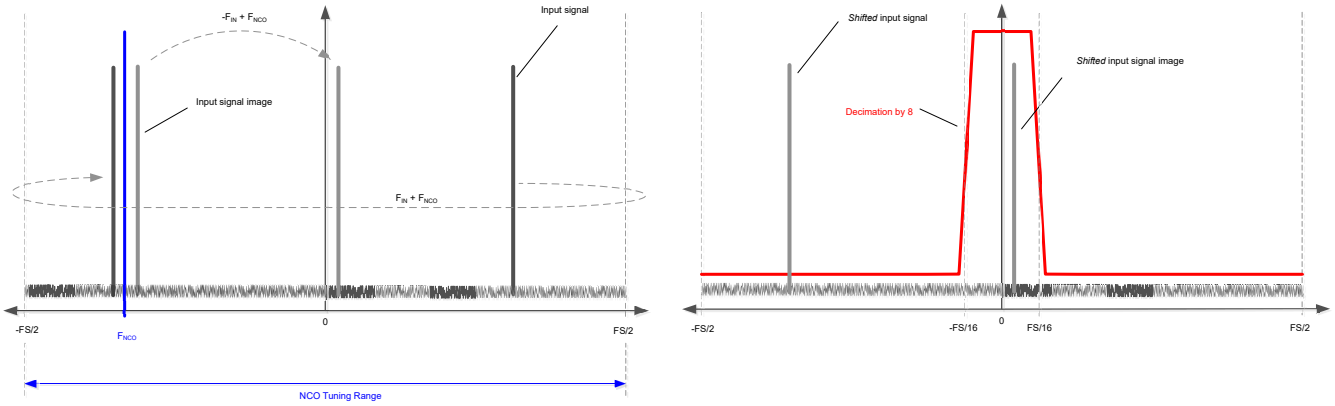


Figure 7-18. Complex Decimation by 8 Example

The real decimation operation is shown in Figure 7-19. There is no mixing in this mode, only the real portion of the complex digital filter is exercised, and the output data rate is reduced. A real decimation by 8 results in an output data rate of $F_{OUT} = F_S/8$ with a spectrum from 0 to $F_S/16$.

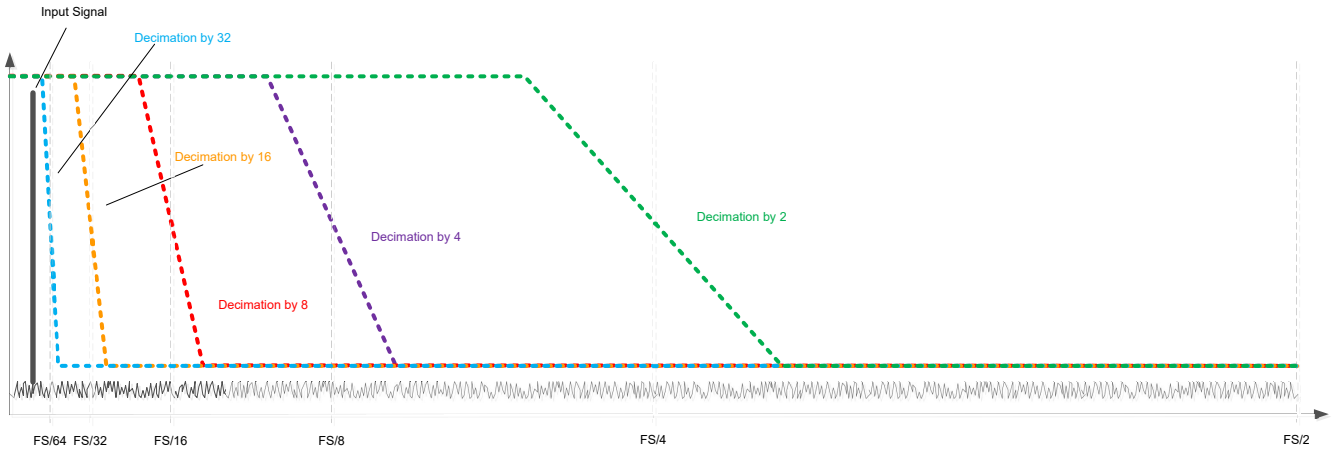


Figure 7-19. Real Decimation Examples

7.3.5.2 Numerically Controlled Oscillator (NCO)

The DDC blocks are equipped with a 32-bit NCOs for mixing in the complex decimation mode prior to the digital filtering. The NCOs provide a complex output of:

$$e^{j\omega n} \text{ or } e^{-j\omega n} \quad (1)$$

where the frequency ω is specified as a 32-bit signed number also known as the frequency control word (FCW).

The complex output is multiplied with the real input from the ADC to mix the desired carrier to a frequency equal to $f_{IN} \pm f_{NCO}$. The NCO frequency can be tuned from $-F_S/2$ to $F_S/2$ and is processed as a signed, 2s complement number. After programming a new NCO frequency, either the NCO_RES (D5 & D1 of 0x26) or the SYNC pin have to be toggled for the new frequency to take effect.

The NCO FCW is calculated as follows:

$$FCW = f_{NCO} \times 2^{32} / F_S \text{ for an } f_{NCO} \text{ in range of 0 to + } F_S/2 \quad (2)$$

$$FCW = (f_{NCO} + F_S) \times 2^{32} / F_S \text{ for an } f_{NCO} \text{ in range of -}F_S/2 \text{ to 0} \quad (3)$$

7.3.5.3 Decimation Filters

Table 7-5 provides an overview of the passband bandwidths and output data rates of the different decimation settings with respect to the ADC sampling rate F_S.

Table 7-5. Decimation Filter Summary and Maximum Available Output Bandwidth

REAL/COMPLEX DECIMATION	DECIMATION SETTING N	OUTPUT RATE	OUTPUT BANDWIDTH	OUTPUT RATE (F_S = 65 MSPS)	OUTPUT BANDWIDTH (F_S = 65 MSPS)
Complex	2	F_S / 2 complex	0.8 × F_S / 2	32.5 MSPS complex	26 MHz
	4	F_S / 4 complex	0.8 × F_S / 4	16.25 MSPS complex	13 MHz
	8	F_S / 8 complex	0.8 × F_S / 8	8.125 MSPS complex	6.5 MHz
	16	F_S / 16 complex	0.8 × F_S / 16	4.0625 MSPS complex	3.25 MHz
	32	F_S / 32 complex	0.8 × F_S / 32	2.03125 MSPS complex	1.625 MHz
Real	2	F_S / 2	0.4 × F_S / 2	32.5 MSPS	13 MHz
	4	F_S / 4	0.4 × F_S / 4	16.25 MSPS	6.5 MHz
	8	F_S / 8	0.4 × F_S / 8	8.125 MSPS	3.25 MHz
	16	F_S / 16	0.4 × F_S / 16	4.0625 MSPS	1.625 MHz
	32	F_S / 32	0.4 × F_S / 32	2.03125 MSPS	0.8125 MHz

The decimation filter responses are normalized to the ADC sampling clock frequency F_S and illustrated in Figure 7-20 to Figure 7-29. Each figure contains the filter passband, transition band(s) and stopband(s).

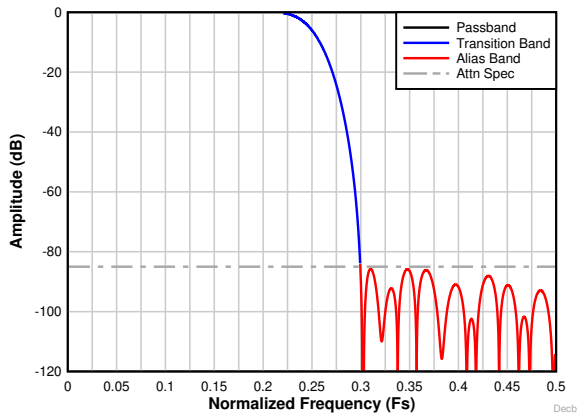


Figure 7-20. Decimation by 2 Filter Frequency Response

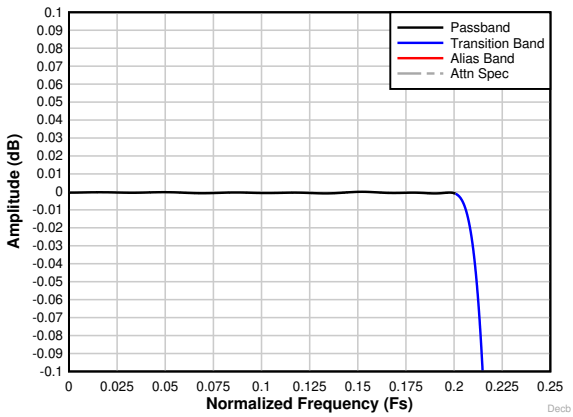


Figure 7-21. Decimation by 2 Filter Passband Ripple Response

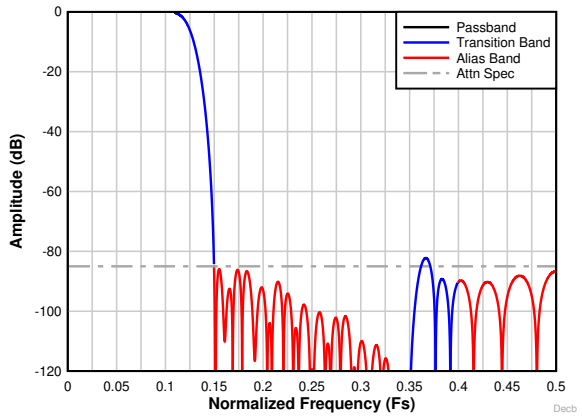


Figure 7-22. Decimation by 4 Filter Frequency Response

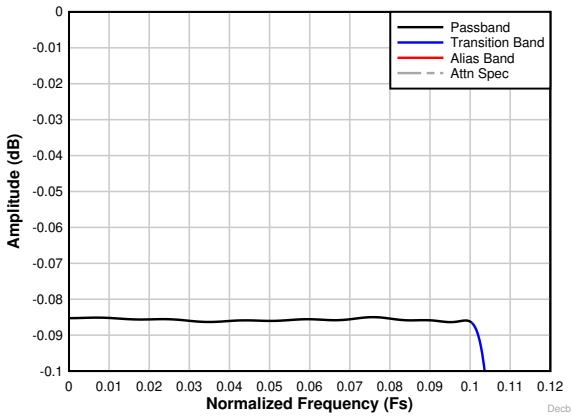


Figure 7-23. Decimation by 4 Filter Passband Ripple Response

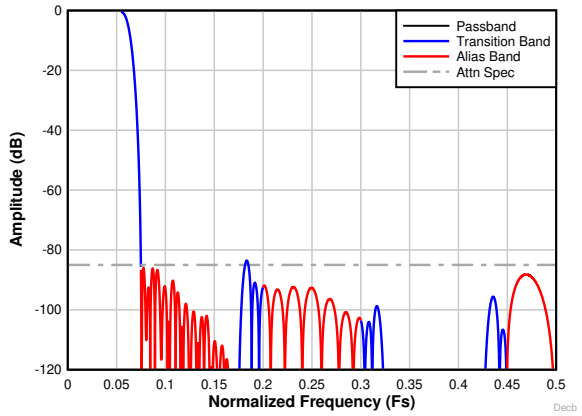


Figure 7-24. Decimation by 8 Filter Frequency Response

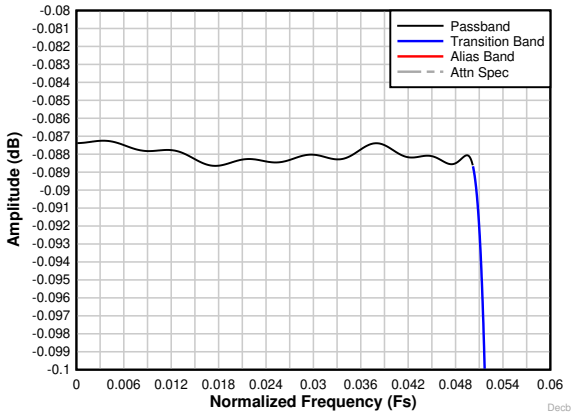


Figure 7-25. Decimation by 8 Filter Passband Ripple Response

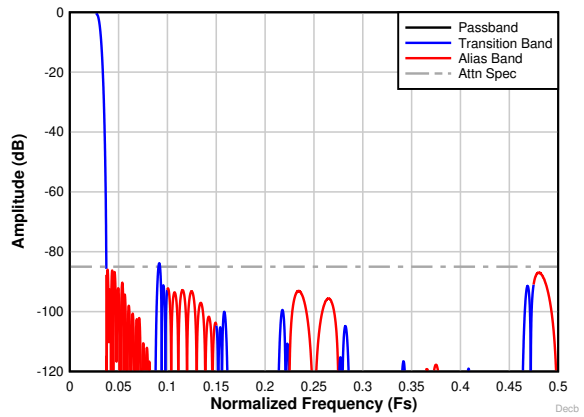


Figure 7-26. Decimation by 16 Filter Frequency Response

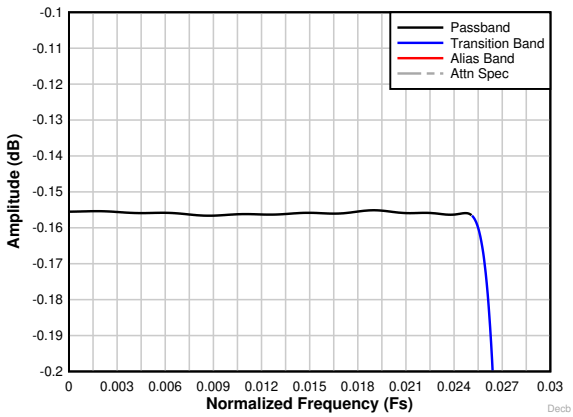


Figure 7-27. Decimation by 16 Filter Passband Ripple Response

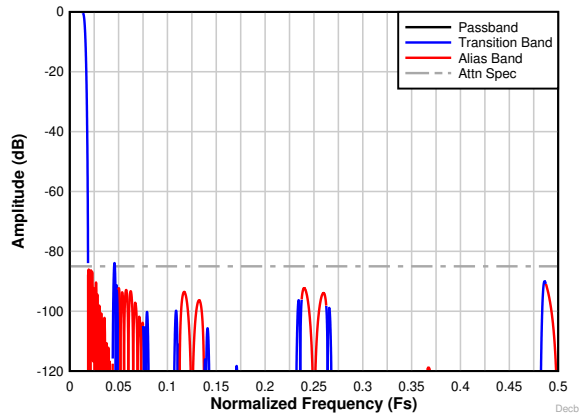


Figure 7-28. Decimation by 32 Filter Frequency Response

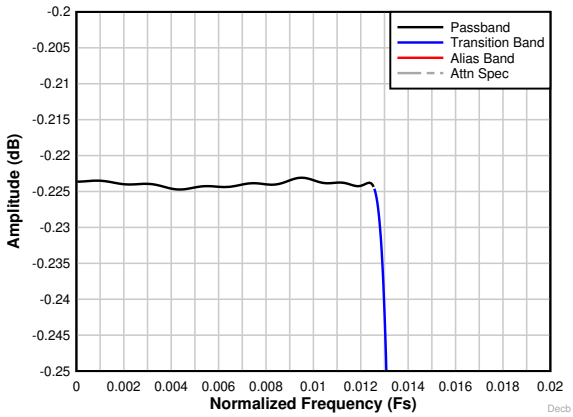


Figure 7-29. Decimation by 32 Filter Passband Ripple Response

7.3.5.4 SYNC

The PDN/SYNC pin can be used to synchronize multiple devices using an external SYNC signal. The PDN/SYNC pin can be configured via SPI to function as the synchronization input. Once configured for SYNC, the SYNC signal is latched by the rising edge of the sampling clock as shown in Figure 7-30.

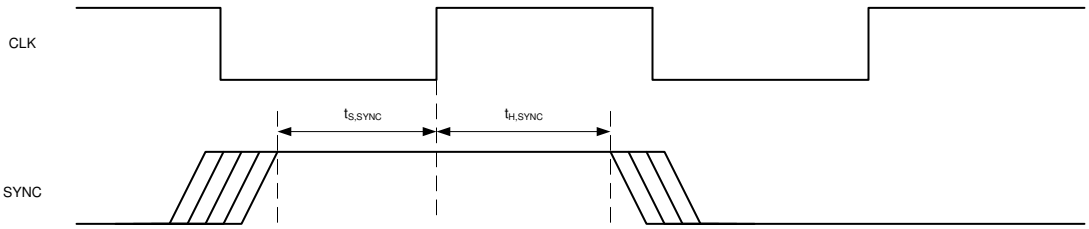


Figure 7-30. External SYNC Timing Diagram

The synchronization signal is only required when using the DDCs. When using the SPI based SYNC or the PDN/SYNC pin, the internal clock divider is reset. If no SYNC signal is given, the internal clock dividers may not be synchronized across devices. The SYNC signal also resets the NCO phase, and loads the new NCO frequency. The SYNC signal should be provided as a single pulse with a pulse width of at least 256 clock cycles.

7.3.5.5 Output Data Format with Decimation

When using decimation, the digital output data is formatted as shown in Figure 7-31 (complex decimation) and Figure 7-32 (real decimation). The figures are representative of 14-bit output resolution.

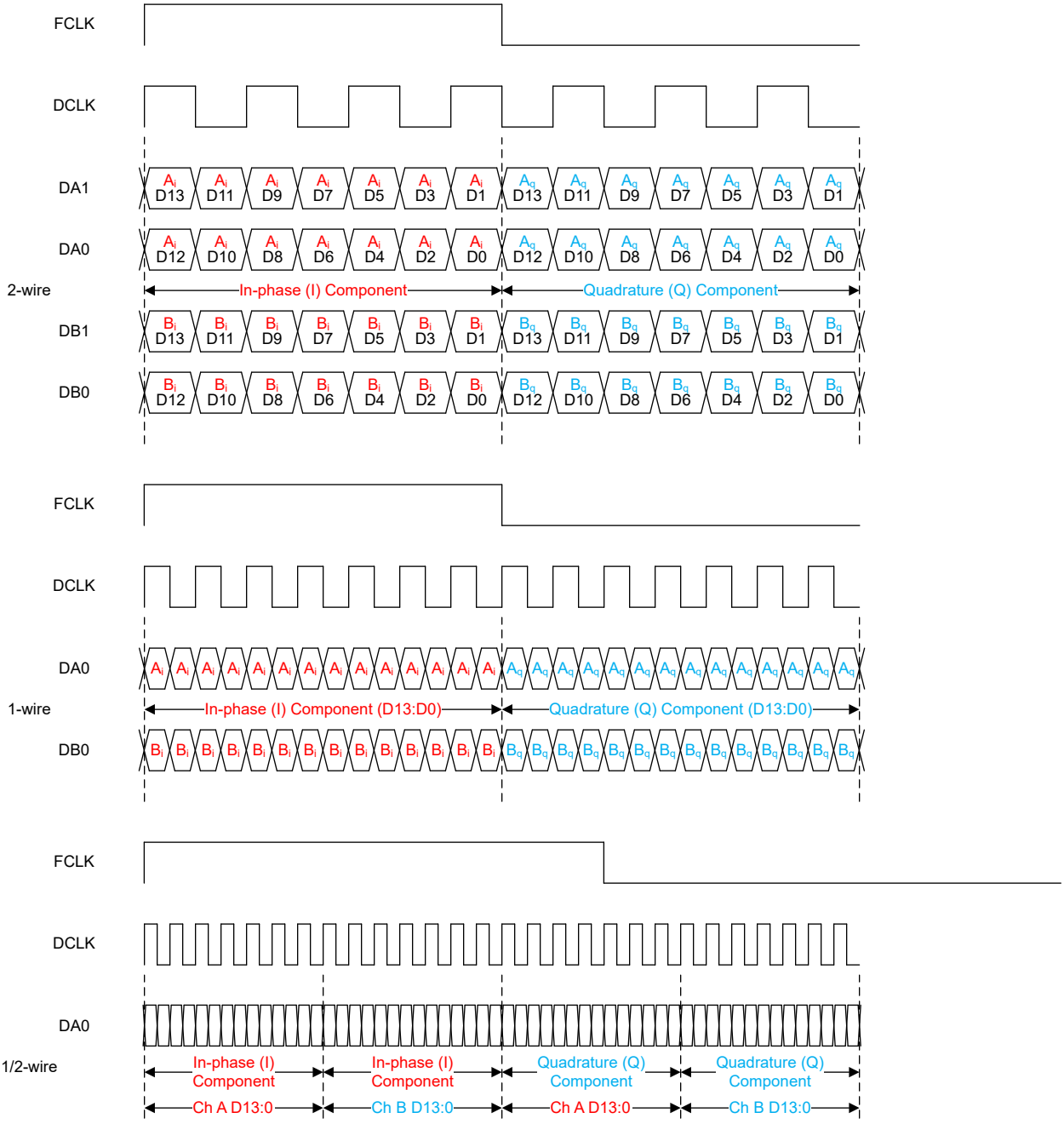


Figure 7-31. Output Data Format in Complex Decimation (14-bit Output Resolution)

Figure 7-32. Output Data Format in Real Decimation (14-bit Output Resolution)

7.4 Device Functional Modes

7.4.1 Low Latency Mode

The ADC3664-SP low latency mode can be configured by disabling the digital signal processing (DSP) features. The DSP features can be disabled via SPI (D2 of 0x24) to make sure the ADC latency is 2 clock cycles in 2-wire mode or 1 clock cycle in 1-wire mode.

7.4.2 Averaging Mode

The ADC3664-SP includes a digital channel averaging feature which enables improvement of the ADC SNR (see Figure 7-33). The same input signal is given to both ADC inputs externally and the outputs of the two ADCs are averaged internally. Through averaging, uncorrelated noise (such as ADC thermal noise) adds incoherently which improves SNR by about 3dB.

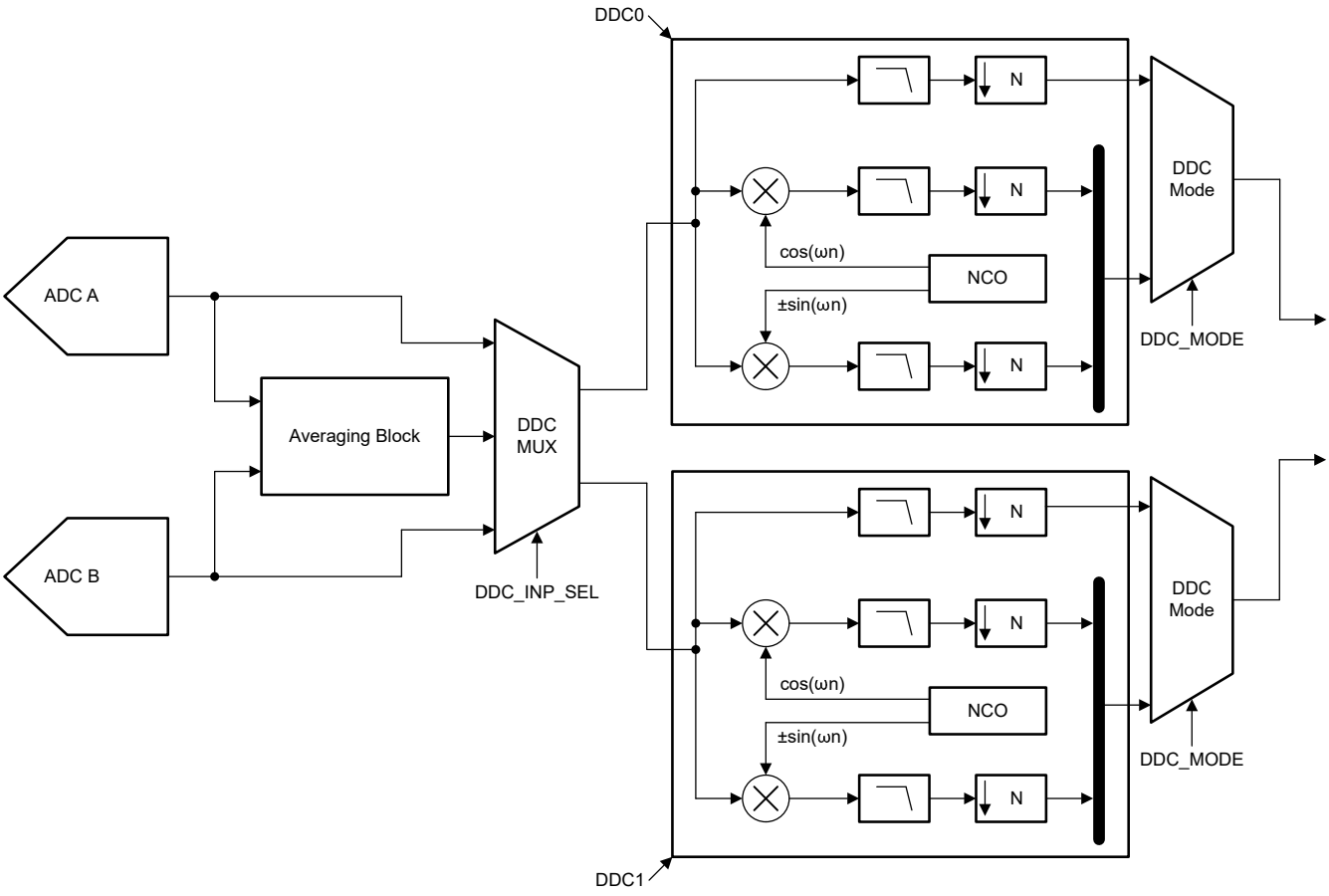


Figure 7-33. Averaging Diagram

7.5 Programming

The device is primarily configured and controlled using the Serial Peripheral Interface (SPI); however, the device can operate in a default configuration without requiring the SPI. The power down state, internal or external reference selection, and sampling clock input type are configurable via the PDN/SYNC and CTRL pins.

Note

The power down functionality requires the ADC sampling clock to be present.

7.5.1 Pin Control

The ADC voltage reference and sampling clock input type can be selected using the CTRL pin. Even though there is an internal 100kΩ pull-up resistor to AVDD, the CTRL pin should be set to a voltage externally and not left floating. When using a voltage divider to set the CTRL pin voltage, resistor values less than 5kΩ should be used.

Table 7-6. CTRL Pin Settings

CTRL PIN VOLTAGE	VOLTAGE REFERENCE OPTION	CLOCKING TYPE
> 1.7V (Default)	External reference	Differential clock input
0.5 - 0.7V	Internal reference	Differential clock input
< 0.1V	Internal reference	Single-ended clock input

7.5.2 Serial Peripheral Interface (SPI)

The device has a set of internal registers that can be accessed via SPI formed by the $\overline{\text{SEN}}$ (serial interface enable), SCLK (serial interface clock) and SDIO (serial interface data input/output) pins. Bits are serially shifted into the device when $\overline{\text{SEN}}$ is low. Input data is latched at every SCLK rising edge when $\overline{\text{SEN}}$ is active (low). The serial data is loaded into the register at the 24th SCLK rising edge when $\overline{\text{SEN}}$ is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active $\overline{\text{SEN}}$ pulse. The interface can function with SCLK frequencies from 20MHz down to as slow as a few hertz.

7.5.2.1 Register Write

The internal registers can be programmed by following these steps:

1. Drive the $\overline{SEN}$ pin low.
2. Set the R/W bit to 0 (bit A15 of the 16-bit address) and bits A[14:12] in the address field to 0.
3. Initiate a serial interface cycle by specifying the address of the register (A[11:0]) whose content is to be written.
4. Write the 8-bit data that to be latched on the SCLK rising edges.

Figure 7-34 shows the relevant timing requirements for the register write operation.

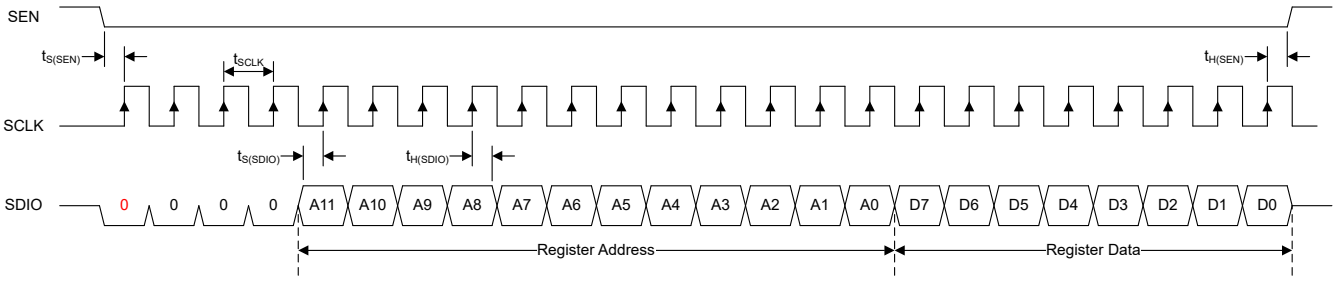


Figure 7-34. Serial Register Write Timing Diagram

7.5.2.2 Register Read

The device includes a mode where the contents of the internal registers can be read back using the SDIO pin. This read back mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the $\overline{SEN}$ pin low.
2. Set the R/W bit (A15) to 1. Set A[14:12] in the address field to 0.
3. Initiate a serial interface cycle specifying the address of the register (A[11:0]) whose content will be read.
4. The device launches the contents (D[7:0]) of the selected register on the SDIO pin on SCLK falling edge.
5. The external controller can capture the contents on the SCLK rising edge.

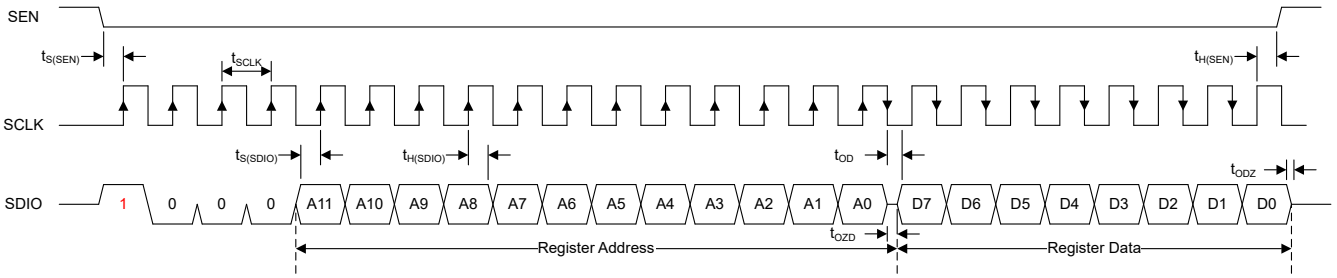


Figure 7-35. Serial Register Read Timing Diagram

7.5.3 Device Configuration Steps

The following sequence summarizes all the relevant registers for changing the ADC3664-SP modes including the digital signal processing (DSP) features and the output interface. Steps 1 and 2 must come first since the E-Fuse load resets some of the device registers, the remaining steps can come in any order.

Table 7-7. Configuration Steps for the ADC3664-SP

<table>
<tr><th>STEP</th><th>FEATURE</th><th>ADDRESS</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="6">1</td><td rowspan="15">Output Interface</td><td rowspan="6">0x07</td><td colspan="4">Select the output interface mode based on output resolution.</td></tr>
<tr><td>Output Resolution</td><td>2-wire</td><td>1-wire</td><td>1/2-wire</td></tr>
<tr><td>14-bit</td><td>0x2B</td><td rowspan="4">0x6C</td><td rowspan="4">0x8D</td></tr>
<tr><td>16-bit</td><td>0x4B</td></tr>
<tr><td>18-bit</td><td>0x2B</td></tr>
<tr><td>20-bit</td><td>0x4B</td></tr>
<tr><td>2</td><td>0x13</td><td colspan="4">Load the output interface bit mapping using the E-fuse loader (D0 of 0x13). Write 0x01 to 0x13, wait ~ 1ms so that the bit mapping is loaded properly, and write 0x00 to 0x13.</td></tr>
<tr><td rowspan="8">3</td><td rowspan="8">0x19</td><td colspan="4">Configure the FCLK settings based on the desired device modes and interface modes.</td></tr>
<tr><td>Mode</td><td>Interface Mode</td><td>FCLK_SRC</td><td>FCLK_DIV</td><td>TOG_FCLK</td></tr>
<tr><td rowspan="3">DSP Features Disabled/Real Decimation</td><td>2-wire</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>1-wire</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1/2-wire</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td rowspan="3">Complex Decimation</td><td>2-wire</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1-wire</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>1/2-wire</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>4</td><td>0x1B</td><td colspan="4">Select the output interface resolution.</td></tr>
<tr><td rowspan="10">5</td><td rowspan="10">0x20
0x21
0x22</td><td colspan="4">Configure the FCLK pattern based on device modes.</td></tr>
<tr><td>Mode</td><td>Output Resolution</td><td>2-wire</td><td>1-wire</td><td>1/2-wire</td></tr>
<tr><td rowspan="4">DSP Features Disabled/Real Decimation</td><td>14-bit</td><td rowspan="8">0xFFC00</td><td>0xFE000</td><td rowspan="4">0xFFC00</td></tr>
<tr><td>16-bit</td><td>0xFF000</td></tr>
<tr><td>18-bit</td><td>0xFF800</td></tr>
<tr><td>20-bit</td><td>0xFFC00</td></tr>
<tr><td rowspan="4">Complex Decimation</td><td>14-bit</td><td rowspan="4">0xFFFFF</td><td rowspan="4">0xFFFFF</td></tr>
<tr><td>16-bit</td></tr>
<tr><td>18-bit</td></tr>
<tr><td>20-bit</td></tr>
<tr><td>6</td><td>0x39..0x60
0x61..0x88</td><td colspan="4">Change output bit mapping from the default as needed (for example, if enabling the scrambler).</td></tr>
<tr><td>7</td><td>0x24
0x22</td><td colspan="4">Optionally, the scrambler can be enabled if the device is configured in the 2-wire interface mode.</td></tr>
<tr><td>8</td><td rowspan="5">Digital Down converters</td><td>0x24</td><td colspan="4">Optionally, enable the DDCs.</td></tr>
<tr><td>9</td><td>0x25</td><td colspan="4">If using the DDCs, configure the DDCs settings.</td></tr>
<tr><td>10</td><td>0x2A/B/C/D
0x31/2/3/4</td><td colspan="4">If using complex decimation, program the desired NCO frequency.</td></tr>
<tr><td rowspan="4">11</td><td rowspan="4">0x27
0x2E</td><td colspan="4">Set both bits to 0 if not using complex decimation.</td></tr>
<tr><td colspan="2">Interface Mode</td><td>IQ_ORDER</td><td>Q_DEL</td></tr>
<tr><td colspan="2">2-wire</td><td>1</td><td>0</td></tr>
<tr><td colspan="2">1-wire</td><td>0</td><td>1</td></tr>
<tr><td colspan="2">1/2-wire</td><td>1</td><td>1</td></tr>
<tr><td>12</td><td>0x26</td><td colspan="4">Set the DDC gain and toggle the NCO reset bit to update the NCO frequency.</td></tr>
</table>

7.5.4 Register Map

Table 7-8. Register Map Summary

REGISTER ADDRESS	REGISTER DATA							
A[11:0]	D7	D6	D5	D4	D3	D2	D1	D0
0x00	0	0	0	0	0	0	0	RESET
0x07	IF_MAPPER_SEL			0	IF_SEL_EN	IF_MODE_SEL		
0x08	0	0	0	0	0	PDN_A	PDN_B	PDN_GLOBAL
0x09	0	0	0	0	PDN_DA1	PDN_DA0	PDN_DB1	PDN_DB0
0x0E	SYNC_PIN_EN	SPI_SYNC_VAL	SYNC_SRC_SEL	0	CTRL_MODE	REF_SEL		SE_CLK_EN
0x11	0	0	0	0	0	DLL_PDN	0	0
0x13	0	0	0	0	0	0	0	FUSE_LD
0x14	PAT_DATA[7:0]							
0x15	PAT_DATA[15:8]							
0x16	TP1_MODE			TP0_MODE			PAT_DATA_[17:16]	
0x19	FCLK_SRC	0	0	FCLK_DIV	0	0	0	TOG_FCLK
0x1A	0	HALF_SWING_EN	0	0	0	0	0	0
0x1B	RES_SEL_EN	20B_EN	RES_SEL			0	0	0
0x1E	0	0	0	0	LVDS_DATA_DEL		LVDS_DCLK_DEL	
0x20	FCLK_PAT[7:0]							
0x21	FCLK_PAT[15:8]							
0x22	0	SCR_EN	0	0	FCLK_PAT[19:16]			
0x24	0	0	AVG_EN	DDC_INP_SEL		DSP_EN	DDC_EN	0
0x25	DDC_MUX_EN	DEC_FACTOR			DDC_MODE	0	0	0
0x26	DDC0_GAIN		NCO0_RES	0	DDC1_GAIN		NCO1_RES	0
0x27	0	0	0	IQ0_ORDER	Q0_DEL	0	0	0
0x2A	FCW0[7:0]							
0x2B	FCW0[15:8]							
0x2C	FCW0[23:16]							
0x2D	FCW0[31:24]							
0x2E	0	0	0	IQ1_ORDER	Q1_DEL	0	0	0
0x31	FCW1[7:0]							
0x32	FCW1[15:8]							
0x33	FCW1[23:16]							
0x34	FCW1[31:24]							
0x39..0x60	BIT_MAPPER_A							
0x61..0x88	BIT_MAPPER_B							
0x8F	0	0	0	0	0	0	FORMAT_A	0
0x92	0	0	0	0	0	0	FORMAT_B	0
0x244	0	0	DCLKIN_VCM	0	0	0	0	0

7.5.4.1 Detailed Register Description

Figure 7-36. Register 0x00

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	RESET
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-9. Register 0x00 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0	Must write 0.
0	RESET	R/W	0	This bit resets all internal registers to the default values and self clears to 0.

Figure 7-37. Register 0x07

7	6	5	4	3	2	1	0
IF_MAPPER_SEL			0	IF_SEL_EN	IF_MODE_SEL		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-10. Register 0x07 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	IF_MAPPER_SEL	R/W	000	Select the proper bit mapping based on the desired interface mode. The bit mapping for each mode is described under Section 7.3.4.5. The default bit mapping for each interface mode is loaded from internal fuses and also requires a fuse load sequence (see Table 7-15). It is imperative that this field is set before the fuse load sequence. 001: bit mapping for 2-wire, 18-bit and 14-bit. 010: bit mapping for 2-wire, 16-bit. 011: bit mapping for 1-wire. 100: bit mapping for 1/2-wire.
4	0	R/W	0	Must write 0.
3	IF_SEL_EN	R/W	0	Enables selection of the output interface mode. 0: interface mode selection is disabled. 1: interface mode selection is enabled.
2-0	IF_MODE_SEL	R/W	000	Select the desired output interface mode (2-wire, 1-wire, or 1/2-wire). IF_SEL_EN must be set to 1 for this setting to take effect. 011: interface mode set to 2-wire. 100: interface mode set to 1-wire. 101: interface mode set to 1/2-wire.

Figure 7-38. Register 0x08

7	6	5	4	3	2	1	0
0	0	0	0	0	PDN_A	PDN_B	PDN_ GLOBAL
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-11. Register 0x08 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R/W	0	Must write 0.
2	PDN_A	R/W	0	Power down ADC A. 0: ADC A is enabled. 1: ADC A is powered down.
1	PDN_B	R/W	0	Power down ADC B. 0: ADC B is enabled. 1: ADC B is powered down.
0	PDN_GLOBAL	R/W	0	Device global power down. 0: device is enabled. 1: device is powered down.

Figure 7-39. Register 0x09

7	6	5	4	3	2	1	0
0	0	0	0	PDN_DA1	PDN_DA0	PDN_DB1	PDN_DB0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-12. Register 0x09 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0	Must write 0.
3	PDN_DA1	R/W	0	Lane A1 power down control. This lane is not powered down automatically in the 1-wire and 1/2-wire interface modes. 0: lane A1 is enabled. 1: lane A1 is powered down.
2	PDN_DA0	R/W	0	Lane A0 power down control. 0: lane A0 is enabled. 1: lane A0 is powered down.
1	PDN_DB1	R/W	0	Lane B1 power down control. This lane is not powered down automatically in the 1-wire and 1/2-wire interface modes. 0: lane B1 is enabled. 1: lane B1 is powered down.
0	PDN_DB0	R/W	0	Lane B0 power down control. This lane is not powered down automatically in the 1/2-wire interface mode. 0: lane B0 is enabled. 1: lane B0 is powered down.

Figure 7-40. Register 0x0E

7	6	5	4	3	2	1	0
SYNC_ PIN_EN	SPI_SYNC_ VAL	SYNC_SRC_ SEL	0	CTRL_MODE	REF_SEL		SE_CLK_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-13. Register 0x0E Field Descriptions

Bit	Field	Type	Reset	Description
7	SYNC_PIN_EN	R/W	0	The PDN/SYNC pin is a dual purpose pin. 0: the PDN/SYNC pin is configured as the global power down control pin. 1: the PDN/SYNC pin is configured as a SYNC pin.
6	SPI_SYNC_VAL	R/W	0	Set the internal SYNC state when SYNC_SRC_SEL is set. SPI_SYNC_VAL should be toggled to issue a SYNC sequence. Doesn't automatically reset to 0. 0: internal SYNC state is set to 0 (normal operation). 1: internal SYNC state set to 1 (initiate SYNC sequence).
5	SYNC_SRC_SEL	R/W	0	Select the SYNC source for the device. 0: SYNC internal state from the PDN/SYNC pin. 1: SYNC internal state from the SPI_SYNC_VAL field.
4	0	R/W	0	Must write 0.
3	CTRL_MODE	R/W	0	Select if the ADC reference mode and sample clock type is set through the CTRL pin or based on the REF_SEL and SE_CLK_EN fields. 0: the CTRL pin controls the ADC reference mode and sample clock input type. 1: the REF_SEL and SE_CLK_EN fields control the ADC reference mode and sampling clock type, respectively.
2-1	REF_SEL	R/W	00	Select the ADC reference mode via SPI. CTRL_MODE must be set to 1 for this setting to take effect. 00: internal 1.6V reference used as the ADC reference. 10: the ADC reference is provided externally.
0	SE_CLK_EN	R/W	0	Select the ADC sampling clock input type. CTRL_MODE must be set to 1 for this setting to take effect. 0: the ADC sampling clock input configured as a differential input. 1: the ADC sampling clock input configured as a single-ended input.

Figure 7-41. Register 0x11

7	6	5	4	3	2	1	0
0	0	0	0	0	DLL_PDN	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-14. Register 0x11 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	0	R/W	0	Must write 0.
2	DLL_PDN	R/W	0	Select power down state for an internal DLL. See Section 7.3.2.2.
1-0	0	R/W	0	Must write 0.

Figure 7-42. Register 0x13

7	6	5	4	3	2	1	0
0	0	0	0	0	0		FUSE_LD
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-15. Register 0x13 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	R/W	0	Must write 0.
0	FUSE_LD	R/W	0	Internal fuse load control. Set to 1, wait for ~1ms, and set to 0 to load the device configuration based on the interface mode settings.

Figure 7-43. Register 0x14/15/16

7	6	5	4	3	2	1	0
PAT_DATA[7:0]							
PAT_DATA[15:8]							
TP1_MODE			TP0_MODE			PAT_DATA[17:16]	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-16. Register 0x14/15/16 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	TP1_MODE	R/W	000	Located in 0x16. Select the mode for test pattern 1 (default data path for ADC B). 000: test pattern is disabled (normal output mode). 010: ramp pattern mode where PAT_DATA sets the ramp pattern increment size. 011: constant pattern mode where PAT_DATA[17:0] is the MSB aligned constant pattern.
4-2	TP0_MODE	R/W	000	Located in 0x16. Select the mode for test pattern 0 (default data path for ADC A). 000: test pattern is disabled (normal output mode). 010: ramp pattern mode where PAT_DATA sets the ramp pattern increment size. 011: constant pattern mode where PAT_DATA[17:0] is the MSB aligned constant pattern.
1-0, 7-0, 7-0	PAT_DATA[17:0]	R/W	0	PAT_DATA[17:0] is split across three registers: [17:16] in 0x16, [15:8] in 0x15, and [7:0] in 0x14. The PAT_DATA: • Used as the constant pattern when the test pattern mode is set to constant pattern. • Used as the ramp pattern step size when test pattern mode is set to ramp pattern.

Figure 7-44. Register 0x19

7	6	5	4	3	2	1	0
FCLK_SRC	0	0	FCLK_DIV	0	0	0	TOG_FCLK
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-17. Register 0x19 Field Descriptions

Bit	Field	Type	Reset	Description
7	FCLK_SRC	R/W	0	Select the FCLK signal source. See Table 7-18.
6-5	0	R/W	0	Must write 0.
4	FCLK_DIV	R/W	0	Select the FCLK divider setting. See Table 7-18.
3-1	0	R/W	0	Must write 0.
0	TOG_FCLK	R/W	0	Select the FCLK toggle setting. See Table 7-18.

Table 7-18. FCLK Settings Based on Device Mode

Mode	Interface Mode	FCLK_SRC	FCLK_DIV	TOG_FCLK
DSP Features Disabled/Real Decimation	2-wire	0	1	0
	1-wire	0	0	0
	1/2-wire	0	0	0
Complex Decimation	2-wire	1	0	0
	1-wire	1	0	0
	1/2-wire	0	0	1

Figure 7-45. Register 0x1A

7	6	5	4	3	2	1	0
0	HALF_ SWING_EN	0	0	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-19. Register 0x1A Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0	Must write 0.
6	HALF_SWING_EN	R/W	0	This bit reduces the LVDS output swing.
5-0	0	R/W	0	Must write 0.

Figure 7-46. Register 0x1B

7	6	5	4	3	2	1	0
RES_SEL_EN	20B_EN	RES_SEL			0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-20. Register 0x1B Field Descriptions

Bit	Field	Type	Reset	Description
7	RES_SEL_EN	R/W	0	Select if the resolution select block is enabled. The resolution select block is not needed for setting the output resolution to 20-bit. 0: the resolution select block is disabled. 1: the resolution select block is enabled.
6	20B_EN	R/W	0	Control 20-bit output resolution mode. 0: 20-bit output resolution mode is disabled. 1: 20-bit output resolution mode is enabled.
5-3	RES_SEL	R/W	010	Select the output resolution. If the DSP features are disabled, RES_SEL_EN needs to be set to 1 for this setting to take effect. 000: the output resolution is set to 18-bit. 001: the output resolution is set to 16-bit. 010: the output resolution is set to 14-bit.
2-0	0	R/W	0	Must write 0.

Table 7-21. Setting Output Resolution Based on Mode

Mode	RES_SEL_EN	RES_SEL
DSP Features Disabled	1	000: the output resolution is set to 18-bit. 001: the output resolution is set to 16-bit. 010: the output resolution is set to 14-bit.
Real Decimation	0	
Complex Decimation	0	

Figure 7-47. Register 0x1E

7	6	5	4	3	2	1	0
0	0	0	0	LVDS_DATA_DEL		LVDS_DCLK_DEL	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-22. Register 0x1E Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R/W	0	Must write 0
3-2	LVDS_DATA_DEL	R/W	00	Control delay on the data lanes. 00: no delay (normal mode). 01: the data lanes are advanced by 50ps. 10: the data lanes are delayed by 50ps. 11: the data lanes are delayed by a 100ps.
1-0	LVDS_DCLK_DEL	R/W	00	Control delay on the interface data clock. 00: no delay (normal mode). 01: DCLK is advanced by 50ps. 10: DCLK is delayed by 50ps. 11: DCLK is delayed by a 100ps.

Figure 7-48. Register 0x20/21/22

7	6	5	4	3	2	1	0
FCLK_PAT[7:0]							
FCLK_PAT_[15:8]							
0	SCR_EN	0	0	FCLK_PAT_[19:16]			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-23. Register 0x20/21/22 Field Descriptions

Bit	Field	Type	Reset	Description
6	SCR_EN	R/W	0	Located in 0x22. Configure the scrambler enable state. Scrambler should only be used in the 2-wire interface mode. DSP_EN needs to be set to 1 for this setting to take effect. 0: the output scrambler is disabled. 1: the output scrambler is enabled.
3-0, 7-0, 7-0	FCLK_PAT[19:0]	R/W	0xFFC00	FCLK_PAT is split across three registers. [19:16] in 0x22, [15:8] in 0x21, and [7:0] in 0x20. See Table 7-24.

Table 7-24. FCLK Pattern in Different Modes

Mode	Output Resolution	2-wire	1-wire	1/2-wire
DSP Features Disabled/Real Decimation	14-bit	0xFFC00	0xFE000	0xFFC00
	16-bit		0xFF000	
	18-bit		0xFF800	
	20-bit		0xFFC00	
Complex Decimation	14-bit		0xFFFFF	0xFFFFF
	16-bit			
	18-bit			
	20-bit			

Figure 7-49. Register 0x24

7	6	5	4	3	2	1	0
0	0	AVG_EN	DDC_INP_SEL		DSP_EN	DDC_EN	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-25. Register 0x24 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0.
5	AVG_EN	R/W	0	Control the averaging block which averages the outputs of ADCs A & B. 0: the averaging block is disabled. 1: the averaging block is enabled.
4-3	DDC_INP_SEL	R/W	0	Select the source of the DDC input. DDC_MUX_EN must be set to 1 for this setting to take effect. 00: output of ADC A as DDC0 input. Output of ADC B as DDC1 input. 01: output of ADC A as DDC0 and DDC1 input. 10: output of ADC B as DDC0 and DDC1 input. 11: output of ADC averaging block as DDC0 and DDC1 input.
2	DSP_EN	R/W	0	Enable the DSP features data path. 0: DSP features data path is disabled. 1: DSP features data path is enabled.
1	DDC_EN	R/W	0	Enable the DDCs. 0: DDCs are disabled. 1: DDCs are enabled.
0	0	R/W	0	Must write 0.

Figure 7-50. Register 0x25

7	6	5	4	3	2	1	0
DDC_MUX_EN	DEC_FACTOR			DDC_MODE	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-26. Register 0x25 Field Descriptions

Bit	Field	Type	Reset	Description
7	DDC_MUX_EN	R/W	0	Control the DDC_MUX enable. The DDC_MUX must be enabled for DDC_INP_SEL to take effect. 0: the DDC_MUX is disabled. 1: the DDC_MUX enabled,
6-4	DEC_FACTOR	R/W	000	Decimation factor setting. 000: no decimation. 001: decimation by 2. 010: decimation by 4. 011: decimation by 8. 100: decimation by 16. 101: decimation by 32.
3	DDC_MODE	R/W	0	DDC mode and applies to both DDCs. 0: the DDC mode is set to complex decimation. 1: the DDC mode is set to real decimation.
2-1	0	R/W	0	Must write 0.

Figure 7-51. Register 0x26

7	6	5	4	3	2	1	0
DDC0_GAIN		NCO0_RES	0	DDC1_GAIN		NCO1_RES	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-27. Register 0x26 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DDC0_GAIN	R/W	00	Select the digital gain setting for DDC0 to compensate for the complex decimation amplitude reduction for DDC0. 00: no digital gain added. 10: 6-dB digital gain is added (useful in the complex decimation mode only).
5	NCO0_RES	R/W	0	Toggling this bit resets the NCO phase of NCO0 in DDC0 and loads the current FCW0 as the NCO frequency. This setting is not self clearing.
4	0	R/W	0	Must write 0.
3-2	DDC0_GAIN	R/W	00	Select the digital gain setting for DDC1 to compensate for the complex decimation amplitude reduction for DDC1. 00: no digital gain added. 10: 6-dB digital gain is added (useful in the complex decimation mode only).
1	NCO1_RES	R/W	0	Toggling this bit resets the NCO phase of NCO1 in DDC1 and loads the current FCW1 as the NCO frequency. This setting is not self clearing.
0	0	R/W	0	Must write 0.

Figure 7-52. Register 0x27

7	6	5	4	3	2	1	0
0	0	0	IQ0_ORDER	Q0_DEL	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-28. Register 0x27 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0.
4	IQ0_ORDER	R/W	0	Swaps the I and Q output order for DDC0. Set to 0 if not using complex decimation; otherwise, see Table 7-29.
3	Q0_DEL	R/W	0	This delays the quadrature output of DDC0 by one sample. Set to 0 if not using complex decimation; otherwise, see Table 7-29.
2-0	0	R/W	0	Must write 0

Table 7-29. IQ_ORDER and Q_DEL Register Settings for Complex Decimation

Interface Mode	IQ_ORDER	Q_DEL
2-wire	1	0
1-wire	0	1
1/2-wire	1	1

Figure 7-53. Register 0x2A/B/C/D

7	6	5	4	3	2	1	0
FCW0[7:0]							
FCW0[15:8]							
FCW0[23:16]							
FCW0[31:24]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-30. Register 0x2A/2B/2C/2D Field Descriptions

Bit	Field	Type	Reset	Description
	FCW0[31:0]	R/W	0	FCW for NCO0 and is split across four registers. [31:24] in 0x2D, [23:16] in 0x2C, [15:8] in 0x2B, and [7:0] in 0x2A.

Figure 7-54. Register 0x2E

7	6	5	4	3	2	1	0
0	0	0	IQ1_ORDER	Q1_DEL	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-31. Register 0x2E Field Descriptions

Bit	Field	Type	Reset	Description
7-5	0	R/W	0	Must write 0
4	IQ1_ORDER	R/W	0	Swaps the I and Q output order for DDC1. Set to 0 if not using complex decimation; otherwise, see Table 7-29.
3	Q1_DEL	R/W	0	This delays the quadrature output of DDC1 by one sample. Set to 0 if not using complex decimation; otherwise, see Table 7-29.
2-0	0	R/W	0	Must write 0.

Figure 7-55. Register 0x31/32/33/34

7	6	5	4	3	2	1	0
FCW1[7:0]							
FCW1[15:8]							
FCW1[23:16]							
FCW1[31:24]							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-32. Register 0x31/32/33/34 Field Descriptions

Bit	Field	Type	Reset	Description
	FCW1[31:0]	R/W	0	FCW for NCO1 and is split across four registers. [31:24] in 0x34, [23:16] in 0x33, [15:8] in 0x32, and [7:0] in 0x31.

Figure 7-56. Register 0x39..0x60

7	6	5	4	3	2	1	0
BIT_MAPPER_A							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-33. Register 0x39..0x60 Field Descriptions

Bit	Field	Type	Reset	Description
	BIT_MAPPER_A	R/W	0	See the Section 7.3.4.5.

Figure 7-57. Register 0x61..0x88

7	6	5	4	3	2	1	0
BIT_MAPPER_B							
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-34. Register 0x61..0x88 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BIT_MAPPER_B	R/W	0	See the Section 7.3.4.5.

Figure 7-58. Register 0x8F

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FORMAT_A	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-35. Register 0x8F Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0	Must write 0
1	FORMAT_A	R/W	0	Sets the output data format for the channel A data path. The DSP_EN must be set to 1 for this setting to take effect. 0: output data format is 2s complement. 1: output data format is offset binary.
0	0	R/W	0	Must write 0

Figure 7-59. Register 0x92

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FORMAT_B	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-36. Register 0x92 Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	R/W	0	Must write 0
1	FORMAT_B	R/W	0	Sets the output data format for the channel B data path. The DSP_EN must be set to 1 for this setting to take effect. 0: output data format is 2s complement. 1: output data format is offset binary.
0	0	R/W	0	Must write 0

Table 7-37. Register 0x244

7	6	5	4	3	2	1	0
0	0	DCLKIN_VCM	0	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 7-38. Register 0x244 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	R/W	0	Must write 0.
5	DCLKIN_VCM	R/W	0	This bit sets the common-mode source for DCLKIN. 0: DCLKIN common-mode is provided externally. 1: DCLKIN is internally biased to a 1.2V common-mode.
4-0	0	R/W	0	Must write 0.

8 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ADC3664-SP can be used in a variety of space applications as a high speed and low latency digitizer. Some of the common applications for the ADC3664-SP are found in optical imaging payloads.

8.2 Typical Application

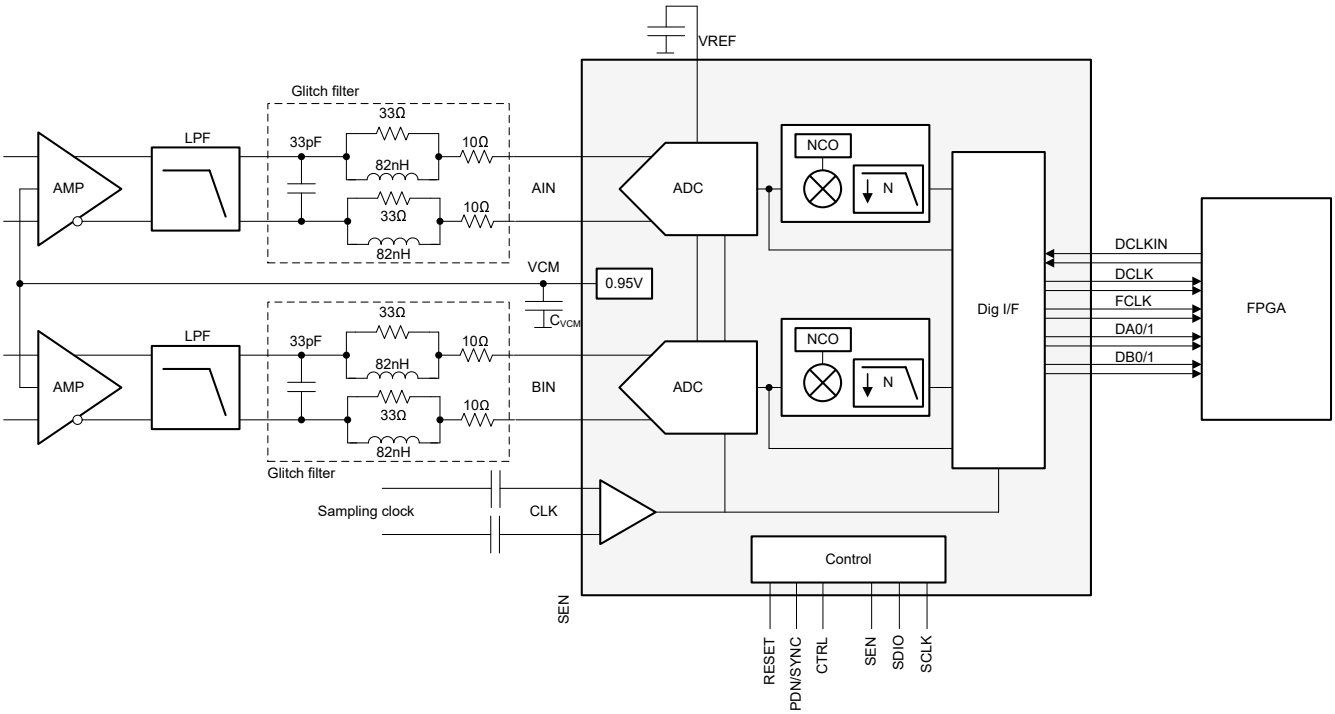


Figure 8-1. Typical Configuration of a DC Coupled Digitizer

8.2.1 Design Requirements

Table 8-1. Design Requirements

Requirement	Description
Signal Bandwidth	DC to 20MHz
Input Driver	Single ended to differential signal conversion and DC coupling
Clock Source	Low jitter differential clock

8.2.2 Detailed Design Procedure

The application requirements are provided in Table 8-1. Since the supported signal bandwidth is as low as DC, an amplifier is used to DC couple the signal to the input of the ADC. Additionally, the ADC VCM output provides the amplifier common-mode as shown in Figure 8-1.

When designing the amplifier or filter driving circuit, the ADC input full-scale voltage needs to be taken into consideration. For example, the ADC3664-SP input full-scale is $3.2V_{PP}$. Texas Instruments (TI) offers a variety of amplifiers to be used in space applications such as LMH5485-SP and THS4511-SP. For best DC accuracy an external reference can be used.

8.3 Initialization Set Up

The following steps should be followed for device initialization.

1. Apply AVDD and IOVDD (no specific sequence required). After AVDD is applied, the internal reference powers up and settles in approximately 2ms.
2. Configure the CTRL pin and apply the sampling clock.
3. Apply a hardware reset. After the hardware reset is released, the default registers are loaded from internal fuses and the internal power up calibration is initiated. The calibration takes approximately 200000 clock cycles.
4. Begin programming via the SPI.

Table 8-2. Power Up Timing

		Minimum Time	Unit
t_1	Delay from power up to logic level of CTRL pin	2	ms
t_2	RESET pulse width	1	µs
t_3	Delay from RESET disable to $\overline{SEN}$ active	~ 200000	Clock Cycles

8.4 Power Supply Recommendations

The ADC3664-SP requires two different power supplies. The A_{VDD} supply provides power for the internal analog circuits and to the ADC while the I_{OVDD} supply powers the digital interface and the internal digital circuits. Power sequencing is not required.

A low noise power supply should supply the AVDD rail to achieve data sheet performance.

There are two recommended power-supply architectures:

1. A high efficiency switching regulator followed by a low noise LDO to suppress the switching noise and improve voltage accuracy.
2. Directly step down to the final ADC supply voltage using a high efficiency switching regulator. This approach provides the best efficiency; however, care must be taken to make sure the switching regulator noise doesnot degrade the ADC performance.

The TPS7H4002-SP is recommended as the first stage radiation hardened switching regulator. The switching regulator can be followed by either the TPS7A4501-SP or the TPS7H1111-SP which are both space hardened LDOs.

Note

A_{VDD} and I_{OVDD} supply voltages should not be shared to prevent digital switching noise from coupling into the analog signal chain.

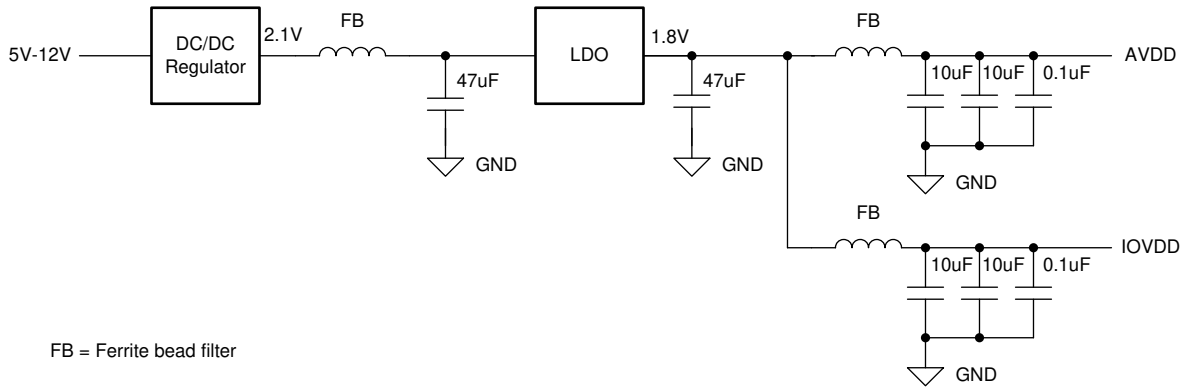


Figure 8-2. Example LDO Based Approach

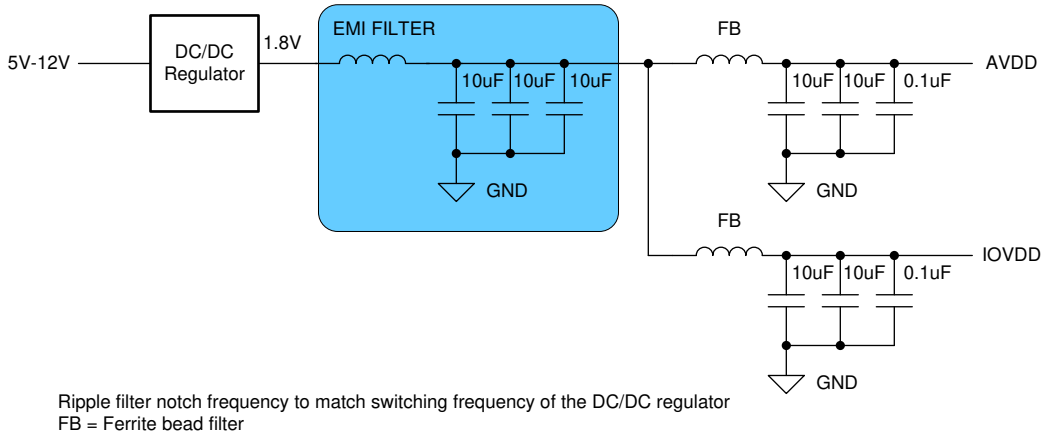


Figure 8-3. Example Switcher Only Approach

8.5 Layout

8.5.1 Layout Guidelines

There are several critical signals which require specific care during board design:

1. Analog inputs and clock signals:
   - Traces should be as short as possible and vias should be avoided where possible to minimize impedance discontinuities.
   - Traces should be routed using loosely coupled 100Ω differential traces.
   - Differential trace lengths should be matched as close as possible to minimize phase imbalance and HD2 degradation.
2. Digital output interface:
   - Traces should be routed using tightly coupled 100Ω differential traces.
   - Make sure the LVDS lanes are routed as far as possible from the analog inputs to minimize coupling.
3. Voltage reference:
   - The decoupling capacitors should be placed as close to the device pins as possible and connected between VREF and REFGND – avoid using vias by having the capacitors on the same layer as the device.
4. Power and ground connections:
   - Provide low resistance connection paths to all power and ground pins.
   - Avoid narrow and isolated paths which increase the connection resistance.
   - Add GND layers between power and signal layers in the PCB stack up.

8.5.2 Layout Example

The following is an example showing the top layer layout of the ADC3664-SP on the ADC3664-SP EVM.

- Signal and clock inputs are routed as differential signals on the top layer.
- LVDS lanes go through vias to the bottom layer to minimize coupling on the analog inputs.

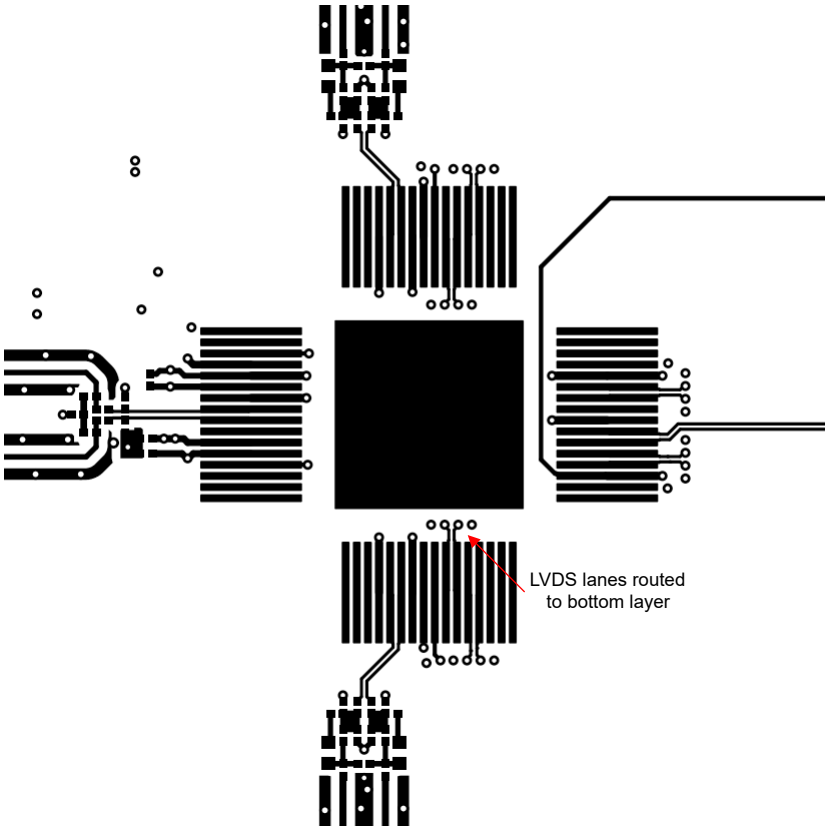


Figure 8-4. Layout Example for the ADC3664-SP EVM

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

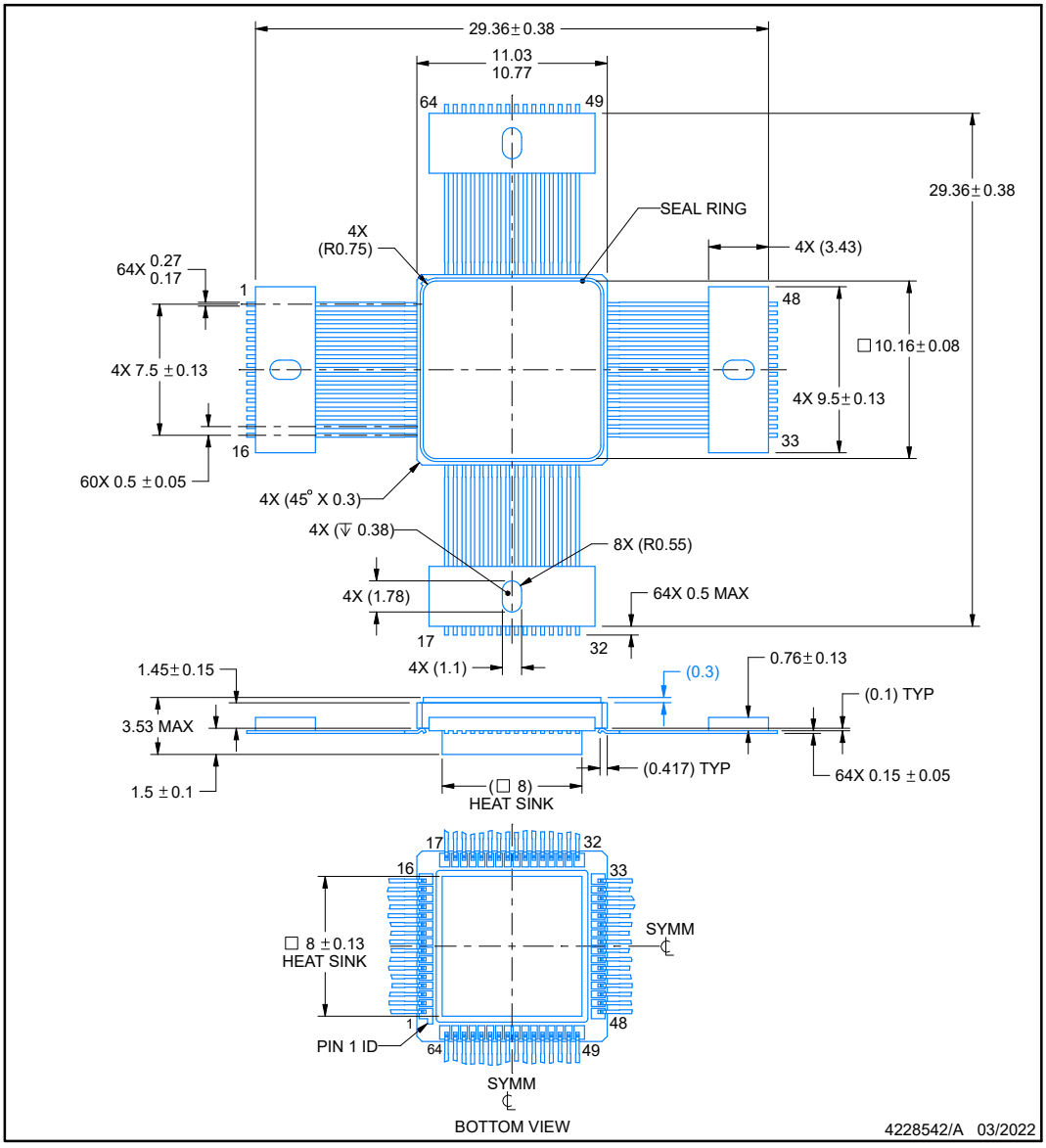
11.1 Mechanical Data

HBP0064A

PACKAGE OUTLINE

CFP - 3.53 mm max height

CERAMIC FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid.
4. Ground pad to be electronic connected to heat sink and seal ring.
5. The leads are gold plated and can be solder dipped.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC3664HBP/EM	ACTIVE	CFP	HBP	64	24	RoHS & Green	Call TI	Call TI	25 to 25	ADC3664HBP/EM EVAL ONLY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ADC3664-SP :

- Catalog : ADC3664

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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