CLASS V, 13 BIT, 250 MSPS ANALOG-TO-DIGITAL CONVERTER

Check for Samples: ADS5444-SP

FEATURES

- **13 Bit Resolution**
- **250 MSPS Sample Rate**
- **SNR = 67.6 dBc at 230 MHz IF and 250 MSPS**
- **SFDR = 74.0 dBc at 230 MHz IF and 250 MSPS**
- **2.2 V_{PP} Differential Input Voltage**
- **Fully Buffered Analog Inputs**
- **5 V Analog Supply Voltage**
- **LVDS Compatible Outputs**
- **Total Power Dissipation: 2 W**
- **Offset Binary Output Format**
- **Pin Compatible With the ADS5440**
- **Military Temperature Range (–55°C to 125°C T_{case})**

APPLICATIONS

- **Test and Measurement**
- **Software-Defined Radio**
- **Multichannel Base Station Receivers**
- **Base Station Tx Digital Predistortion**
- **Communications Instrumentation**
- **Engineering Evaluation (/EM) Samples are Available** (1)

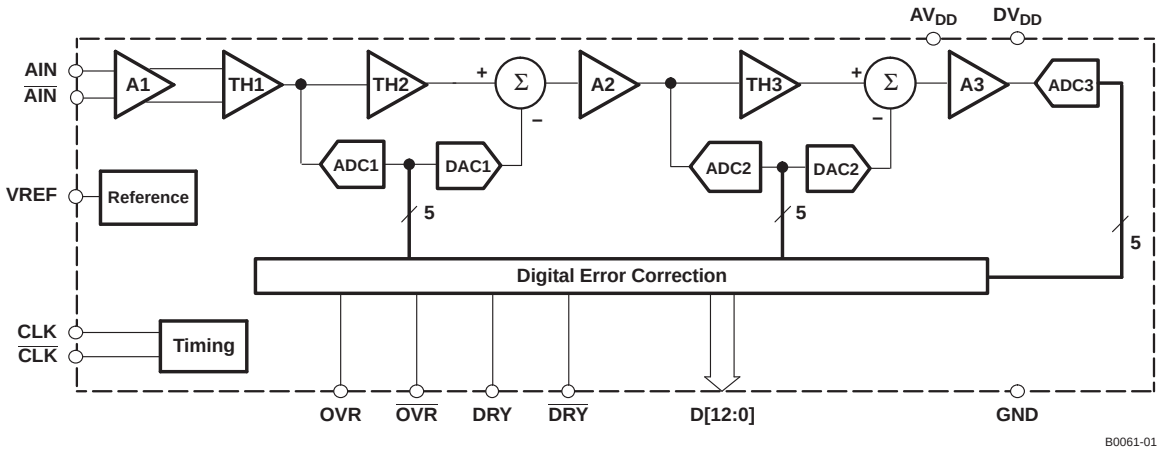
RELATED PRODUCTS

- **ADS5424 - 14 Bit, 105 MSPS ADC**
- **ADS5423 - 14 Bit, 80 MSPS ADC**
- **ADS5440 - 13 Bit, 210 MSPS ADC**

(1) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (e.g. no burn-in, etc.) and are tested to temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing or flight use. Parts are not warranted for performance on full MIL specified temperature range of -55°C to 125°C or operating life.

DESCRIPTION

The ADS5444 is a 13 bit 250 MSPS analog-to-digital converter (ADC) that operates from a 5 V supply, while providing LVDS-compatible digital outputs from a 3.3 V supply. The ADS5444 input buffer isolates the internal switching of the onboard track and hold (T&H) from disturbing the signal source. An internal reference generator is also provided to further simplify the system design. The ADS5444 has outstanding low noise and linearity over input frequency.



The ADS5444 is available in a 84 pin ceramic nonconductive tie-bar package (HFG). The ADS5444 is built on a state-of-the-art Texas Instruments complementary bipolar process (BiCom3X) and is specified over the full military temperature range (–55°C to 125°C T_{case}).

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating temperature range (unless otherwise noted)(1)

		VALUE/UNIT
Supply voltage	AV_{DD} to GND	6 V
	DRV_{DD} to GND	5 V
Analog input to GND		–0.3 V to AV_{DD} + 0.3 V
Clock input to GND		–0.3 V to AV_{DD} + 0.3 V
CLK to $\overline{CLK}$		±2.5 V
Digital data output to GND		–0.3 V to DRV_{DD} + 0.3 V
T_C	Characterized case operating temperature range	–55°C to 125°C
T_J	Maximum junction temperature	150°C
T_{stg}	Storage temperature range	–65°C to 150°C
ESD Human Body Model (HBM)		2.5 kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified is not implied.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
SUPPLIES					
AV_{DD}	Analog supply voltage	4.75	5	5.25	V
DRV_{DD}	Output driver supply voltage	3	3.3	3.6	V
ANALOG INPUT					
	Differential input range		2.2		V_{PP}
V_{CM}	Input common mode		2.4		V
CLOCK INPUT					
	ADCLK input sample rate (sine wave)	10		250	MSPS
	Clock amplitude, differential sine wave		3		V_{PP}
	Clock duty cycle		50%		
T_C	Operating case temperature	–55		125	°C

ELECTRICAL CHARACTERISTICS

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 250 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Resolution				13		Bits
ANALOG INPUTS							
	Differential input range				2.2		V_{pp}
	Differential input resistance (DC)				1		kΩ
	Differential input capacitance				1.5		pF
	Analog input bandwidth				800		MHz
INTERNAL REFERENCE VOLTAGE							
VREF	Reference voltage			2.38	2.4	2.42	V
DYNAMIC ACCURACY							
	No missing codes				Assured		
DNL	Differential linearity error	f_{IN} = 100 MHz	Full temp range	–0.98	±0.4	2	LSB
INL	Integral linearity error	f_{IN} = 100 MHz	T_C = 25°C and $T_{C,MAX}$	–2.8		2.8	LSB
			T_C = $T_{C,MIN}$	–4.8		4.8	
	Offset error		Full temp range	–0.6		0.6	%FS
	Offset temperature coefficient				0.0005		%FS/°C
	Gain error		Full temp range	–5		5	%FS
	Gain temperature coefficient				–0.02		%FS/°C
POWER SUPPLY							
I_{AVDD}	Analog supply current	V_{IN} = full scale, f_{IN} = 170 MHz, F_S = 250 MSPS			340	410	mA
I_{DRVDD}	Output buffer supply current				80	100	mA
	Power dissipation				2	2.29	W
DYNAMIC AC CHARACTERISTICS							
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz	T_C = 25°C	68.0	69.1		dBc
			T_C = $T_{C,MAX}$	66.8			
			T_C = $T_{C,MIN}$	63.2			
		f_{IN} = 70 MHz			69.0		
		f_{IN} = 100 MHz	T_C = 25°C	67.3	68.9		
			T_C = $T_{C,MAX}$	66.5			
			T_C = $T_{C,MIN}$	62.1			
		f_{IN} = 170 MHz	T_C = 25°C	66.5	68.4		
			T_C = $T_{C,MAX}$	66.1			
			T_C = $T_{C,MIN}$	60.8			
		f_{IN} = 230 MHz			67.6		
		f_{IN} = 300 MHz			66.5		
		f_{IN} = 400 MHz			65.5		

ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 250 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SFDR	Spurious free dynamic range	f_{IN} = 10 MHz	T_C = 25°C	75.0	84.0		dBc
			$T_C = T_{C,MAX}$	74.0			
			$T_C = T_{C,MIN}$	75.0			
		f_{IN} = 70 MHz			71.8		
		f_{IN} = 100 MHz	T_C = 25°C	62.0	67.4		
			$T_C = T_{C,MAX}$	74.5			
			$T_C = T_{C,MIN}$	63.0			
		f_{IN} = 170 MHz	T_C = 25°C	63.0	70.0		
			$T_C = T_{C,MAX}$	65.0			
			$T_C = T_{C,MIN}$	59.0			
		f_{IN} = 230 MHz			74.0		
		f_{IN} = 300 MHz			65.8		
		f_{IN} = 400 MHz			60.5		
HD2	Second harmonic	f_{IN} = 10 MHz	T_C = 25°C	75.0	92.0		dBc
			$T_C = T_{C,MAX}$	74.0			
			$T_C = T_{C,MIN}$	76.5			
		f_{IN} = 70 MHz			71.8		
		f_{IN} = 100 MHz	T_C = 25°C	62.0	67.4		
			$T_C = T_{C,MAX}$	76.0			
			$T_C = T_{C,MIN}$	63.0			
		f_{IN} = 170 MHz	T_C = 25°C	63.0	73.0		
			$T_C = T_{C,MAX}$	65.0			
			$T_C = T_{C,MIN}$	59.0			
		f_{IN} = 230 MHz			74.0		
		f_{IN} = 300 MHz			65.8		
		f_{IN} = 400 MHz			60.6		
HD3	Third harmonic	f_{IN} = 10 MHz	T_C = 25°C	81.0	84.0		dBc
			Full temp range	78.5			
		f_{IN} = 70 MHz			72.8		
		f_{IN} = 100 MHz	T_C = 25°C	72.0	78.4		
			$T_C = T_{C,MAX}$	74.5			
			$T_C = T_{C,MIN}$	65.0			
		f_{IN} = 170 MHz	T_C = 25°C	65.0	70.1		
			$T_C = T_{C,MAX}$	69.0			
			$T_C = T_{C,MIN}$	63.0			
		f_{IN} = 230 MHz			94.0		
		f_{IN} = 300 MHz			77.7		
		f_{IN} = 400 MHz			64.1		

ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 250 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Worst other harmonic/spur (other than HD2 and HD3)	f_{IN} = 10 MHz	T_C = 25°C	80.0	89.0		dBc
			$T_C = T_{C,MAX}$	81.0			
			$T_C = T_{C,MIN}$	75.0			
		f_{IN} = 70 MHz			82.7		
		f_{IN} = 100 MHz	T_C = 25°C	74.0	86.6		
			$T_C = T_{C,MAX}$	78.0			
			$T_C = T_{C,MIN}$	69.0			
		f_{IN} = 170 MHz	T_C = 25°C	70.0	88.2		
			$T_C = T_{C,MAX}$	78.0			
			$T_C = T_{C,MIN}$	64.0			
		f_{IN} = 230 MHz			81.8		
		f_{IN} = 300 MHz			83.6		
		f_{IN} = 400 MHz			82.0		
THD	Total harmonic distortion	f_{IN} = 10 MHz	T_C = 25°C	74.5	83.0		dBc
			$T_C = T_{C,MAX}$	73.0			
			$T_C = T_{C,MIN}$	74.0			
		f_{IN} = 70 MHz			68.9		
		f_{IN} = 100 MHz	T_C = 25°C	61.5	67.0		
			$T_C = T_{C,MAX}$	73.0			
			$T_C = T_{C,MIN}$	60.0			
		f_{IN} = 170 MHz	T_C = 25°C	62.0	68.2		
			$T_C = T_{C,MAX}$	63.5			
			$T_C = T_{C,MIN}$	58.0			
		f_{IN} = 230 MHz			73.2		
		f_{IN} = 300 MHz			65.5		
		f_{IN} = 400 MHz			59.0		
SINAD	Signal-to-noise and distortion	f_{IN} = 10 MHz	T_C = 25°C	67.7	69.2		dBc
			$T_C = T_{C,MAX}$	66.4			
			$T_C = T_{C,MIN}$	62.9			
		f_{IN} = 70 MHz			69.2		
		f_{IN} = 100 MHz	T_C = 25°C	62.2	68.9		
			$T_C = T_{C,MAX}$	66.2			
			$T_C = T_{C,MIN}$	59.4			
		f_{IN} = 170 MHz	T_C = 25°C	61.7	68.3		
			$T_C = T_{C,MAX}$	62.9			
			$T_C = T_{C,MIN}$	57.6			
		f_{IN} = 230 MHz			67.5		
		f_{IN} = 300 MHz			66.6		
		f_{IN} = 400 MHz			65.4		

ELECTRICAL CHARACTERISTICS (continued)

Typical values at T_C = 25°C, full temperature range is $T_{C,MIN}$ = –55°C to $T_{C,MAX}$ = 125°C, sampling rate = 250 MSPS, 50% clock duty cycle, AV_{DD} = 5 V, DRV_{DD} = 3.3 V, –1 dBFS differential input, and 3 V_{PP} differential clock (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	f_{IN} = 10 MHz	T_C = 25°C	10.9	11.3		Bits
			$T_C = T_{C,MAX}$	10.7			
			$T_C = T_{C,MIN}$	10.1			
		f_{IN} = 100 MHz	T_C = 25°C	10.0	11.3		
			$T_C = T_{C,MAX}$	10.7			
			$T_C = T_{C,MIN}$	9.5			
		f_{IN} = 170 MHz	T_C = 25°C	9.9	11.2		
			$T_C = T_{C,MAX}$	10.1			
			$T_C = T_{C,MIN}$	9.2			
RMS idle channel noise		Inputs tied to common-mode			0.4		LSB
DIGITAL CHARACTERISTICS – LVDS DIGITAL OUTPUTS							
Differential output voltage				247		452	mV
Output offset voltage				1.125	1.25	1.375	V

TIMING CHARACTERISTICS

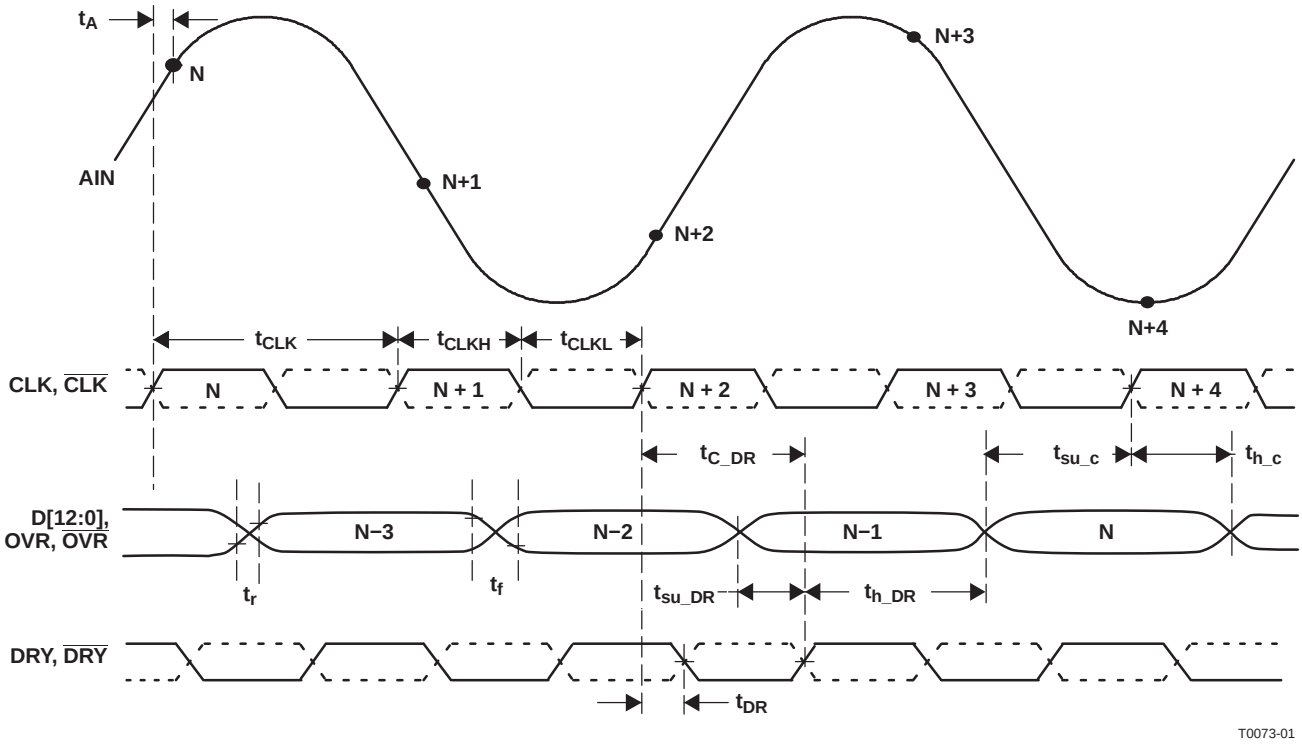


Figure 1. Timing Diagram

TIMING CHARACTERISTICS

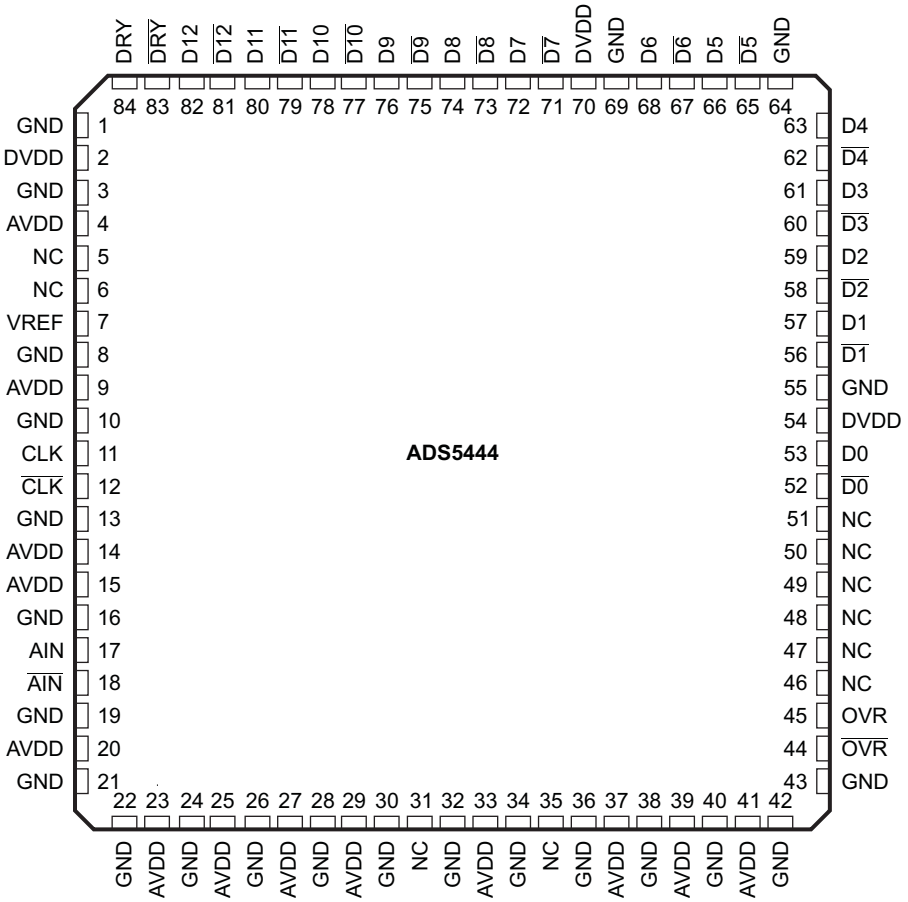
Typical values at T_C = 25°C, 50% clock duty cycle, sampling rate = 250 MSPS, AV_{DD} = 5 V, DRV_{DD} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_A	Aperture delay			500		ps
t_J	Clock slope independent aperture uncertainty (jitter)			200		fs RMS
	Latency			4		cycles
Clock Input						
t_{CLK}	Clock period			4		ns
t_{CLKH}	Clock pulse width high			2		ns
t_{CLKL}	Clock pulse width low			2		ns
Clock to DataReady (DRY)						
t_{DR}	Clock rising to DataReady falling			1.1		ns
t_{C_DR}	Clock rising to DataReady rising	Clock duty cycle = 50% (1)	2.7	3.1	3.5	ns
Clock to DATA, OVR (2)						
t_r	Data rise time (20% to 80%)			0.6		ns
t_f	Data fall time(80% to 20%)			0.6		ns
t_{su_c}	Data valid to clock (setup time)			3.1		ns
t_{h_c}	Clock to invalid data (hold time)			0.2		ns
DataReady (DRY)/DATA, OVR (2)						
$t_{su(DR)}$	Data valid to DRY		1.5	2		ns
$t_{h(DR)}$	DRY to invalid data		0.9	1.3		ns

(1) $t_{C\_DR} = t_{DR} + t_{CLKH}$ for clock duty cycles other than 50%
(2) Data is updated with clock falling edge or DRY rising edge.

DEVICE INFORMATION

HFG PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
AVDD	4, 9, 14, 15, 20, 23, 25, 27, 29, 33, 37, 39, 41	Analog power supply
DVDD	2, 54, 70	Output driver power supply
GND	1, 3, 8, 10, 13, 16, 19, 21, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40, 42, 43, 55, 64, 69	Ground
VREF	7	Reference voltage
CLK	11	Differential input clock (positive). Conversion initiated on rising edge.
$\overline{\text{CLK}}$	12	Differential input clock (negative)
AIN	17	Differential input signal (positive)
$\overline{\text{AIN}}$	18	Differential input signal (negative)
OVR, $\overline{\text{OVR}}$	44, 45	Over range indicator LVDS output. A logic high signals an analog input in excess of the full-scale range.
D0, $\overline{\text{D0}}$	52, 53	LVDS digital output pair, least-significant bit (LSB)
D1–D4, $\overline{\text{D1}}$–$\overline{\text{D4}}$	56–63	LVDS digital output pairs
D5–D6, $\overline{\text{D5}}$–$\overline{\text{D6}}$	65–68	LVDS digital output pairs

TERMINAL FUNCTIONS (continued)

TERMINAL		DESCRIPTION
NAME	NO.	
D7–D11, $\overline{D7}$–$\overline{D11}$	71–80	LVDS digital output pairs
D12, $\overline{D12}$	81, 82	LVDS digital output pair, most-significant bit (MSB)
DRY, $\overline{DRY}$	83, 84	Data ready LVDS output pair
NC	5, 6, 31, 35, 46–51	No connect

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	TYP	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, per JESD 51-5 methodology	21.813	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	MIL-STD-883 Test Method 1012	0.849	°C/W

THERMAL NOTES

This CQFP package has built in vias that electrically and thermally connect the bottom of the die to a pad on the bottom of the package. To efficiently remove heat and provide a low-impedance ground path, a thermal land is required on the surface of the PCB directly underneath the body of the package. During normal surface mount flow solder operations, the heat pad on the underside of the package is soldered to this thermal land creating an efficient thermal path. Normally, the PCB thermal land has a number of thermal vias within it that provide a thermal path to internal copper areas (or to the opposite side of the PCB) that provide for more efficient heat removal. TI typically recommends an 11,9-mm^2 board-mount thermal pad. This allows maximum area for thermal dissipation, while keeping leads away from the pad area to prevent solder bridging. A sufficient quantity of thermal/electrical vias must be included to keep the device within recommended operating conditions. This pad must be electrically at ground potential.

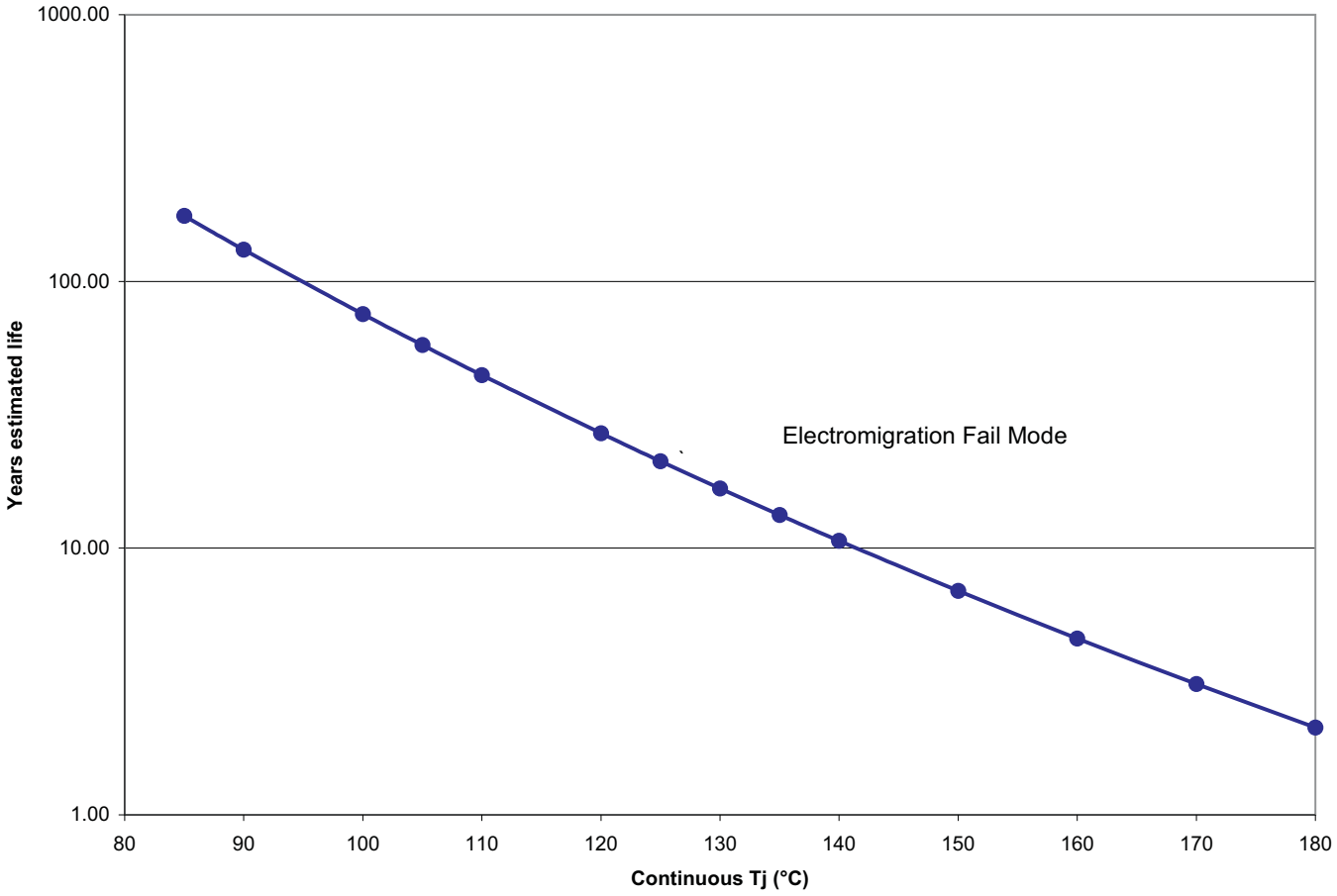


Figure 2. ADS5444 Estimated Device Life at Elevated Temperatures Electromigration Fail Mode

DEFINITION OF SPECIFICATIONS

Analog Bandwidth The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

Aperture Delay The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

Aperture Uncertainty (Jitter) The sample-to-sample variation in aperture delay.

Clock Pulse Width/Duty Cycle The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine wave clock results in a 50% duty cycle.

Maximum Conversion Rate The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

Minimum Conversion Rate The minimum sampling rate at which the ADC functions.

Differential Nonlinearity (DNL) An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSB.

Integral Nonlinearity (INL) The INL is the deviation of the ADCs transfer function from a best fit line determined by a least squares curve fit of that transfer function. The INL at each analog input value is the difference between the actual transfer function and this best fit line, measured in units of LSB.

Gain Error The gain error is the deviation of the ADCs actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

DEFINITION OF SPECIFICATIONS (continued)

Offset Error Offset error is the deviation of output code from mid-code when both inputs are tied to common-mode.

Temperature Drift Temperature drift (with respect to gain error and offset error) specifies the change from the value at the nominal temperature to the value at T_{MIN} or T_{MAX}. It is computed as the maximum variation the parameters over the whole temperature range divided by $T_{MIN} – T_{MAX}$.

Signal-to-Noise Ratio (SNR) SNR is the ratio of the power of the fundamental (P_S) to the noise floor power (P_N), excluding the power at dc and the first five harmonics.

$$SNR = 10\log_{10} \frac{P_S}{P_N} \quad (1)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Signal-to-Noise and Distortion (SINAD) SINAD is the ratio of the power of the fundamental (P_S) to the power of all the other spectral components including noise (P_N) and distortion (P_D), but excluding dc.

$$SINAD = 10\log_{10} \frac{P_S}{P_N + P_D} \quad (2)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

Effective Resolution Bandwidth The highest input frequency where the SNR (dB) is dropped by 3 dB for a full-scale input amplitude.

Total Harmonic Distortion (THD) THD is the ratio of the power of the fundamental (P_S) to the power of the first five harmonics (P_D).

$$THD = 10\log_{10} \frac{P_S}{P_D} \quad (3)$$

THD is typically given in units of dBc (dB to carrier).

Two-Tone Intermodulation Distortion IMD3 is the ratio of the power of the fundamental (at frequencies f_1, f_2) to the power of the worst spectral component at either frequency $2f_1 – f_2$ or $2f_2 – f_1$). IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

TYPICAL CHARACTERISTICS

AC Performance vs Input Amplitude (100 MHz)

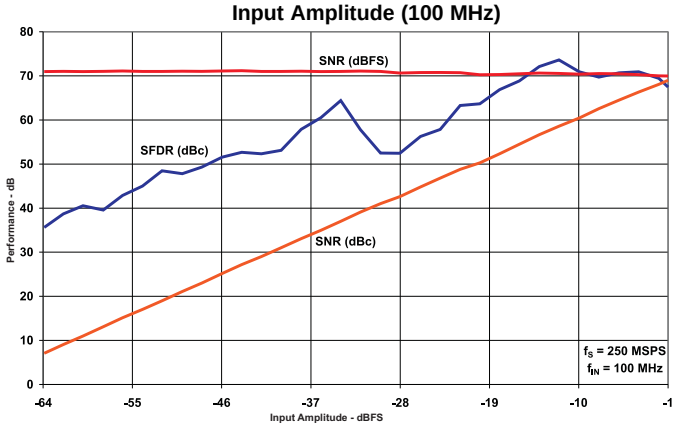


Figure 3.

AC Performance vs Input Amplitude (230 MHz)

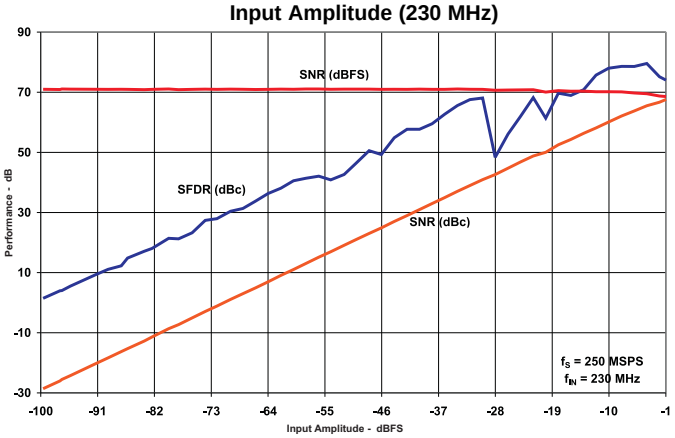


Figure 4.

SFDR vs Clock Level

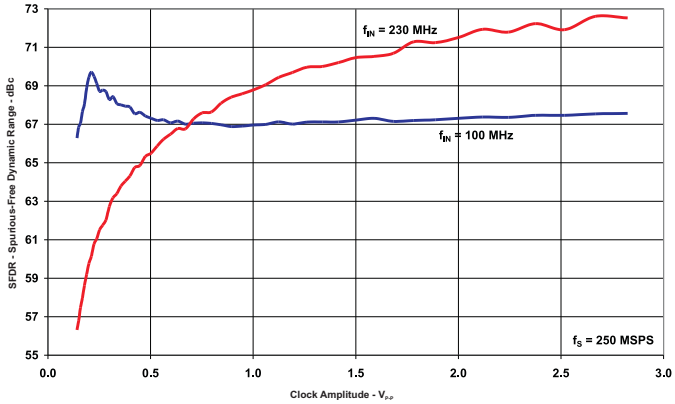


Figure 5.

SNR vs Clock Level

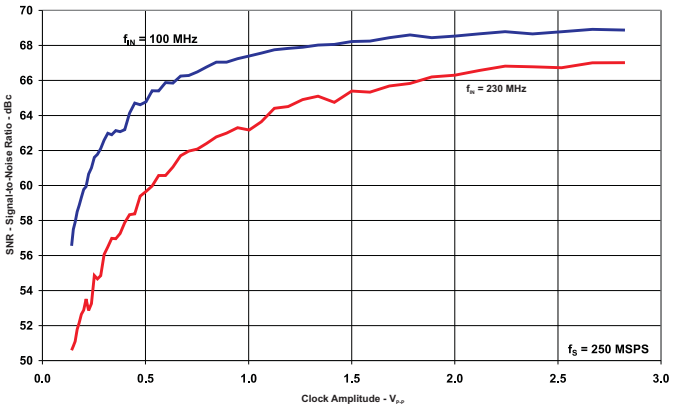


Figure 6.

SFDR vs AVDD Across Temperture

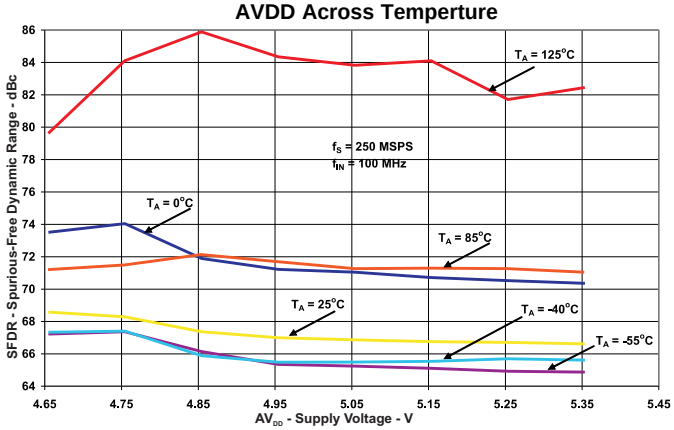


Figure 7.

SNR vs AVDD Across Temperture

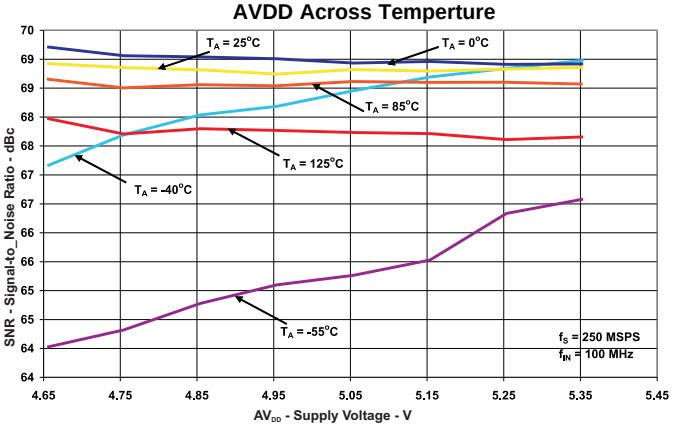


Figure 8.

TYPICAL CHARACTERISTICS (continued)

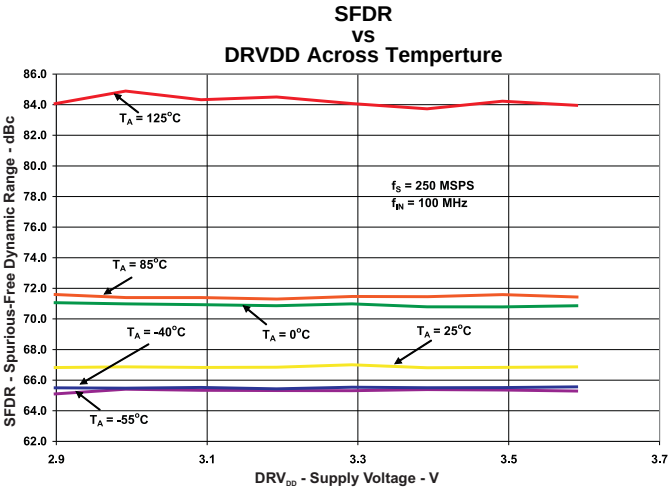


Figure 9.

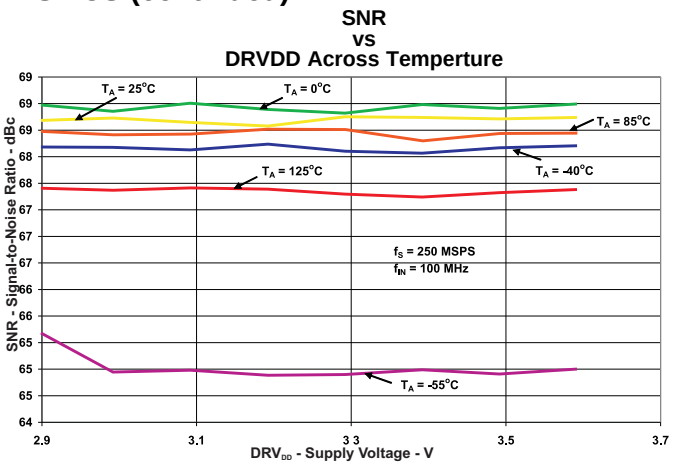


Figure 10.

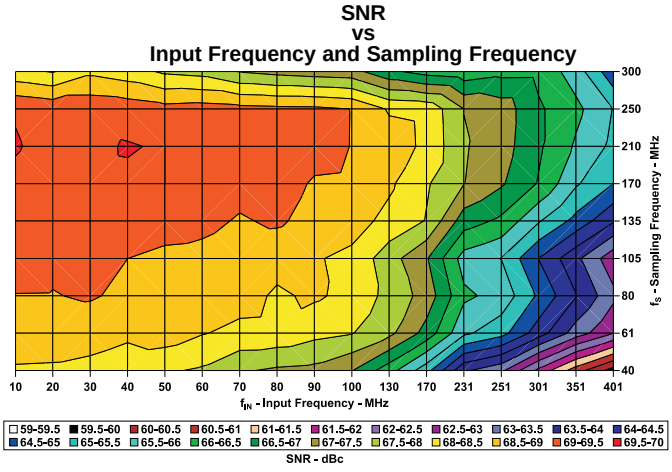


Figure 11.

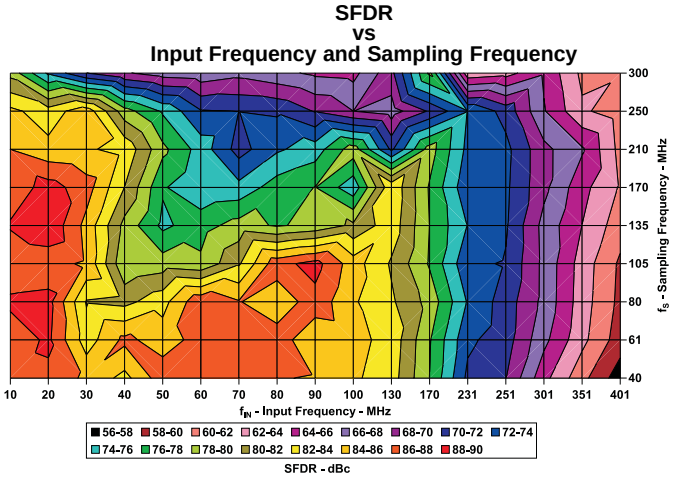


Figure 12.

APPLICATION INFORMATION

Theory of Operation

The ADS5444 is a 13 bit, 250 MSPS, monolithic pipeline analog-to-digital converter (ADC). Its bipolar analog core operates from a 5 V supply, while the output uses a 3.3 V supply to provide LVDS compatible outputs. The conversion process is initiated by the rising edge of the external input clock. At that instant, the differential input signal is captured by the input track and hold (T&H) and the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. Both the rising and the falling clock edges are used to propagate the sample through the pipeline every half clock cycle. This process results in a data latency of four clock cycles, after which the output data is available as a 13 bit parallel word, coded in offset binary format.

Input Configuration

The analog input for the ADS5444 consists of an analog differential buffer followed by a bipolar T&H. The analog buffer isolates the source driving the input of the ADC from any internal switching. The input common mode is set internally through a 500 Ω resistor connected from 2.4 V to each of the inputs. This results in a differential input impedance of 1 kΩ.

For a full-scale differential input, each of the differential lines of the input signal (pins 17 and 18) swings symmetrically between 2.4 + 0.55 V and 2.4 – 0.55 V. This means that each input has a maximum signal swing of 1.1 V_{PP} for a total differential input signal swing of 2.2 V_{PP}. The maximum swing is determined by the internal reference voltage generator eliminating the need for any external circuitry for this purpose.

The ADS5444 obtains optimum performance when the analog inputs are driven differentially. The circuit in Figure 13 shows one possible configuration using an RF transformer with termination either on the primary or on the secondary of the transformer. If voltage gain is required, a step up transformer can be used. For voltage gains that would require an impractical transformer turn ratio, a single-ended amplifier driving the transformer is shown in Figure 14.

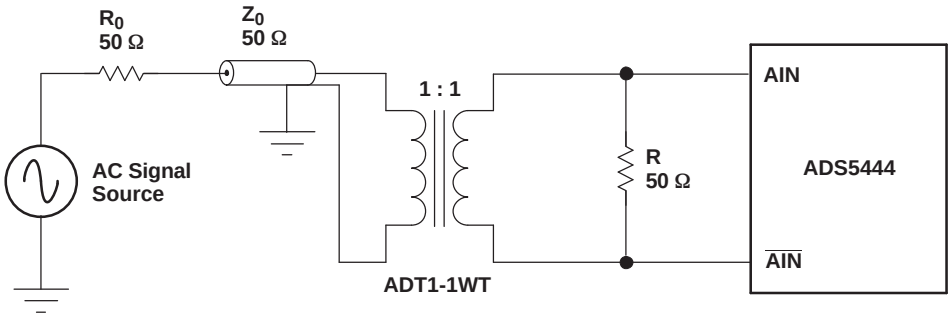


Figure 13. Converting a Single-Ended Input to a Differential Signal Using RF Transformers

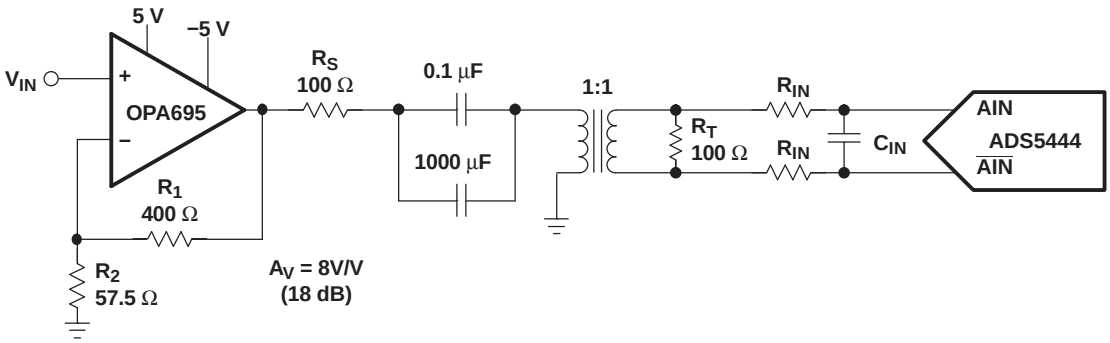


Figure 14. Using the OPA695 with the ADS5444

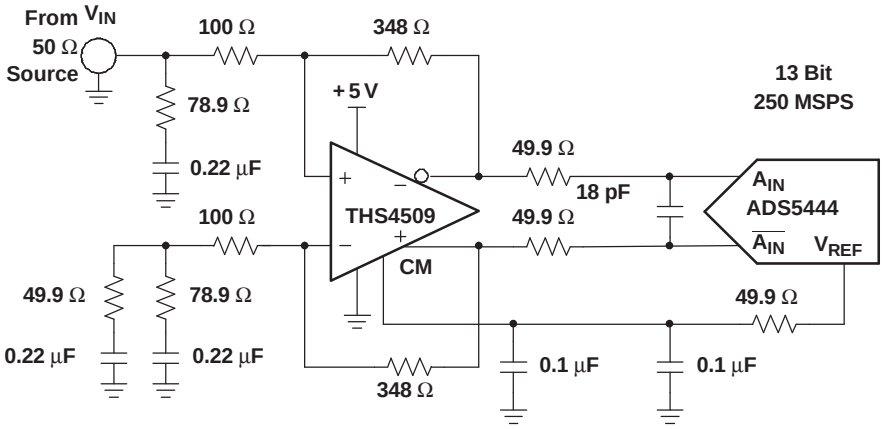


Figure 15. Using the THS4509 with the ADS5444

Besides the OPA695, TI offers a wide selection of single-ended operational amplifiers that can be selected depending on the application. An RF gain block amplifier, such as the TI THS9001, can also be used with an RF transformer for high input frequency applications. For applications requiring dc-coupling with the signal source, a differential input/differential output amplifier like the THS4509 (see Figure 15) is a good solution, as it minimizes board space and reduces the number of components.

In this configuration, the THS4509 amplifier circuit provides 10 dB of gain, converts the single-ended input to differential, and sets the proper input common-mode voltage to the ADS5444.

The 50 Ω resistors and 18 pF capacitor between the THS4509 outputs and ADS5444 inputs (along with the input capacitance of the ADC) limit the bandwidth of the signal to about 70 MHz (–3 dB).

Input termination is accomplished via the 78.9 Ω resistor and 0.22 µF capacitor to ground in conjunction with the input impedance of the amplifier circuit. A 0.22 µF capacitor and 49.9 Ω resistor are inserted to ground across the 78.9 Ω resistor and 0.22 µF capacitor on the alternate input to balance the circuit.

Gain is a function of the source impedance, termination, and 348 Ω feedback resistor. See the THS4509 data sheet for further component values to set proper 50 Ω termination for other common gains.

Because the ADS5444 recommended input common-mode voltage is 2.4 V, the THS4509 is operated from a single power supply input with V_{S+} = 5 V and V_{S-} = 0 V (ground). This maintains maximum headroom on the internal transistors of the THS4509.

Clock Inputs

The ADS5444 clock input can be driven with either a differential clock signal or a single-ended clock input, with little or no difference in performance between both configurations. In low-input frequency applications, where jitter may not be a big concern, the use of single-ended clock (see Figure 16) could save some cost and board space without any trade-off in performance. When driven on this configuration, it is best to connect CLK to ground with a 0.01 µF capacitor, while CLK is ac-coupled with a 0.01 µF capacitor to the clock source, as shown in Figure 16.

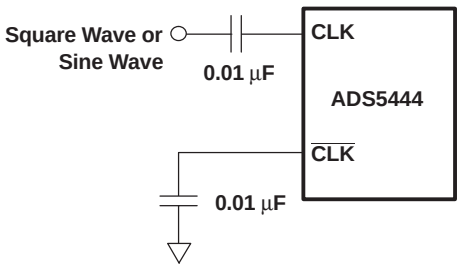


Figure 16. Single-Ended Clock

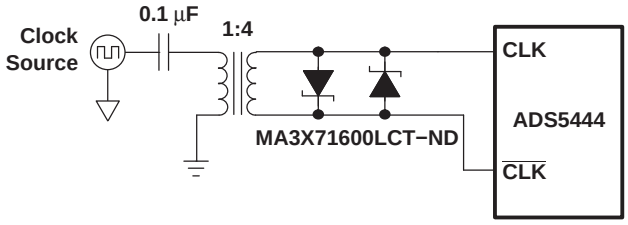


Figure 17. Differential Clock

For jitter-sensitive applications, the use of a differential clock has some advantages (as with any other ADC) at the system level. The first advantage is that it allows for common-mode noise rejection at the PCB level.

A differential clock also allows for the use of bigger clock amplitudes without exceeding the absolute maximum ratings. In the case of a sinusoidal clock, this results in higher slew rates and reduces the impact of clock noise on jitter. See *Clocking High Speed Data Converters* (SLYT075) for more details.

Figure 17 shows this approach. The back-to-back Schottky diodes can be added to limit the clock amplitude in cases where this would exceed the absolute maximum ratings, even when using a differential clock.

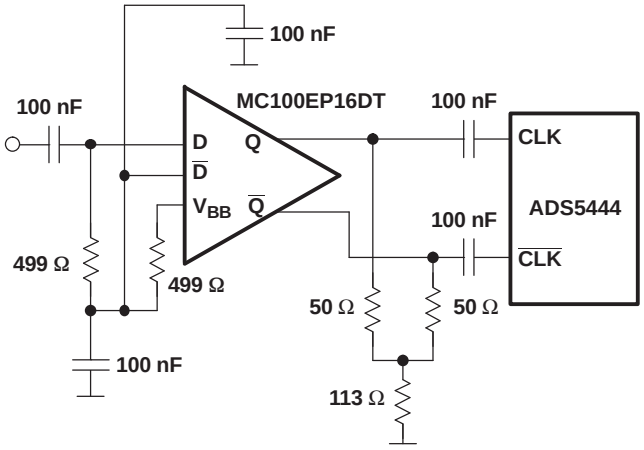


Figure 18. Differential Clock Using PECL Logic

Another possibility is the use of a logic-based clock, such as PECL. In this case, the slew rate of the edges is most likely much higher than the one obtained for the same clock amplitude based on a sinusoidal clock. This solution would minimize the effect of the slope dependent ADC jitter. Using logic gates to square a sinusoidal clock may not produce the best results, as logic gates may not have been optimized to act as comparators, adding too much jitter while squaring the inputs.

The common-mode voltage of the clock inputs is set internally to 2.4 V using internal 1 kΩ resistors. It is recommended to use ac coupling, but if this scheme is not possible due to, for instance, asynchronous clocking, the ADS5444 features good tolerance to clock common-mode variation.

Additionally, the internal ADC core uses both edges of the clock for the conversion process. Ideally, a 50% duty cycle clock signal should be provided.

Digital Outputs

The ADC provides 13 data outputs (D12 to D0, with D12 being the MSB and D0 the LSB), a data-ready signal (DRY), and an over-range indicator (OVR) that equals a logic high when the output reaches the full-scale limits. The output format is offset binary. It is recommended to use the DRY signal to capture the output data of the ADS5444.

The ADS5444 digital outputs are LVDS compatible.

Power Supplies

The use of low-noise power supplies with adequate decoupling is recommended. Linear supplies are the preferred choice versus switched ones, which tend to generate more noise components that can be coupled to the ADS5444.

The ADS5444 uses two power supplies. For the analog portion of the design, a 5 V AVDD is used, while for the digital outputs supply (DRVDD) TI recommends the use of 3.3 V. All the ground pins are marked as GND, although AGND pins and DRGND pins are not tied together inside the package.

Layout Information

The evaluation board represents a good guideline of how to lay out the board to obtain the maximum performance out of the ADS5444. General design rules such as the use of multilayer boards, single ground plane for ADC ground connections and local decoupling ceramic chip capacitors should be applied. The input traces should be isolated from any external source of interference or noise including the digital outputs, as well as the clock traces. The clock signal traces should also be isolated from other signals, especially in applications where low jitter is required as high IF sampling.

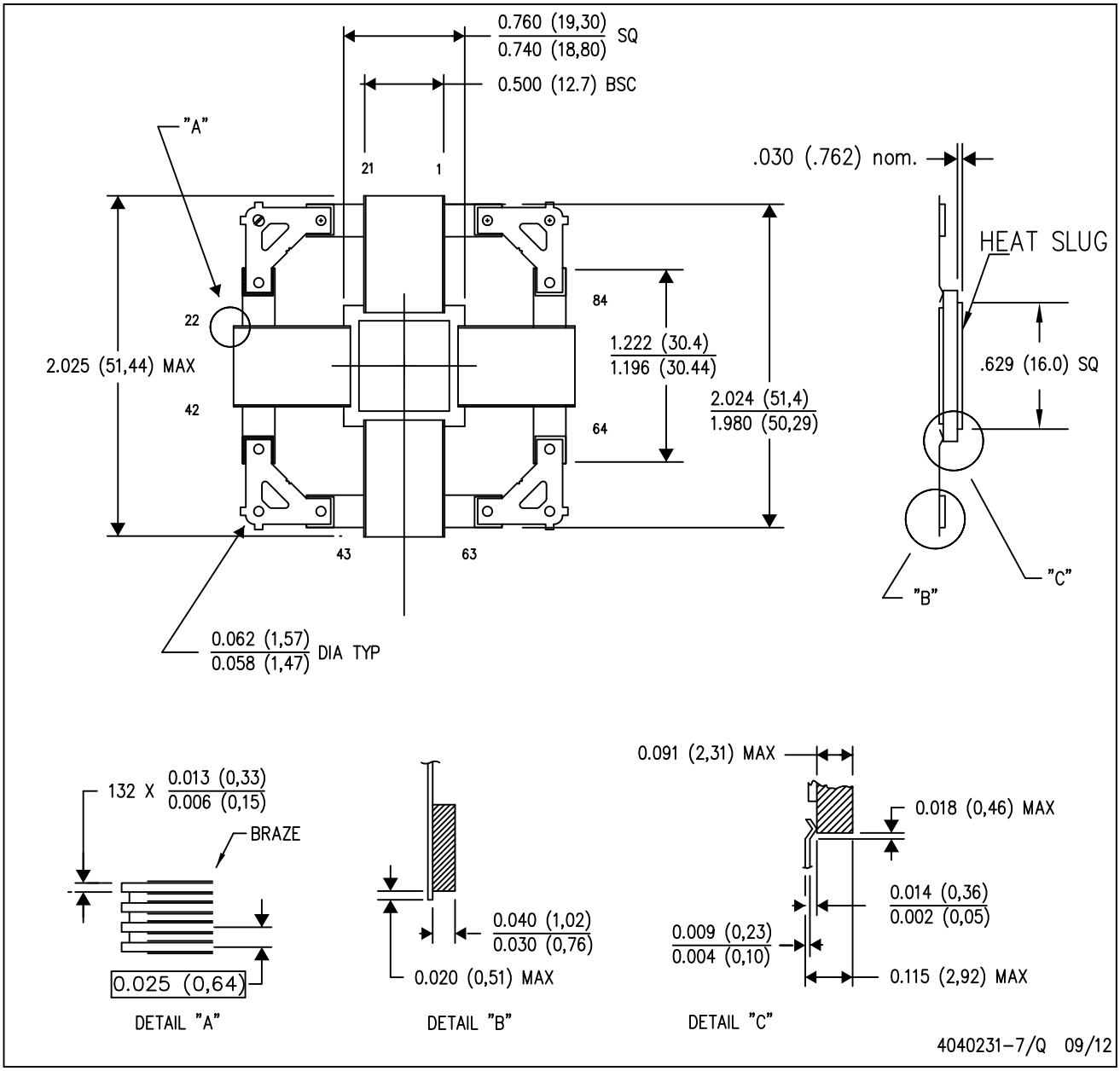
Besides performance-oriented rules, care has to be taken when considering the heat dissipation out of the device.

REVISION HISTORY

Changes from Revision B (February 2012) to Revision C **Page**

- Added /EM bullet to FEATURES 1
- Deleted ORDERING INFORMATION table 1

HFG (S–CQFP–F84) CERAMIC QUAD FLATPACK WITH NCTB



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Ceramic quad flatpack with flat leads brazed to non–conductive tie bar carrier.
D. This package is hermetically sealed with a metal lid.
E. The leads are gold plated and can be solderdipped.
F. Leads not shown for clarity purposes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-0720701VXC	ACTIVE	CFP	HFG	84	1	RoHS-Exempt & Green	Call TI	N / A for Pkg Type	-55 to 125	5962-0720701VXC ADS5444MHFG-V	Samples
ADS5444HFG/EM	ACTIVE	CFP	HFG	84	1	RoHS-Exempt & Green	Call TI	N / A for Pkg Type	25 to 25	ADS5444HFG/EM EVAL ONLY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ADS5444-SP :

- Catalog : ADS5444
- Enhanced Product : ADS5444-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

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