AFE3010 Ground Fault Circuit Interrupter (GFCI) With Self-Test and Neutral-Ground Fault Detection

1 Features

- Single-chip GFCI controller to aid in the design of UL-943 compliant systems
  - Built-in self-test to detect end-of-life, blink the LED, and/ or trip the load switch
  - Detect ground fault leakage path, and trip the load switch
  - Detect neutral-ground leakage path, and trip the load switch
- Protection against single-component failure
- Dual VDD and GND pins for redundancy
- Integrated noise filter to prevent false trips
- Simultaneously protects against HOT to GND and neutral to GND faults
- Adjustable fault current thresholds through external feedback resistors
- Fast response time
  - 150 ms for ±5mA ground fault current
  - 85 ms for ±10-mA ground fault current
  - 40 ms for ±30-mA ground fault current
  - 10 ms for ±50-mA ground fault current
- Onboard shunt regulator powers the system through passives
- Supports 120-V/ 60-Hz or 220-V/ 50-Hz systems
- Operating temperature range: –40 ºC to 105 ºC

2 Applications

- GFCI Outlet Receptacles
- GFCI Circuit Breakers
- Power Cord (In-Line GFCI)
- Hair Dryer
- Dish Washer

3 Description

The AFE3010 is a precision, low-power, Ground Fault Circuit Interrupter (GFCI) controller used for detecting ground fault leakage paths in electrical circuits. This device is a single IC solution that continuously monitors an electrical circuit for multiple fault conditions to verify that the system is operating correctly.

In addition to a ground fault leakage detection, the AFE3010 can detect a grounded neutral condition which can also lead to a harmful shock from a connected appliance. The device implements a unique closed-loop grounded neutral detection scheme that eliminates the need for component resonance tuning, resulting in optimized system development time. Periodic self-test is performed once in every 180 cycles of the AC power line to ensure all the components related to ground fault control system are working properly. In case of any component failure the device enables an LED light, and/ or trips a solenoid to open the load switch. In applications where an LED light indicator is not needed, the ALARM pin can be configured as a secondary SCR driver to drive an additional solenoid for redundancy purpose.

The AFE3010 integrates shunt and LDO regulators to directly power from an AC line through a diode bridge and passive components.

The AFE3010 offers flexible configurable options to implement robust application specific protection schemes in different end-equipments such as electrical receptacles, circuit breakers, and so forth.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AFE3010	VQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

GFCI Application

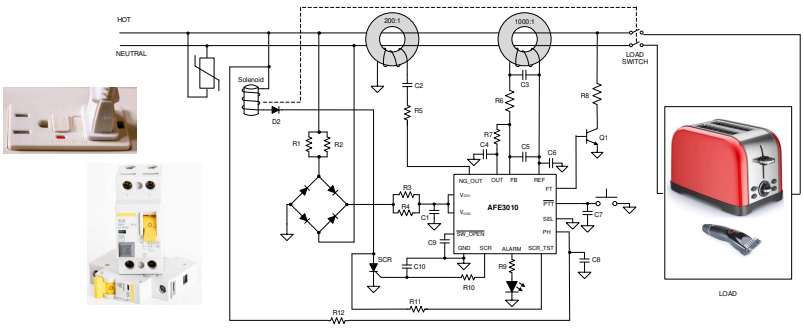


Table of Contents

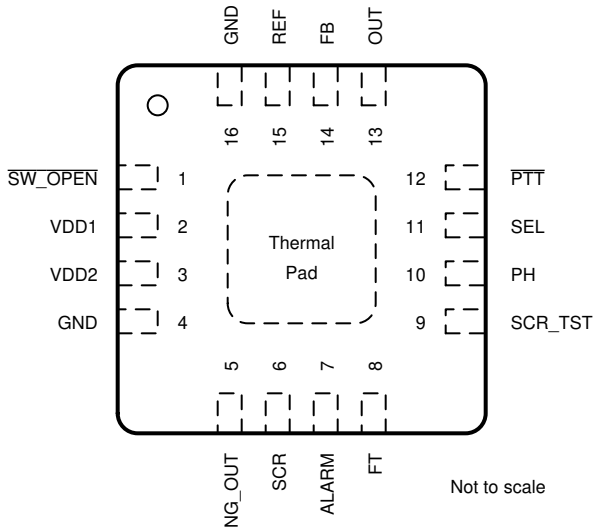
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
June 2020	*	Initial release.

5 Pin Configuration and Functions

RGT Package
16-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{\text{SW\_OPEN}}$	Input	Controls ALARM pin while asserted low. Refer to Table 3 for more details.
2	VDD1	Power	Power supply to the part from rectifying diode through series resistor. There is also a decoupling cap at this pin.
3	VDD2	Power	Redundant power supply pin.
4	GND	Ground	Ground pin for the device.
5	NG_OUT	Output	Generates a pulse to start the Ground to Neutral fault detection scheme. Drives the secondary winding of the 200:1 transformer through an AC-coupled capacitor. Leave this pin floating if Neutral-GND fault detection is not needed.
6	SCR	Output	Current output pin that drives the SCR after a fault is detected.
7	ALARM	Output	Alarm/ LED driver output. Drives a 3-KHz signal that can be used to drive an LED or buzzer to indicate that the self-test failed. Can be configured as secondary SCR driver when a 500-KΩ resistor is connected between SEL pin and ground. Refer to Table 2 for more details.
8	FT	Output	Drives the base of a bipolar transistor to emulate fault event during self-test.
9	SCR_TST	I/O	Monitors the phase of the sine wave of HOT power line after the solenoid. Drives a weak HIGH output during SCR self-test. Clamped to VDD through an internal diode.
10	PH	Input	Monitors the phase of the sine wave of HOT power line. Clamped to VDD through an internal diode.
11	SEL	Input	Control pin to configure the device. Refer to Table 2 for more details.
12	$\overline{\text{PTT}}$	Input	Active-low push-to-test pin. Starts self-test and fires SCR if self-test passes.
13	OUT	Output	Amplifier output node.
14	FB	Input	Amplifier inverting input.
15	REF	I/O	Amplifier non-inverting input. Typically 2.5 V derived from an internal 5-V regulator.
16	GND	Ground	Ground pin for the device.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply Voltage	VDD1, VDD2	0	26	V
Input Voltage	PH, SCR_TST	–0.3	26	V
	REF, FB, SW_OPEN, PTT, SEL	–0.3	6	V
Output Voltage	NG_OUT	–0.3	26	V
	FT, OUT, SCR, ALARM	–0.3	6	V
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, allpins(1)	±2000	V
		Charged device model (CDM), per JEDEC specificationJESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{REF}, V_{FB}, V_{SW_OPEN}, V_{PTT}, V_{SEL}	Input voltage			5.5	V
T_A	Ambient temperature	–40		105	°C

6.4 Thermal Information

THERMAL METRIC(1)		AFE3010 RGT (QFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND REFERENCE						
V_{VDD}	Power Supply Shunt Regulator Voltage		19.5	20	20.5	V
		T_A = –0 °C to 105 °C		30	60	ppm/°C
I_{REF}	Clamping Current at VREF	V_{REF} = 0 V	1	1.7	2.5	mA
V_{REF}	Reference Voltage		2.42	2.5	2.58	V
		T_A = –40 °C to 105 °C		80	100	ppm/°C
I_Q	Quiescent Current	Force VDD to 19 V through 50-Ω, Measured VDD to GND		900	1250	µA
		Force 19 V to VDD through 50-Ω, Measured VDD to GND, T_A = –40 °C to 105 °C			1500	µA
AMPLIFIER						
V_{OS}	Offset Voltage, RTI		–150		150	µV
		T_A = –40 °C to 105 °C			0.5	µV/°C
V_{n_inp}	Input Voltage Noise			10		nV/√Hz
I_{in_inp}	Input Current Noise			2		pA/√Hz
ZOL	Open-loop Transimpedance			7		Gohms
BW	Application Bandwidth (1)			6.5		kHz
V_{osw_vdd}	VOUT Swing to VDD	No Load	4.8			V
V_{osw_gnd}	VOUT Swing to GND	No Load			0.1	V
DIGITAL CONTROL						
t_{gf_resp}	Ground Fault Response Time	Leakage Current = ±5 mA		0.15		s
		Leakage Current = ±10 mA		0.085		s
		Leakage Current = ±30 mA		0.04		s
		Leakage Current > ±50 mA		0.01		s
t_{d1}	Debounce Time from '$\overline{\text{PTT}}$ High to Low Transition' to Self-test Start			80		ms
t_{d2}	Debounce Time from '$\overline{\text{SW\_OPEN}}$ High to Low Transition' to SCR Fire (Long Pulse)			130		ms
t_{d3}	Debounce Time from '$\overline{\text{SW\_OPEN}}$ Low to High Transition' to ALARM Off			140		ms
t_{d4}	$\overline{\text{SW\_OPEN}}$ Low Time to Execute Fault Counter RESET without SCR Fire (Short Pulse)			55		ms
SCR DRIVER						
IOH	High-Level Output Current	VO = 1.0 V		2	3	mA
ROUT	Output Impedance			550		Ω
ALARM DRIVER						
VOH	High-Level Output Voltage	IOH =-1 mA	3	3.2		V
VOL	Low-Level Output Voltage	IOL =1 mA		0.25	0.35	V
f_{LED_AL}	LED/ Alarm Frequency			3		KHz
FT DRIVER						
IOH	High-Level Output Current	VO = 1.0 V		2	3	mA
ROUT	Output Impedance			550		Ω
NG_OUT DRIVER						
VOL	Low-Level Output Voltage	IOL = 4 mA		0.2	0.4	V
VOH	High-Level Output Voltage	IOH = –0.1 mA	V_{VDD}–0.8	V_{VDD}–0.2		V

(1) The typical bandwidth of the current feedback amplifier is measured based off the recommended component values in the Application and Implementation section. This number will vary if the component values change in a particular application.

6.6 Typical Characteristics

at T_A = 25 °C typical (unless otherwise noted)

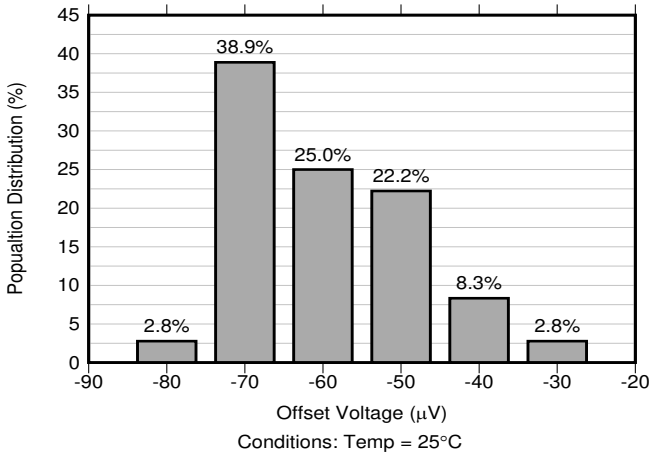


Figure 1. Amplifier Offset Voltage Distribution

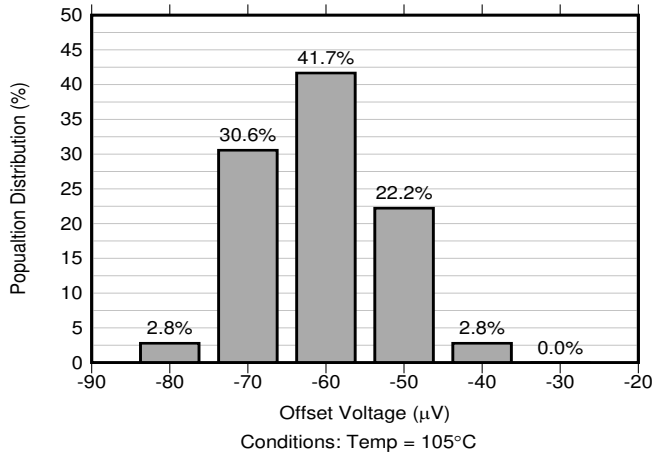


Figure 2. Amplifier Offset Voltage Distribution

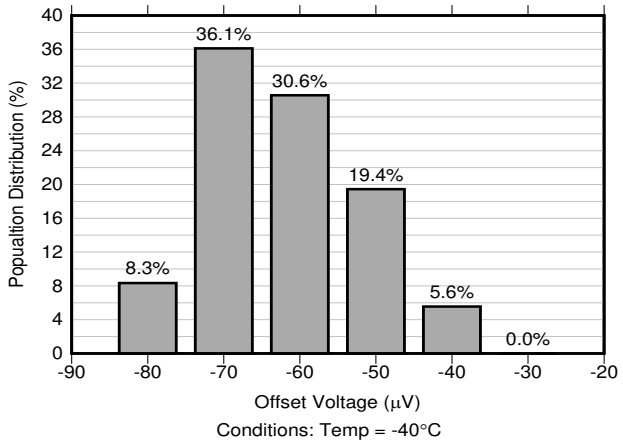


Figure 3. Amplifier Offset Voltage Distribution

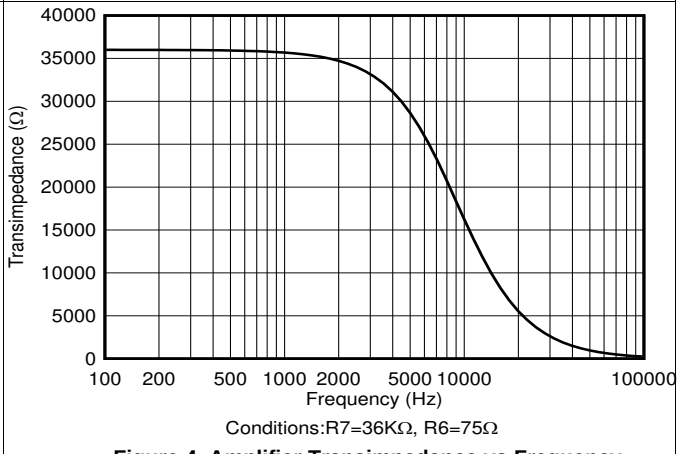


Figure 4. Amplifier Transimpedance vs Frequency

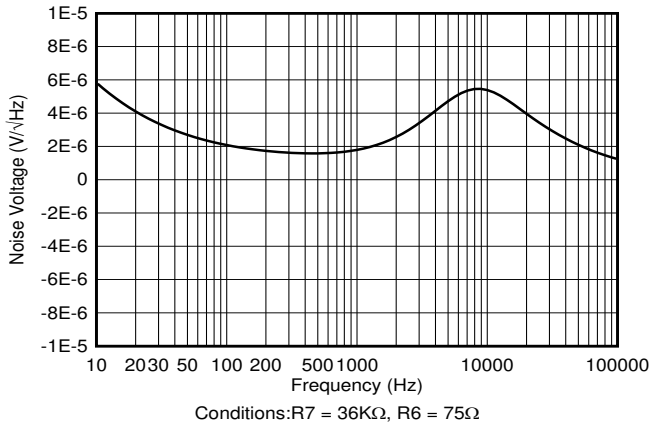


Figure 5. Amplifier Output Noise

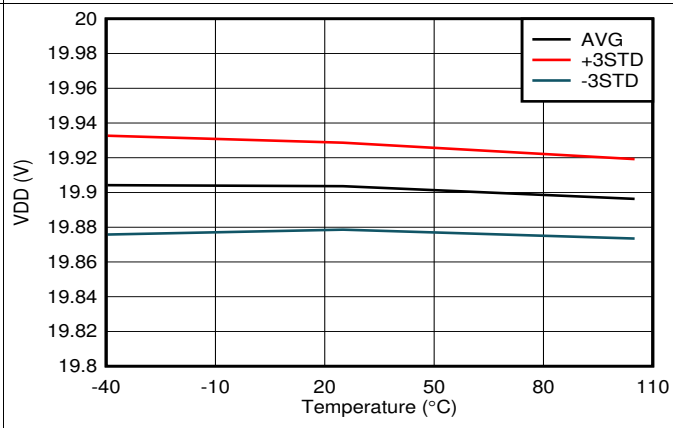


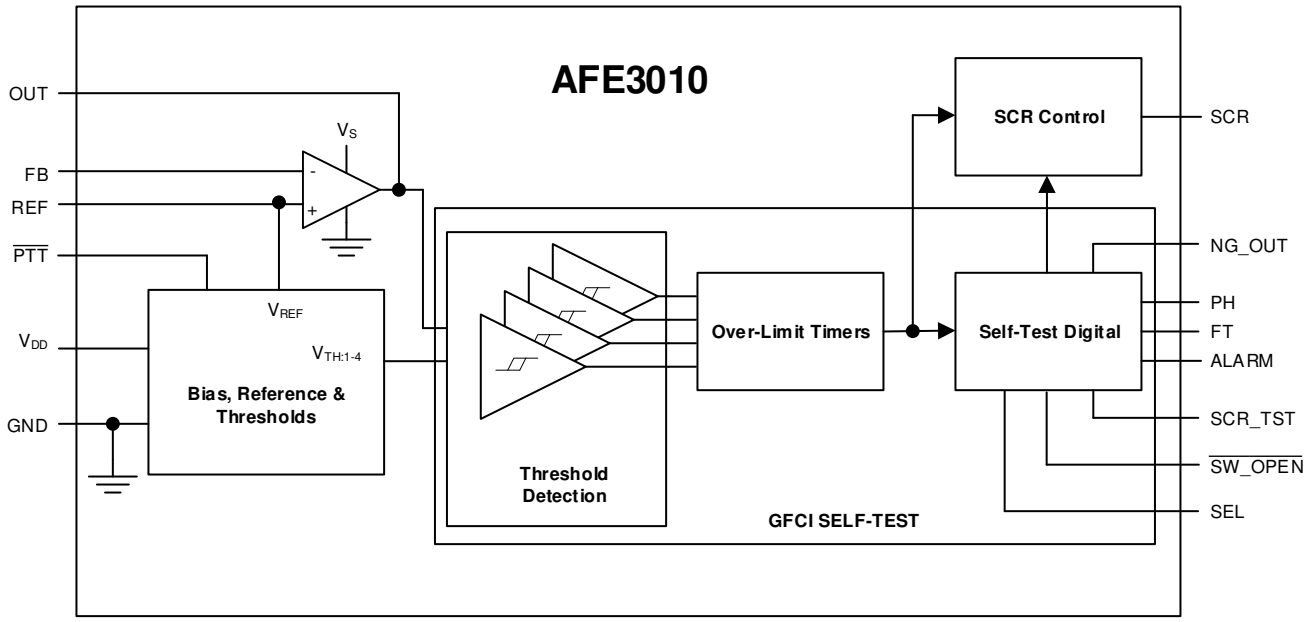
Figure 6. VDD Drift Across Temperature

7 Detailed Description

7.1 Overview

The AFE3010 is a Ground Fault Circuit Interrupter (GFCI) controller to detect the presence of leakage paths that could lead to potential injuries from electric shock. This device is designed to develop UL-943 compliant system like a GFCI receptacle or circuit-breaker. The self-test functionality ensures that the circuit is operating correctly prior to an actual fault event. A GFCI device relies on the imbalance of differential current through the transformer to detect a ground fault. The presence of a neutral-ground leakage path can potentially mask some of this imbalance through the transformer during an actual ground fault event, resulting in safety hazard for the downstream equipments connected to the GFCI unit. The AFE3010 employs an unique closed-loop neutral-ground leakage detection scheme to alleviate this safety hazard. The precision, low-noise amplifier along with the threshold detection filters in the AFE3010 ensure accurate detection of fault events while minimizing unintended false alerts.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Powering The AFE3010

Figure 7 shows the recommended components and configurations to develop a GFCI system using the AFE3010. The AFE3010 features an internal 20-V shunt regulator that connects to an external rectifier output through limiting resistors R1 and R2. The two separate VDD and GND pins offer redundancy during single component failure events in GFCI systems. An internal 5-V rail powers the majority of the internal circuitry, and drives all the signal pins except the NG_OUT, PH, and SCR_TST pins. The NG_OUT pin is referenced to the 20-V VDD through an internal reverse blocking diode inside the device.

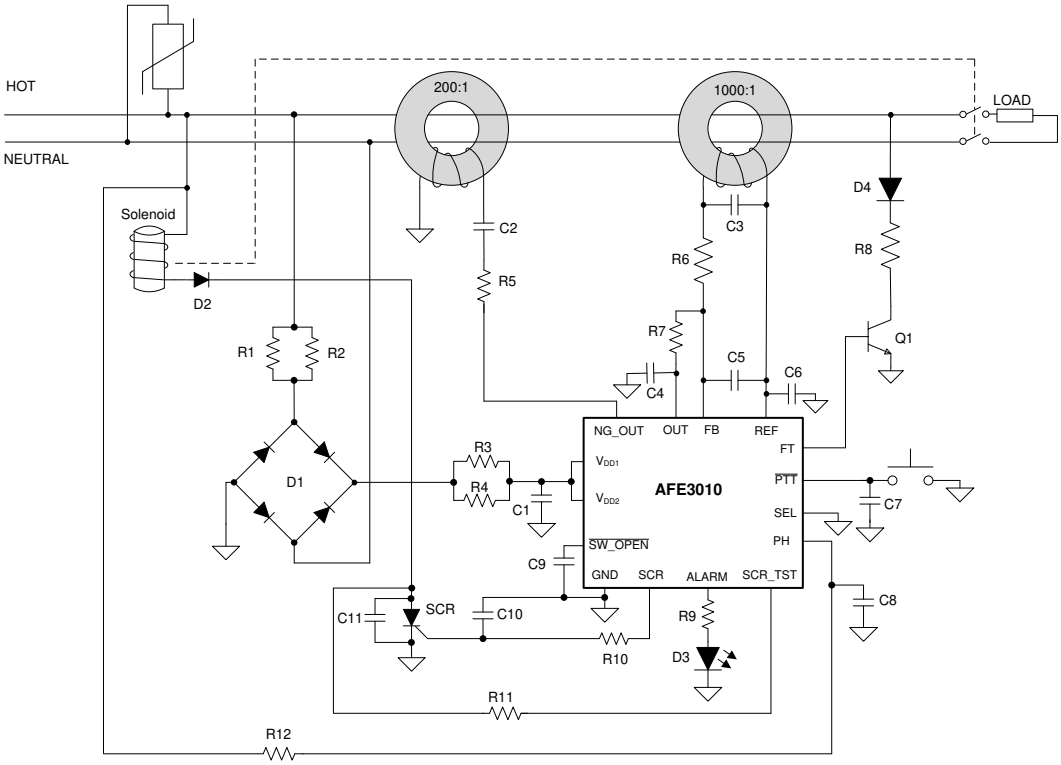


Figure 7. AFE3010 Application Diagram

7.3.2 Sensing Amplifier

The AFE3010 employs a current-feedback chopper amplifier topology to sense a wide range of fault currents with high precision. The current-feedback topology allows the device to maintain consistent gain across the wide fault current limits. Hence no degradation of accuracy is experienced at large fault current measurements. The device REF, FB, and OUT pins are the noninverting, inverting, and output terminals of the amplifier, respectively. The user access of all three pins helps system designers develop their own current sensing thresholds and bandwidths by optimizing the corresponding passive component values.

7.3.3 Noise Filter

As shown in Figure 8, the AFE3010 uses a unique 2-stage filter architecture to provide robust protection against false trips. A series of internal comparators register the fault current thresholds at the output of the sensing amplifier. Once a valid fault threshold is detected, the filter searches for a pre-determined pattern of fault occurrences in the consecutive cycles. If the specific pattern is detected, the filter will enable the SCR driver to open the power line switch. As shown in Table 1, the AFE3010 response time is faster than the UL943 mandated requirements.

Feature Description (continued)

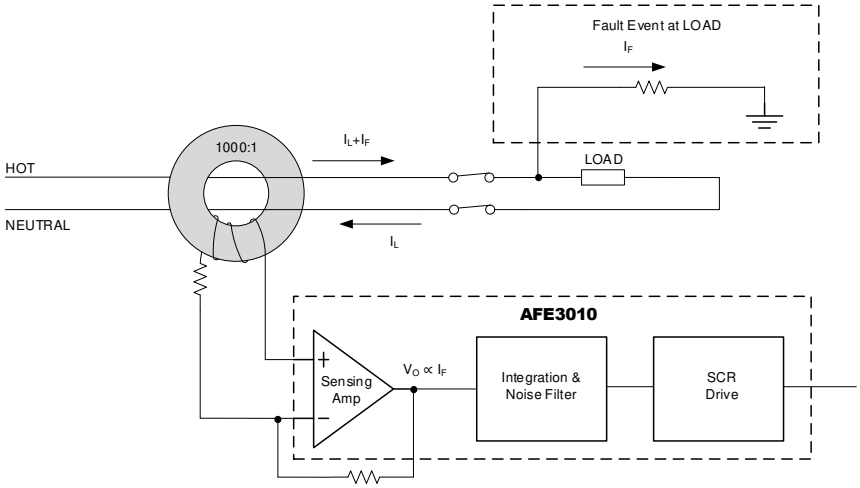


Figure 8. AFE3010 Filter Scheme During Fault Conditions

Table 1. AFE3010 Response Time

FAULT CURRENT	FAULT RESPONSE TIME	
mA	UL943 TIMING REQUIREMENTS (S)	AFE3010 TYPICAL RESPONSE TIME (S)
> ±5	< 6.335	0.150
> ±10	<1.000	0.085
> ±30	< 0.371	0.040
> ±50	< 0.100	0.010

7.3.4 ALARM (LED) Driver

The AFE3010 ALARM pin can be used to drive an LED or a buzzer. Under normal system operation the ALARM output remains low. During active operation, the ALARM signal generates a 3-KHz signal for the duration of positive half of the power cycle and remains low for the duration of the negative half power cycle. Figure 9 shows the ALARM signal scheme over a 60-Hz power line.

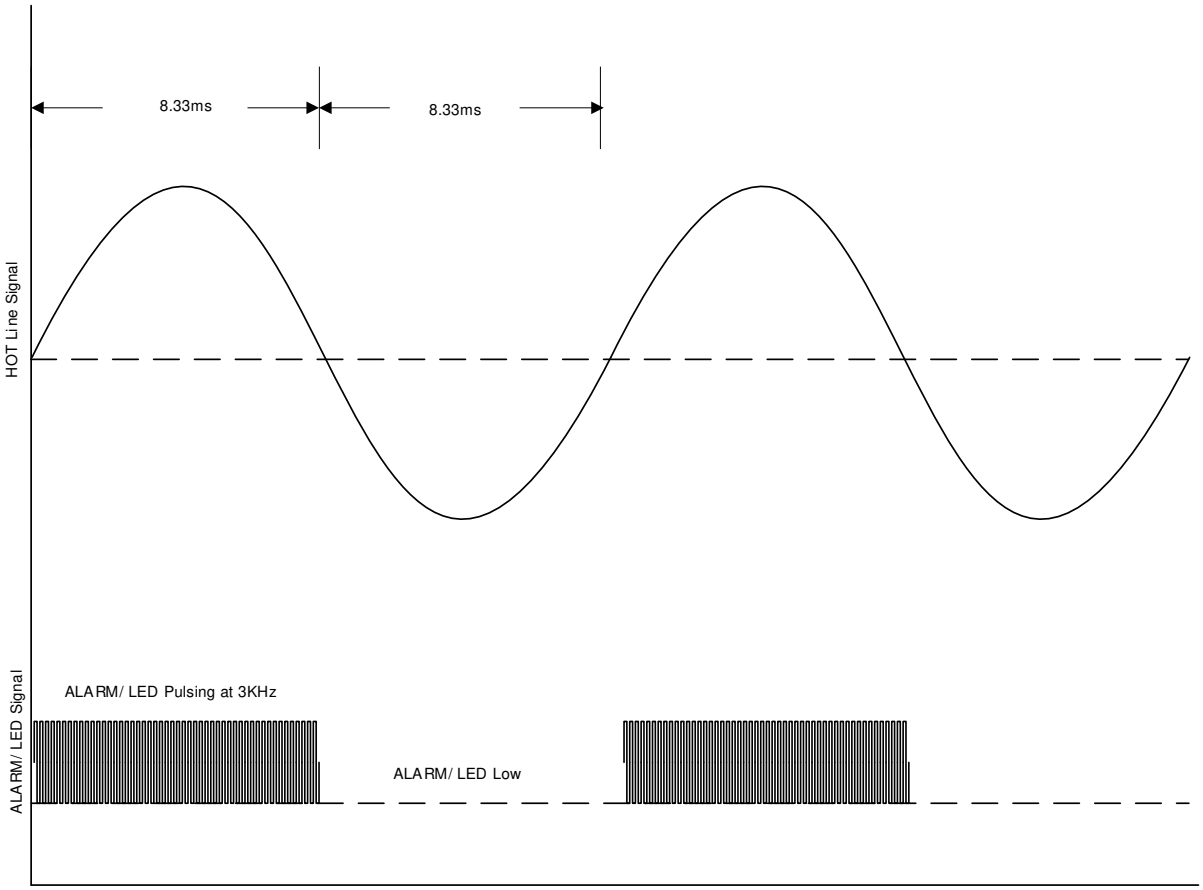


Figure 9. AFE3010 ALARM Signal Active Mode Definition (Time Calculation Shown for a 60-Hz Power Line)

7.3.5 Phase Detection

The AFE3010 monitors power line signal phase at any given time through the PH and SCR_TST pins. Both pins are clamped to VDD through internal clamping diodes. The PH pin is connected directly to the HOT power line. This enables the device to monitor the power signal instantaneously. Phase measurement is critical for faster and accurate response to system fault conditions. The SCR_TST pin measures the phase after the rectifying diode.

7.3.6 SCR Control

The AFE3010 triggers an external SCR through the device SCR pin during a load fault event or self-test fail event. This SCR trigger event activates a solenoid to trip the load switch disconnecting the load.

7.3.7 Self-Test Function

The AFE3010 performs two different types of self-tests: periodic self-test and continuous self-test.

7.3.7.1 Periodic Self-Test

At system power up, the self-test starts after 60 cycles of power line signal, and retests within 60 cycles if the first self-test fails. Five consecutive self-test fails drive the SCR and assert the ALARM signal blinking at 1-second intervals (for 60-Hz systems). After the first self-test pass, the device fires ALARM for 250-ms period to indicate the successful pass of the first self-test. During normal operating conditions, the self-test repeats every 180 cycles. Figure 10 shows the periodic self-test sequences and decision blocks. The device requires one cycle from the AC power line to complete the periodic self-tests listed below:

1. Ground Fault Test: the AFE3010 generates a fault current through the FT pin. The device reads a test pass if the AFE3010 detects the fault current through the transformer. If the fault current is not detected, the device reads a test fail. This fail event triggers another self-test within next 60 cycles. After five consecutive fails, the AFE3010 fires the SCR and sets the ALARM blinking at 1-s intervals (for 60-Hz systems). The ground fault test covers the integrity check of the transformer, fault current generator components, feedback resistors, and the AFE3010 fault detection circuits.
2. SCR Integrity Test: The AFE3010 performs SCR integrity test after completing the ground fault test. The device induces a SCR anode signal transition with the help of SCR_TST pin. If the SCR anode signal low transition is not detected, the AFE3010 reads a test fail. This fail event triggers another self-test within next 60 cycles. After five consecutive fails it fires the SCR and sets ALARM blinking at 1-s intervals (for 60-Hz systems).

7.3.7.2 Continuous Self-Test

The AFE3010 performs the following continuous mode self-tests. If any of these tests fail, the device does not wait to perform another self-test. Rather, the AFE3010 immediately fires the SCR and sets the ALARM blinking as 1-s intervals (for 60-Hz systems).

1. Open Solenoid Test: The AFE3010 checks for transition of AC line signal at the PH and SCR_TST pins. If the device does not detect a transition of the line signal at PH or SCR_TST pins for approximately 100 ms, then the device reads a self-test fail.
2. Diode Bridge Test: if a diode is shorted in the diode bridge rectifier, the device is able to detect the variation in supply current from the diode bridge. This detection is considered a self-test fail, and the AFE3010 fires the SCR and sets the ALARM blinking at 1-s intervals (for 60-Hz systems).
3. Amplifier Short/ Open: The device monitors for sustained fault current conditions, even after the fault current has been detected and SCR has fired. The primary purpose of this self-test is to detect a single-point failure with the amplifier signal pins and associated components. If a failure is detected, the device fires SCR one more time and LED starts blinking. In the event the load switch doesn't open after SCR is fired, this self-test recognizes a failure and starts the LED blinking.

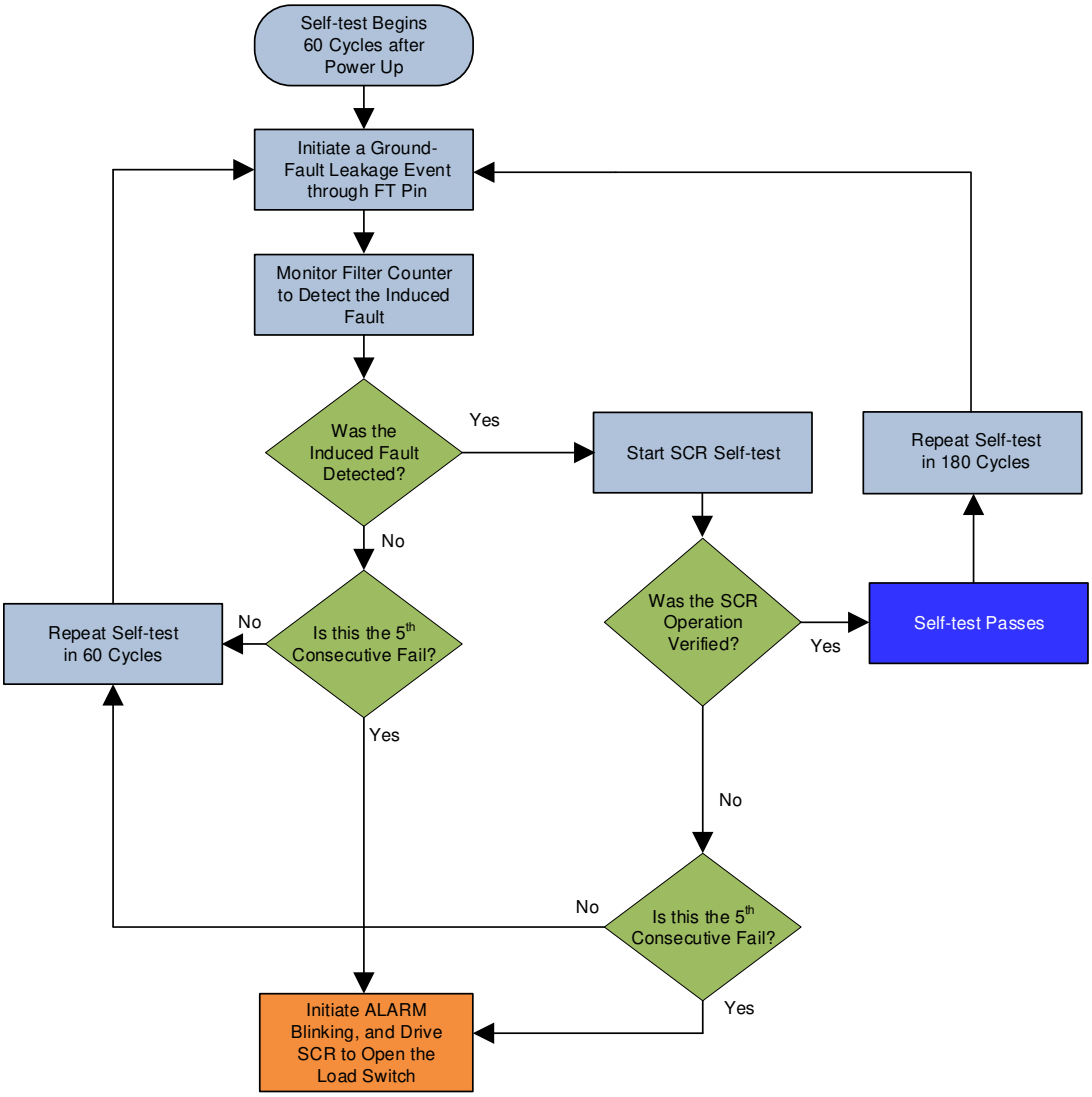


Figure 10. AFE3010 Self-test Sequence

7.4 Device Functional Modes

7.4.1 Pin Configuration

The AFE3010 offers multiple operating modes and pin functions. These modes can be set by the SEL pin per Table 2.

Table 2. Pin Configuration

SEL	SCR SELF-TEST	ALARM
5 V (Leave floating)	No	Works as ALARM/ LED driver.
2.5 V (Connect 500-KΩ resistor to GND)	Yes	Works as secondary SCR driver in applications where ALARM (LED) function is not needed.
0 V (Connect to GND)	Yes	Works as ALARM/ LED driver.

7.4.2 ALARM Modes to Drive LED

The AFE3010 supports three different modes when the ALARM pin is used as an LED driver:

1. Successful power-up indication: The LED turns on for 250-ms when the first periodic self-test is completed after power up. On a 60-Hz system, this event occurs approximately one second after power up.
2. LED blinking due to self-test fail: In case of a self-test fail, the ALARM pin sets the LED in blinking mode a frequency of 0.5-Hz. In this state, the LED is on for one second and off for one second. When the ALARM pin goes into blinking mode, a system power recycle or a successful self-test pass through the $\overline{\text{PTT}}$ press will deactivate the ALARM signal.
3. LED on through the $\overline{\text{SW\_OPEN}}$ pin: If the $\overline{\text{SW\_OPEN}}$ pin is low, the LED will turn on without 0.5-Hz blinking. During a self-test fail event, the device overrides the $\overline{\text{SW\_OPEN}}$ state and puts the LED blinking mode at 0.5 Hz.

Table 3. ALARM (LED) Operating Modes

AFE3010 STATUS	$\overline{\text{SW\_OPEN}}$ PIN	ALARM (LED) FUNCTION	COMMENTS
Self-test fails	Floating	ALARM (LED) blinks	Self-test fail dominates ALARM (LED) behavior and ignores the $\overline{\text{SW\_OPEN}}$ signal
	Low		
Load switch open due to H-G or N-G fault	Floating	ALARM (LED) remains off	
	Low	ALARM (LED) remains on without blinking	
At power up, during the first self-test only	Floating	ALARM (LED) on for 0.25 s after first self-test pass	Indicates the event of first self-test pass after power up
	Low	ALARM (LED) on without blinking	

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Manual Self-Test Using $\overline{\text{PTT}}$ Pin

The AFE3010 supports manual self-test using the $\overline{\text{PTT}}$ pin.

8.1.1.1 Successful Self-Test

Figure 11 shows a successful manual self-test timing with the $\overline{\text{PTT}}$ pin.

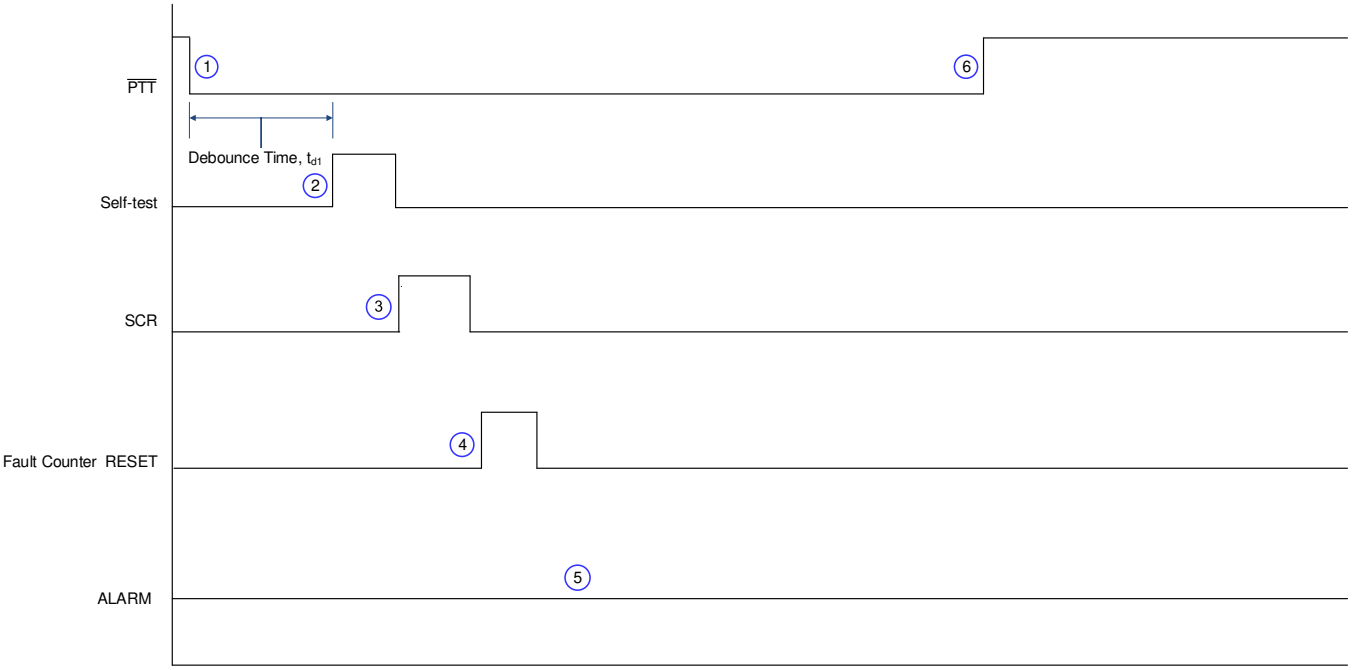


Figure 11. Successful Manual Self-Test Using $\overline{\text{PTT}}$ Pin

1. The test sequence starts when $\overline{\text{PTT}}$ transitions from high to low.
2. After a debounce time to ensure there is no false transition, the device starts the self-test.
3. If the self-test passes, the SCR fires.
4. The internal fault counter resets.
5. The ALARM signal remains low to indicate the self-test passed.
6. The $\overline{\text{PTT}}$ signal transitions low to high to complete the self-test event.

Application Information (continued)

8.1.1.2 Unsuccessful Self-Test

Figure 12 shows an unsuccessful manual self-test timing with the $\overline{\text{PTT}}$ pin.

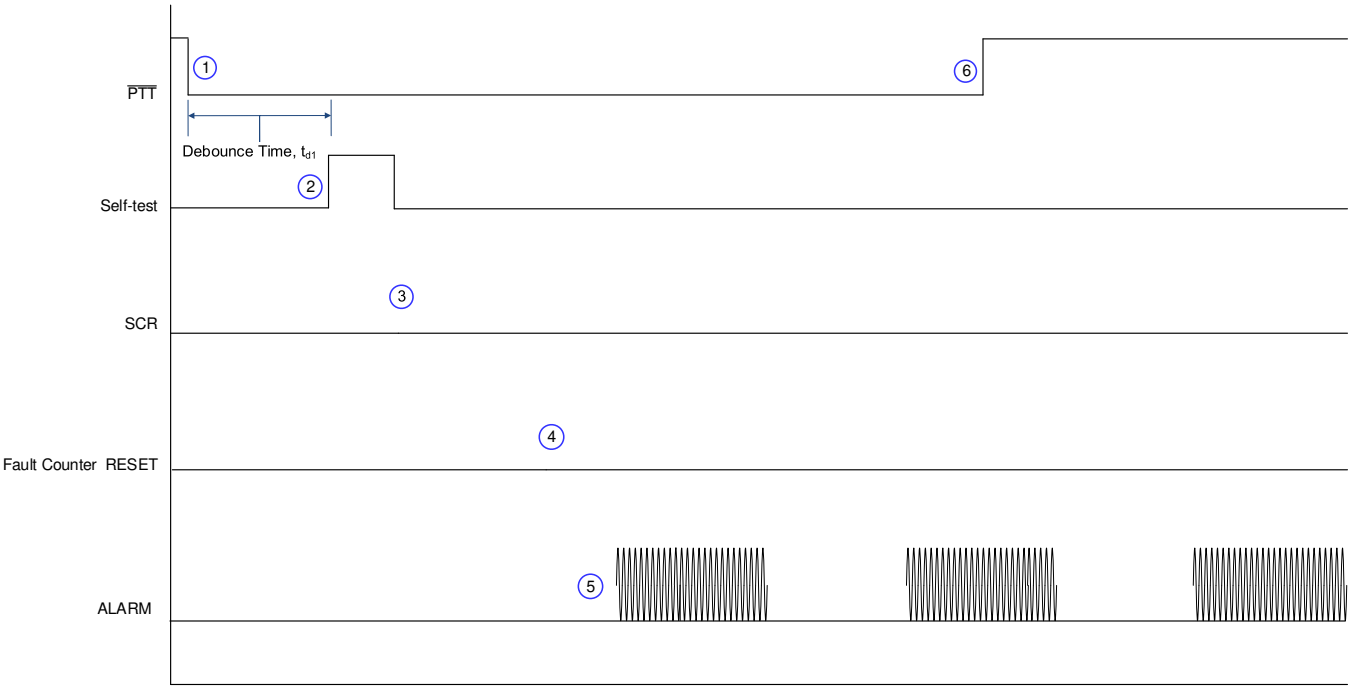


Figure 12. Unsuccessful Manual Self-Test Using $\overline{\text{PTT}}$ Pin

1. The test sequence starts when $\overline{\text{PTT}}$ transitions from high to low.
2. After a debounce time to ensure there is no false transition, the device starts the self-test.
3. If the self-test does not pass, the SCR does not fire.
4. The internal fault counter doesn't reset.
5. The ALARM signal starts to blink at 0.5Hz (for 60-Hz systems) to indicate the self-test fail.
6. The $\overline{\text{PTT}}$ signal transitions low to high to complete the self-test event.

8.1.2 ALARM and RESET Function With $\overline{\text{SW\_OPEN}}$

The $\overline{\text{SW\_OPEN}}$ pin can be used as a reset signal to the device through a mechanical assembly or a micro controller. When the $\overline{\text{SW\_OPEN}}$ remains low longer than the debounce time t_{d2}, the device fires the SCR. For applications that require a reset without the SCR fire, keep the $\overline{\text{SW\_OPEN}}$ low state for shorter duration (in between 55 ms to 75 ms) before transition to high state. The ALARM (LED) function is also modified using the $\overline{\text{SW\_OPEN}}$ function. Connect a noise-blocking capacitor to the $\overline{\text{SW\_OPEN}}$ pin if this function is not needed.

Application Information (continued)

8.1.2.1 No Self-Test Fail Event

If there is no self-test failure event, the ALARM is turned on without blinking when the $\overline{\text{SW\_OPEN}}$ signal goes from high to low. Figure 13 describes the sequence of events.

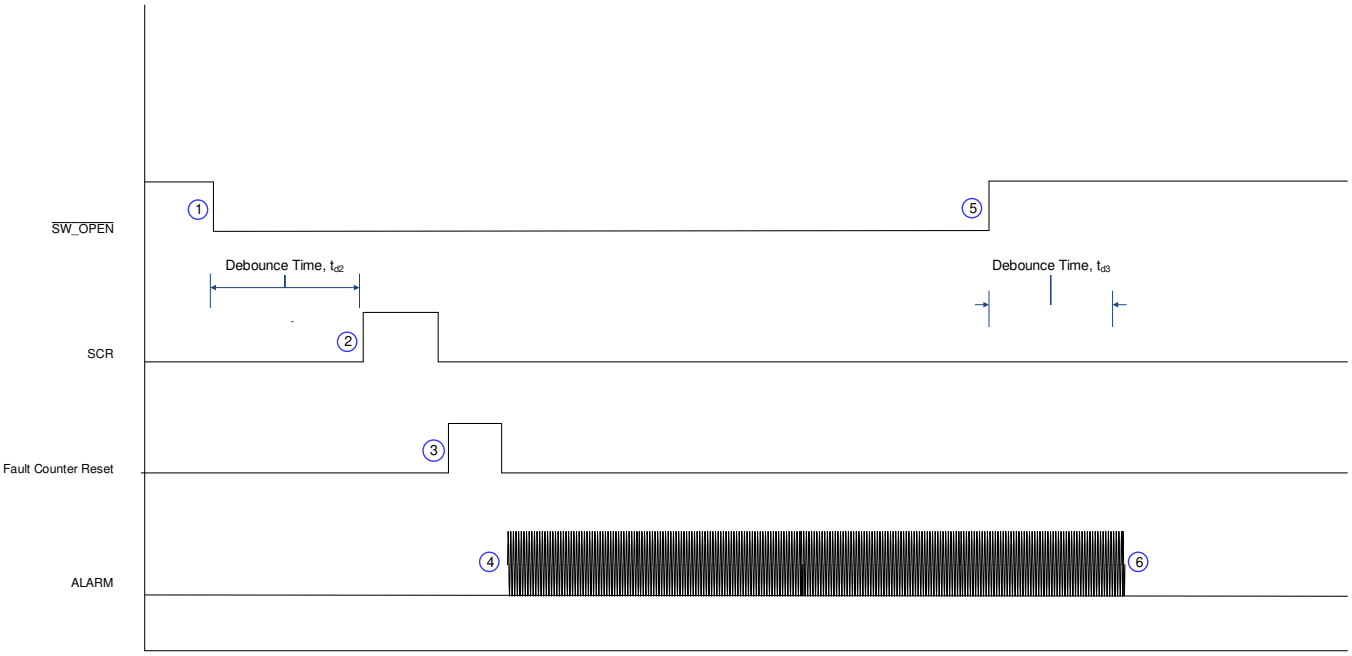


Figure 13. ALARM With $\overline{\text{SW\_OPEN}}$ Transition to Low. No Self-Test Failure.

1. The $\overline{\text{SW\_OPEN}}$ signal transitions from high to low.
2. After a debounce time to ensure there is no false transition, the device fires the SCR.
3. The internal fault counter resets.
4. The ALARM turns on.
5. The $\overline{\text{SW\_OPEN}}$ signal transitions low to high.
6. After a debounce time to ensure there is no false transition, the ALARM turns off.

Application Information (continued)

8.1.2.2 Self-Test Fail Event

If there is a prior self-test failure event, the ALARM will continue to blink at 0.5 Hz (for 60-Hz systems) when the $\overline{\text{SW\_OPEN}}$ signal goes from high to low. Figure 14 describes the sequence of events.

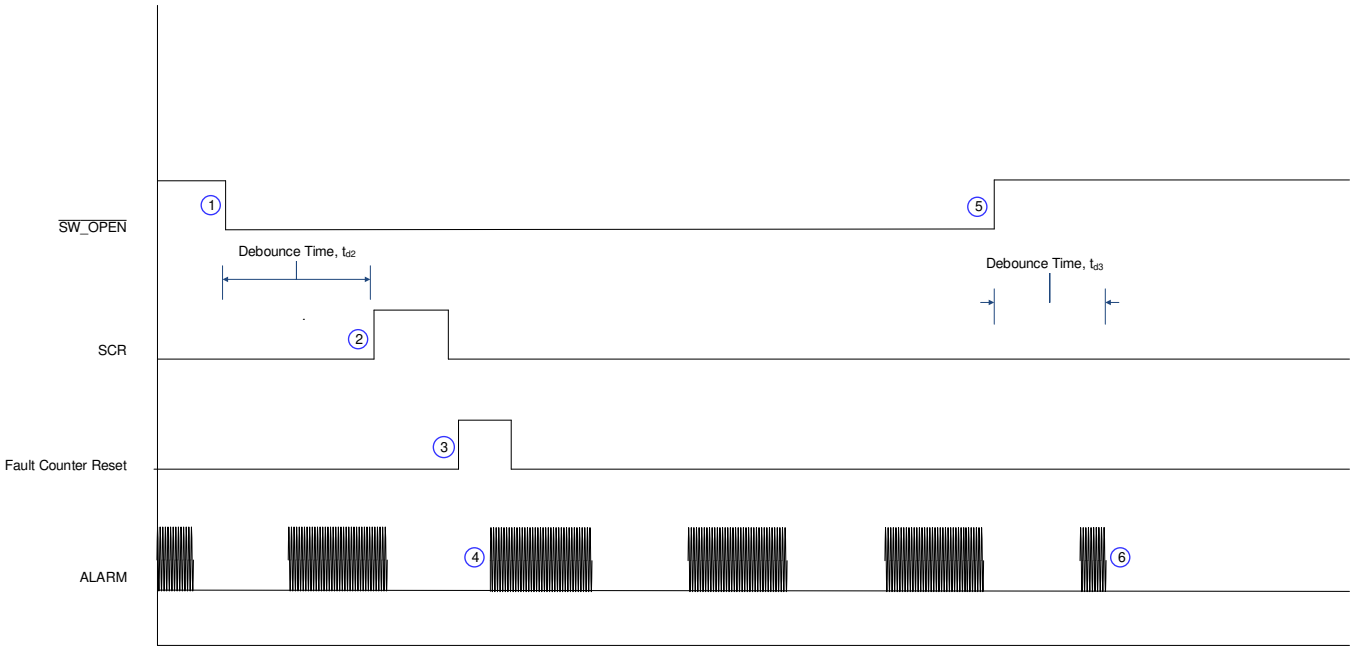


Figure 14. ALARM With $\overline{\text{SW\_OPEN}}$ Transition to Low and Prior Self-Test Failure

1. $\overline{\text{SW\_OPEN}}$ signal transitions from high to low.
2. After a debounce time to ensure there is no false transition, the device fires the SCR.
3. The internal fault counter resets.
4. The ALARM continues to blink at 0.5 Hz (for 60-Hz systems) because the self-test fail overrides $\overline{\text{SW\_OPEN}}$ function.
5. The $\overline{\text{SW\_OPEN}}$ signal transitions low to high.
6. After a debounce time to ensure there is no false transition, the ALARM turns off.

8.2 Typical Application

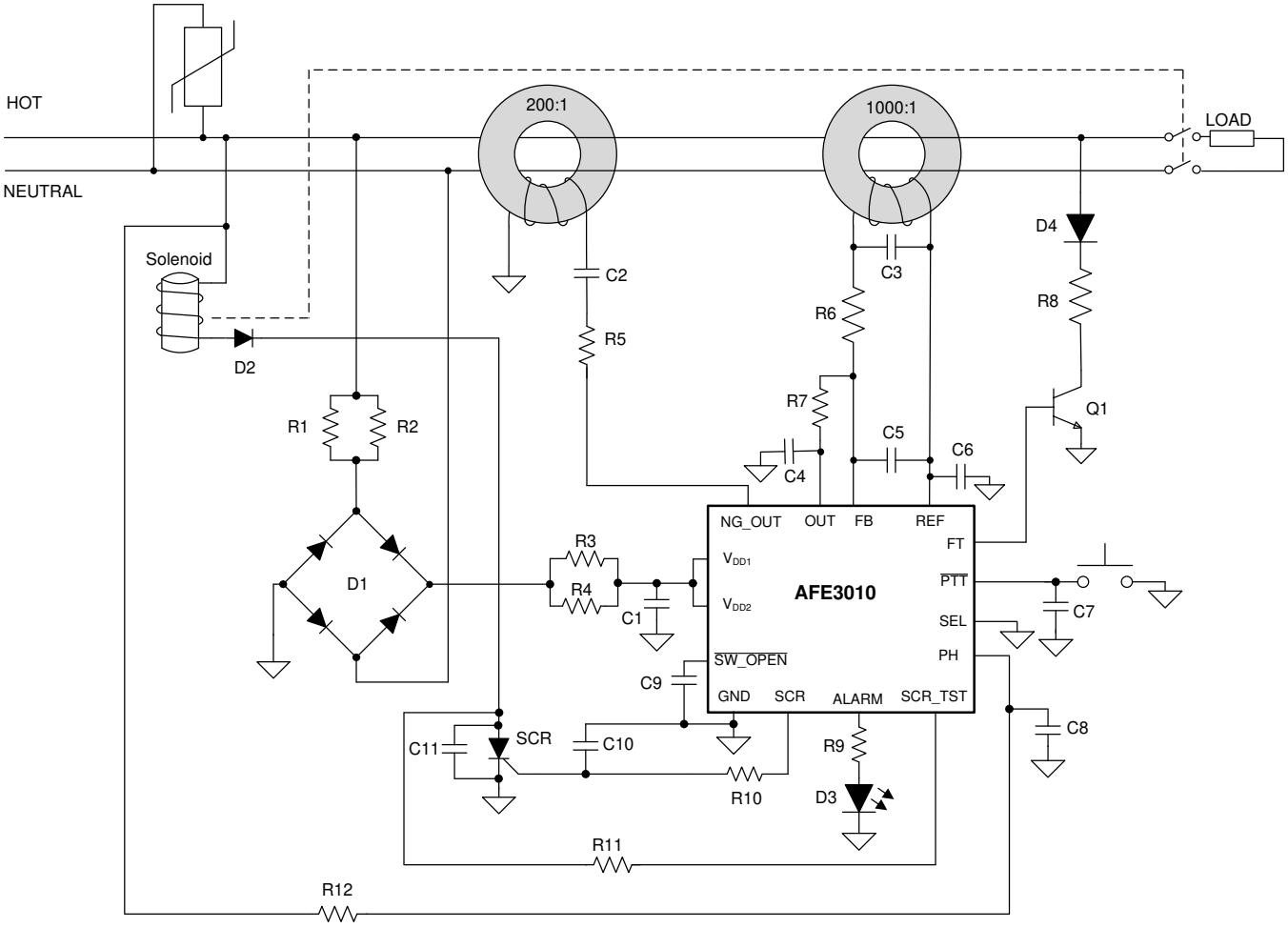


Figure 15. Typical GFCI Application Schematic With AFE3010

8.2.1 Design Requirements

Figure 15 is the typical application for the AFE3010 when the SEL pin is grounded. The system requirements shown in Table 4 are based upon the UL-943 standard. The required component power and voltage ratings should be chosen based upon the line voltage. See Table 5 for more information on power ratings.

Table 4. Design Requirements

DESIGN PARAMETER	VALUE
Line or source voltage	120 VAC (±15%)
Line frequency	50-60 Hz
Line polarity (connection to GFCI unit)	Normal and reverse polarity
Operational temperature	–40 °C to +105 °C
Rated load	20 A RMS
Ground fault threshold (trip point)	5 mA RMS
Ground fault threshold variation over all parameters	±0.5 mA RMS
Neutral-to-ground fault detection	Per UL-943

8.2.2 Detailed Design Procedure

The following procedure details how to design a GFCI system with the AFE3010. The procedure is not intended to represent all of the validation required for a GFCI system to comply with the necessary regulations. The main goals are to tune the ground fault trip level and neutral-to-ground (N-G) detection of the system.

Table 5 presents the key parameters needed for the components in Figure 15. Table 5 also provides brief explanations of components and parameters. Component voltage ratings are dependent upon either the 20-V internal shunt regulator, the internal 5-V rail, or by the line voltage itself. Note that while Table 5 shows tested and working values, some components could be optimized further to reduce necessary power and voltage ratings depending upon the system requirements.

Table 5. Summary of Components in AFE3010 Typical Application

COMPONENT DESIGNATOR	COMPONENT VALUE	COMPONENT RATINGS	DESCRIPTION
C1	3.3 µF	50 V, ±10%, X7R	Primary decoupling capacitance for AFE3010. Voltage rating dependent upon the 20-V shunt regulator.
C2	0.1 µF	50 V, ±10%, NP0	Capacitive load for NG_OUT driver to generate a current pulse. Voltage rating dependent upon the 20-V shunt regulator.
C3	0.47 µF	> 5 V, ±10%, X7R	Tunes and stabilizes the amplifier response so V_{OUT} is inverted with Line at normal polarity.
C4	1 nF	> 5 V, ±10%, NP0	Improves the noise immunity of the amplifier and comparators. TI does not recommend to increase this value further.
C5	1 nF	> 5 V, ±10%, NP0	Improves the noise immunity of the amplifier. It can be increased up to 150 nF given R6 and R7 do not change. Always check for amplifier stability over-temperature when increasing this value.
C6	180 pF	> 5 V, ±10%, NP0	It helps keep the reference voltage buffer stable from high-frequency noise transients. TI does not recommend to increase this value further.
C7, C8, C9	1 nF	> 5 V, ±10%, NP0	These capacitors filter noise coupled to their respective digital pins.
C10	0.47 µF	> 5 V, ±10%, X7R	These capacitors help prevent noise coupling into the gate of the SCR.
C11	2 .2 nF	250 VAC, ±10%, X7R	Helps keep the SCR anode stable. Voltage rating dependent upon line voltage.
D1	N/A	600 V, 1 A	Provides line voltage rectification for AFE3010 VDD. Voltage rating dependent upon line voltage.
D2	N/A	1000 V, 1 A	Provides current rectification for SCR and solenoid. Voltage rating dependent upon line voltage.
D3	Red	Red LED	LED driven by ALARM to indicate initial passing of self-test on power up and self-test failure.
D4	N/A	600 V, 1 A	Prevents any current flowing from emitter to collector in Q1, which protects the AFE3010 from current injection during abnormal states of Q1.
Q1	400 V	400 V, 1 A	NPN transistor controlled by FT driver to perform periodic self-tests.
R1, R2, R3, R4	18.0 kΩ	5%, 0.5 W	Limit current for AFE3010 shunt regulator at VDD. Resistors are placed in two parallel pairs to ensure normal operation even if a resistor fails. One pair is placed above the bridge (D1) to limit current in event of a D1 failure. Power rating determined by line voltage and supply current.
R5	100 Ω	1%, 0.1 W	Limits current into NG_OUT pin during inductive kickback from driving 200-turn coil. Limiting the current will keep the internal ESD cells from turning on and potentially damaging the device. Thus, take caution when decreasing this value to improve N-G detection. To reduce R5 and protect AFE3010, a Schottky diode can be used at NG_OUT to clamp pin voltage during inductive kickback.
R6	75 Ω	1%, 0.1 W	Input resistor for the internal amplifier. R6 can be adjusted to improve N-G detection.
R7	36 kΩ	1%, 0.1 W	Feedback resistor for the internal amplifier. Sets the gain for ground fault signals. Thus, R7 can be adjusted to change the device trip point.

Table 5. Summary of Components in AFE3010 Typical Application (continued)

COMPONENT DESIGNATOR	COMPONENT VALUE	COMPONENT RATINGS	DESCRIPTION
R8	10.5 kΩ	1%, 0.5 W	Sets the level of fault current used in the periodic self-test when Q1 is turned on. The fault current should be greater than the trip point for successful detection and operation. The self-test will be hardest to pass when line connects to GFCI with reverse polarity and there is a small leakage current that is below the trip current. The worst-case power condition will be when a device cannot detect the self-test fault current and thus Q1 is on for a half-cycle of line.
R9	1.5 kΩ	5%, 0.1 W	Limits the output current of the ALARM driver. Using a higher R9 value will reduce supply current when ALARM is driving D3.
R10	560 Ω	5%, 0.1 W	Limits the output current of the SCR driver.
R11	51 kΩ	5%, 1/3 W	Limits the current into the SCR_TST pin when regulating to 20 V and sets internal biasing. The value of the resistor should not change from the recommendation when SEL = LOW. The lowest acceptable value is a 1% 49.9 kΩ. Given a 170-V peak line voltage, the average power rating required is calculated with [((170 V – 20 V)^2) /R11] / [2 × SQRT(2)].
R12	1 MΩ	5%, 0.1 W	Limits the current into PH pin.

WARNING

When evaluating this device, implement high-voltage safety precaution and procedures.

1. The first step in the design of a system with AFE3010 is to determine the correct transformer orientation and coil connections. The AFE3010 internal detection scheme requires the fault waveforms to have a specific polarity to the Hot-to-Neutral line voltage. The two rules the design must follow are:
   a. The amplifier output voltage (V_{OUT}) must be approximately 180° out of phase with the Hot-Neutral line voltage when line voltage connects to a GFCI unit with normal polarity. Thus, when line is connected to system with reverse polarity, the V_{OUT} signal must be in-phase with line voltage. The amplifier's polarity is determined by the value of C3, the connection of amplifier inputs (REF and FB) to the 1000-turn coil, and by the direction of the line wires through the transformer core. Refer to Figure 17 for the correct waveform. Note that normal line polarity means that the Hot and neutral nodes of the source are connected correctly to the Hot and Neutral input connectors of the system, respectively, which means the PH pin and D4 are also connected to Hot as shown in Figure 15.
   b. The N-G pulse on V_{OUT} when there is a N-G fault must look like Figure 18. The N-G pulse measured on V_{OUT} should first increase above 2.5 V and then decrease below 2.5 V. The second, downward pulse should be greater in amplitude and energy than the initial positive pulse. This rule should be true regardless of line polarity. N-G pulse polarity is determined by the connection of NG_OUT and GND pins to the 200-turn coil and by the polarity of the line wires through the transformer core.
2. Populate the board with the recommended values shown in Table 5.
3. Tune the amplifier's ground fault threshold (trip point).
   a. Set up the system with an adjustable Hot-to-ground (H-G) fault load and an ammeter in-series to measure the fault (or leakage) current.
   b. Adjust the fault load so that the ammeter reads < 3 mA RMS of fault current.
   c. Power off and then power on the system to reset any possible trips by the system.
   d. Slowly increase the fault current until the AFE3010 SCR driver is pulsed and trips the solenoid. Note the ammeter reading once the system trips.
   e. If the system trips too early (< 4.5 mA RMS), then disconnect the system from power and decrease R7.
   f. If the system trips too late (> 5.5 mA RMS), then disconnect the system from power and increase R7.
4. Tune the system's Neutral-to-ground (N-G) detection.
   a. Set up the system according to Figure 16. Note that this initial design process does not require testing N-G detection with H-G fault or load currents.

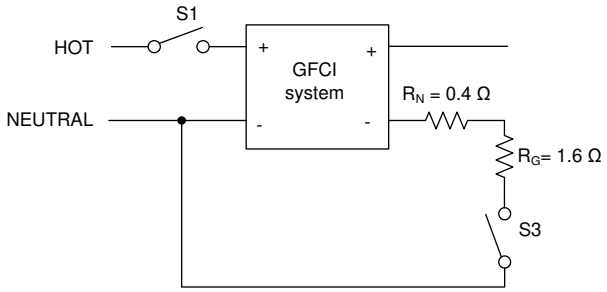


Figure 16. Neutral-to-Ground Detection Test Setup for AFE3010 Design Procedure

b. Choose the R_N and R_G pair that creates the largest total resistance, as this is the worst-case for the AFE3010's N-G detection. In this procedure, the total N-G resistance to test is 2 Ω.
c. Using the relays S1 and S3, switch in the N-G fault and check if the system trips. Note that either relay may be closed first.
d. If the system successfully trips, then re-test the detection over temperature.
e. If the system successfully detects N-G fault overtemperature, then the first-pass component optimization is complete.
f. If the system fails to detect the N-G, then consider the following component modifications:
    i. Adjust R6. Decreasing R6 has shown to increase the N-G pulse sensed by amplifier with minimal effect on amplifier gain.
    ii. Increase R7. The trip point must be checked again because the amplifier gain will increase.
    iii. Reduce the NG_OUT resistor R5. Note that there is a lower bound to the value of R5, depending on the impedance of the 200-turn coil. R5 helps limit current from any activated internal ESD cells during the inductive kickback on the NG_OUT pin. If R5 must be decreased, consider adding a Schottky diode at the NG_OUT pin to clamp the NG_OUT voltage above the Absolute Maximum Rating of –0.3 V.
    iv. Add a small capacitor from the REF pin to GND. Values between 100 pF and 300 pF are acceptable.

5. Successful operation of the AFE3010 can be seen with the successful passing of the internal self-tests. A successful self-test can be observed with the ALARM LED (D3) blinking once one second after device power up.
6. Perform the rest of the testing specified in the UL-943 standard.

8.2.3 Application Curves

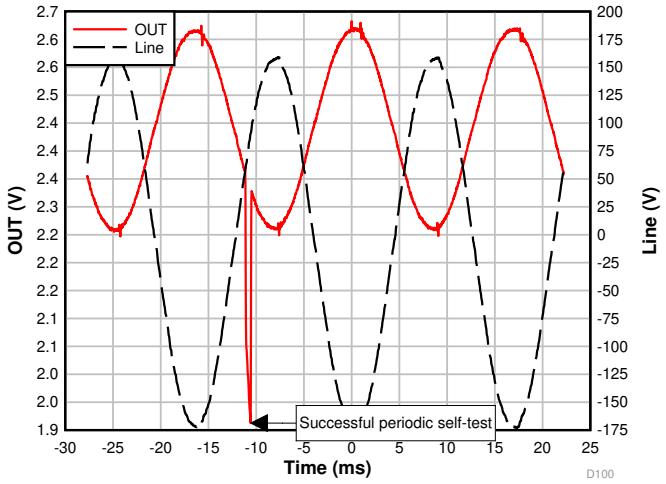


Figure 17. Amplifier Output During a 3.7-mA Ground Fault With Normal Line Polarity

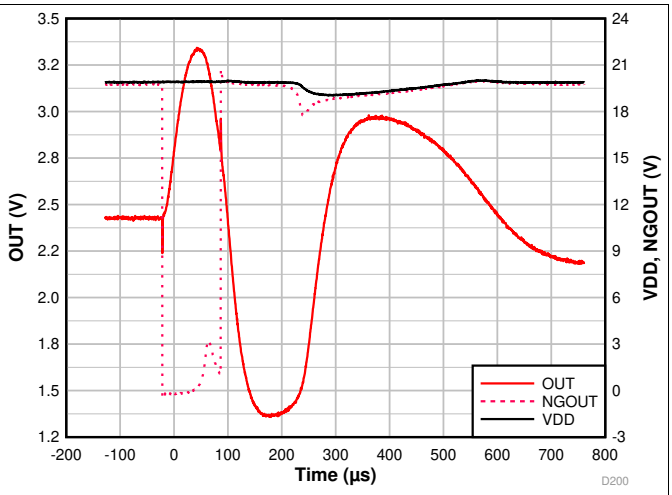


Figure 18. Neutral-Ground Pulse on V_{OUT} With 2-Ω N-G Fault. No Load or Fault Currents.

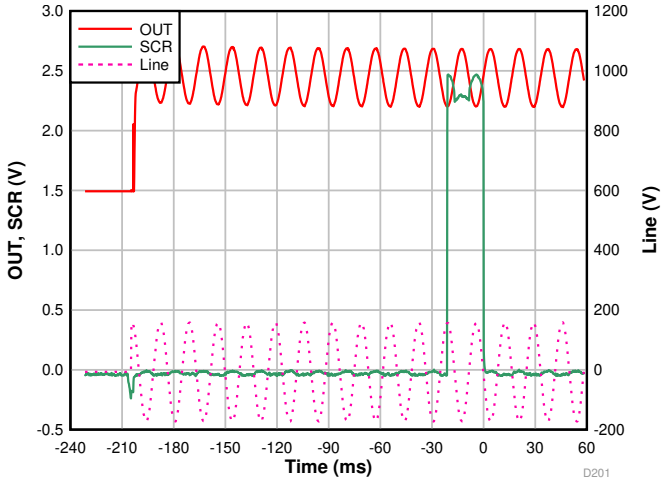


Figure 19. Device Trip to 5-mA RMS Ground Fault on Device Power Up

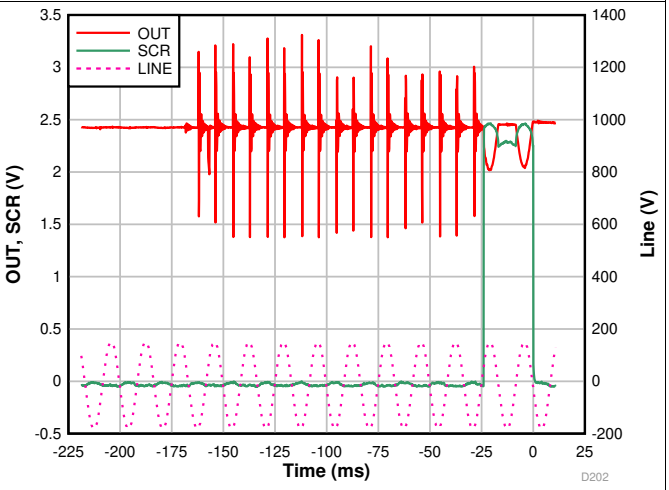


Figure 20. Device Trip to 2-Ω N-G Fault. No Load Or Fault Currents.

8.3 What to Do and What Not to Do

Do:

- Check that the system can pass its own periodic self-test before performing system testing and characterization.
- Make R8 small enough so the AFE3010 can pass a self-test even when there is some small leakage current and the line is connected with reverse polarity.
- Make R5 large enough so that the NG_OUT driver current does not burn or break the 200-turn coil.
- Make R5 large enough so that the NG_OUT pin voltage does not drop below –0.3 V or does not sink more 5 mA of current during inductive kickback.
- Always re-test the trip point and N-G detection whenever making changes to the system component values.
- Place filter capacitors as close a possible to the device pins, especially for the amplifier, VDD, PH, $\overline{\text{PTT}}$, and $\overline{\text{SW\_OPEN}}$ pins.

9 Power Supply Recommendations

It is important to choose proper resistors and capacitors for the VDD pins. Sufficient decoupling capacitance is required to keep the internal 20-V shunt regulator stable during events in which the AFE3010 is driving loads with the ALARM, SCR, or NG_OUT pins. The values recommended in the typical application schematic and Table 5 have shown to maintain a stable VDD even during events when diodes in D1 rectifier were shorted. Additionally, the VDD regulator maintained sufficient voltage even when one of the current limiting resistors (R1 through R4) was disconnected. As a general rule, do not let the VDD regulator drop below 8 V during board failure events, or else the device could reset. If the capacitance at VDD is too large, then the device takes longer to power up, which adds to trip times when device is powered up with a fault current. The recommended values shown in Table 5 have shown to yield power-up trip times compliant with the UL 943 standard.

The current-limiting resistors for VDD (R1 through R4) should have enough resistance to reduce power dissipation, but should not be large enough to affect power-on trip times. To determine the maximum total power rating needed by these resistors, calculate the maximum instantaneous supply current (I_{VDD}) needed by summing the maximum quiescent current and the maximum ALARM and SCR driver currents. The NG_OUT driver current has shown minimal effect on VDD regulation.

Place the decoupling capacitors as close as possible to the VDD pins to generate a short, low-impedance return current path to ground.

10 Layout

10.1 Layout Guidelines

The layout of the AFE3010 and its surrounding circuit is critical to maintaining performance and minimizing unwanted noise coupling. Follow these layout guidelines:

- Place all capacitors as close as possible to their respective pins or nodes.
- Route the signal traces from the 1000-turn coil to the amplifier as a differential pair.
- Provide low-impedance ground connections throughout the board, especially between the ground pin of the rectifier (D1) and the ground pin of the AFE3010.
- Connect the bottom AFE3010 thermal pad to board ground to help with noise immunity.

10.2 Layout Example

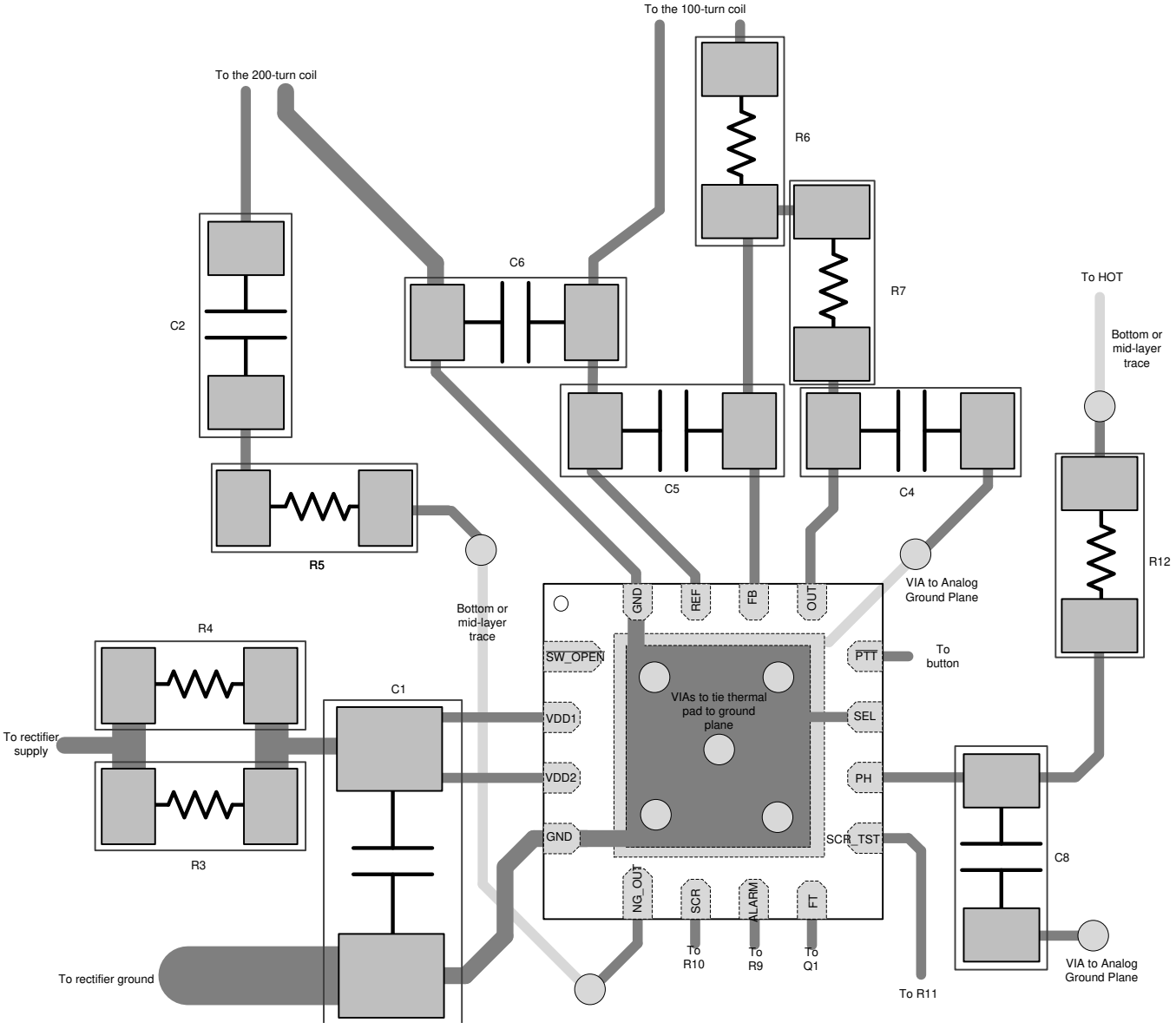


Figure 21. AFE3010 Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE3010AIRGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	A3010	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

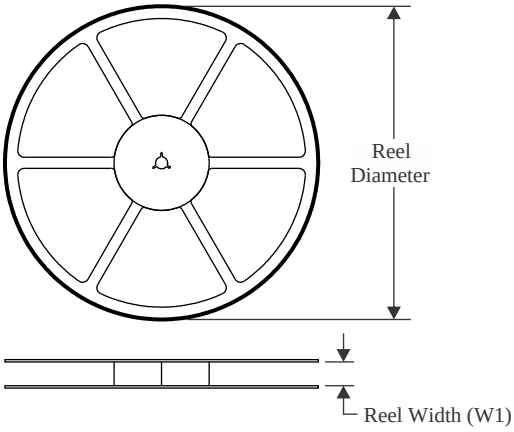
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

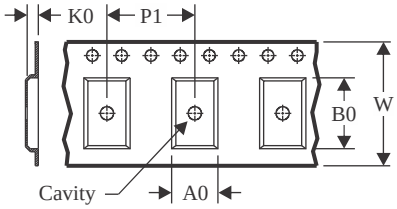
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

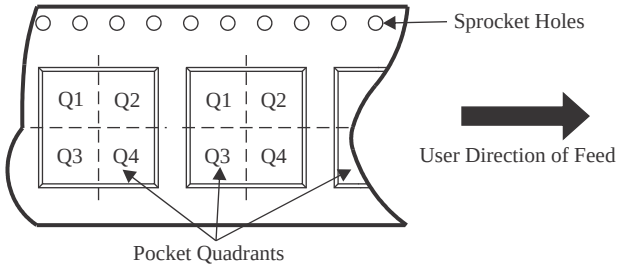


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

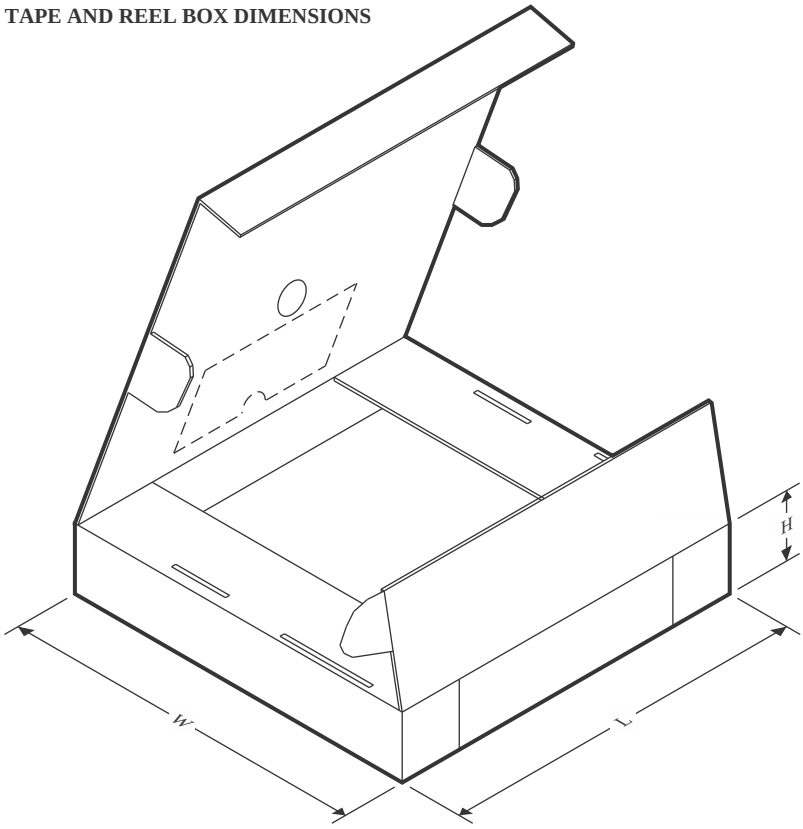
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE3010AIRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

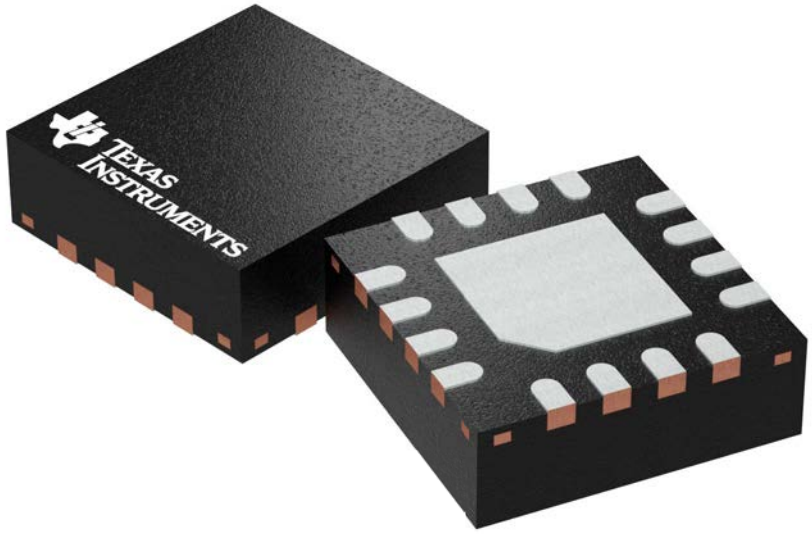


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE3010AIRGTR	VQFN	RGT	16	3000	367.0	367.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



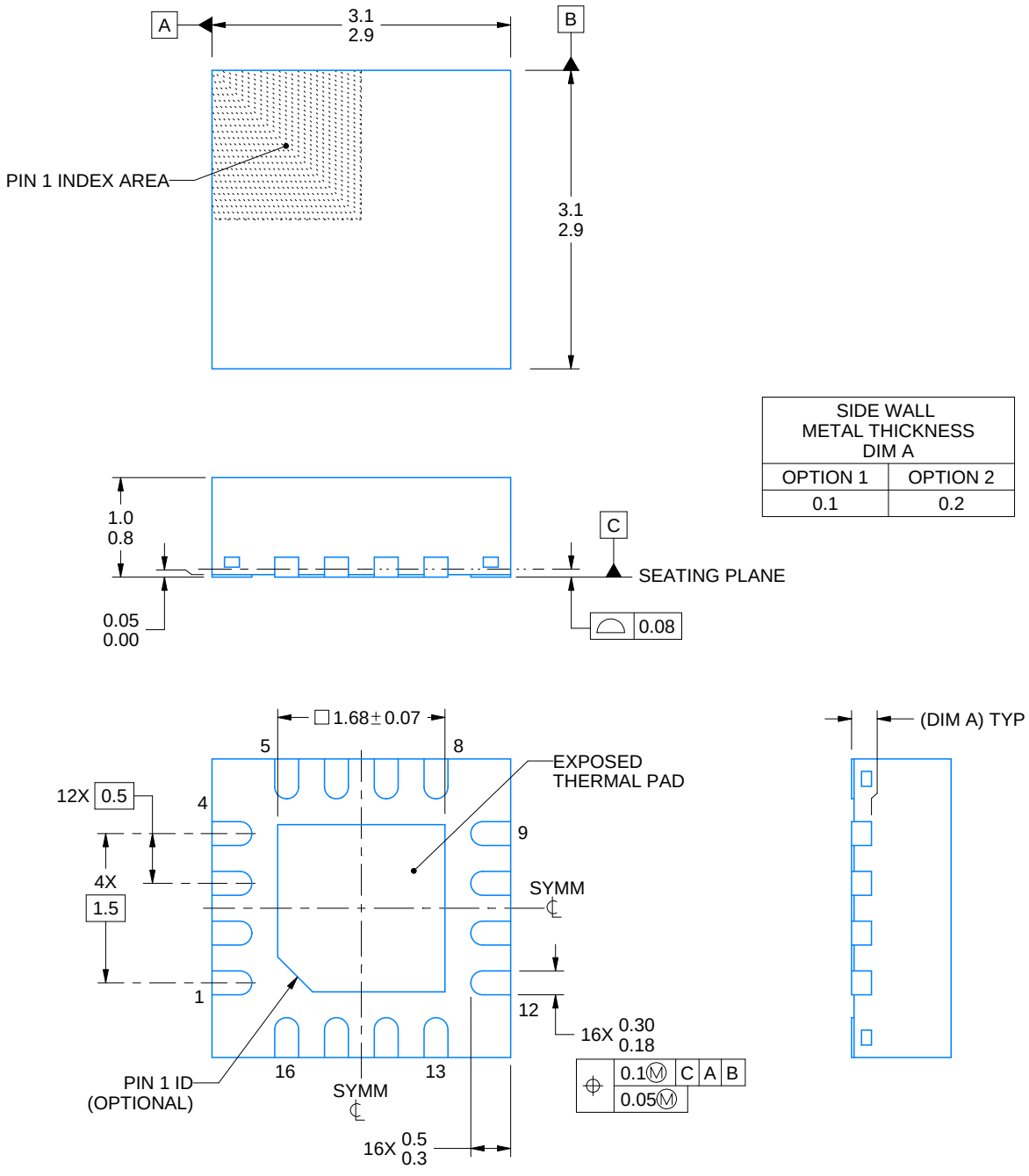
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

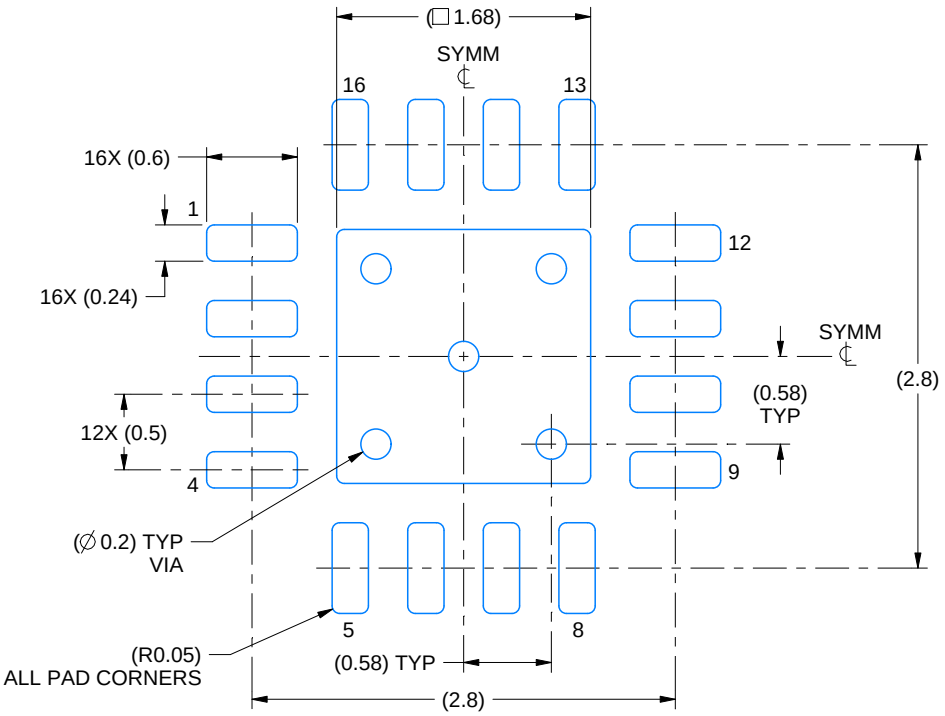
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

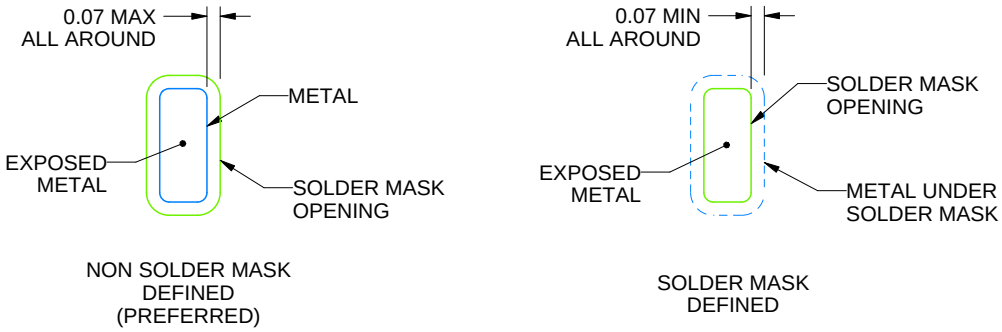


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

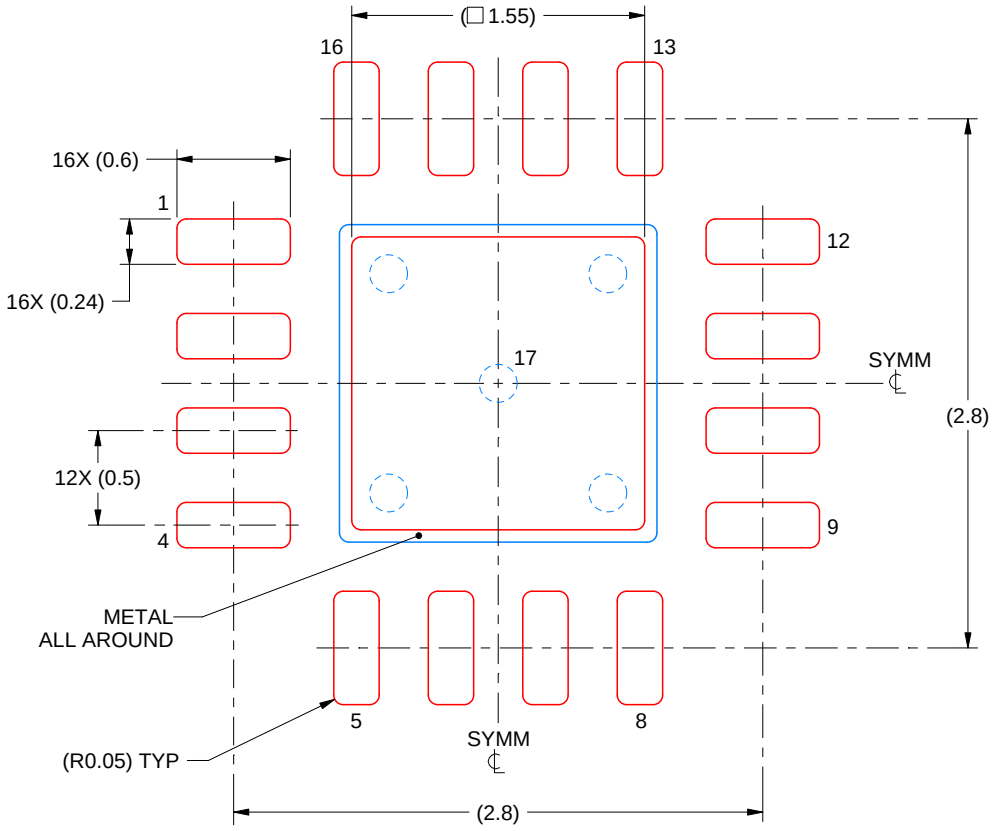


SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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