# AFE58JD28 16-Channel Ultrasound AFE with 102-mW/Channel Power, 0.8-nV/√Hz Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC, Digital Demodulator, JESD or LVDS Interface, and Passive CW Mixer

## 1 Features

- 16-Channel AFE for Ultrasound Applications:
  - Optimized Signal Chains for TGC and CW Modes
  - Four Programmable TGC Profiles
- Low-Noise Amplifier (LNA) With:
  - Programmable Gain: 21 dB, 18 dB, and 15 dB
  - Linear Input Signal Amplitude: 0.37 $V_{PP}$, 0.5 $V_{PP}$, and 0.71 $V_{PP}$
  - Active Termination
- Voltage-Controlled Attenuator (VCAT):
  - Attenuation Range: 0 dB–36 dB
- Programmable Gain Amplifier (PGA):
  - 18 dB–27 dB in Steps of 3 dB
- 3rd-Order, Linear-Phase, Low-Pass Filter (LPF):
  - Cutoff Frequency From 10 MHz to 30 MHz
- ADC Modes (Idle-Channel SNR):
  - 14-Bit, 65-MSPS Mode: 75-dBFS
  - 12-Bit, 80-MSPS Mode: 72-dBFS
- Optimized for Noise and Power:
  - TGC Mode: 102 mW/Ch at 0.8 nV/√Hz, 65-MSPS, 14-Bit Output
  - CW Mode: 63 mW/Ch
- Excellent Device-to-Device Gain Matching:
  - ±0.4 dB (Typical)
- Fast and Consistent Overload Recovery
- Continuous Wave (CW) Path With:
  - Low Close-In Phase Noise of –159 dBc/Hz at 1-kHz Frequency Offset off 2.5-MHz Carrier
  - Phase Resolution: λ / 16
  - Supports 16x and 8x CW Clocks
  - 12-dB Suppression of 3rd and 5th Harmonics
- Digital I/Q Demodulator:
  - Fractional Decimation Filter M = 1 to 63 With Increments of 0.25
  - Data Throughput Reduction After Decimation
  - On-Chip RAM With 32 Preset Profiles
- LVDS Interface With a Speed Up to 1 Gbps
- 5-Gbps JESD Interface:
  - JESD204B Subclass 0, 1, and 2
  - 2, 4, or 8 Channels per JESD Lane
- Small Package: 15-mm × 15-mm NFBGA-289

## 2 Applications

- Medical Ultrasound Imaging
- Nondestructive Evaluation Equipment
- Sonar Imaging Equipment

## 3 Description

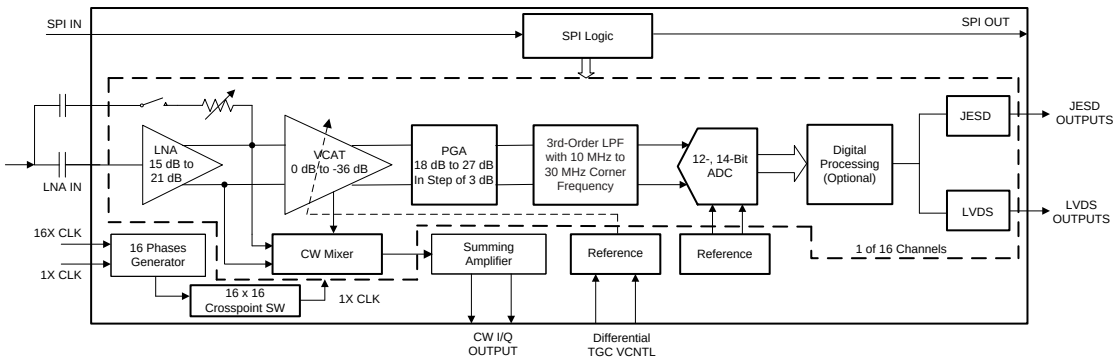
The AFE58JD28 device is a highly-integrated, analog front-end (AFE) solutions specifically designed for ultrasound systems where high performance, low power, and small size are required.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| AFE58JD28 | nFBGA (289) | 15.00 mm × 15.00 mm |

(1) For all available packages, see the package option addendum at the end of the datasheet.

**Simplified Block Diagram**



## 4 Description (continued)

The AFE58JD28 is an integrated AFE optimized for medical ultrasound application. The device is realized through a multichip module (MCM) with two dies: one voltage-controlled amplifier (VCA) die and one analog-to-digital converter (ADC) die. The VCA die has 16 channels that interface with the 16 channels of the ADC die.

Each channel in the VCA die can be configured in one of two modes: time gain compensation (TGC) mode or continuous wave (CW) mode. In TGC mode, each channel includes a low-noise amplifier (LNA), a voltage-controlled attenuator (VCAT), a programmable gain amplifier (PGA), and a third-order, low-pass filter (LPF). The LNA is programmable in gains of 21 dB, 18 dB, or 15 dB. The LNA also supports active termination. The VCAT supports an attenuation range of 0 dB to 36 dB, with analog voltage control for the attenuation. The PGA provides gain options from 18 dB to 27 dB in steps of 3 dB. The LPF cutoff frequency can be set between 10 MHz and 30 MHz to support ultrasound applications with different frequencies. In CW mode, the output of the LNA goes to a low-power passive mixer with 16 selectable phase delays followed by a summing amplifier with a band-pass filter. Different phase delays can be applied to each analog input signal to perform an on-chip beamforming operation. A harmonic filter in the CW mixer suppresses the third and fifth harmonic to enhance the sensitivity of the CW Doppler measurement.

The 16 channels of the ADC die can be configured to operate with a resolution of 14 bits or 12 bits. The ADC resolution can be traded off with conversion rate, and can operate at maximum speeds of 65 MSPS and 80 MSPS at 14-bit and 12-bit resolution, respectively. The ADC is designed to scale its power with sampling rate. The output interface of the ADC comes out through a low-voltage differential signaling (LVDS) that can easily interface with low-cost field-programmable gate arrays (FPGAs).

The AFE58JD28 additionally includes a digital demodulator and JESD204B data packing blocks. The digital in-phase and quadrature (I/Q) demodulator with programmable decimation filters accelerates computationally-intensive algorithms at low power. The device also supports an optional JESD204B interface that runs up to 5 Gbps and further reduces the circuit-board routing challenges in high-channel count systems.

The device also allows various power and noise combinations to be selected for optimizing system performance. Therefore, these devices are suitable ultrasound AFE solutions for systems with strict battery-life requirements.

The device is available in a 15-mm × 15-mm NFBGA-289 package and is pin-compatible with the AFE5818 and AFE5816 family.

# 5 Device and Documentation Support

## 5.1 Documentation Support

### 5.1.1 Related Documentation

For related documentation see the following:

- *AFE5818 16-Channel, Ultrasound, Analog Front-End with 140-mW/Channel Power, 0.75-nV/√Hz Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC, and Passive CW Mixer*
- *AFE5816 16-Channel Ultrasound AFE with 90-mW/Channel Power, 1-nV/√Hz Noise, 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC and Passive CW Mixer*
- *AFE58JD18 16-Channel, Ultrasound AFE with 14-Bit, 65-MSPS or 12-Bit, 80-MSPS ADC, Passive CW Mixer, I/Q Demodulator, and LVDS, JESD204B Outputs*
- *TLV5626 2.7-V to 5.5-V Low-Power Dual 8-Bit Digital-to-Analog Converter With Internal Reference and Power Down*
- *DAC7821 12-Bit, Parallel Input, Multiplying Digital-to-Analog Converter*
- *THS413x High-Speed, Low-Noise, Fully-Differential I/O Amplifiers*
- *OPA1632 High-Performance, Fully-Differential Audio Operational Amplifier*
- *Wideband Differential Transimpedance DAC Output*
- *LMK0482x Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs*
- *CDCM7005 3.3-V High Performance Clock Synchronizer and Jitter Cleaner*
- *CDCE72010 Ten Output High Performance Clock Synchronizer, Jitter Cleaner, and Clock Distributor*
- *OPA2x11 1.1-nv/√Hz Noise, Low Power, Precision Operational Amplifier*
- *ADS8413 16-Bit, 2-MSPS, LVDS Serial Interface, SAR Analog-to-Digital Converter*
- *ADS8472 16-Bit, 1-MSPS, Pseudo-Bipolar, Fully Differential Input, Micropower Sampling Analog-to-Digital Converter With Parallel Interface, Reference*
- *Clocking High-Speed Data Converters* Technical Brief
- *ISO724x High-Speed, Quad-Channel Digital Isolators*
- *SN74AUP1T04 Low Power, 1.8/2.5/3.3-V Input, 3.3-V CMOS Output, Single Inverter Gate*
- *MicroStar BGA Packaging Reference Guide*

## 5.2 Trademarks

All trademarks are the property of their respective owners.

## 5.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 5.4 Glossary

SLYZ022 — *TI Glossary*.

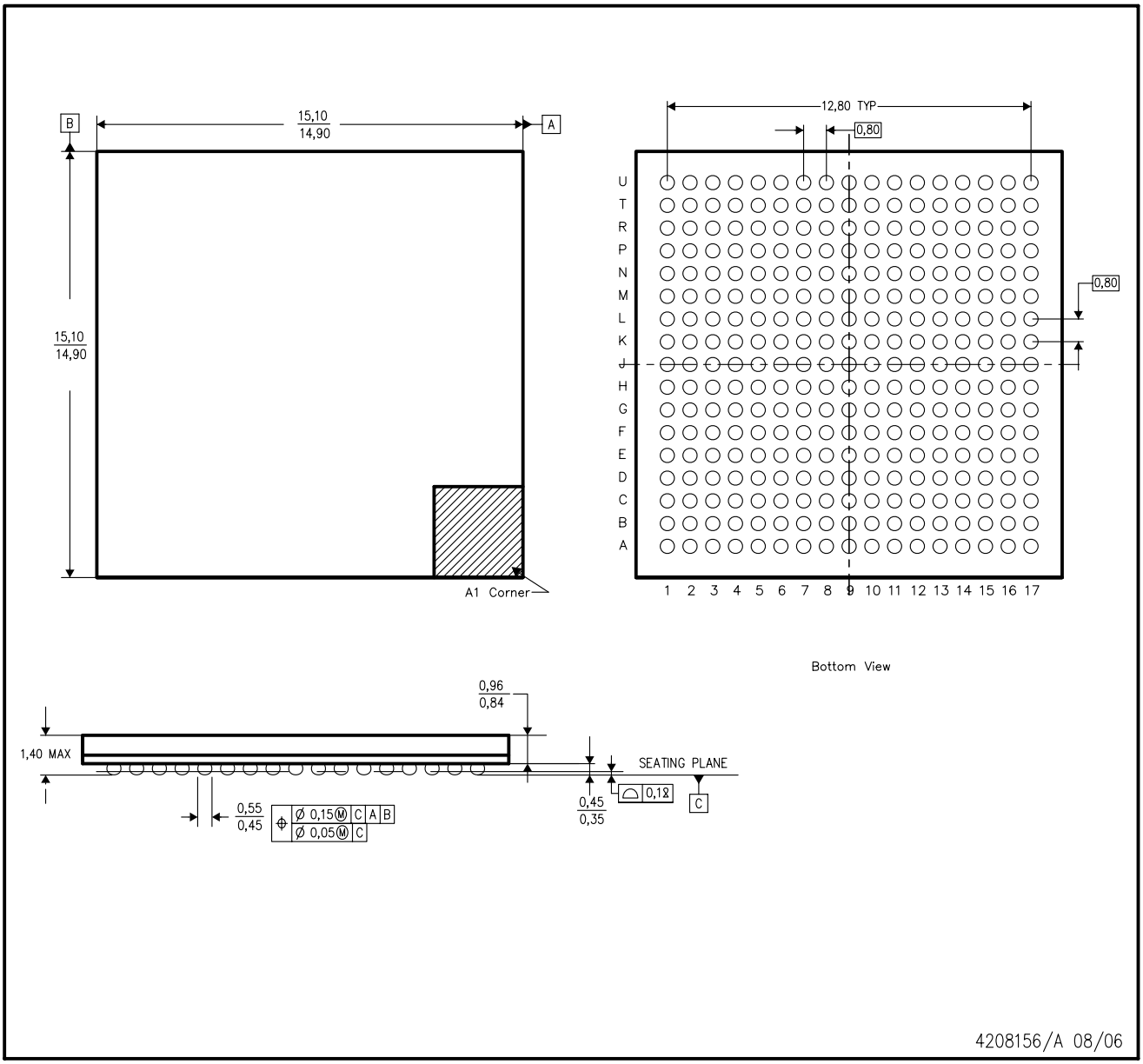
This glossary lists and explains terms, acronyms, and definitions.

# 6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## MECHANICAL DATA

ZAV (S–PBGA–N289) PLASTIC BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AFE58JD28ZAV | ACTIVE | NFBGA | ZAV | 289 | 126 | RoHS & Green | Call TI \| SNAGCU | Level-3-260C-168 HR | -40 to 85 | AFE58JD28 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

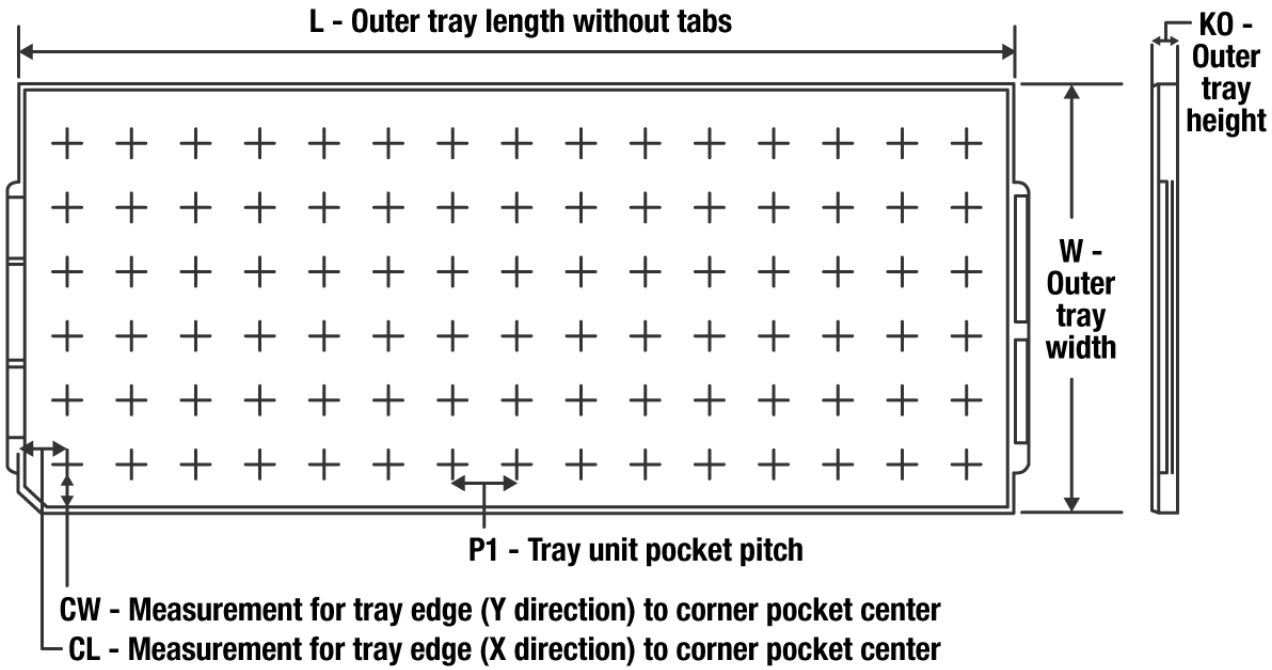
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AFE58JD28ZAV | ZAV | NFBGA | 289 | 126 | 7 X 18 | 150 | 315 | 135.9 | 7620 | 17.2 | 11.3 | 16.35 |

# IMPORTANT NOTICE AND DISCLAIMER

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