TEXAS INSTRUMENTS

Data sheet acquired from Harris Semiconductor
SCHS060C – Revised September 2003

CD4085B Types

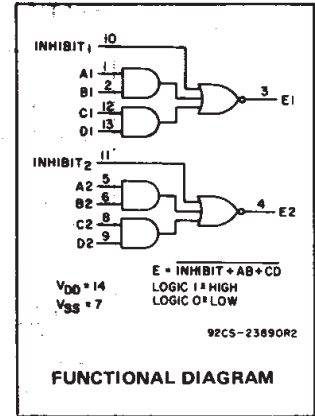## CMOS Dual 2-Wide 2-Input AND-OR-INVERT Gate

High-Voltage Types (20-Volt Rating)

■ CD4085 contains a pair of AND-OR-INVERT gates, each consisting of two 2-input AND gates driving a 3-input NOR gate. Individual inhibit controls are provided for both A-O-I gates.

The CD4085B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Features:

■ Medium-speed operation — t_{PHL} = 90 ns; t_{PLH} = 125 ns (typ.) at 10 V
■ Individual inhibit controls
■ Standardized symmetrical output characteristics
■ 100% tested for quiescent current at 20 V
■ Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
■ Noise margin (over full package-temperature range):
   1 V at V_{DD} = 5 V
   2 V at V_{DD} = 10 V
   2.5 V at V_{DD} = 15 V
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

$E = \overline{INHIBIT + AB + CD}$
LOGIC I = HIGH
LOGIC 0 = LOW

V_{DD} = 14
V_{SS} = 7

92CS-23690R2

FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
   Voltages referenced to V_{SS} Terminal) .... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
   For T_A = -55°C to +100°C 500mW
   For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
   FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) .... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
   At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C
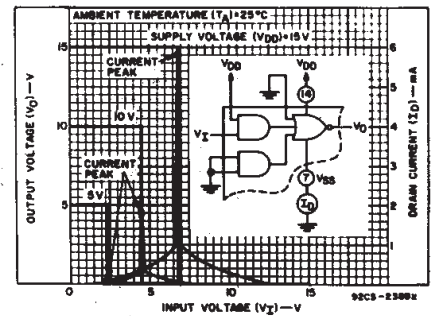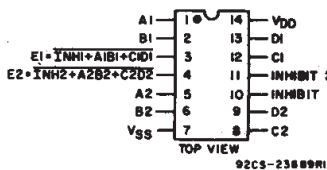

Fig. 1 — Typical voltage and current transfer characteristics.
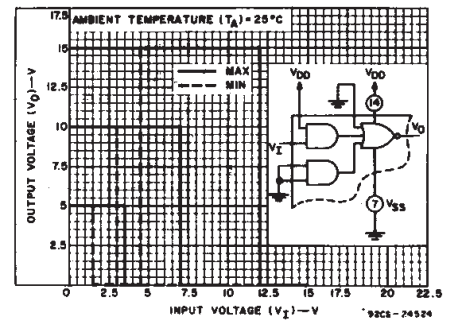
Fig. 2 — Min. and max. voltage transfer characteristics.

RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)	3	18	V

AI — 1   14 — V_{DD}
BI — 2   13 — DI
$E1 = \overline{INH1+A1B1+C1D1}$ — 3   12 — CI
$E2 = \overline{INH2+A2B2+C2D2}$ — 4   11 — INHIBIT 2
A2 — 5   10 — INHIBIT 1
B2 — 6   9 — D2
V_{SS} — 7   8 — C2
TOP VIEW
92CS-23889R1

Terminal Assignment

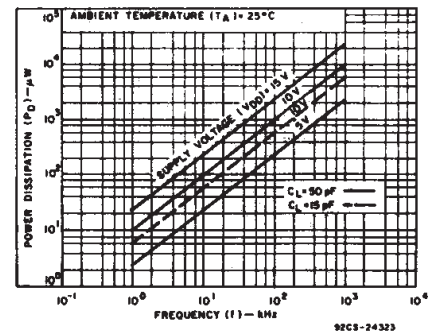

Fig. 3 — Typical power dissipation vs. frequency.

COMMERCIAL CMOS
HIGH VOLTAGE ICs

3

STATIC ELECTRICAL CHARACTERISTICS

| CHARAC-TERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current I_{DD} Max.	–	0,5	5	1	1	30	30	–	0.02	1	μA
	–	0,10	10	2	2	60	60	–	0.02	2	
	–	0,15	15	4	4	120	120	–	0.02	4	
	–	0,20	20	20	20	600	600	–	0.04	20	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current, I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA
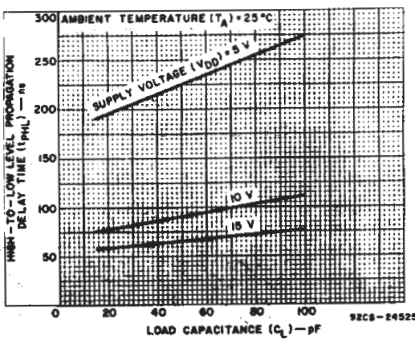
Fig. 4 – Typical data high-to-low level propagation delay time vs. load capacitance.
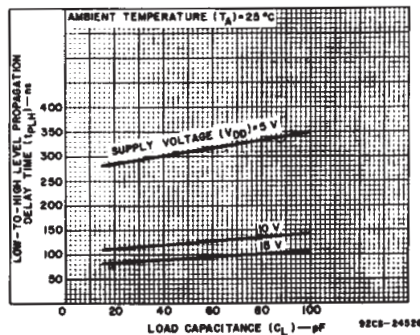

Fig. 5 – Typical data low-to-high level propagation delay time vs. load capacitance.
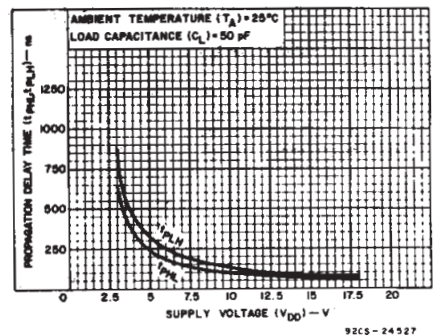

Fig. 6 – Typical data propagation delay time vs. supply voltage.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 KΩ

| CHARACTERISTIC	CONDITIONS V_{DD} V	LIMITS Typ.	LIMITS Max.	UNITS
Propagation Delay Time (Data): High-to-Low Level, t_{PHL}	5	225	450	ns
	10	90	180	
	15	65	130	
Low-to-High Level, t_{PLH}	5	310	620	ns
	10	125	250	
	15	90	180	
Propagation Delay Time (Inhibit): High-to-Low Level, t_{PHL}	5	150	300	ns
	10	60	120	
	15	40	80	
Low-to-High Level, t_{PLH}	5	250	500	ns
	10	100	200	
	15	70	140	
Transition Time, t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF
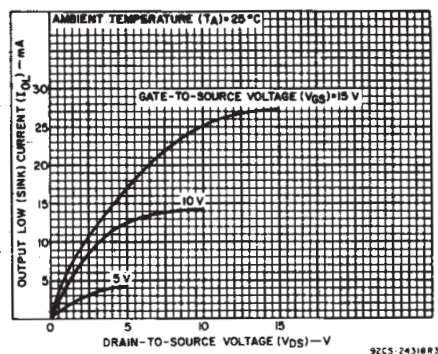
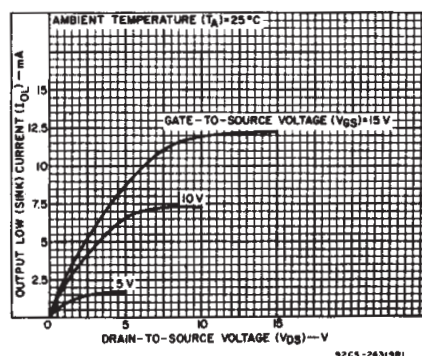Fig. 7 — Typical output low (sink) current characteristics.

Fig. 8 — Minimum output low (sink) current characteristics.
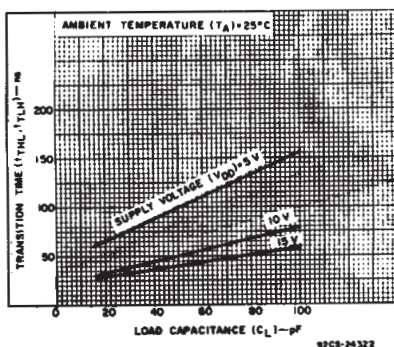

Fig. 9 — Typical transition time vs. load capacitance.

Fig. 10 — Typical output high (source) current characteristics.
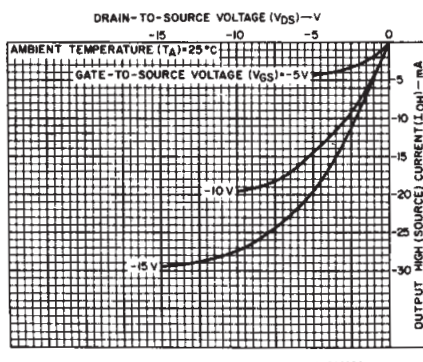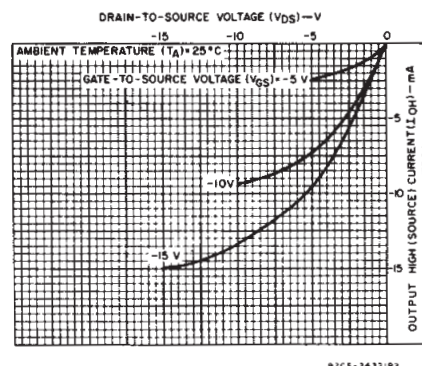

Fig. 11 — Minimum output high (source) current characteristics.
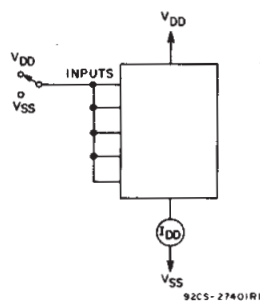
Fig. 12 — Quiescent device current test circuit.
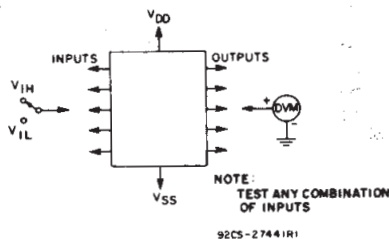
Fig. 13 — Input voltage test circuit.

NOTE:
MEASURE INPUTS SEQUENTIALLY, TO BOTH V_{DD} AND V_{SS}. CONNECT ALL UNUSED INPUTS TO EITHER V_{DD} OR V_{SS}.

Fig. 14 — Input current test circuit.

COMMERCIAL CMOS HIGH VOLTAGE ICs

3

Fig. 15 — CD4085 schematic diagram.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

92CS-32204

Dimensions and Pad Layout for CD4085BH.

PACKAGING INFORMATION

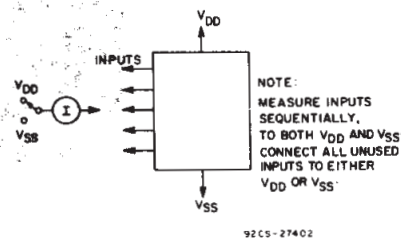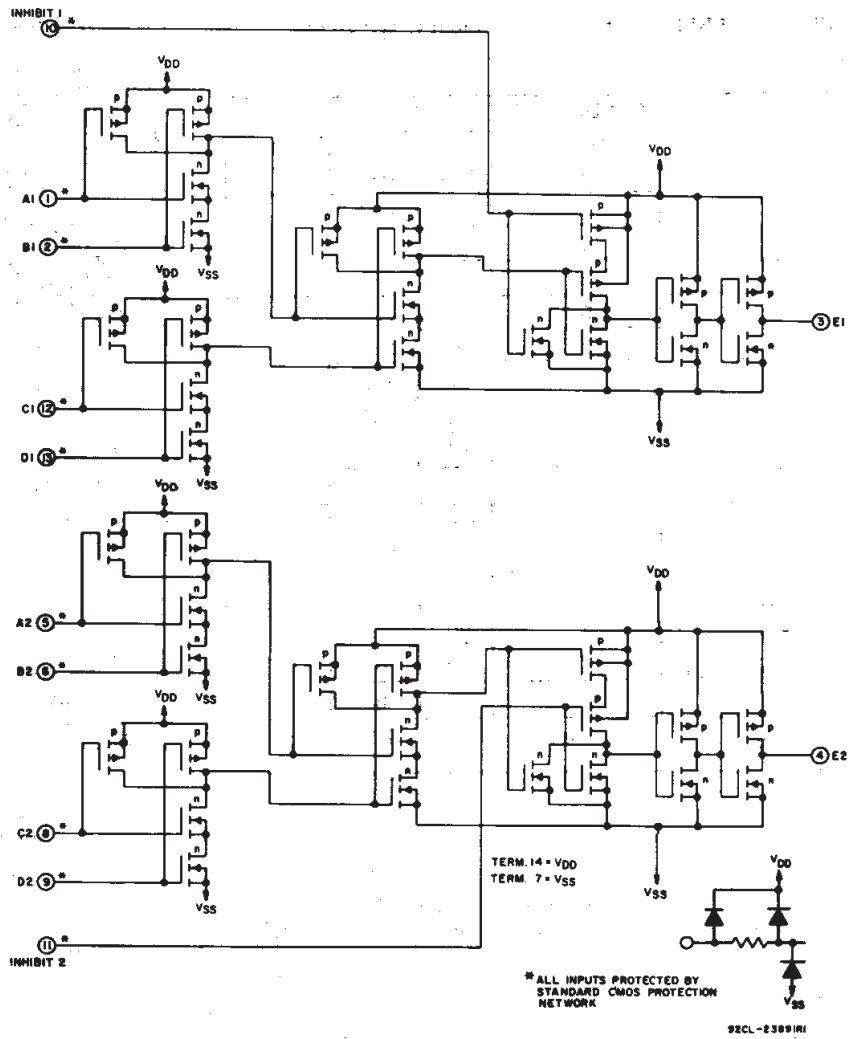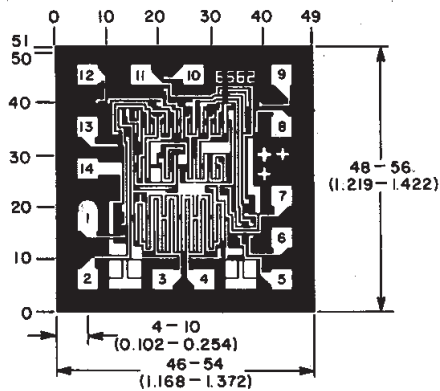| Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4085BE	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD4085BE	Samples
CD4085BF	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4085BF	Samples
CD4085BF3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD4085BF3A	Samples
CD4085BM	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4085BM	Samples
CD4085BPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM085B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD4085B, CD4085B-MIL :

- Catalog : CD4085B

- Military : CD4085B-MIL

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

Reel Diameter

Reel Width (W1)

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

| Q1 | Q2 |
| Q3 | Q4 |

Sprocket Holes

User Direction of Feed

Pocket Quadrants

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4085BPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4085BPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE

T - Tube height

L - Tube length

W - Tube width

B - Alignment groove width

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD4085BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4085BE	N	PDIP	14	25	506	13.97	11230	4.32
CD4085BM	D	SOIC	14	50	506.6	8	3940	4.32

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

TEXAS INSTRUMENTS

PIN 1 ID
(OPTIONAL)

A

12X .100
[2.54]

1

14

7

8

.754-.785
[19.15-19.94]

B

.245-.283
[6.22-7.19]

4X .005 MIN
[0.13]

.015-.060   TYP
[0.38-1.52]

14X .045-.065
[1.15-1.65]

14X .014-.026
[0.36-0.66]

⊕ .010 [0.25] C A B

.2 MAX TYP
[5.08]

.13 MIN TYP
[3.3]

C

SEATING PLANE

.308-.314
[7.83-7.97]
AT GAGE PLANE

.015
[0.38]

GAGE PLANE

0°-15°
TYP

14X .008-.014
[0.2-0.36]

4214771/A   05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

(.300) TYP
[7.62]

SEE DETAIL A

SEE DETAIL B

1

14

12X (.100)
[2.54]

SYMM
₵

14X (∅ .039)
[1]

7

8

SYMM
₵

LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

.002 MAX
[0.05]
ALL AROUND

(.063)
[1.6]

SOLDER MASK
OPENING

METAL

(R.002) TYP
[0.05]

DETAIL A
SCALE: 15X

METAL

(∅ .063)
[1.6]

SOLDER MASK
OPENING

.002 MAX
[0.05]
ALL AROUND

DETAIL B
13X, SCALE: 15X

4214771/A   05/2017

N (R−PDIP−T)**

16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14)   △D

0.045 (1,14)
0.030 (0,76)   △D

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.010 (0,25) NOM

0.125 (3,18) MIN

0.100 (2,54)

0.430 (10,92) MAX

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option   △D

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         △C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS INSTRUMENTS
www.ti.com

SEATING PLANE

6.6
6.2 TYP

A

PIN 1 INDEX AREA

C

□ 0.1 C

1

14

12X 0.65

5.1
4.9
NOTE 3

2X

3.9

7

8

4X (0° -12°)

14X 0.30
0.17

B

4.5
4.3
NOTE 4

⊕ 0.1 Ⓜ C A B

1.2 MAX

SEE DETAIL A

(0.15) TYP

0.25
GAGE PLANE

0.15
0.05

0° -8°

0.75
0.50

DETAIL A
TYPICAL

4220202/B   12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

14X (1.5)

14X (0.45)

1

SYMM

(R0.05) TYP

14

SYMM

12X (0.65)

7

8

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220202/B   12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

14X (1.5)

SYMM

(R0.05) TYP

1

14X (0.45)

14

SYMM

12X (0.65)

7

8

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B   12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

$\frac{6.2}{5.8}$ TYP

A

PIN 1 ID
AREA

1

14

12X [1.27]

$\frac{8.75}{8.55}$
NOTE 3

2X
[7.62]

7

8

14X $\frac{0.51}{0.31}$

B

$\frac{4.0}{3.8}$
NOTE 4

⊕ | 0.25Ⓜ | C | A | B

C

SEATING PLANE

⌓ | 0.1 | C

1.75 MAX

SEE DETAIL A

$\frac{0.25}{0.13}$ TYP

[0.25]
GAGE PLANE

0° - 8°

$\frac{1.27}{0.40}$

$\frac{0.25}{0.10}$

DETAIL A
TYPICAL

4220718/A   09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

TEXAS
INSTRUMENTS
www.ti.com

14X (1.55)

1

14X (0.6)

12X (1.27)

SYMM

14

SYMM

7

8

(R0.05)
TYP

(5.4)

LAND PATTERN EXAMPLE
SCALE:8X

SOLDER MASK
OPENING

METAL

0.07 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220718/A   09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A   09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated