

**High-Speed CMOS Logic  
9-Bit Odd/Even Parity Generator/Checker**

**Features**

- Typical Propagation Delay = 17ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^{\circ}C$
- Replaces LS180 Types
- Easily Cascadable
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^{\circ}C$  to  $125^{\circ}C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

**Description**

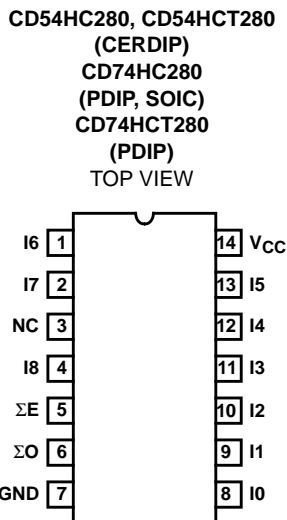
The 'HC280 and 'HCT280 are 9-bit odd/even parity, generator checker devices. Both even and odd parity outputs are available for checking or generating parity for words up to nine bits long. Even parity is indicated ( $\Sigma E$  output is high) when an even number of data inputs is high. Odd parity is indicated ( $\Sigma O$  output is high) when an odd number of data inputs is high. Parity checking for words larger than 9 bits can be accomplished by tying the  $\Sigma E$  output to any input of an additional HC/HCT280 parity checker.

**Ordering Information**

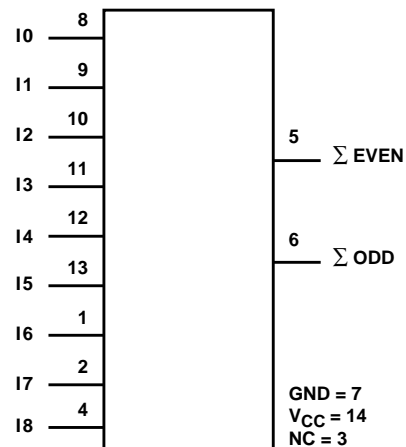
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC280F3A	-55 to 125	14 Ld CERDIP
CD54HCT280F3A	-55 to 125	14 Ld CERDIP
CD74HC280E	-55 to 125	14 Ld PDIP
CD74HC280MT	-55 to 125	14 Ld SOIC
CD74HC280M96	-55 to 125	14 Ld SOIC
CD74HCT280E	-55 to 125	14 Ld PDIP

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

**Pinout**



**Functional Diagram**



# CD54HC280, CD74HC280, CD54HCT280, CD74HCT280

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current, per Output, $I_O$	
For $-0.5V < V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note1)	$\theta_{JA}$ ( $^{\circ}C/W$ )
E (PDIP) Package .....	80
M (SOIC) Package .....	86
Maximum Junction Temperature .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$ (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range, $T_A$ .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

1. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS	
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
<b>HC TYPES</b>													
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-4	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	4	4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$	
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	-	8	-	80	-	160	$\mu A$	

**CD54HC280, CD74HC280, CD54HCT280, CD74HCT280**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	I <sub>O</sub> (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> to GND	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 2)	V <sub>CC</sub> -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

2. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

INPUT	UNIT LOADS
All	1

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

**Switching Specifications** Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
<b>HC TYPES</b>								
Propagation Delay, Any Input to ΣO	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	200	250	300	ns
			4.5	-	40	50	60	ns
			6	-	34	43	51	ns
		C <sub>L</sub> = 15pF	5	17	-	-	-	ns
Propagation Delay, Any Input to ΣE	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	200	250	300	ns
			4.5	-	40	50	60	ns
			6	-	34	43	51	ns
		C <sub>L</sub> = 15pF	5	17	-	-	-	ns

**CD54HC280, CD74HC280, CD54HCT280, CD74HCT280**

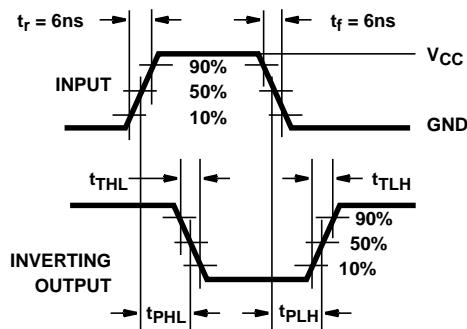
**Switching Specifications** Input  $t_r, t_f = 6\text{ns}$  (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	2	-	75	95	110	ns
			4.5	-	15	19	22	ns
			6	-	13	16	19	ns
Input Capacitance	$C_I$	-	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 3, 4)	$C_{PD}$	-	5	58	-	-	-	pF
<b>HCT TYPES</b>								
Propagation Delay, Any Input to $\Sigma O$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	45	56	68	ns
		$C_L = 15\text{pF}$	5	19	-	-	-	ns
Propagation Delay, Any Input to $\Sigma E$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	42	53	63	ns
		$C_L = 15\text{pF}$	5	18	-	-	-	ns
Output Transition Time	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	15	19	22	ns
Input Capacitance	$C_{IN}$	-	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 3, 4)	$C_{PD}$	-	5	58	-	-	-	pF

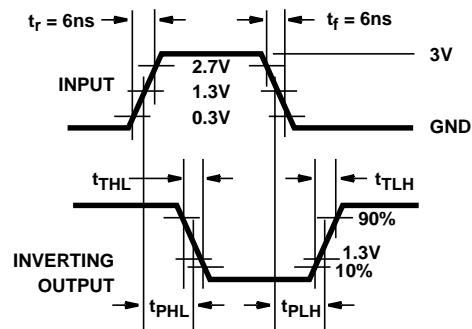
**NOTES:**

- $C_{PD}$  is used to determine the dynamic power consumption, per package.
- $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = Input Frequency,  $f_o$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

**Test Circuits and Waveforms**



**FIGURE 1. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**



**FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
8607701CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8607701CA CD54HC280F3A	<a href="#">Samples</a>
CD54HC280F3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8607701CA CD54HC280F3A	<a href="#">Samples</a>
CD54HCT280F3A	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT280F3A	<a href="#">Samples</a>
CD74HC280E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC280E	<a href="#">Samples</a>
CD74HC280M96	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC280M	<a href="#">Samples</a>
CD74HC280MT	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-55 to 125	HC280M	
CD74HCT280E	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT280E	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HC280, CD54HCT280, CD74HC280, CD74HCT280 :**

- Catalog : [CD74HC280](#), [CD74HCT280](#)
- Military : [CD54HC280](#), [CD54HCT280](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC280M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC280M96	SOIC	D	14	2500	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC280E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC280E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT280E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT280E	N	PDIP	14	25	506	13.97	11230	4.32

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

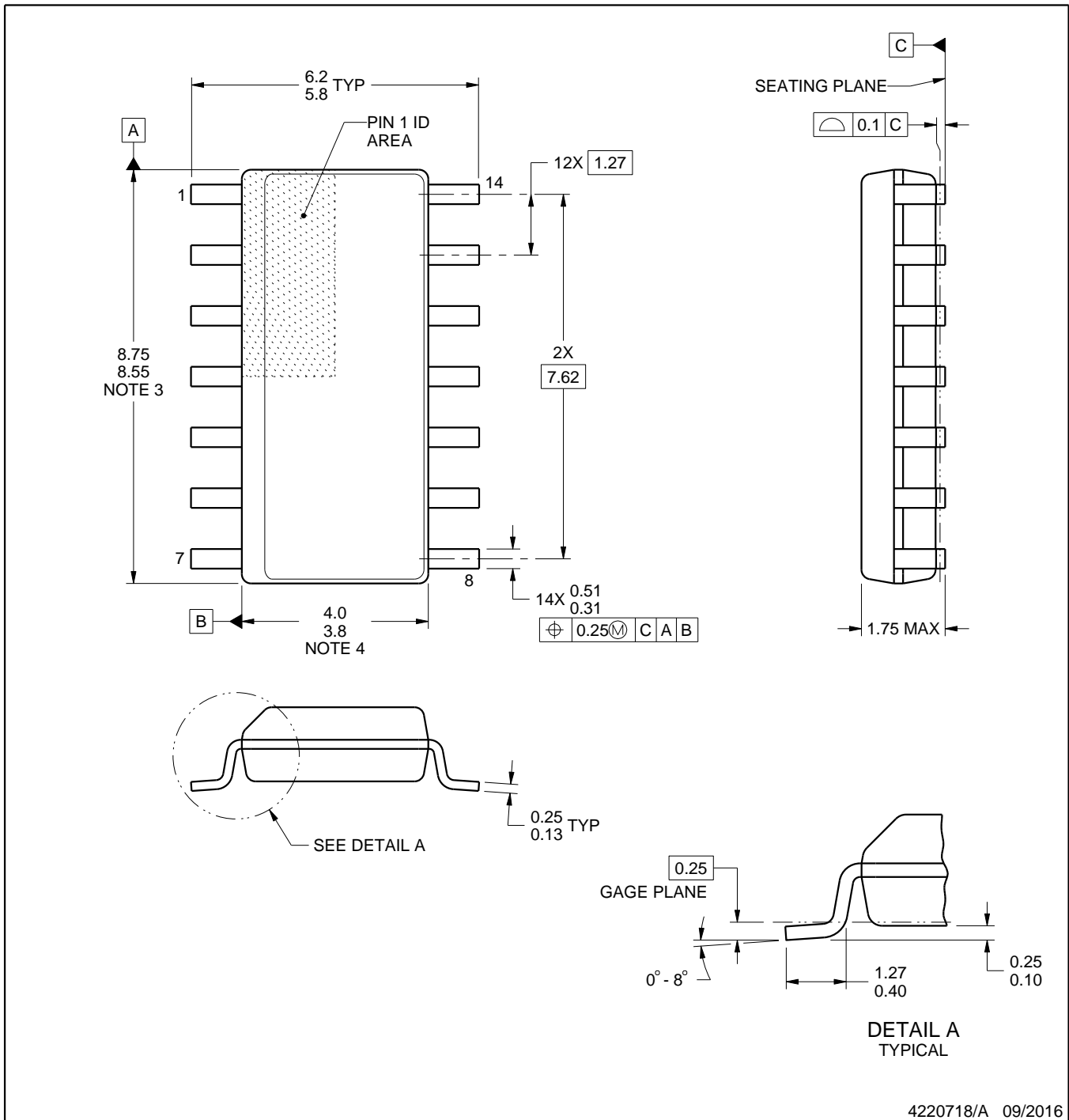
D0014A



# PACKAGE OUTLINE

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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