Dual 1:8 Low Additive Jitter LVDS Buffer

Check for Samples: CDCLVD2108

FEATURES

- **Dual 1:8 Differential Buffer**
- **Low Additive Jitter <300 fs RMS in 10 kHz to 20 MHz**
- **Low Within Bank Output Skew of 50 ps (Max)**
- **Universal Inputs Accept LVDS, LVPECL, LVCMOS**
- **One Input Dedicated for Eight Outputs**
- **Total of 16 LVDS Outputs, ANSI EIA/TIA-644A Standard Compatible**
- **Clock Frequency up to 800 MHz**
- **2.375–2.625V Device Power Supply**
- **LVDS Reference Voltage, V_{AC_REF}, Available for Capacitive Coupled Inputs**
- **Industrial Temperature Range –40°C to 85°C**
- **Packaged in 7mm × 7mm 48-Pin QFN (RGZ)**
- **ESD Protection Exceeds 3 kV HBM, 1 kV CDM**

APPLICATIONS

- **Telecommunications/Networking**
- **Medical Imaging**
- **Test and Measurement Equipment**
- **Wireless Communications**
- **General Purpose Clocking**

DESCRIPTION

The CDCLVD2108 clock buffer distributes two clock inputs (IN0, IN1) to a total of 16 pairs of differential LVDS clock outputs (OUT0, OUT15). Each buffer block consists of one input and 8 LVDS outputs. The inputs can either be LVDS, LVPECL, or LVCMOS.

The CDCLVD2108 is specifically designed for driving 50-Ω transmission lines. In case of driving the inputs in single ended mode, the appropriate bias voltage (V_{AC_REF}) should be applied to the unused negative input pin.

Using the control pin (EN) outputs can be either disabled or enabled. If the EN pin is left open all outputs are active, if switched to a logical '0' all outputs are disabled (static logical 0), if switched to a logical '1', OUT (8..15) are switched off and OUT (0..7) are active. The part supports a fail safe function. It incorporates an input hysteresis, which prevents random oscillation of the outputs in absence of an input signal.

The device operates in 2.5V supply environment and is characterized from –40°C to 85°C (ambient temperature). The CDCLVD2108 is packaged in small 48-pin, 7-mm x 7-mm QFN package.

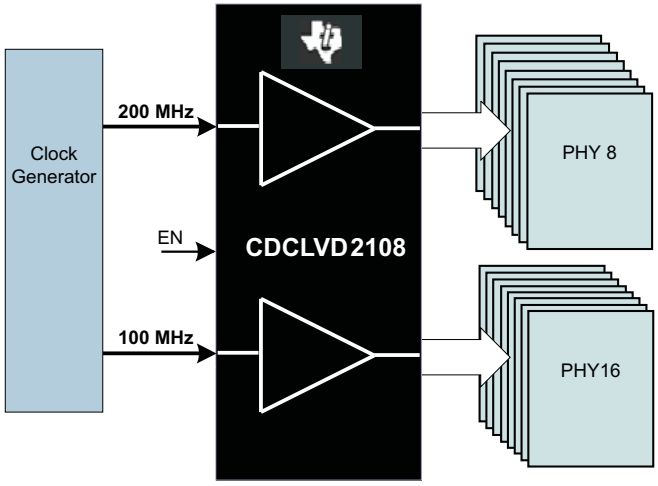


Figure 1. Application Example

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

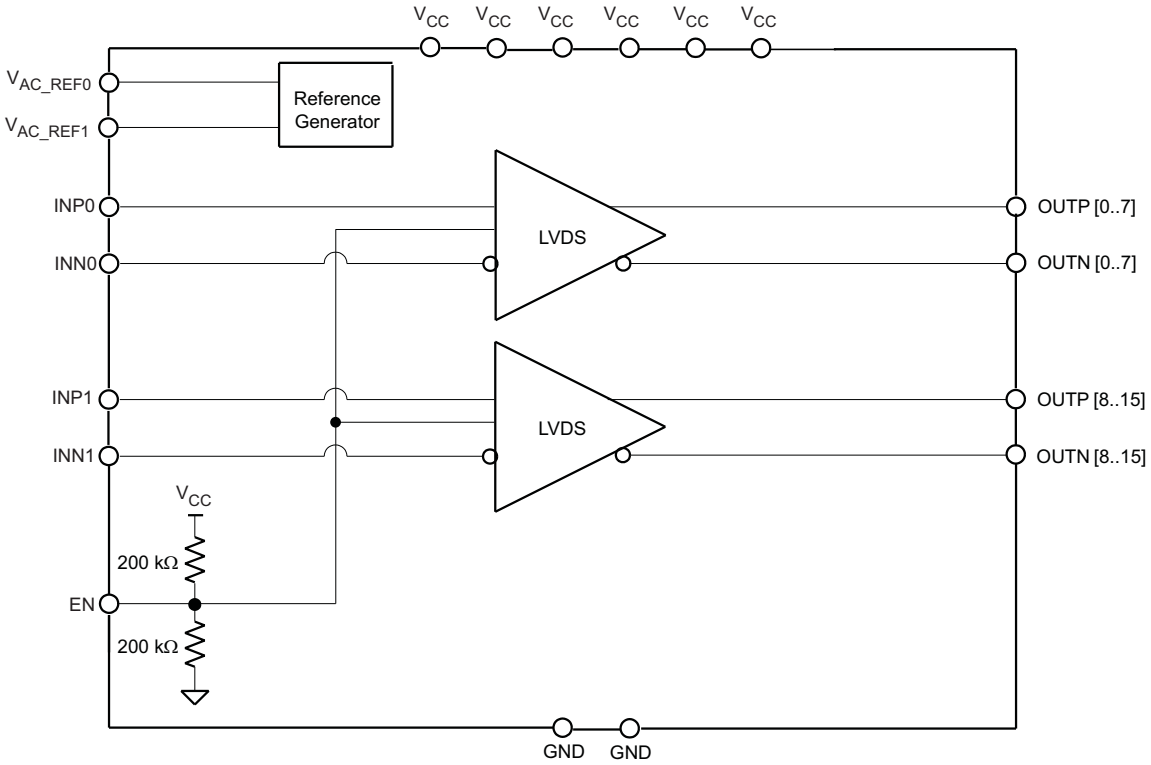
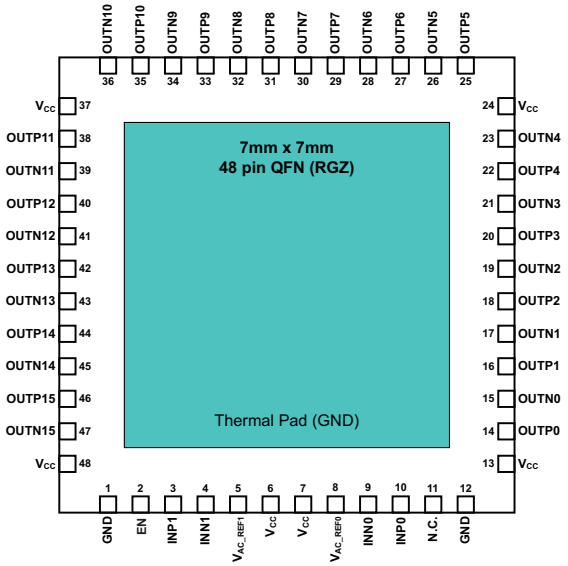


Figure 2. CDCLVD2108 Block Diagram

TOP VIEW



PIN FUNCTIONS

PIN		TYPE	DESCRIPTION	
NAME	NO.			
V_{CC}	6, 7, 13, 24, 37, 48	Power	2.5V supplies for the device	
GND	1,12	Ground	Device ground	
INP0, INN0	10, 9	Input	Differential input pair or single ended input for buffer 0	
INP1, INN1	3,4	Input	Differential input pair or single ended input for buffer 1	
OUTP0, OUTN0	14, 15	Output	Differential LVDS output pair no. 0	INP0/INN0 is the input
OUTP1, OUTN1	16,17	Output	Differential LVDS output pair no. 1	
OUTP2, OUTN2	18,19	Output	Differential LVDS output pair no. 2	
OUTP3, OUTN3	20, 21	Output	Differential LVDS output pair no. 3	
OUTP4, OUTN4	22,23	Output	Differential LVDS output pair no. 4	
OUTP5, OUTN5	25, 26	Output	Differential LVDS output pair no. 5	
OUTP6, OUTN6	27, 28	Output	Differential LVDS output pair no. 6	
OUTP7, OUTN7	29, 30	Output	Differential LVDS output pair no. 7	
OUTP8,OUTN8	31, 32	Output	Differential LVDS output pair no. 8	INP1/INN1 is the input
OUTP9,OUTN9	33, 34	Output	Differential LVDS output pair no. 9	
OUTP10,OUTN10	35, 36	Output	Differential LVDS output pair no. 10	
OUTP11,OUTN11	38, 39	Output	Differential LVDS output pair no. 11	
OUTP12,OUTN12	40, 41	Output	Differential LVDS output pair no. 12	
OUTP13,OUTN13	42, 43	Output	Differential LVDS output pair no. 13	
OUTP14,OUTN14	44, 45	Output	Differential LVDS output pair no. 14	
OUTP15,OUTN15	46, 47	Output	Differential LVDS output pair no. 15	
V_{AC_REF0}	8	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1µF to GND on this pin.	
V_{AC_REF1}	5	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1µF to GND on this pin.	
N.C.	11		No connect	
EN	2	Input with an internal 200kΩ pull-up and pull-down	Control pin – enables or disables the outputs (See Table 1)	
Thermal Pad		Ground	Device ground. Thermal Pad must be soldered to ground. See thermal management recommendations.	

Table 1. Output Control Table

EN	CLOCK OUTPUTS
0	All outputs disabled (static "0")
OPEN	All outputs enabled
1	OUT0 to OUT7 enabled and OUT8 to OUT15 disabled (static "0")

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE / UNIT
V_{CC}	Supply voltage range	–0.3 to 2.8 V
V_I	Input voltage range	–0.2 to (V_{CC} + 0.2) V
V_O	Output voltage range	–0.2 to (V_{CC} + 0.2) V
I_{OSD}	Driver short circuit current	See Note (2)
ESD	Electrostatic discharge (HBM, 1.5 kΩ, 100 pF)	>3000 V

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) The outputs can handle permanent short.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNITS
V_{CC}	Device supply voltage	2.375	2.5	2.625	V
T_A	Ambient temperature	–40		85	°C

THERMAL INFORMATION

THERMAL METRIC(1)		CDCLVD2108 RGZ (48 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	30.6	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	28.5	
θ_{JB}	Junction-to-board thermal resistance	10.5	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	10.2	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	3.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS

At V_{CC} = 2.375 V to 2.625 V and T_A = –40°C to 85°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN CONTROL INPUT CHARACTERISTICS						
V_{dI3}	3-State	Open		0.5×V_{CC}		V
V_{dIH}	Input high voltage		0.7×V_{CC}			V
V_{dIL}	Input low voltage				0.2×V_{CC}	V
I_{dIH}	Input high current	V_{CC} = 2.625 V, V_{IH} = 2.625 V			30	µA
I_{dIL}	Input low current	V_{CC} = 2.625 V, V_{IL} = 0 V			–30	µA
$R_{pull(EN)}$	Input pull-up/ pull-down resistor			200		kΩ
2.5V LVCMOS (see Figure 7) INPUT CHARACTERISTICS						
f_{IN}	Input frequency				200	MHz
V_{th}	Input threshold voltage	External threshold voltage applied to complementary input	1.1		1.5	V
V_{IH}	Input high voltage		V_{th} + 0.1		V_{CC}	V
V_{IL}	Input low voltage		0		V_{th} – 0.1	V
I_{IH}	Input high current	V_{CC} = 2.625 V, V_{IH} = 2.625 V			10	µA
I_{IL}	Input low current	V_{CC} = 2.625 V, V_{IL} = 0 V			–10	µA
ΔV/ΔT	Input edge rate	20% – 80%	1.5			V/ns
C_{IN}	Input capacitance			2.5		pF

ELECTRICAL CHARACTERISTICS (continued)

At V_{CC} = 2.375 V to 2.625 V and T_A = –40°C to 85°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIFFERENTIAL INPUT CHARACTERISTICS						
f_{IN}	Input frequency	Clock input			800	MHz
$V_{IN, DIFF}$	Differential input voltage peak-to-peak	V_{ICM} = 1.25 V	0.3		1.6	V_{PP}
V_{ICM}	Input common-mode voltage range	$V_{IN, DIFF, PP}$ > 0.4V	1.0		V_{CC} – 0.3	V
I_{IH}	Input high current	V_{CC} = 2.625 V, V_{IH} = 2.625 V			10	µA
I_{IL}	Input low current	V_{CC} = 2.625 V, V_{IL} = 0 V			–10	µA
ΔV/ΔT	Input edge rate	20% to 80%	0.75			V/ns
C_{IN}	Input capacitance			2.5		pF
LVDS OUTPUT CHARACTERISTICS						
$\|V_{OD}\|$	Differential output voltage magnitude	$V_{IN, DIFF, PP}$ = 0.3 V,R_L = 100 Ω	250		450	mV
ΔV_{OD}	Change in differential output voltage magnitude		–15		15	mV
$V_{OC(SS)}$	Steady-state common mode output voltage		1.1		1.375	V
$\Delta V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN, DIFF, PP}$ = 0.6 V,R_L = 100 Ω	–15		15	mV
V_{ring}	Output overshoot and undershoot	Percentage of output amplitude V_{OD}			10%	
V_{OS}	Output ac common mode	$V_{IN, DIFF, PP}$ = 0.6 V, R_L = 100 Ω		40	70	mV_{PP}
I_{OS}	Short-circuit output current	V_{OD} = 0 V			±24	mA
t_{PD}	Propagation delay	$V_{IN, DIFF, PP}$ = 0.3 V		1.5	2.5	ns
$t_{SK, PP}$	Part-to-part skew				600	ps
t_{SK, O_WB}	Within bank output skew				50	ps
t_{SK,O_BB}	Bank-to-bank output skew	both inputs are phase aligned			80	ps
$t_{SK,P}$	Pulse skew(with 50% duty cycle input)	Crossing-point-to-crossing-point distortion	–50		50	ps
t_{RJIT}	Random additive jitter (with 50% duty cycle input)	Edge speed 0.75V/ns 10 kHz – 20 MHz			0.3	ps, RMS
t_R/t_F	Output rise/fall time	20% to 80%,100 Ω, 5 pF	50		300	ps
I_{CCSTAT}	Static supply current	Outputs unterminated, f = 0 Hz		27	45	mA
I_{CC100}	Supply current	All outputs enabled, R_L = 100 Ω, f = 100 MHz		119	158	mA
I_{CC800}	Supply current	All outputs enabled, R_L = 100 Ω, f = 800 MHz		168	211	mA
V_{AC_REF} CHARACTERISTICS						
V_{AC_REF}	Reference output voltage	V_{CC} = 2.5 V, I_{load} = 100 µA	1.1	1.25	1.35	V

Typical Additive Phase Noise Characteristics for 100 MHz Clock

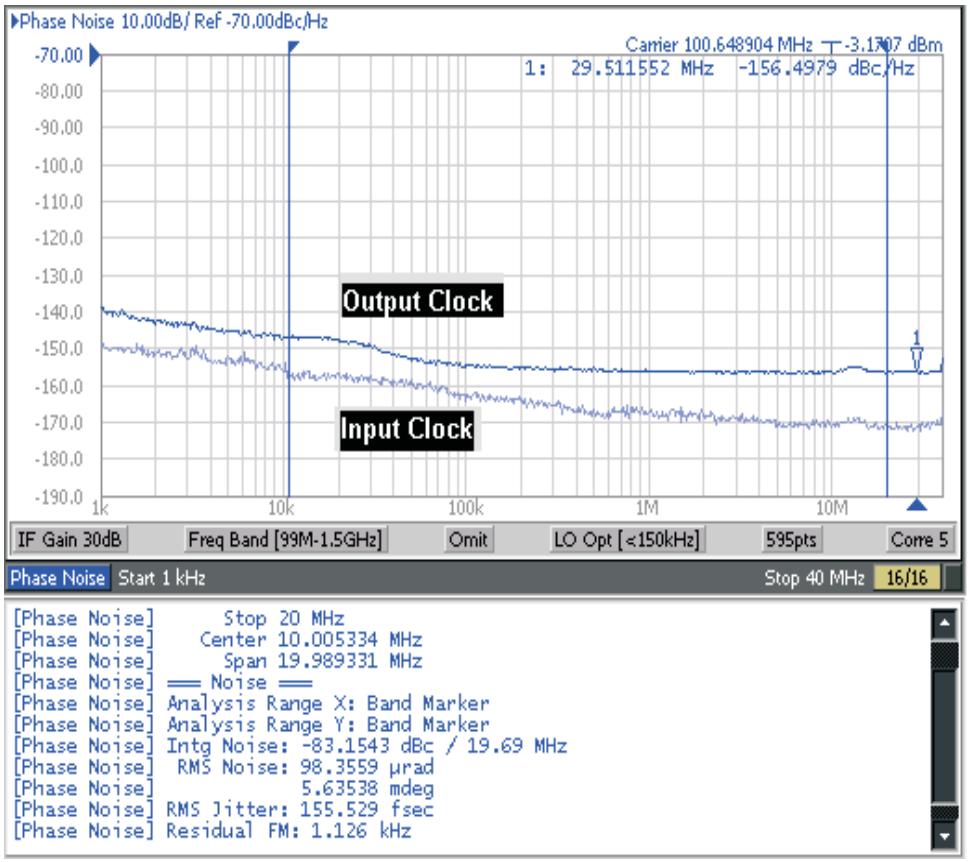
PARAMETER		MIN	TYP	MAX	UNIT
phn_{100}	Phase noise at 100 Hz offset		-132.9		dBc/Hz
phn_{1k}	Phase noise at 1 kHz offset		-138.8		dBc/Hz
phn_{10k}	Phase noise at 10 kHz offset		-147.4		dBc/Hz
phn_{100k}	Phase noise at 100 kHz offset		-153.6		dBc/Hz
phn_{1M}	Phase noise at 1 MHz offset		-155.2		dBc/Hz
phn_{10M}	Phase noise at 10 MHz offset		-156.2		dBc/Hz
phn_{20M}	Phase noise at 20 MHz offset		-156.6		dBc/Hz
t_{RJIT}	Random additive jitter from 10 kHz to 20 MHz		171		fs, RMS

Typical Additive Phase Noise Characteristics for 737.27 MHz Clock

PARAMETER		MIN	TYP	MAX	UNIT
phn_{100}	Phase noise at 100 Hz offset		-80.2		dBc/Hz
phn_{1k}	Phase noise at 1 kHz offset		-114.3		dBc/Hz
phn_{10k}	Phase noise at 10 kHz offset		-138		dBc/Hz
phn_{100k}	Phase noise at 100 kHz offset		-143.9		dBc/Hz
phn_{1M}	Phase noise at 1 MHz offset		-145.2		dBc/Hz
phn_{10M}	Phase noise at 10 MHz offset		-146.5		dBc/Hz
phn_{20M}	Phase noise at 20 MHz offset		-146.6		dBc/Hz
t_{RJIT}	Random additive jitter from 10 kHz to 20 MHz		65		fs, RMS

TYPICAL CHARACTERISTICS

INPUT CLOCK AND OUTPUT CLOCK PHASE NOISES
vs
FREQUENCY FROM THE CARRIER (T_A = 25°C and V_{CC} = 2.5V)



Input clock RMS jitter is 32 fs from 10 kHz to 20 MHz and additive RMS jitter is 152 fs

Figure 3. 100 MHz Input and Output Phase Noise Plot

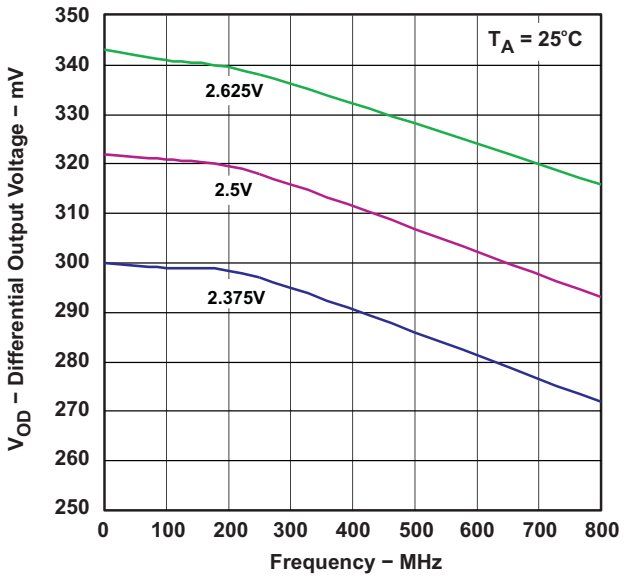


Figure 4. Differential Output Voltage vs Frequency

TEST CONFIGURATIONS

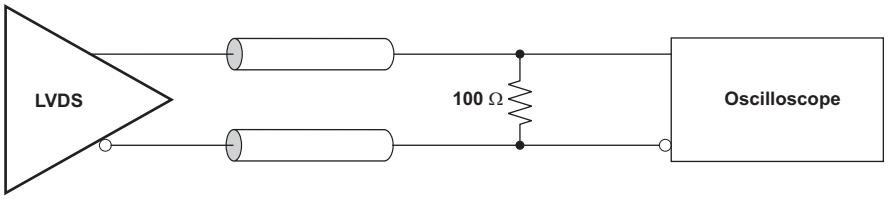


Figure 5. LVDS Output DC Configuration During Device Test

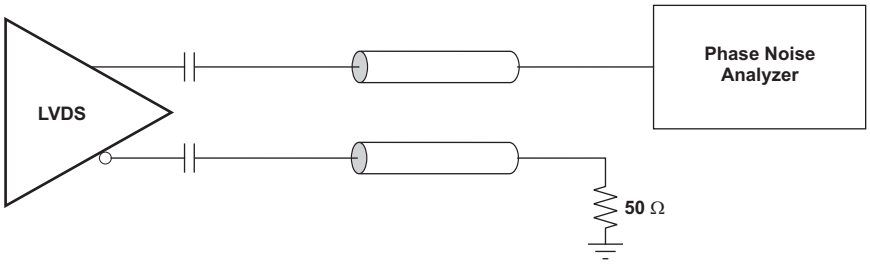


Figure 6. LVDS Output AC Configuration During Device Test

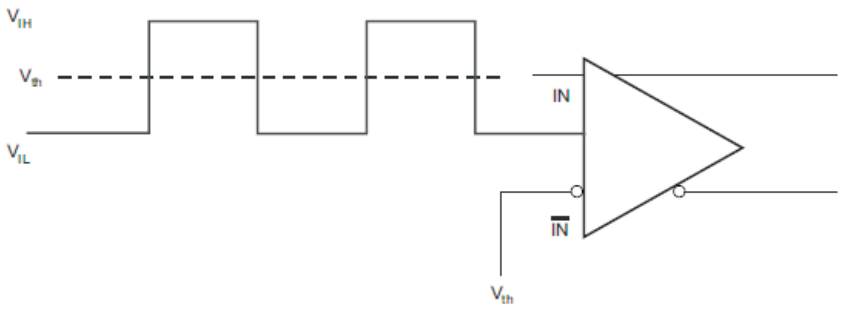


Figure 7. DC Coupled LVCMOS Input During Device Test

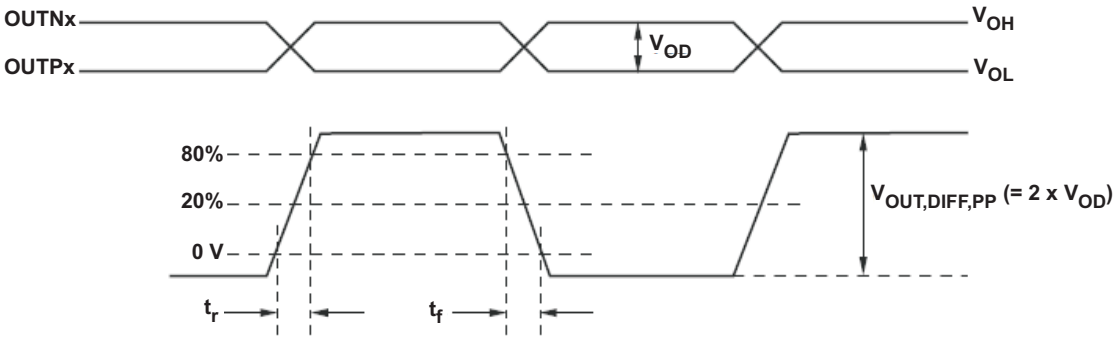
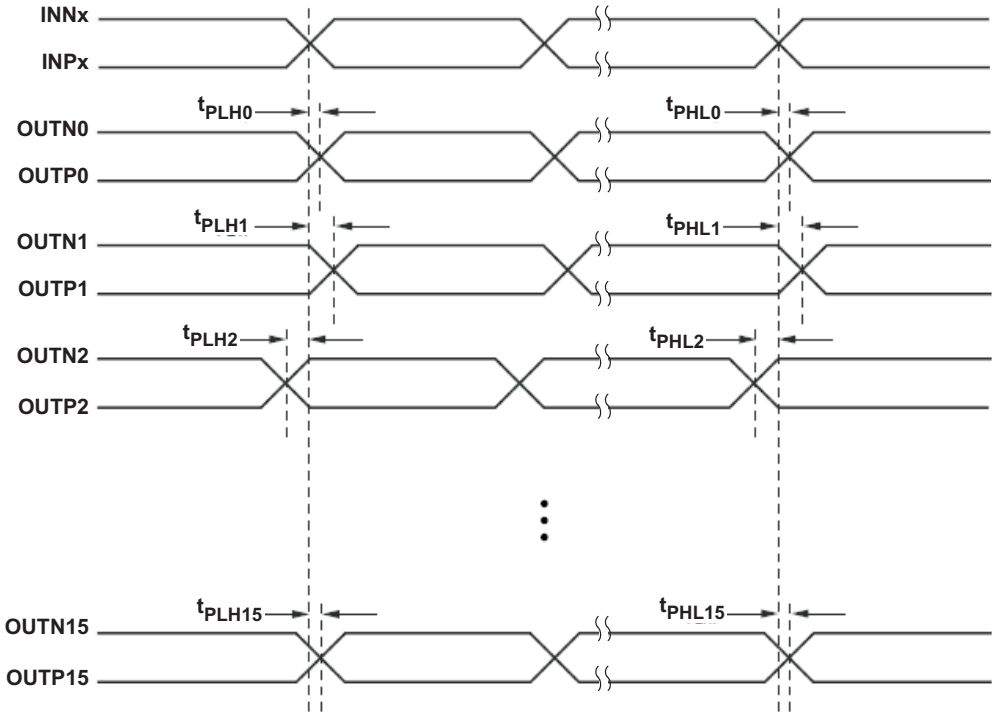


Figure 8. Output Voltage and Rise/Fall Time



A. Output skew is calculated as the greater of the following: As the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} (n = 0, 1, 2, ..15).

B. Part-to-part skew is calculated as the greater of the following: As the difference between the fastest and the slowest t_{PLHn} or the difference between the fastest and the slowest t_{PHLn} across multiple devices (n = 0, 1, 2, ..15).

C. Both inputs (IN0 and IN1) are phase aligned.

Figure 9. Output Skew and Part-to-Part Skew

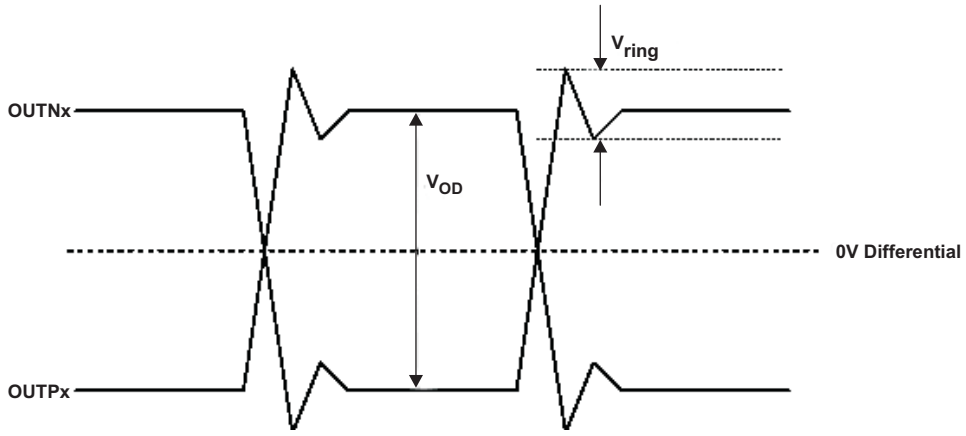


Figure 10. Output Overshoot and Undershoot

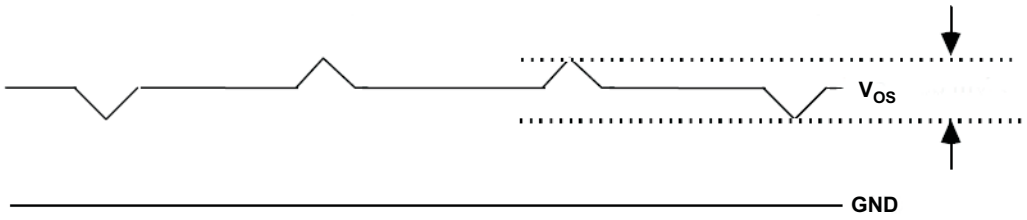


Figure 11. Output AC Common Mode

APPLICATION INFORMATION

THERMAL MANAGEMENT

For reliability and performance reasons, the die temperature should be limited to a maximum of 125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. Check the mechanical data at the end of the data sheet for land and via pattern examples.

POWER-SUPPLY FILTERING

High-performance clock buffers are sensitive to noises on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to the application.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply pins and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1 μF) bypass capacitors as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with very low dc resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

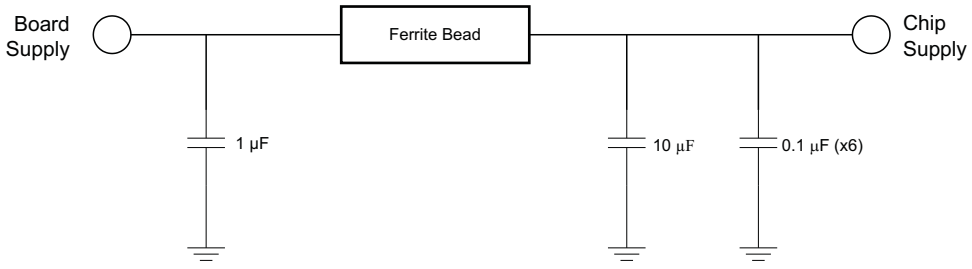


Figure 12. Power-Supply Filtering

LVDS OUTPUT TERMINATION

The proper LVDS termination for signal integrity over two 50 Ω lines is 100 Ω between the outputs on the receiver end. Either dc-coupled termination or ac-coupled termination can be used for LVDS outputs. It is recommended to place termination resister close to the receiver. If the receiver is internally biased to a voltage different than the output common mode voltage of the CDCLVD2108, ac-coupling should be used. If the LVDS receiver has internal 100 Ω termination, external termination must be omitted.

Unused outputs can be left open without connecting any trace to the output pins.

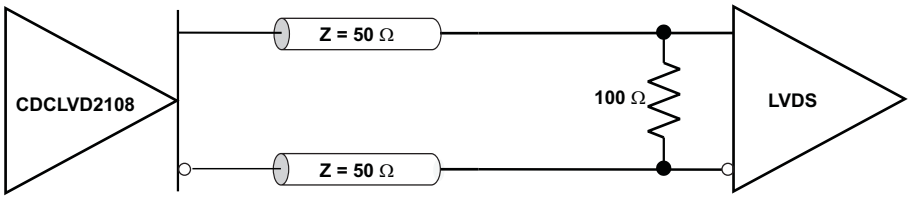


Figure 13. LVDS Output DC Termination

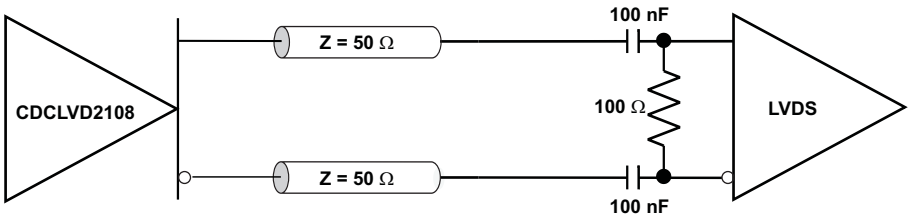


Figure 14. LVDS Output AC Termination With Receiver Internally Biased

INPUT TERMINATION

The CDCLVD2108 inputs can be interfaced with LVDS, LVPECL, or LVCMOS drivers.

LVDS Driver can be connected to CDCLVD2108 inputs with dc or ac coupling as shown Figure 15 and Figure 16, respectively.

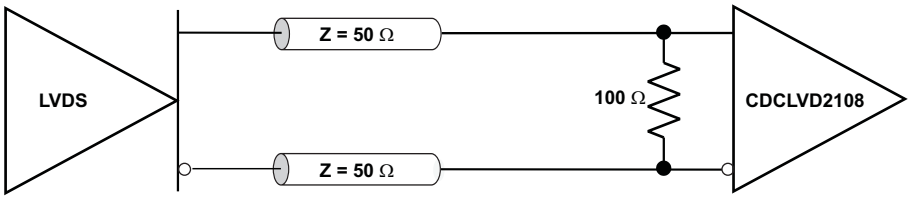


Figure 15. LVDS Clock Driver Connected to CDCLVD2108 Input (DC Coupled)

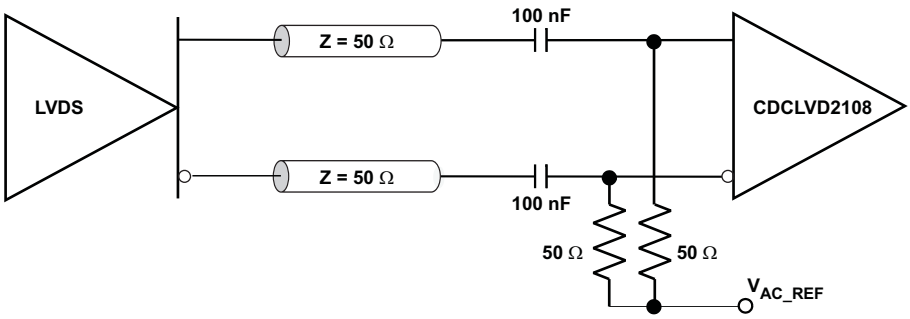


Figure 16. LVDS Clock Driver Connected to CDCLVD2108 Input (AC Coupled)

Figure 17 shows how to connect LVPECL inputs to the CDCLVD2108. The series resistors are required to reduce the LVPECL signal swing if the signal swing is >1.6 V_{PP}.

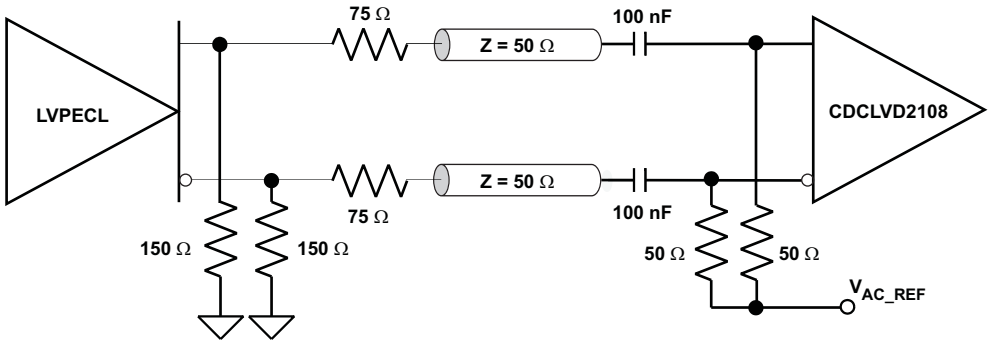


Figure 17. LVPECL Clock Driver Connected to CDCLVD2108 Input

Figure 18 illustrates how to couple a 2.5 V LVCMOS clock input to the CDCLVD2108 directly. The series resistance (R_S) should be placed close to the LVCMOS driver if needed. 3.3 V LVCMOS clock input swing needs to be limited to $V_{IH} \leq V_{CC}$.

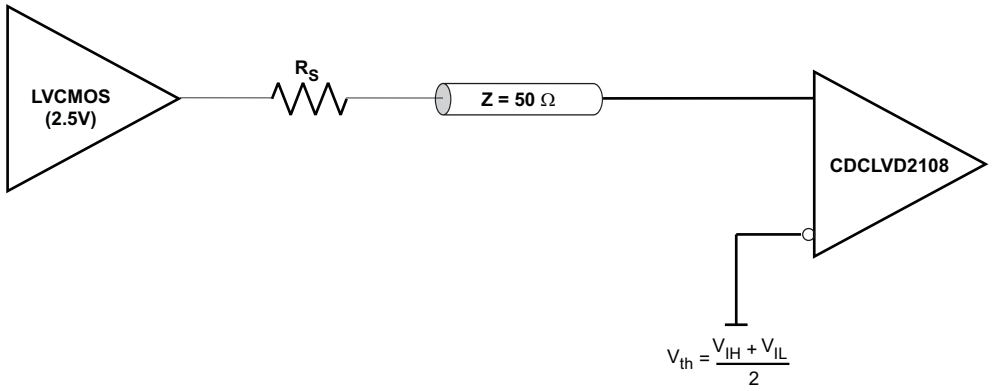


Figure 18. 2.5V LVCMOS Clock Driver Connected to CDCLVD2108 Input

If one of the input buffers is used, the other buffer should be disabled through the EN pin, and unused input pins should be grounded by 1 kΩ resistors.

REVISION HISTORY

Changes from Original (October 2010) to Revision A	Page
• Feature - Low Within Bank Output Skew of 45 ps (Max) To: Low Within Bank Output Skew of 50 ps (Max)	1
• Changed $t_{SK,\ O\_WB}$ Within bank output skew From: 45 ps (Max) To: 50 ps (Max)	5
• Changed $t_{SK,\ O\_WB}$ Bank-to-bank output skew From: 100 ps (Max) To: 80 ps (Max)	5
• Deleted the Recommended PCB Layout illustration	10

Changes from Revision A (November 2010) to Revision B	Page
• Changed the I_{CC100}, Supply current Typ value From: 97 To: 119 mA	5
• Changed the I_{CC800}, Supply current Typ value From: 138 To: 168 mA	5

Changes from Revision B (December 2010) to Revision C	Page
• Changed the device status From: Product Preview To: Production	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCLVD2108RGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCLVD 2108	Samples
CDCLVD2108RGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCLVD 2108	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

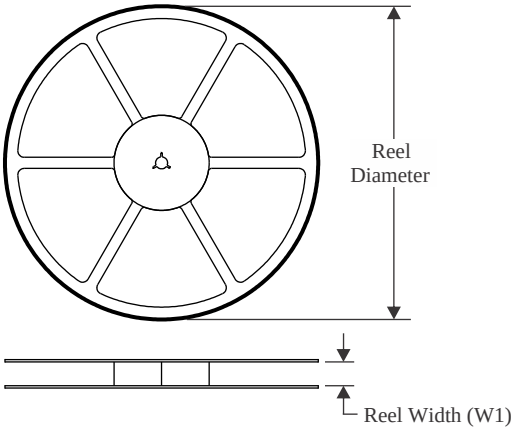
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

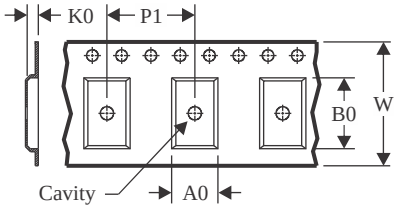
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

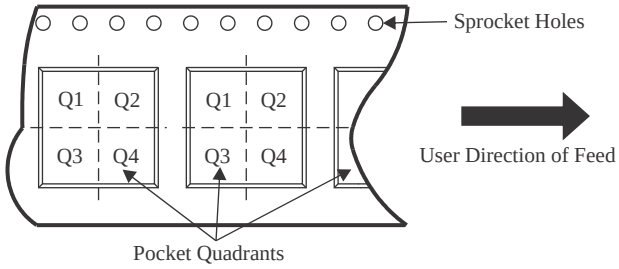


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

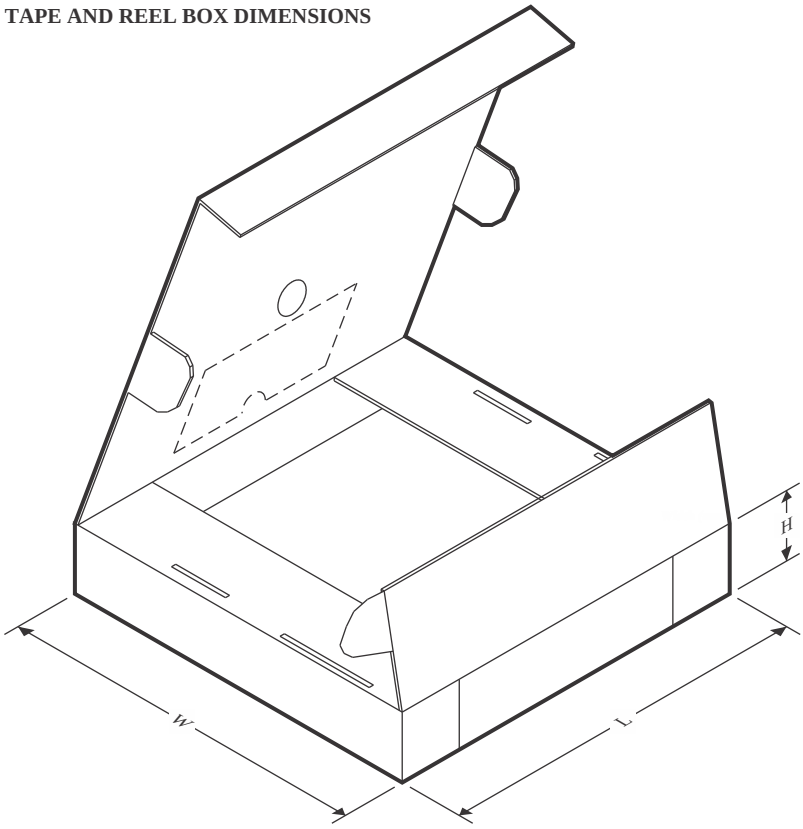
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVD2108RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVD2108RGZR	VQFN	RGZ	48	2500	350.0	350.0	43.0

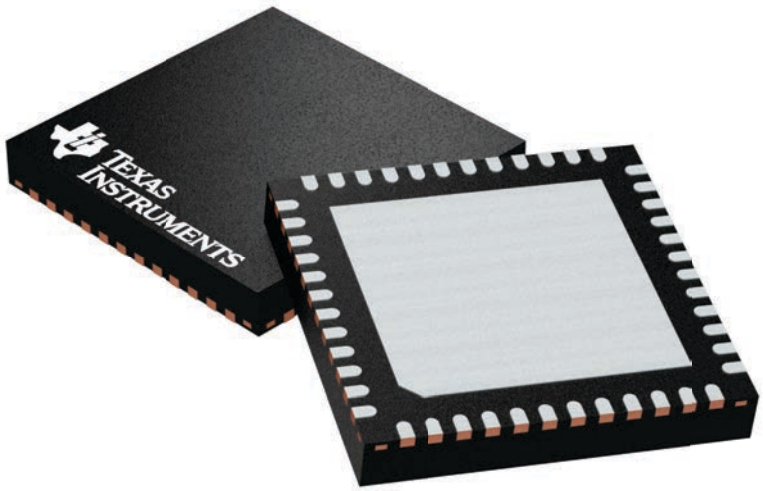
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265