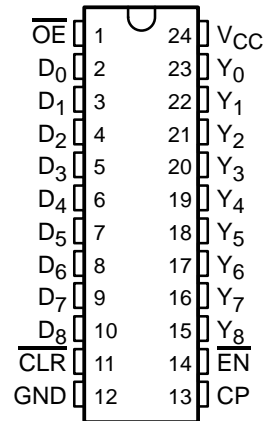


# CY74FCT823T 9-BIT BUS-INTERFACE REGISTER WITH 3-STATE OUTPUTS

SCCS069A – OCTOBER 2001 – REVISED NOVEMBER 2001

- Function, Pinout, and Drive Compatible With FCT, F Logic, and AM29823
- Reduced  $V_{OH}$  (Typically = 3.3 V) Version of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)
- 64-mA Output Sink Current  
32-mA Output Source Current
- High-Speed Parallel Register With Positive-Edge-Triggered D-Type Flip-Flops
- Buffered Common Clock-Enable ( $\overline{EN}$ ) and Asynchronous-Clear ( $\overline{CLR}$ ) Inputs
- 3-State Outputs

P, Q, OR SO PACKAGE  
(TOP VIEW)



## description

This bus-interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The CY74FCT823T is a 9-bit-wide buffered register with clock-enable ( $\overline{EN}$ ) and clear ( $\overline{CLR}$ ) inputs that are ideal for parity bus interfacing in high-performance microprogrammed systems. It is ideal for use as an output port requiring high  $I_{OL}/I_{OH}$ .

This device is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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**ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QSOP – Q	Tape and reel	6	CY74FCT823CTQCT	FCT823C
	SOIC – SO	Tube	6	CY74FCT823CTSOC	FCT823C
		Tape and reel	6	CY74FCT823CTSOCT	
	DIP – P	Tube	7.5	CY74FCT823BTPC	CY74FCT823BTPC
	DIP – P	Tube	10	CY74FCT823ATPC	CY74FCT823ATPC
	QSOP – Q	Tape and reel	10	CY74FCT823ATQCT	FCT823A
	SOIC – SO	Tube	10	CY74FCT823ATSOC	FCT823A
		Tape and reel	10	CY74FCT823ATSOCT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

**PIN DESCRIPTION**

NAME	I/O	DESCRIPTION
D	I	D flip-flop data inputs
$\overline{\text{CLR}}$	I	When $\overline{\text{CLR}}$ is low and $\overline{\text{OE}}$ is low, Q outputs are low. When $\overline{\text{CLR}}$ is high, data can be entered into the register.
CP	O	Clock pulse for the register. Enters data into the register on the low-to-high clock transition.
Y	O	Register 3-state outputs
$\overline{\text{EN}}$	I	Clock enable. When $\overline{\text{EN}}$ is low, data on the D input is transferred to the Q output on the low-to-high clock transition. When $\overline{\text{EN}}$ is high, the Q outputs do not change state, regardless of the data or clock input transitions.
$\overline{\text{OE}}$	I	Output control. When $\overline{\text{OE}}$ is high, the Y outputs are in the high-impedance state. When $\overline{\text{OE}}$ is low, true register data is present at the Y outputs.

**FUNCTION TABLE**

INPUTS					INTERNAL OUTPUTS		FUNCTION
$\overline{\text{OE}}$	$\overline{\text{CLR}}$	$\overline{\text{EN}}$	D	CP	Q	Y	
H	H	L	L	↑	L	Z	Z
H	H	L	H	↑	H	Z	
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	L	Z	Load
H	H	L	H	↑	H	Z	
L	H	L	L	↑	L	L	
L	H	L	H	↑	H	H	

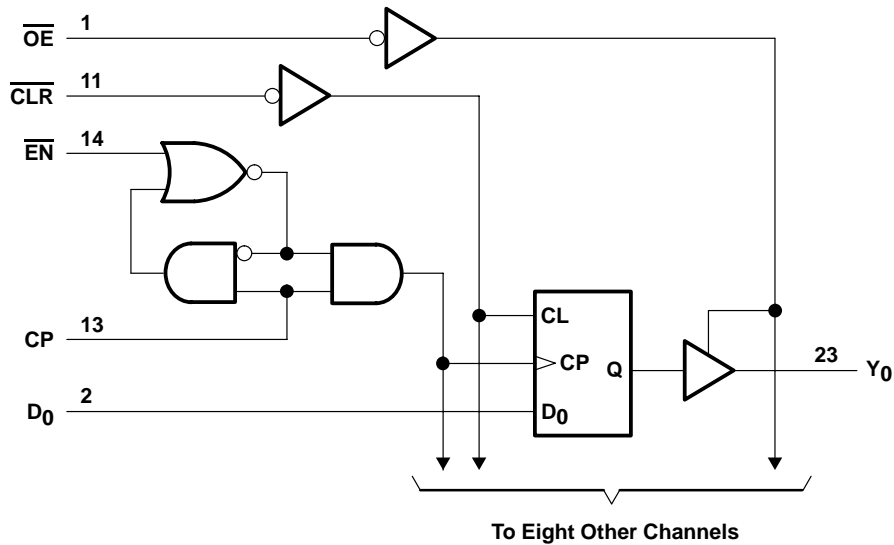
H = High logic level, L = Low logic level, X = Don't care, NC = No change, ↑ = Low-to-high transition, Z = High-impedance state



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**logic diagram (positive logic)**



**absolute maximum rating over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range to ground potential	-0.5 V to 7 V
DC input voltage range	-0.5 V to 7 V
DC output voltage range	-0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): P package	67°C/W
(see Note 2): Q package	61°C/W
(see Note 2): SO package	46°C/W
Ambient temperature range with power applied, $T_A$	-65°C to 135°C
Storage temperature range, $T_{Stg}$	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-3.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5	5.25	V
$V_{IH}$ High-level input voltage	2			V
$V_{IL}$ Low-level input voltage			0.8	V
$I_{OH}$ High-level output current			-32	mA
$I_{OL}$ Low-level output current			64	mA
$T_A$ Operating free-air temperature	-40		85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.



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## 9-BIT BUS-INTERFACE REGISTER

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT	
$V_{IK}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{IN} = -18\text{ mA}$		-0.7	-1.2	V	
$V_{OH}$	$V_{CC} = 4.75\text{ V}$	$I_{OH} = -32\text{ mA}$		2		V	
		$I_{OH} = -15\text{ mA}$		2.4	3.3		
$V_{OL}$	$V_{CC} = 4.75\text{ V}$ ,	$I_{OL} = 64\text{ mA}$		0.3	0.55	V	
$V_{hys}$	All inputs			0.2		V	
$I_I$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = V_{CC}$			5	$\mu\text{A}$	
$I_{IH}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = 2.7\text{ V}$			$\pm 1$	$\mu\text{A}$	
$I_{IL}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} = 0.5\text{ V}$			$\pm 1$	$\mu\text{A}$	
$I_{OZH}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{OUT} = 2.7\text{ V}$			10	$\mu\text{A}$	
$I_{OZL}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{OUT} = 0.5\text{ V}$			-10	$\mu\text{A}$	
$I_{OS}^\ddagger$	$V_{CC} = 5.25\text{ V}$ ,	$V_{OUT} = 0\text{ V}$	-60	-120	-225	mA	
$I_{off}$	$V_{CC} = 0\text{ V}$ ,	$V_{OUT} = 4.5\text{ V}$			$\pm 1$	$\mu\text{A}$	
$I_{CC}$	$V_{CC} = 5.25\text{ V}$ ,	$V_{IN} \leq 0.2\text{ V}$ , $V_{IN} \geq V_{CC} - 0.2\text{ V}$		0.1	0.2	mA	
$\Delta I_{CC}$	$V_{CC} = 5.25\text{ V}$ , $V_{IN} = 3.4\text{ V}^\S$ , $f_1 = 0$ , Outputs open			0.5	2	mA	
$I_{CCD}^\parallel$	$V_{CC} = 5.25\text{ V}$ , One bit switching at 50% duty cycle, Outputs open, $OE = EN = \text{GND}$ , $V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$			0.06	0.12	mA/MHz	
$I_{C\#}$	$V_{CC} = 5.25\text{ V}$ , Outputs open, $OE = EN = \text{GND}$	One bit switching at $f_1 = 5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$		0.7	1.4	mA
			$V_{IN} = 3.4\text{ V}$ or GND		1.2	3.4	
		Eight bits switching at $f_1 = 2.5\text{ MHz}$ at 50% duty cycle	$V_{IN} \leq 0.2\text{ V}$ or $V_{IN} \geq V_{CC} - 0.2\text{ V}$		1.6	3.2	
			$V_{IN} = 3.4\text{ V}$ or GND		3.9	12.2	
$C_i$				5	10	pF	
$C_o$				9	12	pF	

† Typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests,  $I_{OS}$  tests should be performed last.

§ Per TTL-driven input ( $V_{IN} = 3.4\text{ V}$ ); all other inputs at  $V_{CC}$  or GND

¶ This parameter is derived for use in total power-supply calculations.

#  $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$  = Total supply current

$I_{CC}$  = Power-supply current with CMOS input levels

$\Delta I_{CC}$  = Power-supply current for a TTL high input ( $V_{IN} = 3.4\text{ V}$ )

$D_H$  = Duty cycle for TTL inputs high

$N_T$  = Number of TTL inputs at  $D_H$

$I_{CCD}$  = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$  = Clock frequency for registered devices, otherwise zero

$f_1$  = Input signal frequency

$N_1$  = Number of inputs changing at  $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the  $I_{CC}$  formula.



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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER		TEST LOAD	CY74FCT823AT		CY74FCT823BT		CY74FCT823CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CP	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	7	6	6	ns		
		$\overline{\text{CLR}}$ low		6	6	6			
$t_{su}$	Setup time, before CP $\uparrow$	Data	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	4	3	3	ns		
		$\overline{\text{EN}}$		4	3	3			
$t_h$	Hold time, after CP $\uparrow$	Data	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	2	1.5	1.5	ns		
		$\overline{\text{EN}}$		2	0	0			
$t_{rec}$	Recovery time	$\overline{\text{CLR}}$ before CP $\uparrow$	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	6	6	6	ns		

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY74FCT823AT		CY74FCT823BT		CY74FCT823CT		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	CP	Y	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	10		7.5		6		ns
$t_{PHL}$				10		7.5		6		
$t_{PLH}$	CP	Y	$C_L = 300 \text{ pF}$ , $R_L = 500 \Omega$	20		15		12.5		ns
$t_{PHL}$				20		15		12.5		
$t_{PLH}$	$\overline{\text{CLR}}$	Y	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	14		9		8		ns
$t_{PZH}$	$\overline{\text{OE}}$	Y	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	12		8		7		ns
$t_{PZL}$				12		8		7		
$t_{PZH}$	$\overline{\text{OE}}$	Y	$C_L = 300 \text{ pF}$ , $R_L = 500 \Omega$	23		15		12.5		ns
$t_{PZL}$				23		15		12.5		
$t_{PHZ}$	$\overline{\text{OE}}$	Y	$C_L = 5 \text{ pF}$ , $R_L = 500 \Omega$	7		6.5		6		ns
$t_{PLZ}$				7		6.5		6		
$t_{PHZ}$	$\overline{\text{OE}}$	Y	$C_L = 50 \text{ pF}$ , $R_L = 500 \Omega$	8		7.5		6.5		ns
$t_{PLZ}$				8		7.5		6.5		



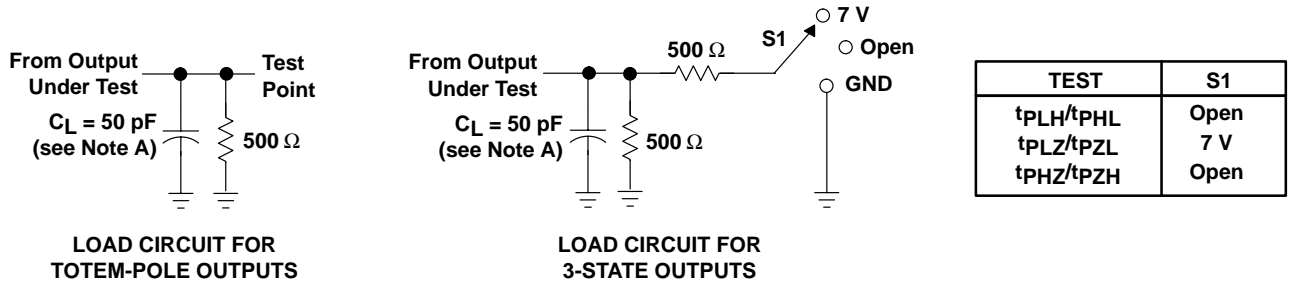
# CY74FCT823T

## 9-BIT BUS-INTERFACE REGISTER

### WITH 3-STATE OUTPUTS

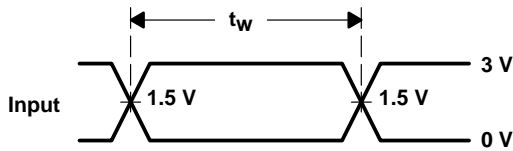
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#### PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR 3-STATE OUTPUTS



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT823ATQCT	ACTIVE	SSOP	DBQ	24	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FCT823A	<a href="#">Samples</a>
CY74FCT823ATSOC	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT823A	<a href="#">Samples</a>
CY74FCT823CTSOC	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT823C	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

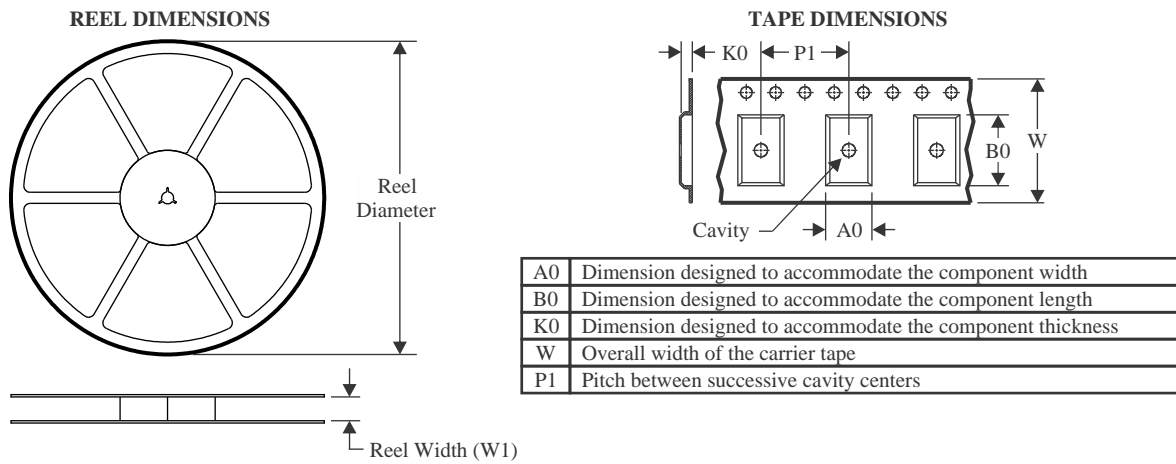
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CY74FCT823ATQCT	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CY74FCT823ATQCT	SSOP	DBQ	24	2500	356.0	356.0	35.0

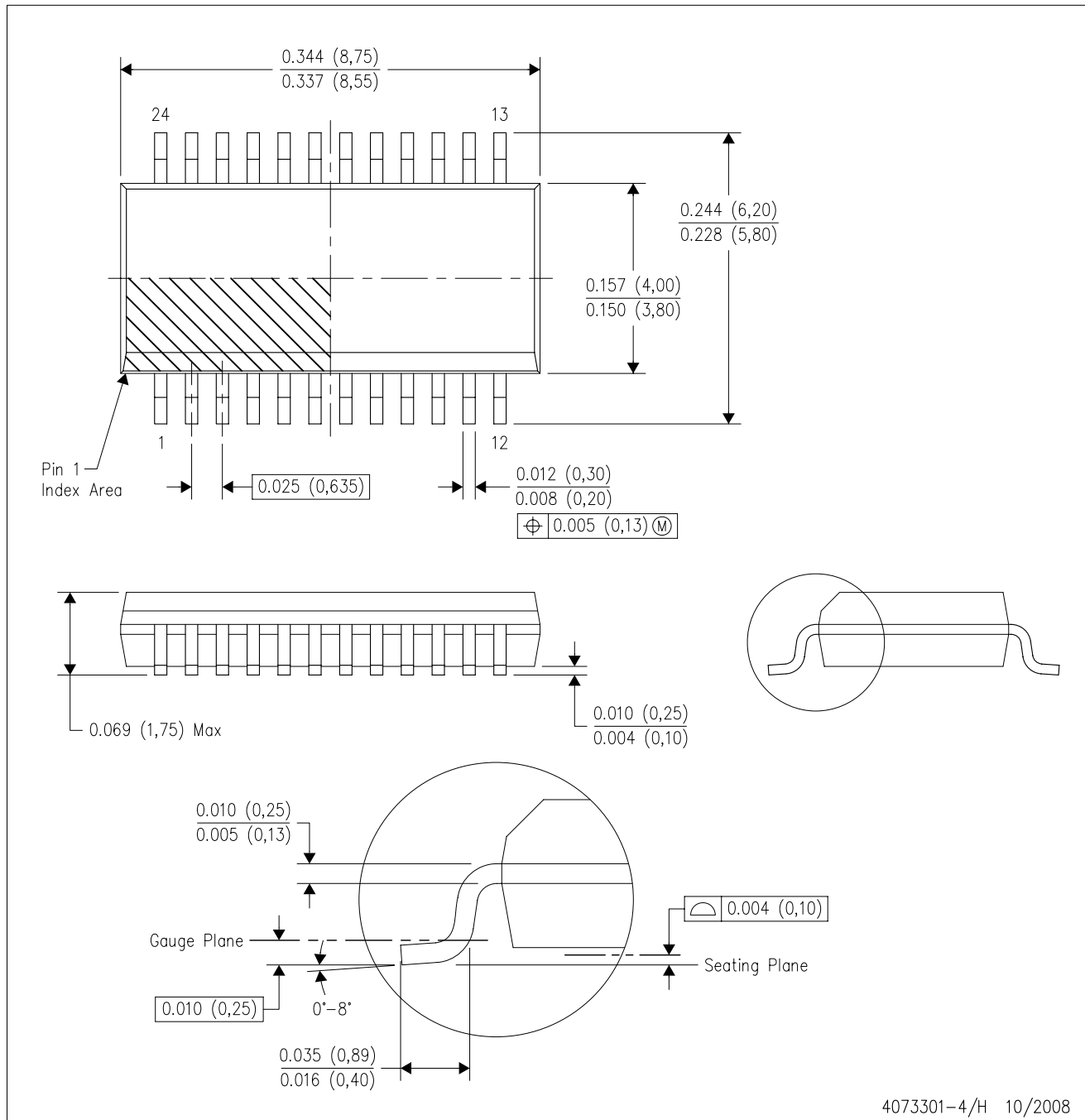
**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CY74FCT823ATSOC	DW	SOIC	24	25	506.98	12.7	4826	6.6
CY74FCT823CTSOC	DW	SOIC	24	25	506.98	12.7	4826	6.6

DBQ (R-PDSO-G24)

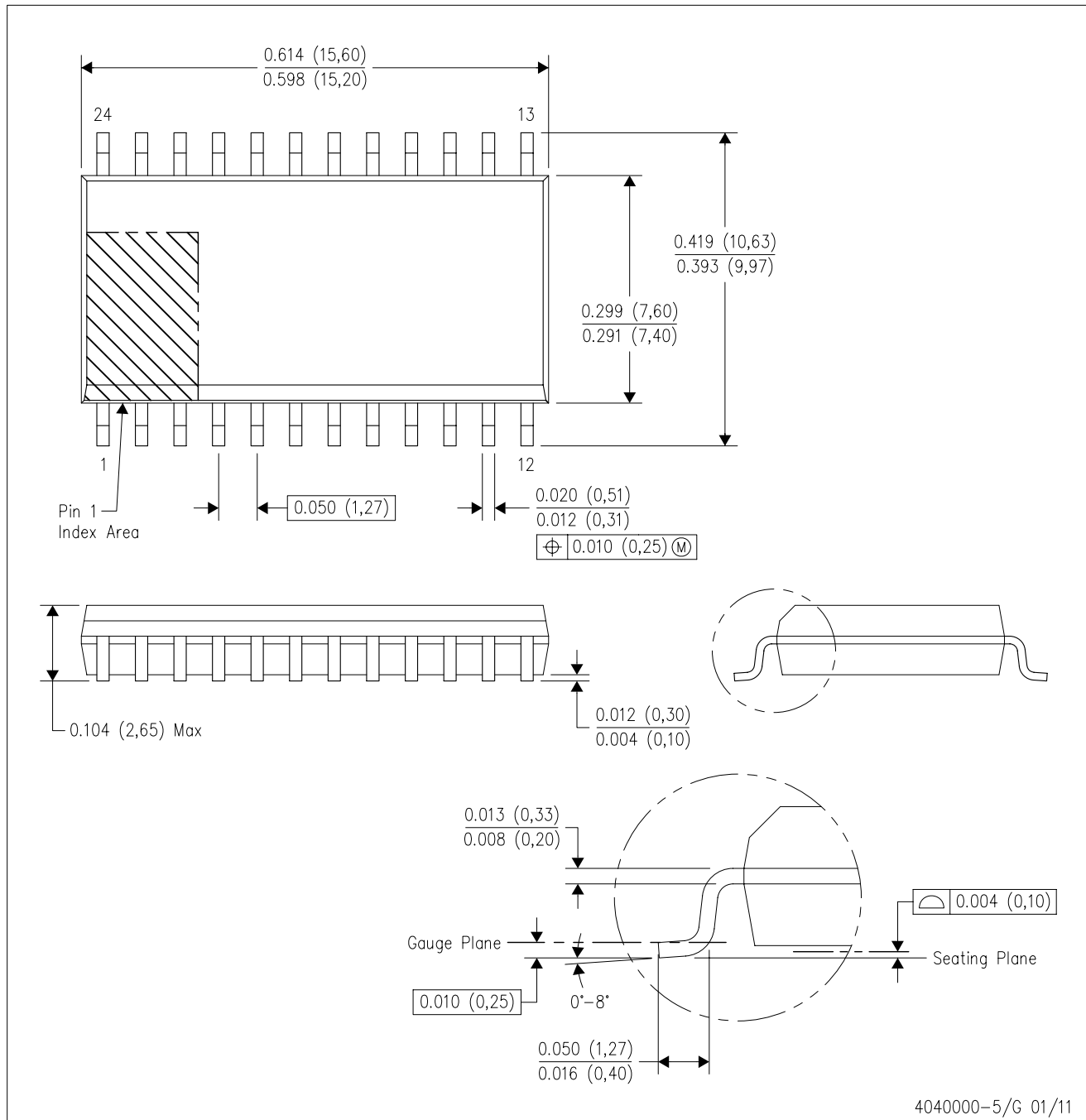
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - D. Falls within JEDEC MO-137 variation AE.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

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