DLP5500 DLP 0.55-Inch XGA Series 450 Digital Micromirror Device

1 Features

- 0.55-inch micromirror array diagonal
  - 1024 × 768 array of aluminum, micrometer-sized mirrors (XGA resolution)
  - 10.8μm micromirror pitch
  - ±12° micromirror tilt angle (relative to flat state)
  - Designed for corner illumination
- Designed for use with broadband visible light (420nm–700nm):
  - Window transmission 97% (single pass, through two window surfaces)
  - Micromirror reflectivity 88%
  - Array diffraction efficiency 86%
  - Array fill factor 92%
- 16-bit, low voltage differential signaling (LVDS) double data rate (DDR) input data bus
- 200 MHz input data clock rate
- Dedicated DLPC200 controller for high-speed pattern rates:
  - 5,000Hz (1-bit binary patterns)
  - 500Hz (8-bit grayscale patterns)
- Dedicated DLPC900 controller for high-speed pattern rates:
  - 10,638.298Hz (1-bit binary patterns)
  - 266.453Hz (8-bit grayscale patterns)
- Series 450 package characteristics:
  - Thermal area 18mm × 12mm enabling high on-screen lumens (>2000lm)
  - 149 micro pin grid array robust electrical connection
  - Package mates to Amphenol Intercon Systems 450-2.700-L-13.25-149 socket

2 Applications

- Industrial
  - 3D scanners for machine vision and quality control
  - 3D printing
  - Direct imaging lithography
  - Laser marking and repair
  - Industrial and medical imaging
  - Medical instrumentation
  - Digital exposure systems
- Medical
  - Opthamology
  - 3D scanners for limb and skin measurement
  - Hyperspectral imaging
- Displays
  - 3D imaging microscopes
  - Intelligent and adaptive lighting

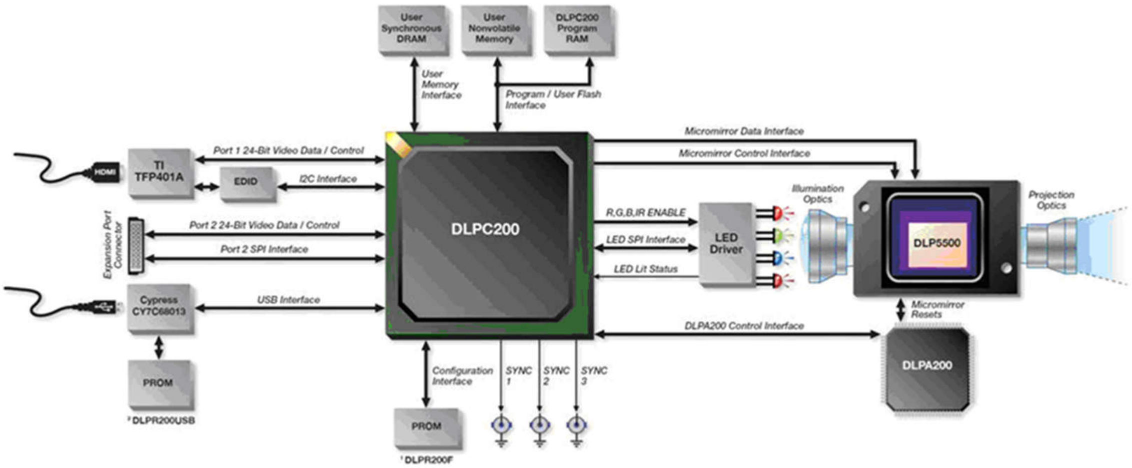
3 Description

Featuring over 750000 micromirrors, the high-resolution DLP5500 (0.55" XGA) digital micromirror device (DMD) is a spatial light modulator (SLM) that modulates the amplitude, direction, and/or phase of incoming light. This advanced light control technology has numerous applications in the industrial, medical, and consumer markets. The DLP5500 enables fine resolution for 3D printing applications.

Device Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE
DLP5500	CPGA (149)	22.30mm × 32.20mm

(1) For more information, see Section 13.



Typical Application

Table of Contents

4 Description (continued)

The XGA resolution has the direct benefit of scanning large objects for 3D machine vision applications. Reliable function and operation of the DLP5500 requires that it be used in conjunction with the DLPC200 digital controller and the DLPA200 analog driver. This dedicated chipset provides a robust, high resolution XGA, and high speed system solution.

5 Pin Configuration and Functions

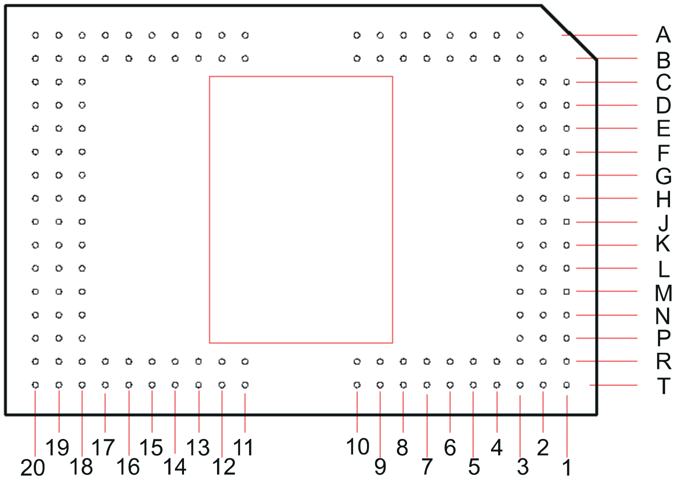


Figure 5-1. FYA Package 149-Pin CPGA Series 450 Bottom View

Table 5-1. Pin Functions

PIN[1]		TYPE (I/O/P)	SIGNAL	DATA RATE[2]	INTERNAL TERM[3]	CLOCK	DESCRIPTION	TRACE (mils)[4]
NAME	NO.							
DATA INPUTS								
D_AN1	G20	Input	LVCMOS	DDR	Differential	DCLK_A	Input data bus A (LVDS)	715
D_AP1	H20	Input	LVCMOS	DDR	Differential	DCLK_A		744
D_AN3	H19	Input	LVCMOS	DDR	Differential	DCLK_A		688
D_AP3	G19	Input	LVCMOS	DDR	Differential	DCLK_A		703
D_AN5	F18	Input	LVCMOS	DDR	Differential	DCLK_A		686
D_AP5	G18	Input	LVCMOS	DDR	Differential	DCLK_A		714
D_AN7	E18	Input	LVCMOS	DDR	Differential	DCLK_A		689
D_AP7	D18	Input	LVCMOS	DDR	Differential	DCLK_A		705
D_AN9	C20	Input	LVCMOS	DDR	Differential	DCLK_A		687
D_AP9	D20	Input	LVCMOS	DDR	Differential	DCLK_A		715
D_AN11	B18	Input	LVCMOS	DDR	Differential	DCLK_A		715
D_AP11	A18	Input	LVCMOS	DDR	Differential	DCLK_A		732
D_AN13	A20	Input	LVCMOS	DDR	Differential	DCLK_A		686
D_AP13	B20	Input	LVCMOS	DDR	Differential	DCLK_A		715
D_AN15	B19	Input	LVCMOS	DDR	Differential	DCLK_A		700
D_AP15	A19	Input	LVCMOS	DDR	Differential	DCLK_A		719

Table 5-1. Pin Functions (continued)

PIN[1]		TYPE (I/O/P)	SIGNAL	DATA RATE[2]	INTERNAL TERM[3]	CLOCK	DESCRIPTION	TRACE (mils)[4]
NAME	NO.							
D_BN1	K20	Input	LVCMOS	DDR	Differential	DCLK_B	Input data bus B (LVDS)	716
D_BP1	J20	Input	LVCMOS	DDR	Differential	DCLK_B		745
D_BN3	J19	Input	LVCMOS	DDR	Differential	DCLK_B		686
D_BP3	K19	Input	LVCMOS	DDR	Differential	DCLK_B		703
D_BN5	L18	Input	LVCMOS	DDR	Differential	DCLK_B		686
D_BP5	K18	Input	LVCMOS	DDR	Differential	DCLK_B		714
D_BN7	M18	Input	LVCMOS	DDR	Differential	DCLK_B		693
D_BP7	N18	Input	LVCMOS	DDR	Differential	DCLK_B		709
D_BN9	P20	Input	LVCMOS	DDR	Differential	DCLK_B		687
D_BP9	N20	Input	LVCMOS	DDR	Differential	DCLK_B		715
D_BN11	R18	Input	LVCMOS	DDR	Differential	DCLK_B		702
D_BP11	T18	Input	LVCMOS	DDR	Differential	DCLK_B		719
D_BN13	T20	Input	LVCMOS	DDR	Differential	DCLK_B		686
D_BP13	R20	Input	LVCMOS	DDR	Differential	DCLK_B		715
D_BN15	R19	Input	LVCMOS	DDR	Differential	DCLK_B		680
D_BP15	T19	Input	LVCMOS	DDR	Differential	DCLK_B		700
DCLK_AN	D19	Input	LVCMOS	—	Differential	—	Input data bus A Clock (LVDS)	700
DCLK_AP	E19	Input	LVCMOS	—	Differential	—		728
DCLK_BN	N19	Input	LVCMOS	—	Differential	—	Input data bus B Clock (LVDS)	700
DCLK_BP	M19	Input	LVCMOS	—	Differential	—		728
DATA CONTROL INPUTS								
SCTRL_AN	F20	Input	LVCMOS	DDR	Differential	DCLK_A	Data Control (LVDS)	716
SCTRL_AP	E20	Input	LVCMOS	DDR	Differential	DCLK_A		731
SCTRL_BN	L20	Input	LVCMOS	DDR	Differential	DCLK_B		707
SCTRL_BP	M20	Input	LVCMOS	DDR	Differential	DCLK_B		722
SERIAL COMMUNICATION (SCP) AND CONFIGURATION								
SCP_CLK	A8	Input	LVCMOS	—	Pulldown	—		—
SCP_DO	A9	Output	LVCMOS	—	—	SCP_CLK		—
SCP_DI	A5	Input	LVCMOS	—	Pulldown	SCP_CLK		—
$\overline{\text{SCP\_EN}}$	B7	Input	LVCMOS	—	Pulldown	SCP_CLK		—
$\overline{\text{PWRDN}}$	B9	Input	LVCMOS	—	Pulldown	—		—
MICROMIRROR BIAS CLOCKING PULSE								
MODE_A	A4	Input	LVCMOS	—	Pulldown	—		—
MBRST0	C3	Input	Analog	—	—	—	Micromirror Bias Clocking Pulse "MBRST" signals "clock" micromirrors into state of LVCMOS memory cell associated with each mirror.	—
MBRST1	D2	Input	Analog	—	—	—		—
MBRST2	D3	Input	Analog	—	—	—		—
MBRST3	E2	Input	Analog	—	—	—		—
MBRST4	G3	Input	Analog	—	—	—		—
MBRST5	E1	Input	Analog	—	—	—		—
MBRST6	G2	Input	Analog	—	—	—		—
MBRST7	G1	Input	Analog	—	—	—		—
MBRST8	N3	Input	Analog	—	—	—		—
MBRST9	M2	Input	Analog	—	—	—		—
MBRST10	M3	Input	Analog	—	—	—		—
MBRST11	L2	Input	Analog	—	—	—		—
MBRST12	J3	Input	Analog	—	—	—		—
MBRST13	L1	Input	Analog	—	—	—		—
MBRST14	J2	Input	Analog	—	—	—		—
MBRST15	J1	Input	Analog	—	—	—		—

Table 5-1. Pin Functions (continued)

PIN(1)		TYPE (I/O/P)	SIGNAL	DATA RATE(2)	INTERNAL TERM(3)	CLOCK	DESCRIPTION	TRACE (mils)(4)
NAME	NO.							
POWER								
V_{CC}	B11,B12,B13,B16,R12,R13,R16,R17	Power	Analog	—	—	—	Power for LVCMOS Logic	—
V_{CCI}	A12,A14,A16,T12,T14,T16	Power	Analog	—	—	—	Power supply for LVDS Interface	—
V_{CC2}	C1,D1,M1,N1	Power	Analog	—	—	—	Power for High Voltage CMOS Logic	—
V_{SS}	A6,A11,A13,A15,A17,B4,B5,B8,B14,B15,B17,C2,C18,C19,F1,F2,F19,H1,H2,H3,H18,J18,K1,K2,L19,N2,P18,P19,R4,R9,R14,R15,T7,T13,T15,T17	Power	Analog	—	—	—	Common return for all power inputs	—
RESERVED SIGNALS (Not for use in system)								
RESERVED_R7	R7	Input	LVCMOS	—	Pulldown	—	Pins should be connected to V_{SS}	—
RESERVED_R8	R8	Input	LVCMOS	—	Pulldown	—		—
RESERVED_T8	T8	Input	LVCMOS	—	Pulldown	—		—
RESERVED_B6	B6	Input	LVCMOS	—	Pulldown	—		—
NO_CONNECT	A3, A7, A10, B2, B3, B10, E3, F3, K3, L3, P1, P2, P3, R1, R2, R3, R5, R6, R10, R11, T1, T2, T3, T4, T5, T6, T9, T10, T11	—	—	—	—	—	DO NOT CONNECT	—

(1) The following power supplies are required to operate the DMD: VCC, VCCI, VCC2. VSS must also be connected.
(2) DDR = Double Data Rate. SDR = Single Data Rate. Refer to the Section 6.7 for specifications and relationships.
(3) Refer to Section 6.6 for differential termination specification.
(4) Internal Trace Length (mils) refers to the package electrical trace length.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
ELECTRICAL					
V_{CC}	Voltage applied to V_{CC} (2) (3)		–0.5	4	V
V_{CCI}	Voltage applied to V_{CCI} (2) (3)		–0.5	4	V
	Delta supply voltage $\|V_{CC} – V_{CCI}\|$(4)			0.3	V
$\|V_{ID}\|$	Maximum differential voltage, Damage can occur to internal resistor if exceeded, See Figure 6-6			700	mV
V_{CC2}	Voltage applied to V_{OFFSET} (2) (3) (4)		–0.5	8	V
V_{MBRST}	Voltage applied to MBRST[0:15] Input Pins		–28	28	V
	Voltage applied to all other pins(2)		–0.5	V_{CC} + 0.3	V
I_{OH}	Current required from a high-level output	V_{OH} = 2.4 V		–20	mA
I_{OL}	Current required from a low-level output	V_{OL} = 0.4 V		15	mA
ENVIRONMENTAL					
T_{CASE}	Case temperature: operational (5) (6)		–20	90	°C
	Case temperature: non–operational (6)		–40	90	°C
	Dew Point (Operating and non-Operating)			81	°C

(1) Stresses beyond those listed under *Section 6.1* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Section 6.4*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS} (ground).
(3) Voltages V_{CC}, V_{CCI}, and V_{CC2} are required for proper DMD operation.
(4) Exceeding the recommended allowable absolute voltage difference between V_{CC} and V_{CCI} may result in an excess current draw. The difference between V_{CC} and V_{CCI}, | V_{CC} - V_{CCI}|, should be less than .3V.
(5) Exposure of the DMD simultaneously to any combination of the maximum operating conditions for case temperature, differential temperature, or illumination power density (see *Section 6.4*).
(6) DMD Temperature is the worst-case of any test point shown in Figure 7-4or the active array as calculated by the *Section 7.6*.

6.2 Storage Conditions

applicable before the DMD is installed in the final product

			MIN	MAX	UNIT
T_{stg}	DMD storage temperature		–40	80	°C
T_{DP}	Storage dew point	Storage Dew Point - longterm (1)		24	°C
		Storage Dew Point - short term (2)		28	

(1) Long-term is defined as the usable life of the device.
(2) Dew points beyond the specified long-term dew point are for short-term conditions only, where short-term is defined as less than 60 cumulative days over the usable life of the device (operating, non-operating, or storage).

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Electrostatic discharge immunity for LVCMOS [I/O] pins(2)	±2000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins [power, control pins] except MBRST (1)	±2000	
		Electrostatic discharge immunity for MBRST[0:15] pins(2)	<250	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) Tested in accordance with JESD22-A114-B Electrostatic Discharge (ESD) sensitivity testing Human Body Model (HBM).

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGES(1) (2)					
V_{CC}	Supply voltage for LVCMOS core logic	3.15	3.3	3.45	V
V_{CCI}	Supply voltage for LVDS receivers	3.15	3.3	3.45	V
V_{CC2}	Mirror electrode and HVCMOS supply voltage (1) (2)	8.25	8.5	8.75	V
$\|V_{CCI}–V_{CC}\|$	Supply voltage delta (absolute value) (3)			0.3	V
V_{MBRST}	Micromirror clocking pulse voltages	-27		26.5	V
LVCMOS PINS					
V_{IH}	High level Input voltage (4)	1.7	2.5	VCC + 0.15	V
V_{IL}	Low level Input voltage(4)	– 0.3		0.7	V
I_{OH}	High level output current at V_{OH} = 2.4 V			–20	mA
I_{OL}	Low level output current at V_{OL} = 0.4 V			15	mA
T_{PWRDNZ}	PWRDNZ pulse width(5)	10			ns
SCP INTERFACE					
f_{clock}	SCP clock frequency(6)			500	kHz
t_{SCP_SKEW}	Time between valid SCPDI and rising edge of SCPCLK(7)	–800		800	ns
t_{SCP_DELAY}	Time between valid SCPDO and rising edge of SCPCLK(7)			700	ns
$t_{SCP\_BYTE\_INTERVAL}$	Time between consecutive bytes	1			µs
$t_{SCP\_NEG\_ENZ}$	Time between falling edge of SCPENZ and the first rising edge of SCPCLK	30			ns
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse width (high level)	1			µs
$t_{SCP\_OUT\_EN}$	Time required for SCP output buffer to recover after SCPENZ (from tri-state)			1.5	ns
f_{clock}	SCP circuit clock oscillator frequency (8)	9.6		11.1	MHz

6.4 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
LVDS INTERFACE					
f_{clock}	Clock frequency for LVDS interface, DCLK (all channels)		200		MHz
$\lvert V_{ID} \rvert$	Input differential voltage (absolute value)[9]	100	400	600	mV
V_{CM}	Common mode [9]		1200		mV
V_{LVDS}	LVDS voltage[9]	0		2000	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			10	ns
Z_{IN}	Internal differential termination resistance	95		105	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONMENTAL [10]					
T_{DMD}	Long-term DMD temperature (operational) [11] [12] [16]	10		40 to 70[12]	°C
	Short-term DMD temperature (operational)[11] [17]	–20		75	°C
T_{WINDOW}	Window temperature – operational[13]			90	°C
$T_{CERAMIC\text{-}WINDOW\text{-}DELTA}$	Delta ceramic-to-window temperature -operational [13] [14]			30	°C
	Long-term dew point (operational & non-operational)			24	°C
	Short-term dew point[16] [18] (operational & non-operational)			28	°C
ILL_{UV}	Illumination, wavelength < 420 nm			0.68	mW/cm^2
ILL_{VIS}	Illumination, wavelengths between 420 and 700 nm			Thermally Limited[15]	mW/cm^2
ILL_{IR}	Illumination, wavelength > 700 nm			10	mW/cm^2

(1) Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
(2) VOFFSET supply transients must fall within specified max voltages.
(3) To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than the specified limit.
(4) Tester Conditions for V_{IH} and V_{IL}:
Frequency = 60MHz. Maximum Rise Time = 2.5ns at (20% to 80%)
Frequency = 60MHz. Maximum Fall Time = 2.5ns at (80% to 20%)
(5) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tri-states the SCPDO output pin.
(6) The SCP clock is a gated clock. The duty cycle shall be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(7) Refer to Figure 6-3.
(8) SCP internal oscillator is specified to operate all SCP registers. For all SCP operations, DCLK is required.
(9) Refer to Figure 6-5, Figure 6-6, and Figure 6-7.
(10) Optimal, long-term performance and optical efficiency of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty-cycle, ambient temperature (storage and operating), DMD temperature, ambient humidity (storage and operating), and power on or off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle.
(11) DMD Temperature is the worst-case of any thermal test point in Figure 7-4, or the active array as calculated by the *Section 7.6.3*.
(12) Per Figure 6-1, the maximum operational case temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *Section 7.7* for a definition of micromirror landed duty cycle.
(13) Window temperature as measured at thermal test points TP2, TP3, TP4, and TP5 in Figure 7-4.The locations of thermal test points TP2, TP3, TP4, and TP5 in Figure 7-4 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, a test point should be added to that location.
(14) Ceramic package temperature as measured at test point 1 (TP 1) in Figure 7-4.
(15) Refer to *Section 6.5* and *Section 7.6*.
(16) Long-term is defined as the average over the usable life of the device.
(17) Short-term is defined as less than 60 cumulative days over the usable life of the device.
(18) Dew points beyond the specified long-term dew point (operating, non-operating, or storage) are for short-term conditions only, where short-term is defined as< 60 cumulative days over the usable life of the device.

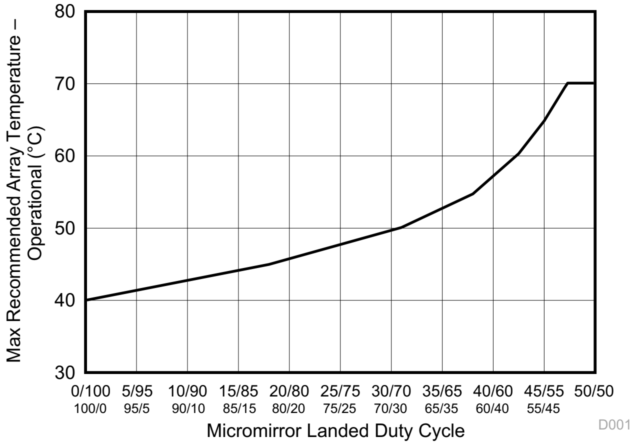


Figure 6-1. Max Recommended DMD Temperature—Derating Curve

6.5 Thermal Information

THERMAL METRIC	DLP5500 FYA (CPGA) 149 PINS	UNIT
Thermal resistance from active array to specified point on case (TP1)(1)	0.6	°C/W

(1) For more information, see *Section 7.6*.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage(1), See Figure 6-2	V_{CC} = 3.0 V,	I_{OH} = –20 mA	2.4			V
V_{OL}	Low-level output voltage(1), See Figure 6-2	V_{CC} = 3.6 V,	I_{OL} = 15 mA			0.4	V
I_{OZ}	High impedance output current(1)	V_{CC} = 3.6 V				10	µA
I_{IL}	Low-level input current(1)	V_{CC} = 3.6 V,	V_I = 0 V			–60	µA
I_{IH}	High-level input current(1)	V_{CC} = 3.6 V,	V_I = V_{CC}			200	µA
I_{CC}	Current into V_{CC} pin	V_{CC} = 3.6 V,				750	mA
I_{CCI}	Current into V_{OFFSET} pin(2)	V_{CCI} = 3.6 V				450	mA
I_{CC2}	Current into V_{CC2} pin	V_{CC2} = 8.75V				25	mA
Z_{IN}	Internal Differential Impedance			95		105	Ω
Z_{LINE}	Line Differential Impedance (PWB or Trace)			90	100	110	Ω
C_I	Input capacitance(1)	f = 1 MHz				10	pF
C_O	Output capacitance(1)	f = 1 MHz				10	pF
C_{IM}	Input capacitance for MBRST[0:15] pins	f = 1 MHz		160		210	pF

(1) Applies to LVCMOS pins only
(2) Exceeding the maximum allowable absolute voltage difference between V_{CC} and V_{CCI} may result in excess current draw. (Refer to *Absolute Maximum Ratings* for details)

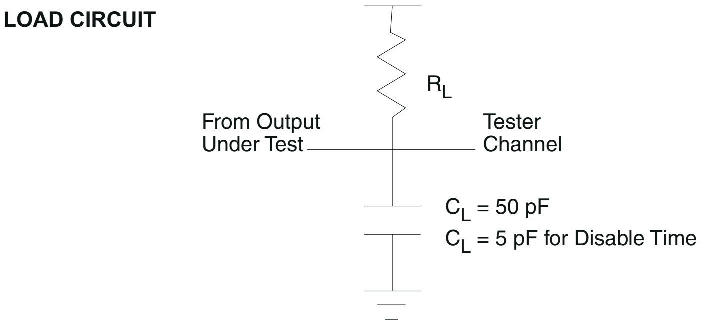


Figure 6-2. Measurement Condition for LVCMOS Output

6.7 Timing Requirements

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
LVDS TIMING PARAMETERS (See Figure 6-9)					
t_c	Clock Cycle DLCK_A or DCLKC_B		5		ns
t_w	Pulse Width DCLK_A or DCLK_B		2.5		ns
t_s	Setup Time, D_A[0:15] before DCLK_A	.35			ns
t_s	Setup Time, D_B[0:15] before DCLK_B	.35			ns
t_h	Hold Time, D_A[0:15] after DCLK_A	.35			ns
t_h	Hold Time, D_B[0:15] after DCLK_B	.35			ns
t_{skew}	Channel B relative to Channel A	–1.25		1.25	ns
LVDS WAVEFORM REQUIREMENTS (See Figure 6-6)					
$\|V_{ID}\|$	Input Differential Voltage (absolute difference)	100	400	600	mV
V_{CM}	Common Mode Voltage		1200		mV
V_{LVDS}	LVDS Voltage	0		2000	mV
t_r	Rise Time (20% to 80%)	100		400	ps
t_r	Fall Time (80% to 20%)	100		400	ps
SERIAL CONTROL BUS TIMING PARAMETERS (See Figure 6-3 and Figure 6-4)					
f_{SCP_CLK}	SCP Clock Frequency	50		500	kHz
t_{SCP_SKEW}	Time between valid SCP_DI and rising edge of SCP_CLK	–300		300	ns
t_{SCP_DELAY}	Time between valid SCP_DO and rising edge of SCP_CLK			2600	ns
$t_{\overline{SCP\_EN}}$	Time between falling edge of $\overline{\text{SCP\_EN}}$ and the first rising edge of SCP_CLK	30			ns
t_{r_SCP}	Rise time for SCP signals			200	ns
t_{fP}	Fall time for SCP signals			200	ns

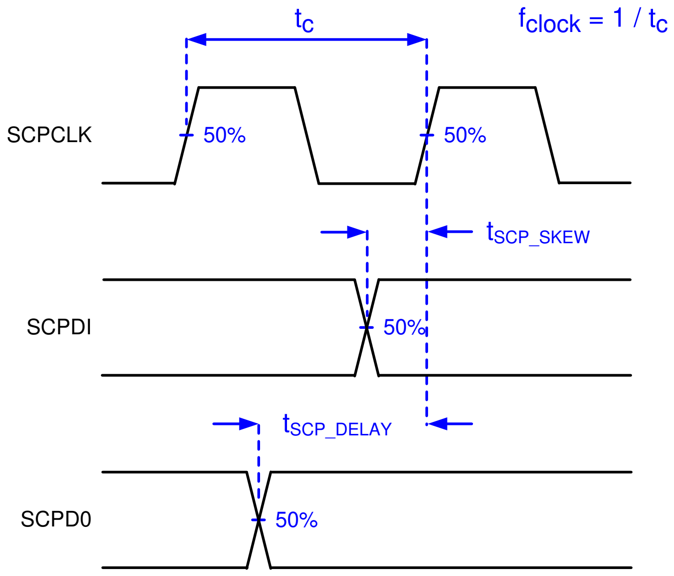


Figure 6-3. Serial Communications Bus Timing Parameters

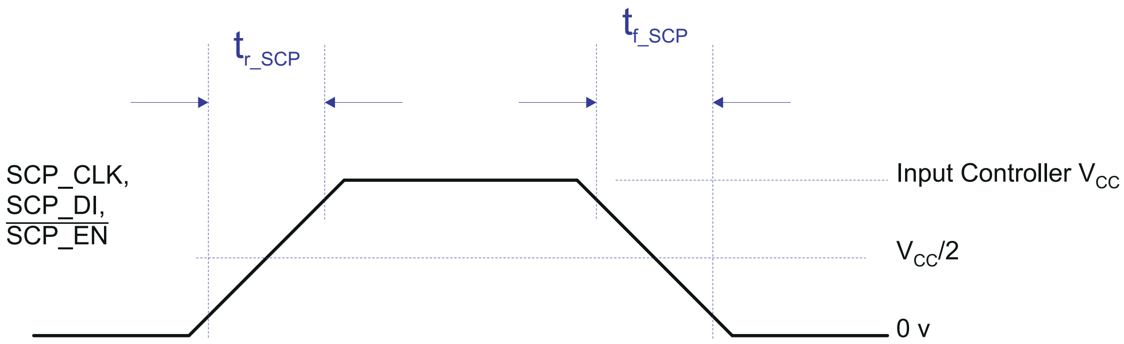
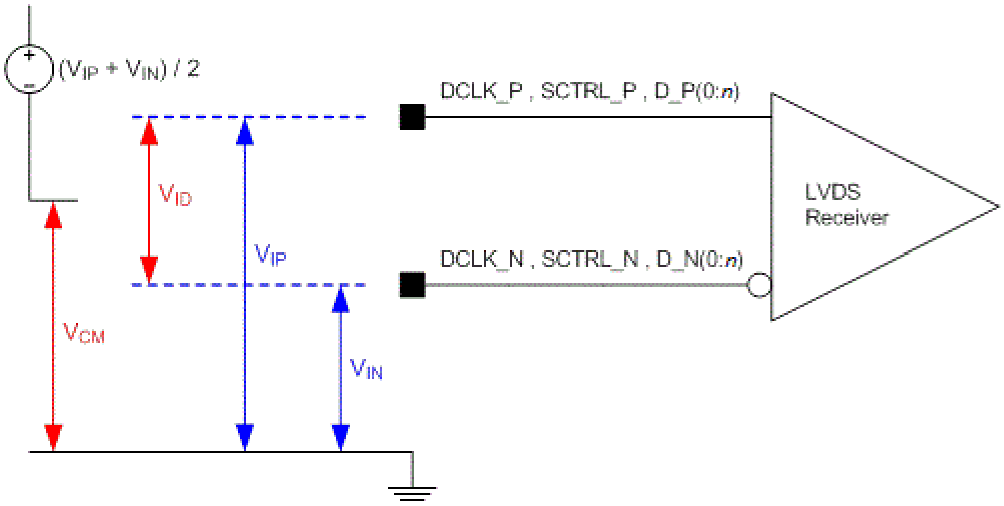


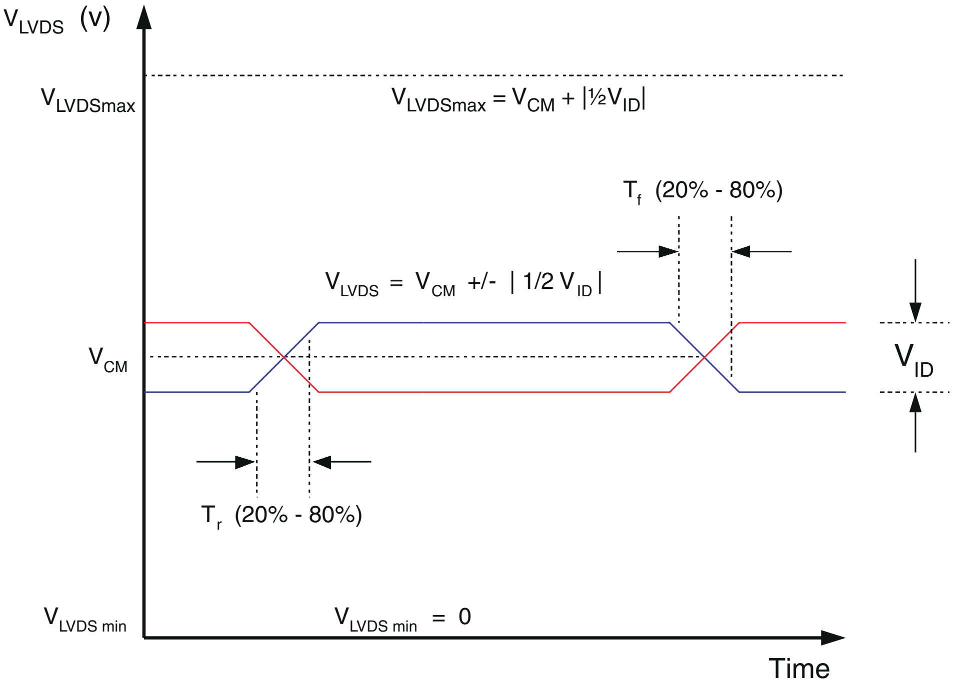
Figure 6-4. Serial Communications Bus Waveform Requirements



Refer to LVDS Interface section of the *Section 6.4*.

Refer to Pin Configuration and Functions for list of LVDS pins.

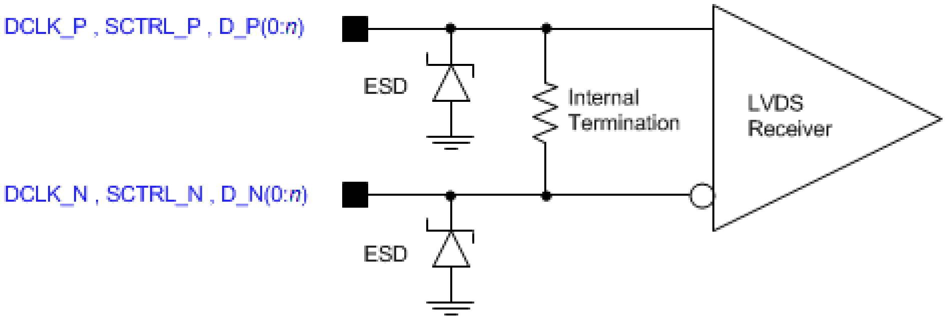
Figure 6-5. LVDS Voltage Definitions (References)



Not to scale.

Refer to the LVDS Interface section of the *Section 6.4*.

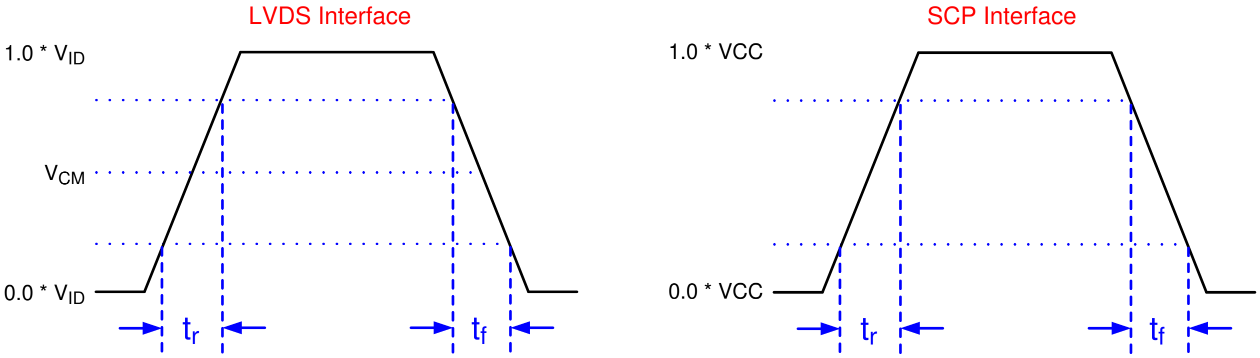
Figure 6-6. LVDS Waveform Requirements



Refer to the LVDS Interface section of the *Section 6.4*.

Refer to *Section 5* for a list of LVDS pins.

Figure 6-7. LVDS Equivalent Input Circuit



Not to scale.

Refer to the *Section 6.7*.

Refer to *Section 5* for a list of LVDS pins and SCP pins.

Figure 6-8. Rise Time and Fall Time

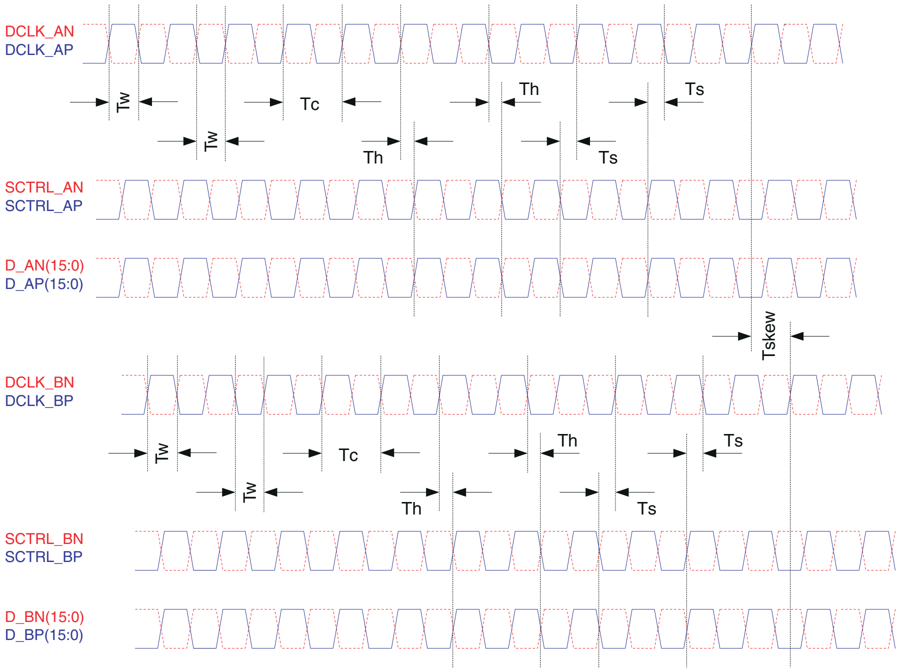


Figure 6-9. LVDS Timing Waveforms

6.8 System Mounting Interface Loads

PARAMETER			MIN	NOM	MAX	UNIT
Maximum system mounting interface load to be applied to the:	Thermal Interface area	Static load applied to the thermal interface area, See Figure 6-10			111	N
	Electrical Interface area	Static load applied to each electrical interface area no. 1 and no. 2, See Figure 6-10			55	N

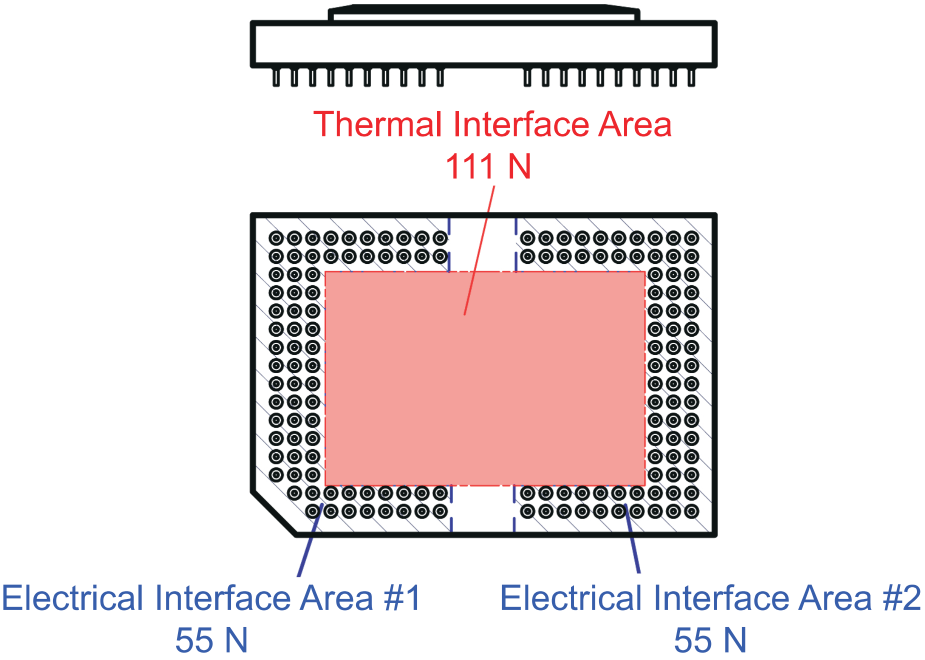


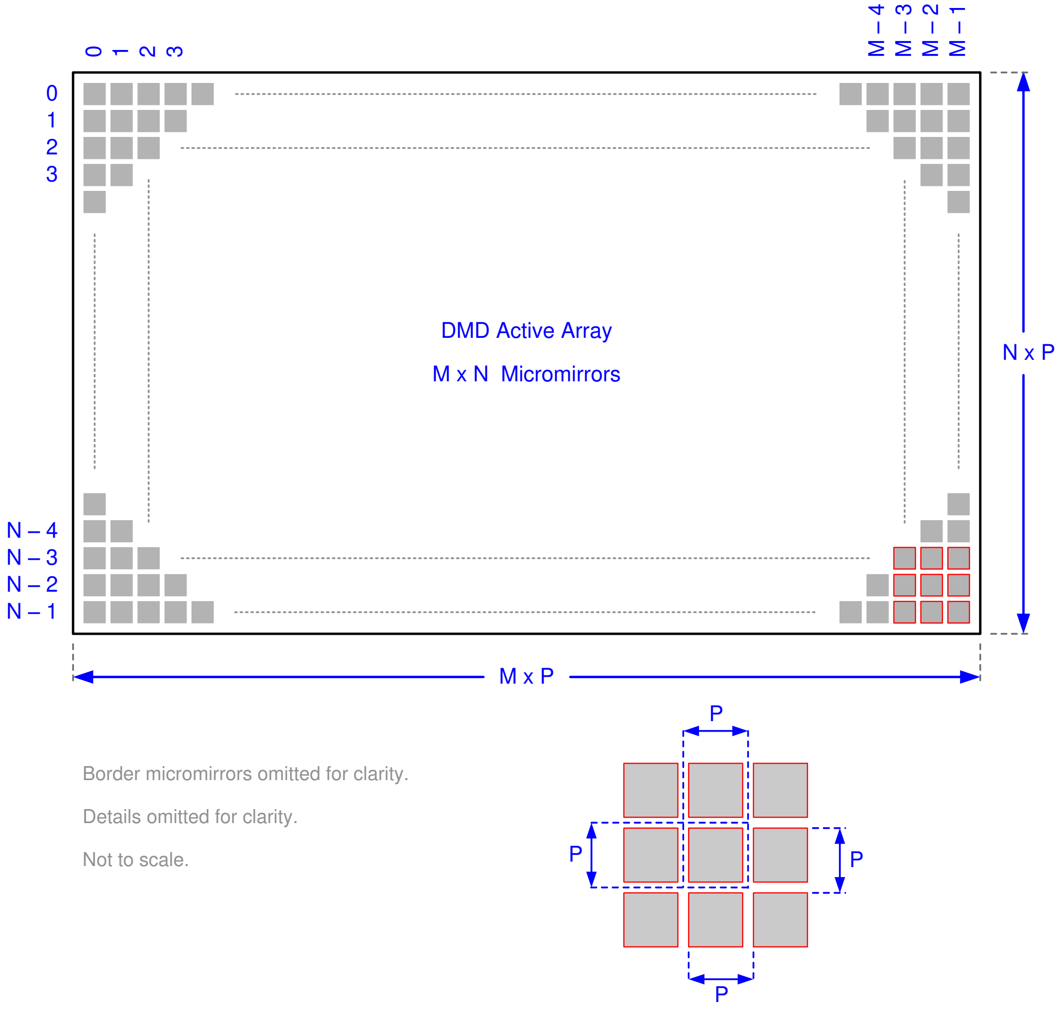
Figure 6-10. System Interface Loads

6.9 Micromirror Array Physical Characteristics

Additional details are provided in the *Section 13* section at the end of this document.

PARAMETER				VALUE	UNIT
M	Number of active micromirror columns		See Micromirror Array Physical Characteristics	1024	micromirrors
N	Number of active micromirror rows			768	
P	Micromirror pitch			10.8	µm
	Micromirror active array width	M × P		11.059	mm
	Micromirror active array height	N × P		8.294	mm
	Micromirror active array border	Pond of Micromirror (POM)(1)		10	micromirrors /side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors called the POM. These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.



Border micromirrors omitted for clarity.

Details omitted for clarity.

Not to scale.

Refer to the *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

Figure 6-11. Micromirror Array Physical Characteristics

6.10 Micromirror Array Optical Characteristics

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. See the Application Notes for additional details, considerations, and guidelines: *TI DLP® System Design: Optical Module Specifications*.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Micromirror tilt angle, **a**	DMD parked state(1) (2) (3), see Figure 7-3.		0		degrees
	DMD landed state(1) (4) (5), see Figure 7-3.		12		
Micromirror tilt angle variation, **b** (1) (4) (6) (7) (8)	See Figure 7-3.	–1		1	degrees
Micromirror Cross Over Time(10)			16	22	µs
Micromirror Switching Time(11)			140		µs
Non-operating micromirrors(12)	Non-adjacent micromirrors			10	micromirrors
	Adjacent micromirrors			0	
Orientation of the micromirror axis-of-rotation(9)	See .	44	45	46	degrees
Micromirror array optical efficiency(13) (14)	420 – 700, with all micromirrors in the ON state		68%		nm
Mirror metal specular reflectivity	420 – 700		89.4%		nm

(1) Measured relative to the plane formed by the overall micromirror array

(2) Parking the micromirror array returns all of the micromirrors to an essentially flat (0°) state (as measured relative to the plane formed by the overall micromirror array).

(3) When the micromirror array is parked, the tilt angle of each individual micromirror is uncontrolled.

(4) Additional variation exists between the micromirror array and the package datums, as shown in the packaging section at the end of the document.

(5) When the micromirror array is landed, the tilt angle of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 will result in a micromirror landing in an nominal angular position of +12 degrees. A binary value of 0 will result in a micromirror landing in an nominal angular position of –12 degrees.

(6) Represents the landed tilt angle variation relative to the Nominal landed tilt angle.

(7) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.

(8) For some applications, it is critical to account for the micromirror tilt angle variation in the overall System Optical Design. With some System Optical Designs, the micromirror tilt angle variations within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some System Optical Designs, the micromirror tilt angle variation between devices may result in colorimetry variations and/or system contrast variations.

(9) Measured relative to the package datums B and C, shown in the *Section 13* section at the end of this document.

(10) Micromirror Cross Over time is primarily a function of the natural response time of the micromirrors.

(11) Micromirror switching is controlled and coordinated by the DLPC200 (see DLPS014), DLPA200, and DLPS015). Nominal Switching time depends on the system implementation and represents the time for the entire micromirror array to be refreshed.

(12) Non-operating micromirror is defined as a micromirror that is unable to transition nominally from the –12 degree position to +12 degree or vice versa.

(13) The minimum or maximum DMD optical efficiency observed in a specific application depends on numerous application-specific design variables, such as but not limited to:

- Illumination wavelength, bandwidth or line-width, degree of coherence
- Illumination angle, plus angle tolerance
- Illumination and projection aperture size, and location in the system optical path
- Illumination overfill of the DMD micromirror array
- Aberrations present in the illumination source and/or path
- Aberrations present in the projection path

The specified nominal DMD optical efficiency is based on the following use conditions:

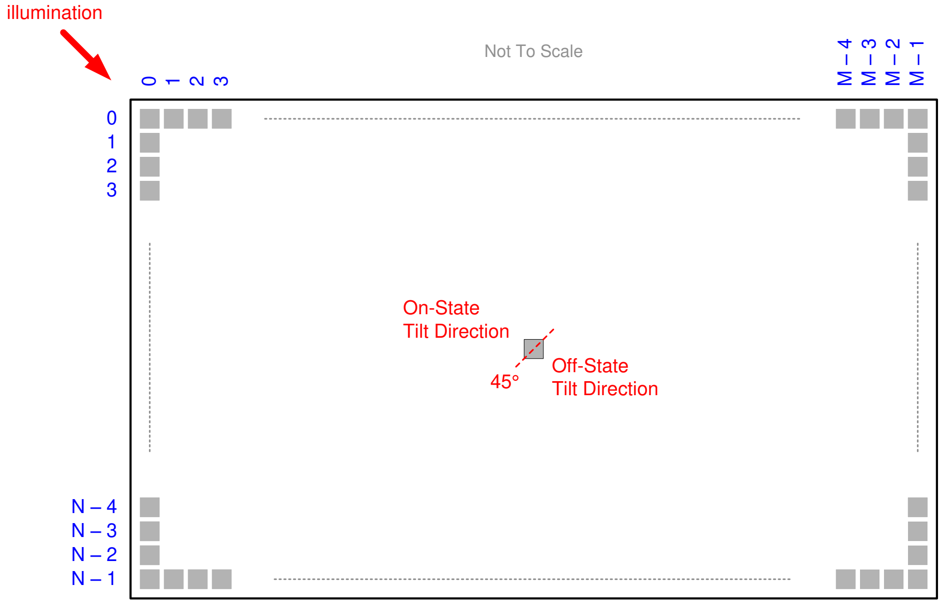
- Visible illumination (420nm – 700nm)
- Input illumination optical axis oriented at 24° relative to the window normal
- Projection optical axis oriented at 0° relative to the window normal
- f/3.0 illumination aperture
- f/2.4 projection aperture

Based on these use conditions, the nominal DMD optical efficiency results from the following four components:

- Micromirror array fill factor: nominally 92%
- Micromirror array diffraction efficiency: nominally 86%
- Micromirror surface reflectivity: nominally 88%

- Window transmission: nominally 97% (single pass, through two surface transitions)

(14) Does not account for the effect of micromirror switching duty cycle, which is application dependent. Micromirror switching duty cycle represents the percentage of time that the micromirror is actually reflecting light from the optical illumination path to the optical projection path. This duty cycle depends on the illumination aperture size, the projection aperture size, and the micromirror array update rate.



Refer to section *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

Figure 6-12. Micromirror Landed Orientation and Tilt

6.11 Window Characteristics

PARAMETER[1]	CONDITIONS	MIN	TYP	MAX	UNIT
Window material designation	Corning Eagle XG				
Window refractive index	at wavelength 546.1nm		1.5119		
Window aperture	See [2]				
Illumination overfill	Refer to *Section 7.5.4* section				
Window transmittance, single–pass through both surfaces and glass [3]	At wavelength 405nm. Applies to 0° and 24° AOI only	95%			
	Minimum within the wavelength range 420nm to 680nm. Applies to all angles 0° to 30° AOI	97%			
	Average over the wavelength range 420nm to 680nm. Applies to all angles 30° to 45° AOI	97%			

(1) See *Section 7.5* for more information.
(2) For details regarding the size and location of the window aperture, see the package mechanical characteristics listed in the Mechanical ICD in the Mechanical, Packaging, and Orderable Information section.
(3) See the TI application report *Wavelength Transmittance Considerations for DLP® DMD Window* DLPA031.

6.12 Chipset Component Usage Specification

The DLP5500 is a component of one or more DLP chipsets. Reliable function and operation of the DLP5500 requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

7 Detailed Description

7.1 Overview

DLP5500 is a 0.55 inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. Pixel array size and square grid pixel arrangement are shown in Figure 6-11.

The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is Low Voltage Differential Signaling (LVDS), Double Data Rate (DDR).

DLP5500 DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of *M* memory cell columns by *N* memory cell rows. Refer to the *Functional Block Diagram*.

The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

Each cell of the $M \times N$ memory array drives its true and complement (‘Q’ and ‘QB’) data to two electrodes underlying one micromirror, one electrode on each side of the diagonal axis of rotation. Refer to *Figure 7-3*. The micromirrors are electrically tied to the micromirror reset signals (MBRST) and the micromirror array is divided into reset groups.

Electrostatic potentials between a micromirror and its memory data electrodes cause the micromirror to tilt toward the illumination source in a DLP projection system or away from it, thus reflecting its incident light into or out of an optical collection aperture. The positive (+) tilt angle state corresponds to an 'on' pixel, and the negative (–) tilt angle state corresponds to an 'off' pixel.

Refer to *Micromirror Array Optical Characteristics* for the ± tilt angle specifications. Refer to the *Pin Configuration and Functions* for more information on micromirror clocking pulse (reset) control.

7.2 Functional Block Diagram

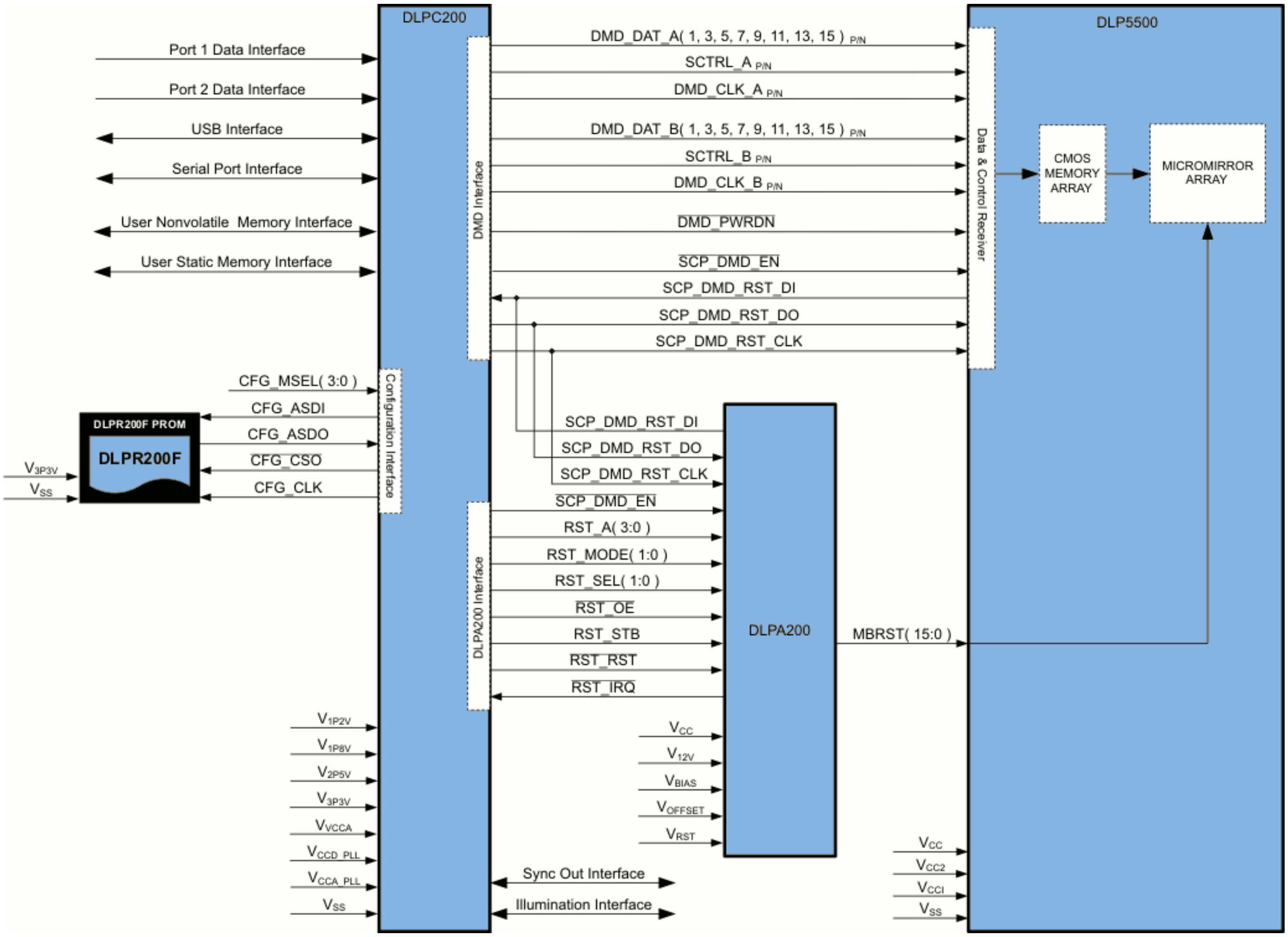


Figure 7-1. Functional Block Diagram

7.3 Feature Description

The DLP5500 device consists of 786,432 highly reflective, digitally switchable, micrometer-sized mirrors (micromirrors) organized in a two-dimensional orthogonal pixel array. Refer to Figure 6-11 and Figure 7-2.

Each aluminum micromirror is switchable between two discrete angular positions, –**a** and +**a**. The angular positions are measured relative to the micromirror array plane, which is parallel to the silicon substrate. Refer to *Micromirror Array Optical Characteristics* and Figure 7-3.

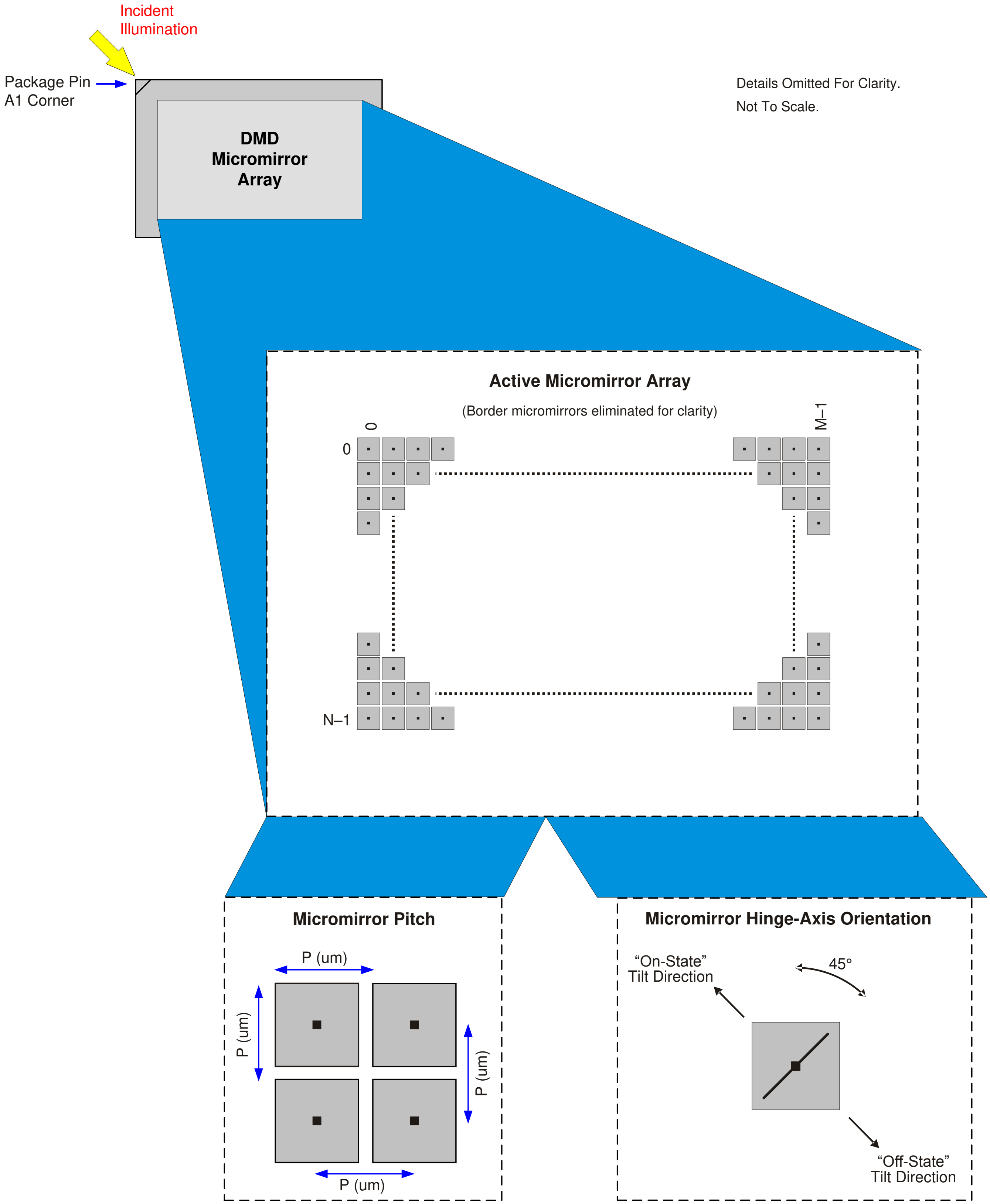
The parked position of the micromirror is not a latched position and is therefore not necessarily perfectly parallel to the array plane. Individual micromirror flat state angular positions may vary. Tilt direction of the micromirror is perpendicular to the hinge-axis. The on-state landed position is directed toward the left-top edge of the package, as shown in Figure 7-2.

Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the mirror clocking pulse is applied. The angular position (–**a** and +**a**) of the individual micromirrors changes synchronously with a micromirror clocking pulse, rather than being coincident with the CMOS memory cell data update.

Writing logic 1 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to the +**a** position. Writing logic 0 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to the – **a** position.

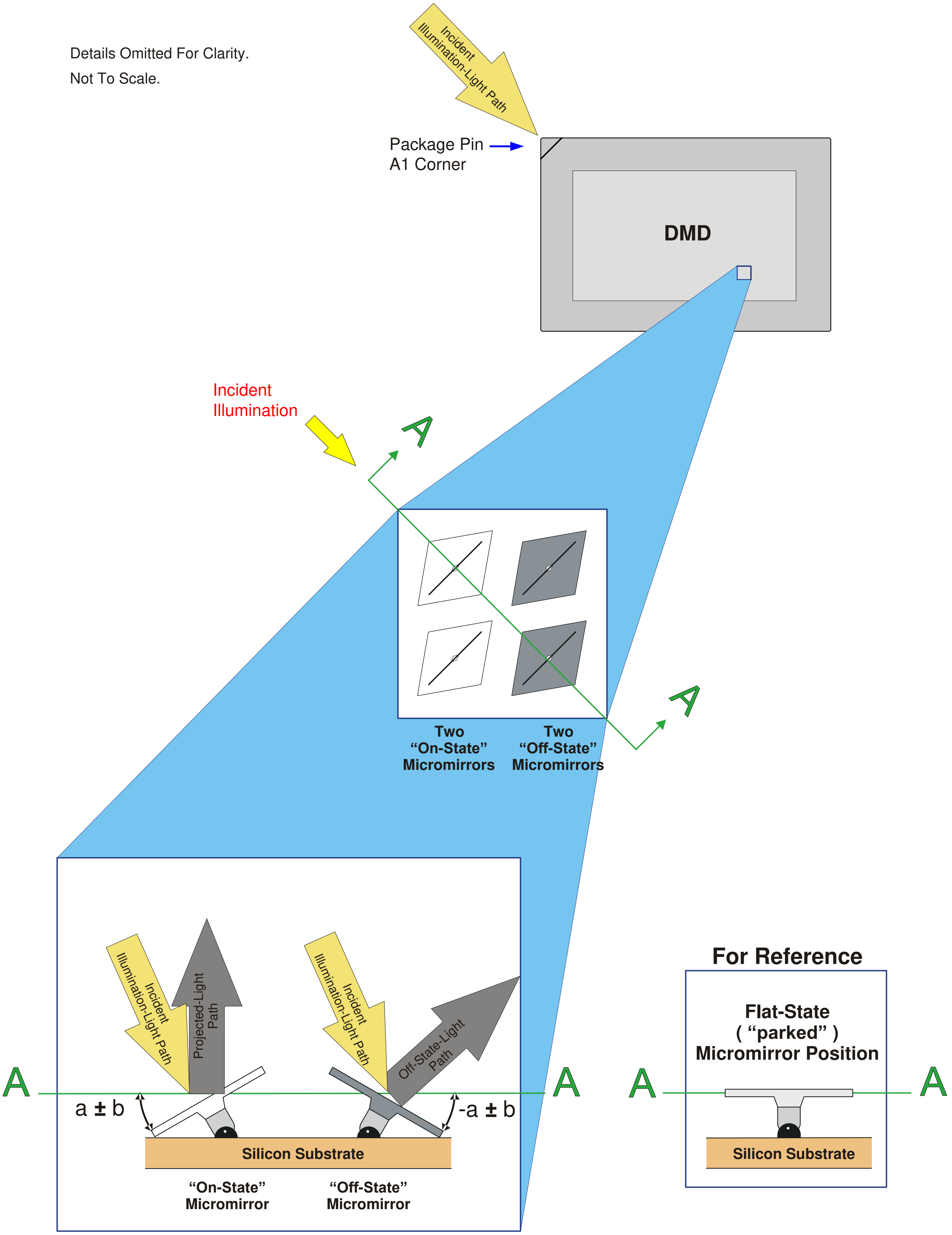
Updating the angular position of the micromirror array consists of two steps. First, update the contents of the CMOS memory. Second, apply a micromirror clocking pulse (reset) to all or a portion of the micromirror array (depending upon the configuration of the system). Micromirror reset pulses are generated externally by the DLPC200 controller in conjunction with the DLPA200 analog driver, with application of the pulses being coordinated by the DLPC200 controller.

For more information, see the TI application report DLPA008, *DMD101: Introduction to Digital Micromirror Device (DMD) Technology*.



Refer to Figure 6-11 and Figure 6-12.

Figure 7-2. Micromirror Array, Pitch, Hinge Axis Orientation



Micromirror States: On, Off, Flat

Figure 7-3. Micromirror States: On, Off, Flat

7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC200 digital display controller. See the DLPC200 data sheet listed in *Section 11.3*. Contact a TI applications engineer for more information.

The DLPC200 provides two basic functional mode types to control the DLP5500 DMD: video and structured light.

7.4.1 Video Modes

The controller accepts RGB-8-8-8 input to port 1 or port 2 through a selectable MUX. XGA video information is displayed on the DMD at 6 to 60fps.

An internal pattern generator can generate RGB-8-8-8 video patterns into an internal selectable MUX for verification and debug purposes.

7.4.2 Structured Light Modes

The DLPC200 provides two structured light modes: static image buffer and real-time structured light.

7.4.2.1 Static Image Buffer Mode

Image data can be loaded into parallel flash memory to load to DDR2 memory at startup to be displayed, or can be loaded over USB or the SPI port directly to DDR2 memory to be displayed. Binary (1-bit) or grayscale (8-bit) patterns can be displayed. The memory will hold 960 binary patterns or 120 grayscale patterns.

Binary (1-bit) patterns can be displayed at up to 5000 binary patterns per second. These patterns assume a constant illumination and do not depend on illumination modulation

Grayscale (8-bit) patterns assume illumination modulation in order to achieve higher pattern rates. When the pattern rate requires that the lower significant bit(s) be shorter than the rate that the DMD can be switched, these bits will require the source to be modulated to achieve the shorter time required. The trade-off is dark time during these bits. At the maximum 500 Hz grayscale pattern rate, the dark time approaches 75%.

7.4.2.2 Real Time Structured Light Mode

RGB-8-8-8 60fps data can be input into port 1 or port 2 and reinterpreted as up to 24 binary (1-bit) patterns or three grayscale (8-bit) patterns. The specified number of patterns is displayed equally during the exposure time specified. Any unused RGB-8-8-8 data in the video frame must be filled with data, usually 0s.

For example, during one video frame (16.67ms), 12 binary patterns of the 24 RGB bits are requested to be displayed during half of the video frame time (exposure time = 8.33ms). Each of the eight red bits and the four most significant green bits are displayed as a binary pattern for 694µs each. The remaining bits are ignored and the remaining 8.33ms of the frame will be dark.

7.5 Window Characteristics and Optics

Note

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

7.5.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance with the optical system operating conditions described in the following sections.

7.5.2 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area should be the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

7.5.3 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° (two degrees) of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

7.5.4 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. The illumination optical system should be designed to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

7.6 Micromirror Array Temperature Calculation

Achieving optimal DMD performance requires proper management of the maximum DMD case temperature, the maximum temperature of any individual micromirror in the active array, the maximum temperature of the window aperture, and the temperature gradient between the case temperature and the predicted micromirror array temperature (see Figure 7-4).

Refer to the *Recommended Operating Conditions* for applicable temperature limits.

7.6.1 Package Thermal Resistance

The DMD is designed to conduct absorbed and dissipated heat to the back of the Series 450 package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the specified operational temperatures, refer to Figure 7-4. The total heat load on the DMD is typically driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array.

7.6.2 Case Temperature

The temperature of the DMD case can be measured directly. For consistency, Thermal Test Point locations TP1 – TP5 are defined, as shown in Figure 7-4.

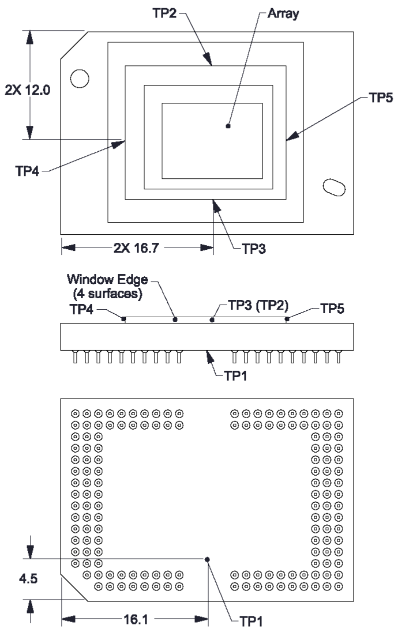


Figure 7-4. Thermal Test Point Location

7.6.3 Micromirror Array Temperature Calculation for Uniform Illumination

Micromirror array temperature cannot be measured directly; therefore it must be computed analytically from measurement points (Figure 7-4), the package thermal resistance, the electrical power, and the illumination heat load. The relationship between micromirror array temperature and the case temperature are provided by Equation 1 and Equation 2:

$$T_{Array} = T_{Ceramic} + (Q_{Array} \times R_{Array\text{-}To\text{-}Ceramic}) \qquad (1)$$

$$Q_{Array} = Q_{ELE} + Q_{ILL} \qquad (2)$$

Where the following elements are defined as:

- T_{Array} = computed micromirror array temperature (°C)
- $T_{Ceramic}$ = Ceramic temperature (°C) (TC2 Location Figure 7-4)
- Q_{Array} = Total DMD array power (electrical + absorbed) (measured in Watts)
- $R_{Array\text{-}To\text{-}Ceramic}$ = thermal resistance of DMD package from array to TC2 (°C/Watt) (see *Section 7.6.1*)
- Q_{ELE} = Nominal electrical power (Watts)
- Q_{ILL} = Absorbed illumination energy (Watts)

An example calculation is provided below based on a traditional DLP Video projection system. The electrical power dissipation of the DMD is variable and depends on the voltages, data rates, and operating frequencies. The nominal electrical power dissipation to be used in the calculation is 2.0 Watts. Thus, Q_{ELE} = 2.0 Watts. The absorbed power from the illumination source is variable and depends on the operating state of the mirrors and the intensity of the light source. It's based on modeling and measured data from DLP projection system.

$$Q_{ILL} = C_{L2W} \times SL \qquad (3)$$

Where:

- C_{L2W} is a Lumens to Watts constant, and can be estimated at 0.00274 Watt/Lumen
- SL = Screen Lumens nominally measured to be 2000 lumens
- Qarray = 2.0 + (0.00274 x 2000) = 7.48 watts, Estimated total power on micromirror Array
- $T_{Ceramic}$ = 55°C, assumed system measurement

- T_{Array}(micromirror active array temperature) = 55°C + (7.48 watts x 0.6 °C/watt) = 59.5°C

For additional explanation of DMD Mechanical and Thermal calculations and considerations please refer to *DLP Series-450 DMD and System Mounting Concepts* (DLPA015).

7.7 Micromirror Landed-on/Landed-Off Duty Cycle

7.7.1 Definition of Micromirror Landed-On/Landed-Off Duty Cycle

The micromirror landed-on/landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the On–state versus the amount of time the same micromirror is landed in the Off–state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the On-state 100% of the time (and in the Off-state 0% of the time); whereas 0/100 would indicate that the pixel is in the Off-state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (On or Off), the two numbers (percentages) always add to 100.

7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD’s micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD’s usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD’s usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the DMD’s usable life. This is quantified in the de-rating curve shown in Figure 6-1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the Maximum Operating DMD Temperature that the DMD should be operated at for a give long-term average Landed Duty Cycle.

7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given period of time, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel will experience a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel will experience a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in Table 7-1.

Table 7-1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100

Table 7-1. Grayscale Value and Landed Duty Cycle (continued)

GRAYSCALE VALUE	LANDED DUTY CYCLE
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where “color cycle time” is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated as follows:

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_\%} \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_\%} \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_\%} \times \text{Blue\_Scale\_Value}) \quad (4)$$

where

- Red_Cycle_%, Green_Cycle_%, and Blue_Cycle_%, represent the percentage of the frame time that Red, Green, and Blue are displayed (respectively) to achieve the desired white point.

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities would be as shown in Table 7-2.

Table 7-2. Example Landed Duty Cycle for Full-Color

Red Cycle Percentage 50%	Green Cycle Percentage 20%	Blue Cycle Percentage 30%	Landed Duty Cycle
Red Scale Value	**Green Scale Value**	**Blue Scale Value**	
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DLP5500 (0.55-inch XGA DMD) is controlled by the DLPC200 contoller in conjunction with the DLPA200 driver. This combination can be used for a number of applications from 3D printers to microscopes.

The most common application is for 3D structured light measurement applications. In this application, patterns (binary, grayscale, or even full color) are projected onto the target and the distortion of the patterns are recorded by an imaging device to extract 3D (x, y, z) surface information.

8.2 Typical Application

A schematic is shown in Figure 8-1 for projecting RGB and IR structured light patterns onto a measurement target. Typically, an imaging device is triggered through one of the three syncs to record the data as each pattern is displayed.

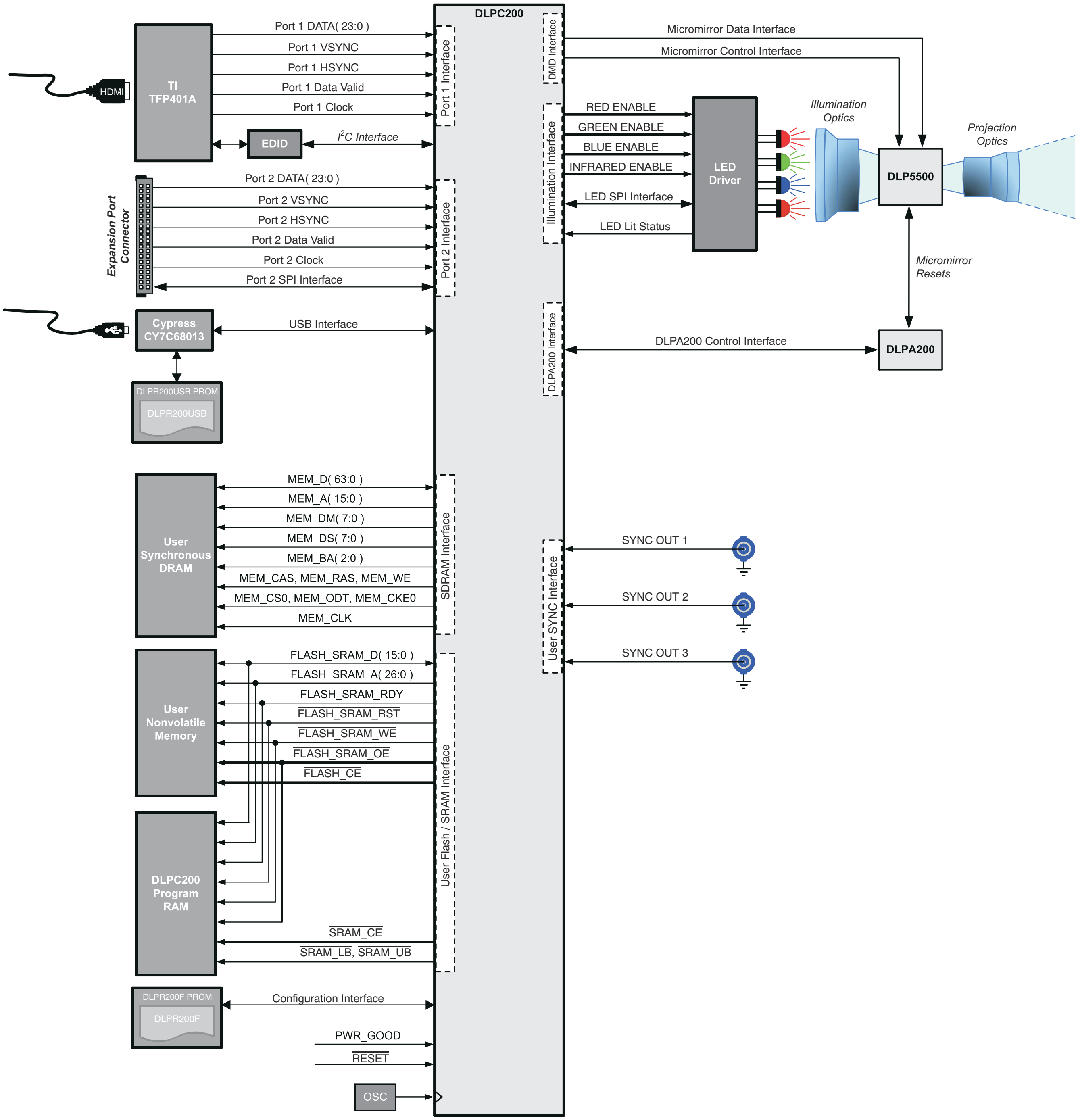


Figure 8-1. Typical RGB + IR Structured Light Application

8.2.1 Design Requirements

All applications using the DLP 0.55-inch XGA chipset require the DLPC200 controller, the DLPA200 driver, and the DLP5500 DMD for correct operation. The system also requires user supplied SRAM and a configuration PROM programmed with the DLPR200F program file and a 50MHz oscillator is for operation. For further details, refer to the DLPC200 controller data sheet (DLPS014) and the DLPA200 analog driver data sheet (DLPS015).

8.2.2 Detailed Design Procedure

8.2.2.1 DLP5500 System Interface

Images are displayed on the DLP5500 via the DLPC200 controller and the DLPA200 driver. The DLP5500 interface consists of a 200MHz (nominal) half-bus DDR input-only interface with LVDS signaling. The serial communications port (SCP), 125kHz nominal, is used by the DLPC200 to read or write control data to both the DLP5500 and the DLPA200. The following listed signals support data transfer to the DLP5500 and DLPA200.

- DMD, 200MHz
  - DMD_CLK_AP, DMD_CLK_AN – DMD clock for A
  - DMD_CLK_BP, DMD_CLK_BN – DMD clock for B
  - DMD_DAT_AP, DMD_DAT_AN(1, 3, 5, 7, 9, 11, 13, 15) – Data bus A (odd-numbered pins are used for half-bus)
  - DMD_DAT_BP, DMD_DAT_BN(1, 3, 5, 7, 9, 11, 13, 15) – Data bus B (odd-numbered pins are used for half-bus)
  - DMD_SCRTL_AP, DMD_SCRTL_AN – S-control for A
  - DMD_SCRTL_BP, DMD_SCRTL_BN – S-control for B
- DLPA200, 125kHz
  - SCP_DMD_RST_CLK – SCP clock
  - SCP_DMD_EN – Enable DMD communication
  - SCP_RST_EN – Enable DLPA200 communication
  - SCP_DMD_RST_DI – Input data
  - SCP_DMD_RST_DO – Output data

9 Power Supply Recommendations

9.1 DMD Power-Up and Power-Down Procedures

The DLP5500 power-up and power-down procedures are defined by the DLPC200 data sheet (DLPS012) and the *0.55 XGA Chipset* data sheet (DLPZ004). These procedures must be followed to ensure reliable operation of the device.

CAUTION

Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability.

10 Layout

10.1 Layout Guidelines

The DLP5500 is part of a chipset that is controlled by the DLPC200 in conjunction with the DLPA200. These guidelines are targeted at designing a PCB board with these components.

10.1.1 Impedance Requirements

Signals should be routed to have a matched impedance of 50Ω ±10% except for LVDS differential pairs (DMD_DAT_Xnn, DMD_DCKL_Xn, and DMD_SCTRL_Xn) and DDR2 differential clock pairs (MEM_CLK_nn), which should be matched to 100Ω ±10% across each pair.

10.1.2 PCB Signal Routing

When designing a PCB board for the DLP5500 controlled by the DLPC200 in conjunction with the DLPA200, the following are recommended:

Signal trace corners should be no sharper than 45°. Adjacent signal layers should have the predominate traces routed orthogonal to each other. TI recommends that critical signals be hand routed in the following order: DDR2 Memory, DMD (LVDS signals), then DLPA200 signals.

TI does not recommend signal routing on power or ground planes.

TI does not recommend ground plane slots.

High-speed signal traces should not cross over slots in adjacent power and ground planes.

Table 10-1. LVDS Trace Constraints

Signal	Constraints
LVDS (DMD_DAT_xnn, DMD_DCKL_xn, and DMD_SCTRL_xn)	P-to-N data, clock, and SCTRL: <10mil (0.25mm); Pair-to-pair <10mil (0.25mm); Bundle-to-bundle <2000mil (50mm, for example DMD_DAT_Ann to DMD_DAT_Bnn). All matching should include internal trace lengths. See *Section 5* for internal package trace lengths. Trace width: 4mil (0.1mm) Trace spacing: In ball field – 4mil (0.11mm); PCB etch – 14mil (0.36mm) Maximum recommended trace length <6 inches (150mm)

Table 10-2. Power and Mirror Clocking Pulse Trace Widths and Spacing

Signal Name	Minimum Trace Width	Minimum Trace Spacing	Layout Requirements
GND	Maximize	5mil (0.13mm)	Maximize trace width to connecting pin as a minimum
VCC, VCC2	20mil (0.51mm)	10mil (0.25mm)	
MBRST[15:0]	10mil (0.25mm)	10mil (0.25mm)	

10.1.3 Fiducials

Fiducials for automatic component insertion should be 0.05-inch copper with a 0.1-inch cutout (antipad). Fiducials for optical auto insertion are placed on three corners of both sides of the PCB.

10.2 Layout Example

For LVDS (and other differential signal) pairs and groups, it is important to match trace lengths. In the area of the dashed lines, Figure 10-1 shows correct matching of signal pair lengths with serpentine sections to maintain the correct impedance.

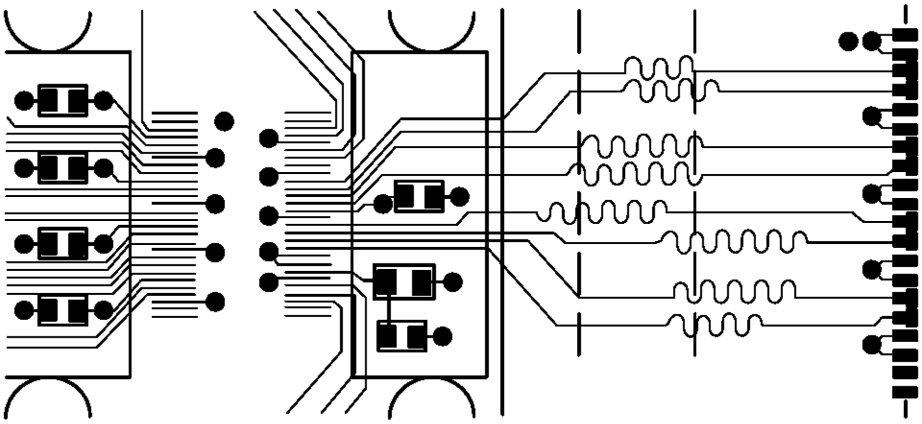


Figure 10-1. Mitering LVDS Traces to Match Lengths

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

The device marking consists of the fields shown in Figure 11-1.

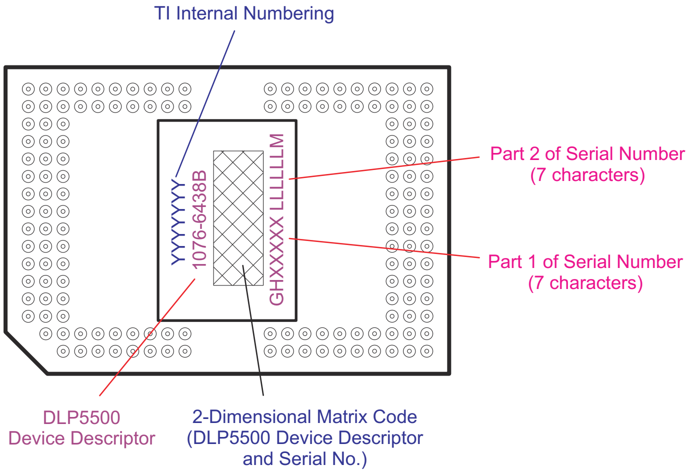


Figure 11-1. DMD Marking (Device Top View)

11.2 Documentation Support

11.2.1 Related Documentation

The following documents contain additional information related to the use of the DLP5500 device:

- DLP 0.55 XGA Chip-Set data sheet DLPZ004
- DLPC200 Digital Controller data sheet DLPS014
- DLPA200 DMD Analog Reset Driver DLPS015
- DLP Series-450 DMD and System Mounting Concepts DLPA015
- DLPC200 API Reference Manual DLPA024
- DLPC200 API Programmer's Guide DLPA014
- s4xx DMD Cleaning Application Note DLPA025
- s4xx DMD Handling Application Note DLPA019

11.3 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
DLPA200	Click here	Click here	Click here	Click here	Click here
DLPC200	Click here	Click here	Click here	Click here	Click here
DLPC900	Click here	Click here	Click here	Click here	Click here

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

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is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Revision History

Changes from Revision G (January 2019) to Revision H (December 2024)	Page
• Added pattern rates for the DLPC900 controller	1
• Added hyperlink to the *TI DLP® System Design: Optical Module Specifications* application note	17
• Added DLPC900 related documents	35

Changes from Revision F (May 2015) to Revision G (December 2018)	Page
• Changed DMD Marking Image Object for Figure 11-1	35

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP5500BFYA	ACTIVE	CPGA	FYA	149	5	RoHS & Green	NI-PD-AU	N / A for Pkg Type	-20 to 90		Samples
DLPA200PFP	ACTIVE	HTQFP	PFP	80	5	TBD	Call TI	Call TI	0 to 75		Samples
DLPC200ZEW	ACTIVE	BGA	ZEW	780	5	TBD	Call TI	Call TI	-20 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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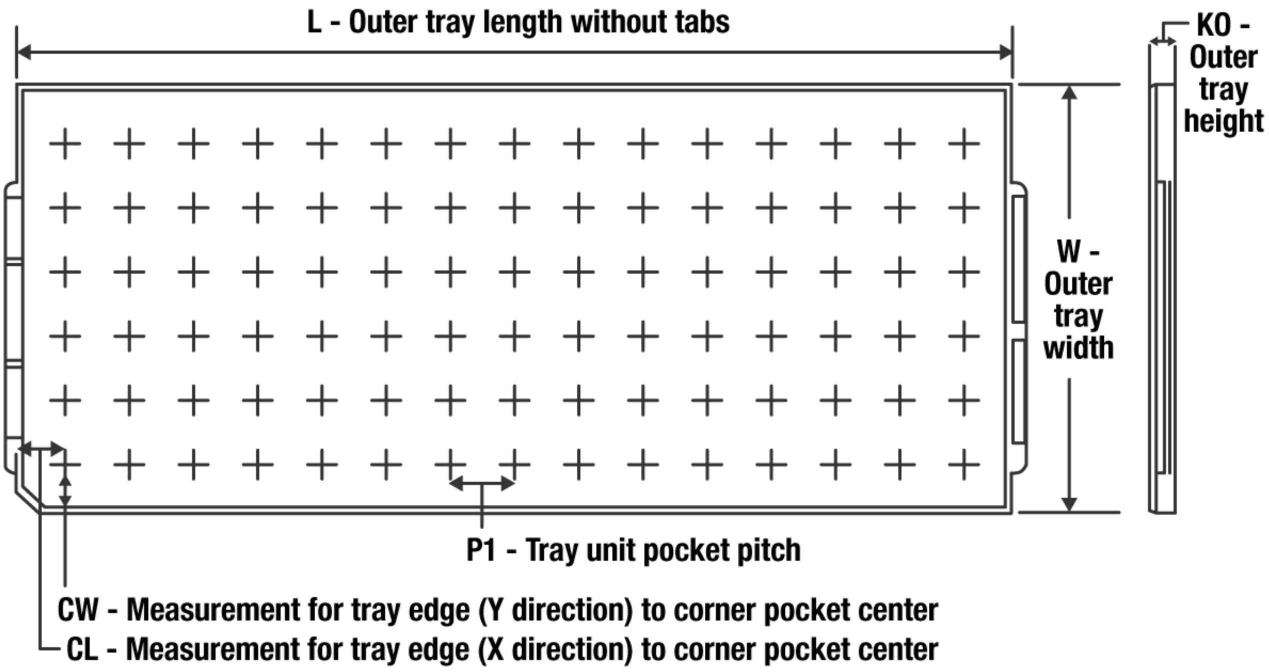
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY

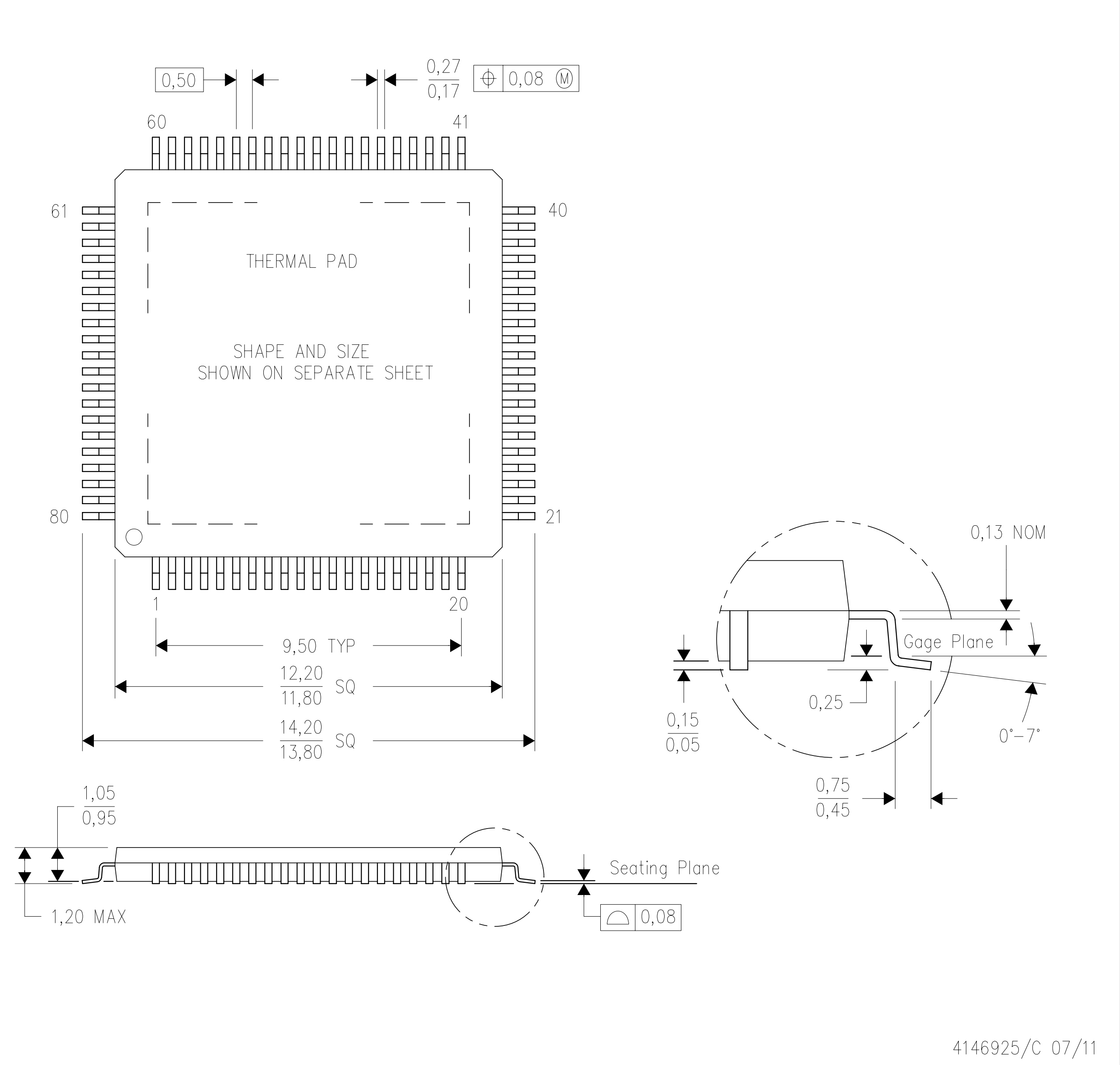


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP5500BFYA	FYA	CPGA	149	5	3 x 11	150	315	135.9	12190	27.5	20	27.45

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

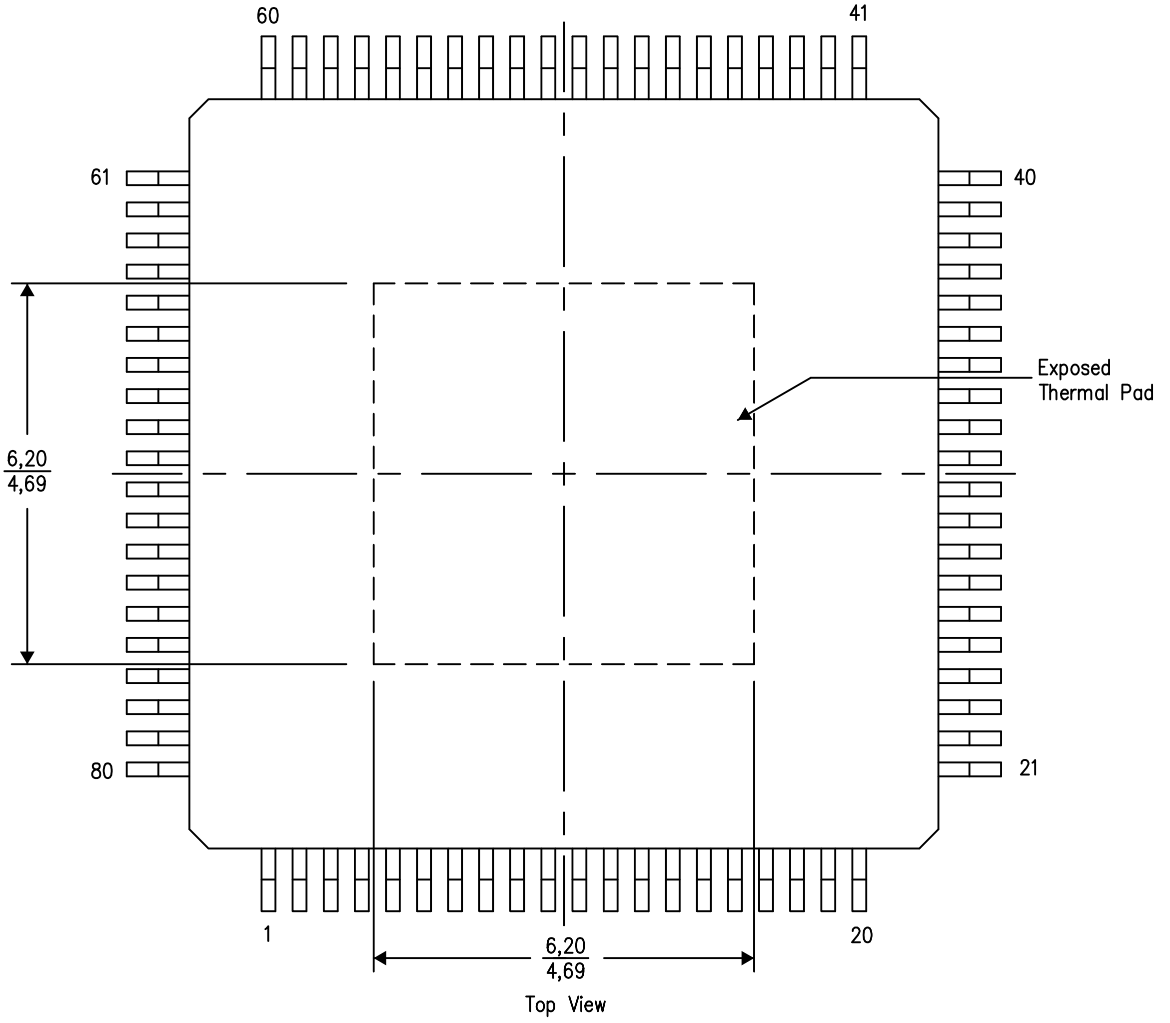
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

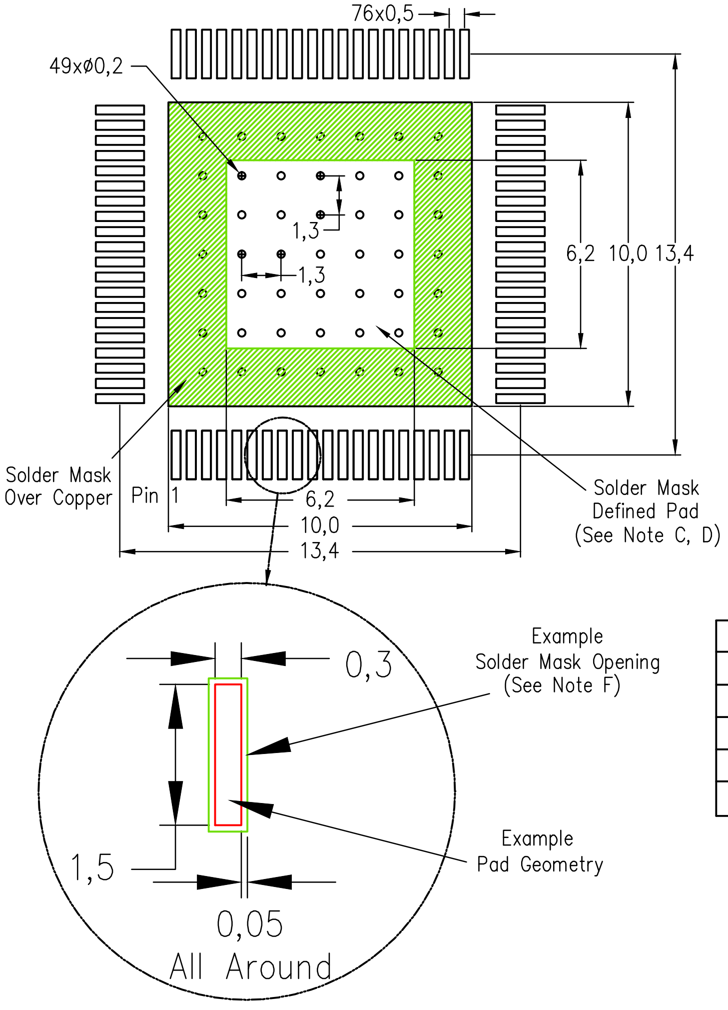
4206327–3/P 05/14

NOTE: A. All linear dimensions are in millimeters

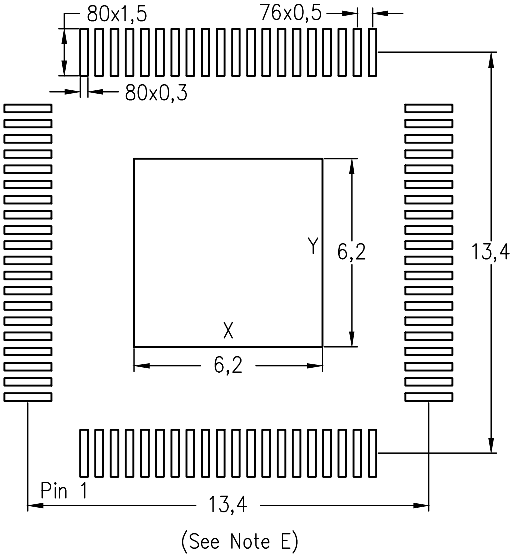
PowerPAD is a trademark of Texas Instruments

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

Example Board Layout
Via pattern and copper area under solder mask
may vary depending on layout constraints



Stencil Openings
Based on a stencil thickness
of .125mm (.005inch).
Reference table below for other
solder stencil thicknesses



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.93	6.93
0.125mm	6.2	6.2
0.15mm	5.66	5.66
0.175mm	5.24	5.24

4208544-3/G 02/16

PowerPAD is a trademark of Texas Instruments.

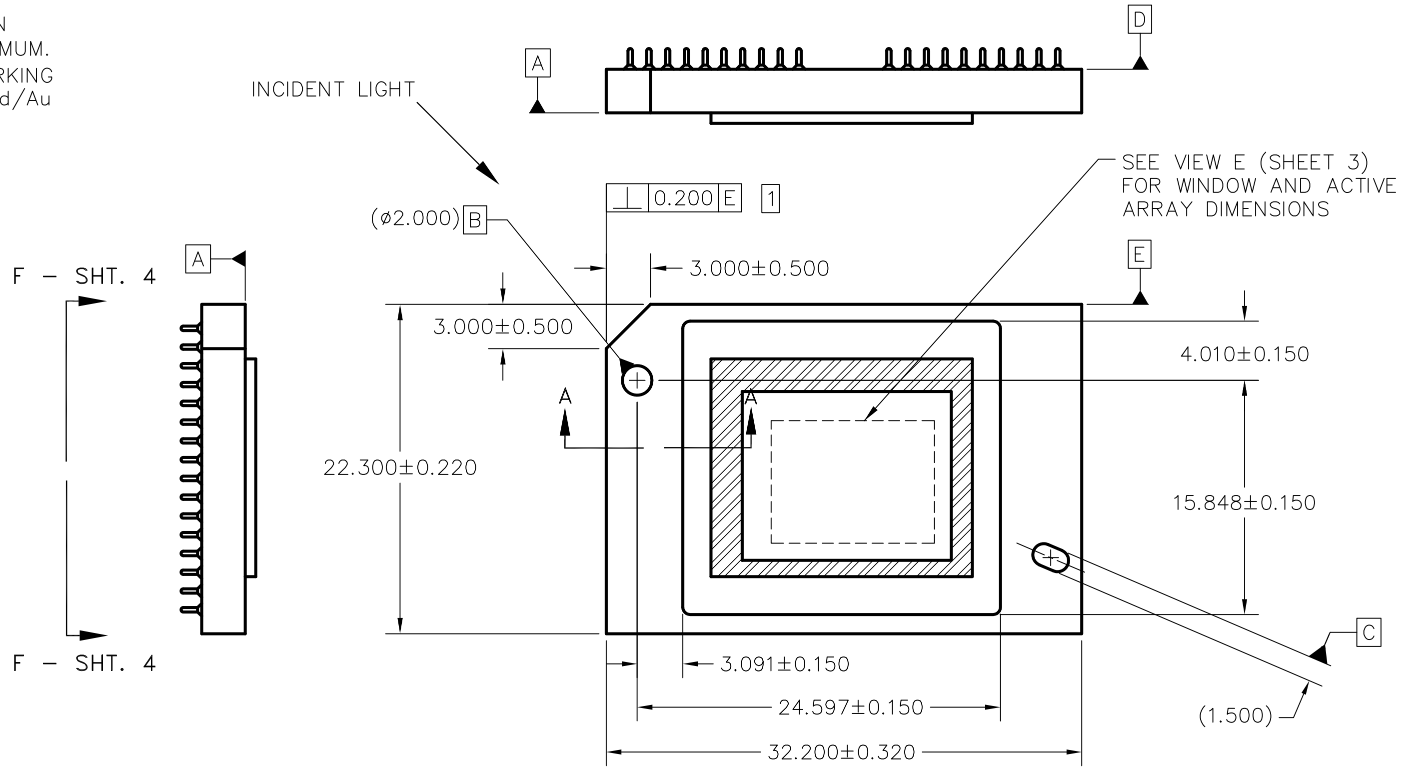
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

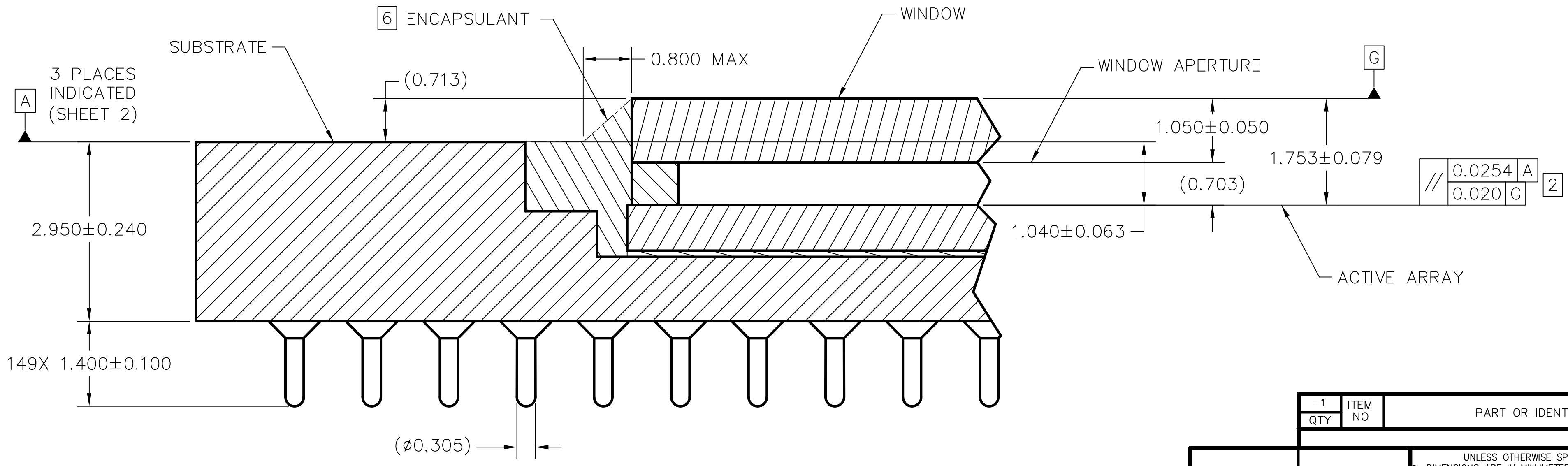
REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2121693, INITIAL RELEASE	01/17/2012	F. ARMSTRONG
B	ECO 2123271, CHG TO LARGE SYMBOLIZATION PAD	03/16/2012	F. ARMSTRONG
C	ECO 2135103, ADD NOTE 8 TO SHEETS 1 & 4	08/02/2013	F. ARMSTRONG
D	ECO 2168422, ADD FYA PACKAGE TO TITLE	08/17/17	M. AVERY

NOTES: UNLESS OTHERWISE SPECIFIED:

1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES TO BE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
5. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
6. MAXIMUM ENCAPSULANT PROFILE SHOWN
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
8. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.





SECTION A–A
SCALE 20/1

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5–1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

DWN	F. ARMSTRONG	DATE 01/17/12
ENGR	F. ARMSTRONG	01/17/12
QA	P. KONRAD	01/19/12
CQE	M. DORAK	01/19/12

NEXT ASSY	USED ON
NONE	0314DA

APPLICATION

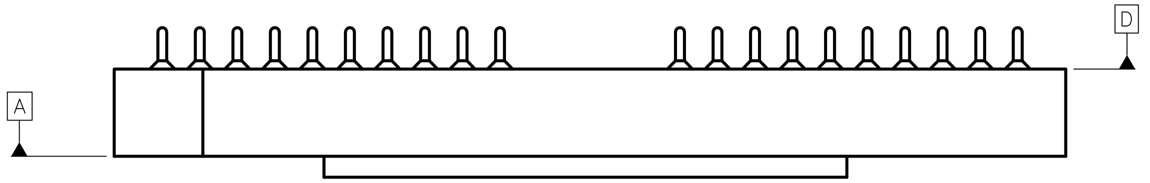
THIRD ANGLE PROJECTION

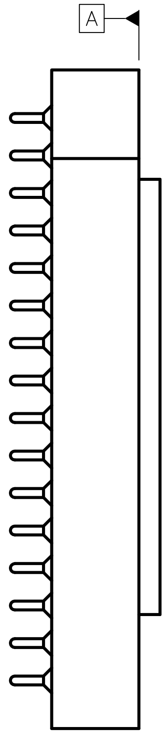
TEXAS INSTRUMENTS
Dallas, Texas

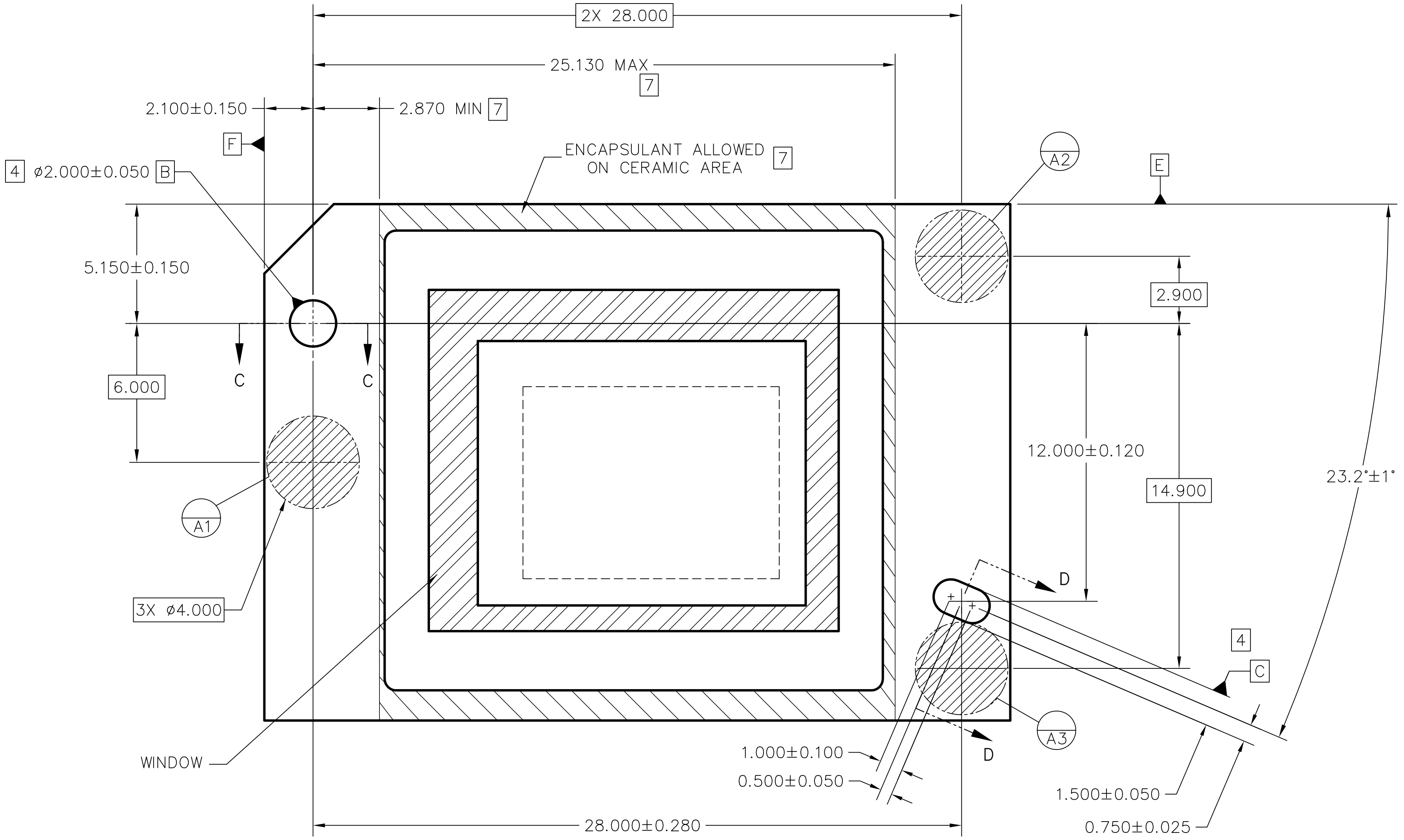
ICD, MECHANICAL, DMD
.55" XGA 2xLVDS V2 SERIES 450
(FYA PACKAGE)

SIZE	DRAWING NO	REV
B	2512194	D

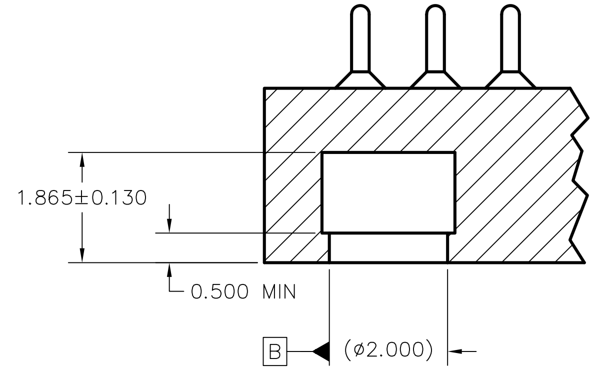
SCALE 4/1 SHEET 1 OF 4



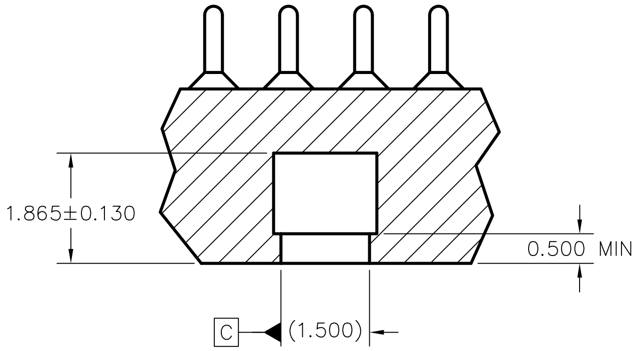




VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1



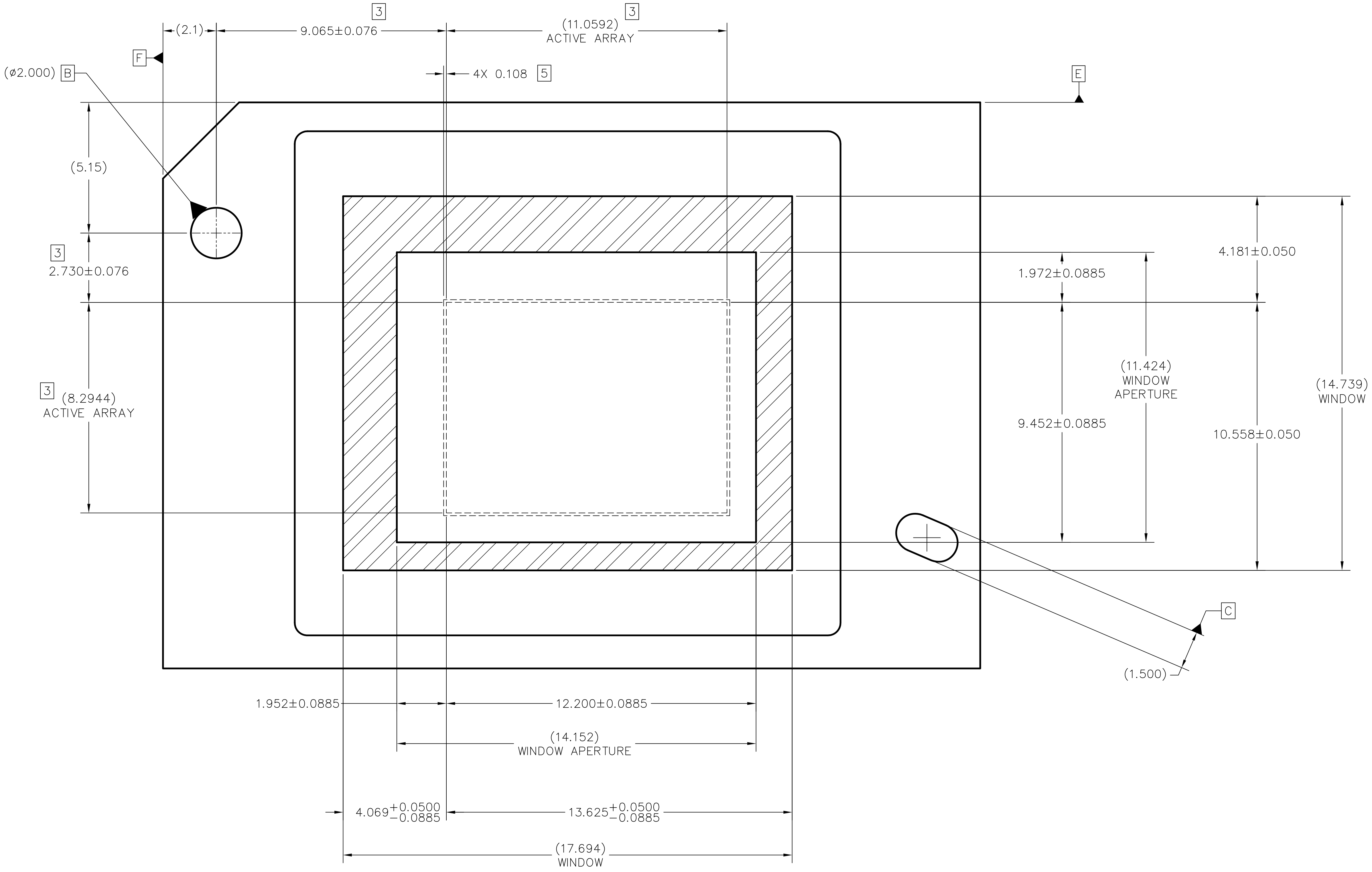
SECTION C–C
DATUM B
SCALE 16/1



SECTION D–D
DATUM C
SCALE 16/1

TEXAS INSTRUMENTS
Dallas, Texas

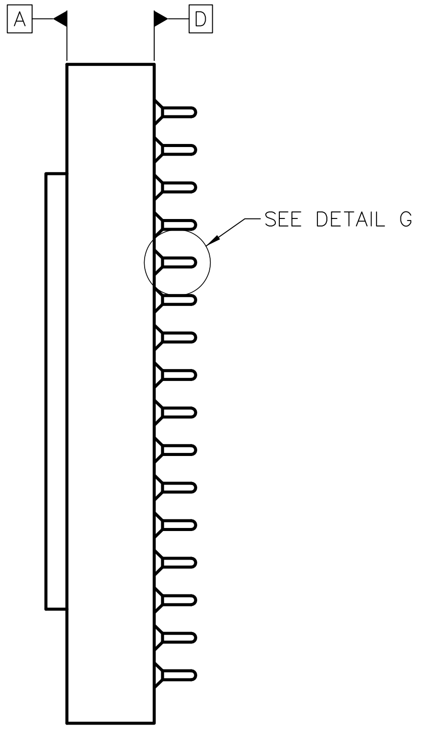
DWN	DATE	
ISSUE DATE		
SIZE B	DRAWING NO 2512194	REV D
SCALE 4/1		SHEET 2

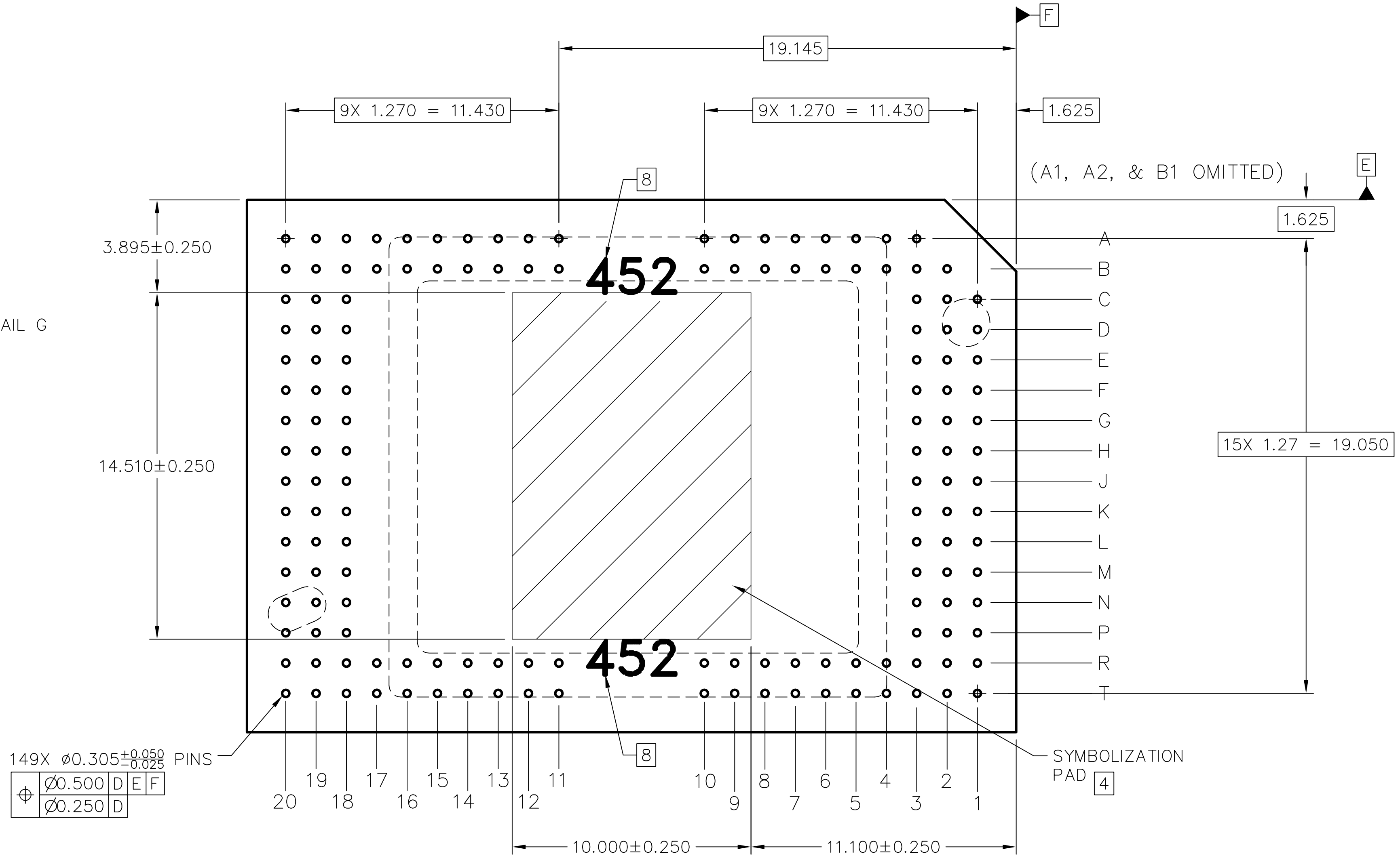


VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12:1

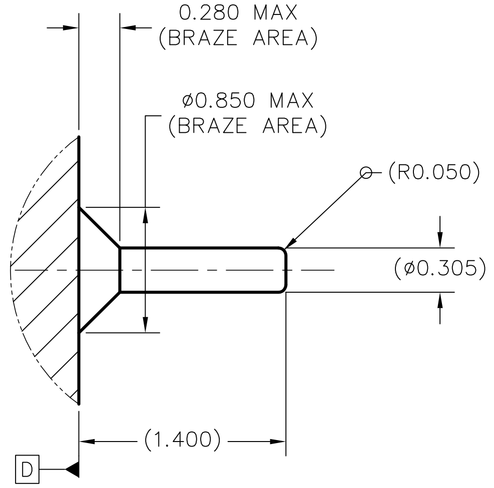
TEXAS INSTRUMENTS Dallas, Texas	DWN DATE ISSUE DATE	SIZE B SCALE 4/1	DRAWING NO 2512194 SHEET 3	REV D

ACED2c





VIEW F–F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1

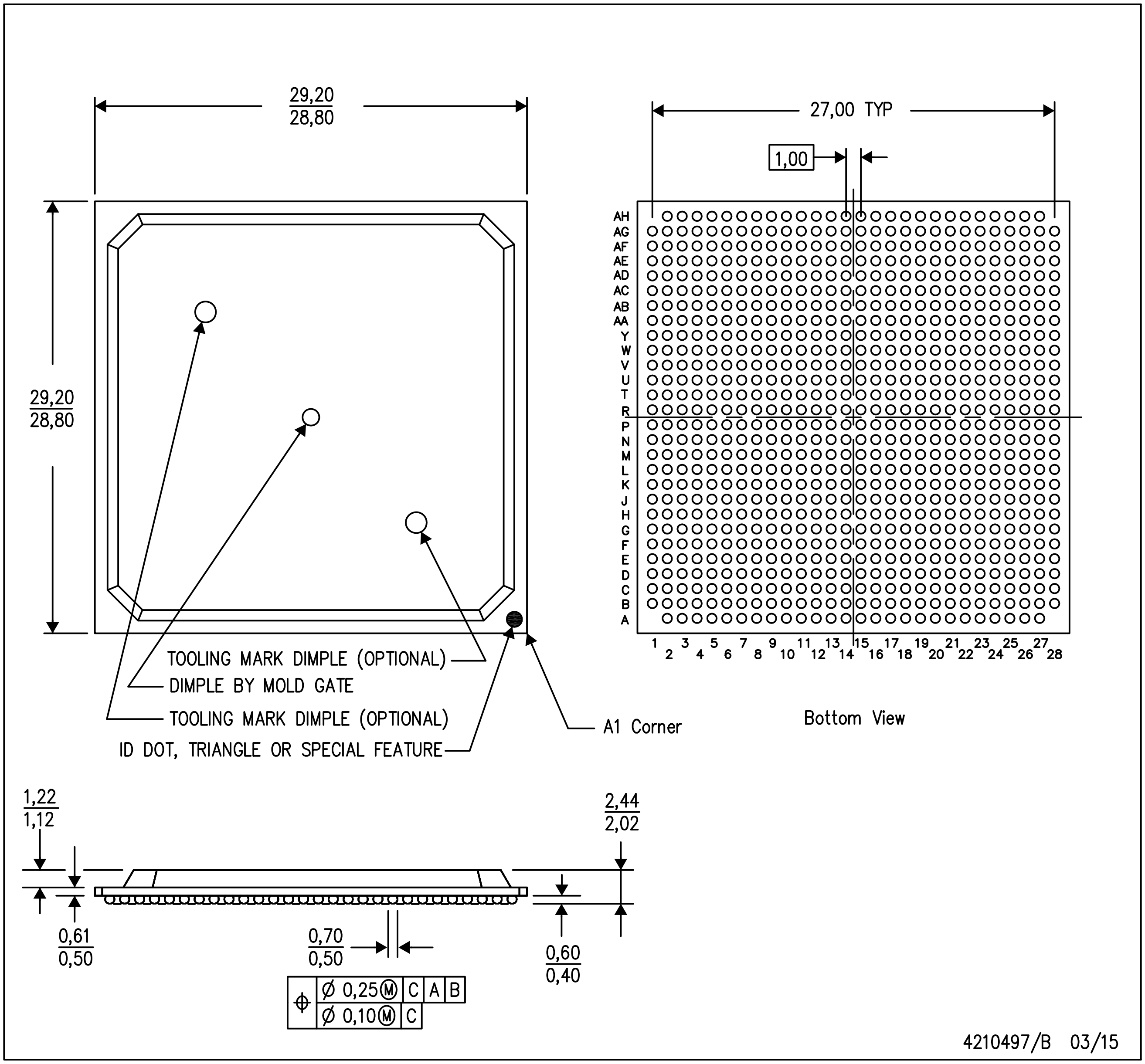


DETAIL G (149 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1

TEXAS INSTRUMENTS
Dallas, Texas

DWN	DATE	SIZE	DRAWING NO	REV
ISSUE DATE		B	2512194	D
		SCALE 4/1	SHEET 4	

ZEW (S–PBGA–N780) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–034, Variation: AAM–1.
D. This package is Pb–free.

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