

# DLP650NE 0.65 1080p Digital Micromirror Device

## 1 Features

- 0.65-inch micromirror array diagonal
  - 1080p (1920 × 1080)
  - 7.56-micron micromirror pitch
  - ± 12° micromirror tilt angle (relative to flat state)
  - Corner illumination
- 2xLVDS input data bus
- The DLP650NE chipset includes:
  - [DLP470TE DMD](#)
  - [DLPC4430 controller](#)
  - [DLPA100 controller power management and motor driver IC](#)

## 2 Applications

- [Full HD \(1080p\) display](#)
- [Laser TV](#)
- [Mobile smart TV](#)
- [Digital signage](#)
- [Gaming](#)
- [Home cinema](#)

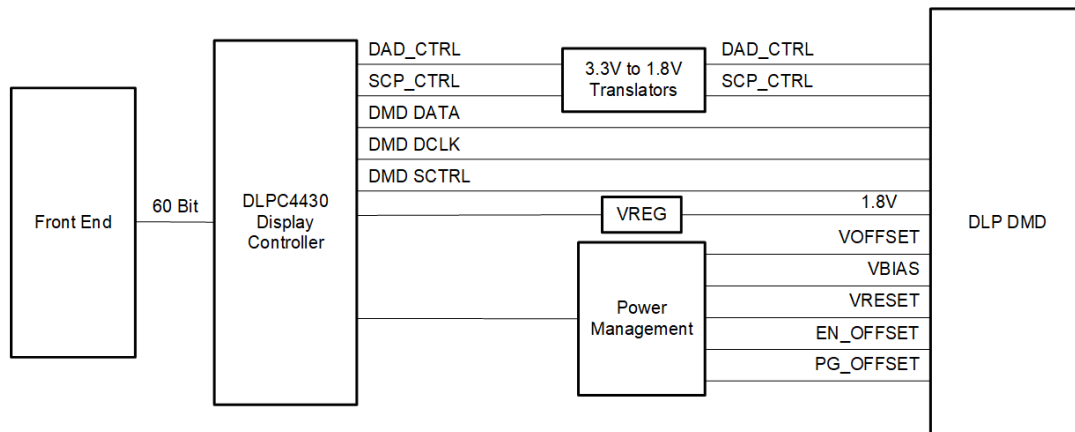
## 3 Description

The TI DLP650NE [digital micromirror device \(DMD\)](#) is a digitally controlled micro-electromechanical system (MEMS) spatial light modulator (SLM) that enables bright, affordable DLP® 0.65 1080p display solutions. The DLP650NE DMD—together with the DLPC4430 display controller and the DLPA100 power manager and motor driver—provides the capability to achieve high performance systems, and is a great fit for display applications that require high resolution and 16:9 aspect ratio, high brightness, and system simplicity.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
DLP650NE	FYE (350)	35.0 mm × 32.2 mm × 5.1 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**DLP650NE Simplified Application**



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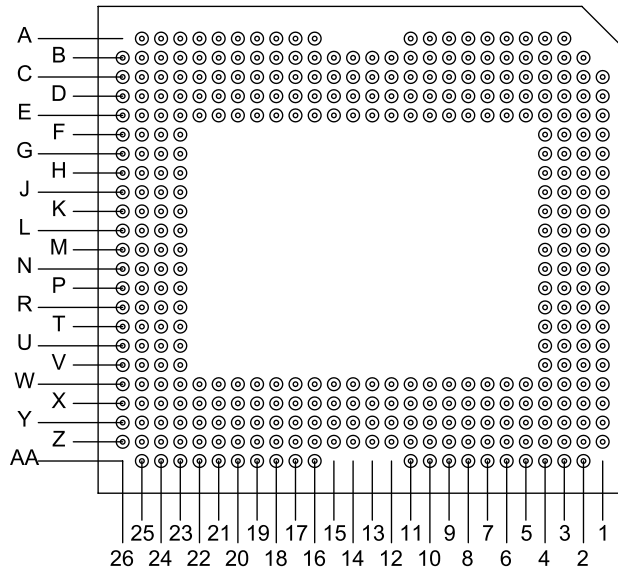
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision * (August 2017) to Revision A (February 2023)</b>	<b>Page</b>
• This document is updated per the latest Texas Instruments and industry data sheet standards. Updated the controller to DLPC4430. Updated the links to chipset components.....	1
• Updated the controller to DLPC4430.....	1
• Added typical values to $I_{\text{OFFSET}}$ , $I_{\text{BIAS}}$ , and $I_{\text{RESET}}$ currents. Removed DLPA4000, not supported.....	14
• Updated controller to DLPC4430.....	22
• Changed device supported modes for technical accuracy.....	24
• Updated <i>DMD Thermal Test Points</i> illustration.....	25
• Updated controller to DLPC4430.....	26
• Removed DLPA4000, not supported as PMIC. Added a table with additional legacy device information and referenced the mechanical ICD.....	29
• Updated controller to DLPC4430.....	29
• Updated <i>Typical DLPC4430 Application</i> schematic.....	30
• Updated controller to DLPC4430.....	32
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• Updated the controller to DLPC4430 and the related documentation.....	36

## 5 Pin Configuration and Functions



**Figure 5-1. FYE Package 350-Pin Bottom View**

**Table 5-1. Pin Functions**

PIN <sup>(1)</sup>		TYPE <sup>(5)</sup>	SIGNAL	DATA RATE <sup>(2)</sup>	INTERNAL TERM <sup>(3)</sup>	DESCRIPTION	TRACE (mils) <sup>(4)</sup>
NAME	NO.						
<b>DATA BUS A</b>							
D_AN(0)	B14	I	LVDS	DDR	Differential	Data, negative	494.88
D_AN(1)	B15	I		DDR	Differential	Data, negative	486.18
D_AN(2)	C16	I		DDR	Differential	Data, negative	495.16
D_AN(3)	K24	I		DDR	Differential	Data, negative	485.67
D_AN(4)	B18	I		DDR	Differential	Data, negative	494.76
D_AN(5)	L24	I		DDR	Differential	Data, negative	490.63
D_AN(6)	C19	I		DDR	Differential	Data, negative	495.16
D_AN(7)	H24	I		DDR	Differential	Data, negative	485.55
D_AN(8)	H23	I		DDR	Differential	Data, negative	495.16
D_AN(9)	B25	I		DDR	Differential	Data, negative	485.59
D_AN(10)	D24	I		DDR	Differential	Data, negative	495.16
D_AN(11)	E25	I		DDR	Differential	Data, negative	495.16
D_AN(12)	F25	I		DDR	Differential	Data, negative	490.04
D_AN(13)	H25	I		DDR	Differential	Data, negative	485.91
D_AN(14)	L25	I		DDR	Differential	Data, negative	495.16
D_AN(15)	G24	I		DDR	Differential	Data, negative	495.16

**Table 5-1. Pin Functions (continued)**

PIN <sup>(1)</sup>		TYPE <sup>(5)</sup>	SIGNAL	DATA RATE <sup>(2)</sup>	INTERNAL TERM <sup>(3)</sup>	DESCRIPTION	TRACE (mils) <sup>(4)</sup>
NAME	NO.						
D_AP(0)	C14	I	LVDS	DDR	Differential	Data, positive	494.84
D_AP(1)	B16	I		DDR	Differential	Data, positive	486.22
D_AP(2)	C17	I		DDR	Differential	Data, positive	494.65
D_AP(3)	K23	I		DDR	Differential	Data, positive	488.42
D_AP(4)	B19	I		DDR	Differential	Data, positive	495.16
D_AP(5)	L23	I		DDR	Differential	Data, positive	490.67
D_AP(6)	C20	I		DDR	Differential	Data, positive	498.11
D_AP(7)	J24	I		DDR	Differential	Data, positive	486.22
D_AP(8)	J23	I		DDR	Differential	Data, positive	495.47
D_AP(9)	C25	I		DDR	Differential	Data, positive	485.94
D_AP(10)	E24	I		DDR	Differential	Data, positive	495.16
D_AP(11)	D25	I		DDR	Differential	Data, positive	494.13
D_AP(12)	G25	I		DDR	Differential	Data, positive	488.98
D_AP(13)	J25	I		DDR	Differential	Data, positive	492.56
D_AP(14)	K25	I		DDR	Differential	Data, positive	495.16
D_AP(15)	F24	I		DDR	Differential	Data, positive	495.16
<b>DATA BUS B</b>							
D_BN(0)	Z14	I	LVDS	DDR	Differential	Data, negative	494.92
D_BN(1)	Z15	I		DDR	Differential	Data, negative	486.18
D_BN(2)	Y16	I		DDR	Differential	Data, negative	496.46
D_BN(3)	P24	I		DDR	Differential	Data, negative	493.74
D_BN(4)	Z18	I		DDR	Differential	Data, negative	494.76
D_BN(5)	N24	I		DDR	Differential	Data, negative	495.16
D_BN(6)	Y19	I		DDR	Differential	Data, negative	492.16
D_BN(7)	T24	I		DDR	Differential	Data, negative	492.68
D_BN(8)	T23	I		DDR	Differential	Data, negative	484.45
D_BN(9)	Z25	I		DDR	Differential	Data, negative	492.09
D_BN(10)	X24	I		DDR	Differential	Data, negative	497.72
D_BN(11)	W25	I		DDR	Differential	Data, negative	495.16
D_BN(12)	V25	I		DDR	Differential	Data, negative	484.17
D_BN(13)	T25	I		DDR	Differential	Data, negative	481.42
D_BN(14)	N25	I		DDR	Differential	Data, negative	495.16
D_BN(15)	U24	I		DDR	Differential	Data, negative	489.8

**Table 5-1. Pin Functions (continued)**

PIN <sup>(1)</sup>		TYPE <sup>(5)</sup>	SIGNAL	DATA RATE <sup>(2)</sup>	INTERNAL TERM <sup>(3)</sup>	DESCRIPTION	TRACE (mils) <sup>(4)</sup>
NAME	NO.						
D_BP(0)	Y14	I	LVDS	DDR	Differential	Data, positive	494.88
D_BP(1)	Z16	I		DDR	Differential	Data, positive	486.26
D_BP(2)	Y17	I		DDR	Differential	Data, positive	495.16
D_BP(3)	P23	I		DDR	Differential	Data, positive	492.48
D_BP(4)	Z19	I		DDR	Differential	Data, positive	495.16
D_BP(5)	N23	I		DDR	Differential	Data, positive	497.99
D_BP(6)	Y20	I		DDR	Differential	Data, positive	495.16
D_BP(7)	R24	I		DDR	Differential	Data, positive	492.05
D_BP(8)	R23	I		DDR	Differential	Data, positive	484.45
D_BP(9)	Y25	I		DDR	Differential	Data, positive	492.24
D_BP(10)	W24	I		DDR	Differential	Data, positive	495.16
D_BP(11)	X25	I		DDR	Differential	Data, positive	494.72
D_BP(12)	U25	I		DDR	Differential	Data, positive	483.78
D_BP(13)	R25	I		DDR	Differential	Data, positive	489.13
D_BP(14)	P25	I		DDR	Differential	Data, positive	499.53
D_BP(15)	V24	I		DDR	Differential	Data, positive	488.66
<b>SERIAL CONTROL</b>							
SCTRL_AN	C23	I	LVDS	DDR	Differential	Serial control, negative	492.95
SCTRL_BN	Y23	I		DDR	Differential	Serial control, negative	493.78
SCTRL_AP	C24	I		DDR	Differential	Serial control, negative	493.78
SCTRL_BP	Y24	I		DDR	Differential	Serial control, negative	493.11
<b>CLOCKS</b>							
DCLK_AN	B23	I	LVDS		Differential	Clock, negative	480.35
DCLK_BN	Z23	I			Differential	Clock, negative	486.22
DCLK_AP	B22	I			Differential	Clock, negative	485.83
DCLK_BP	Z22	I			Differential	Clock, negative	491.93
<b>SERIAL COMMUNICATIONS PORT (SCP)</b>							
SCP_DO	B8	O	LVCMOS	SDR		Serial communications port output	
SCP_DI	B7	I		SDR		Serial communication port data I	
SCP_CLK	B6	I			Pulldown	Serial communications port clock	
SCP_ENZ	C8	I				Active-low serial communications port enable	

**Table 5-1. Pin Functions (continued)**

PIN <sup>(1)</sup>		TYPE <sup>(5)</sup>	SIGNAL	DATA RATE <sup>(2)</sup>	INTERNAL TERM <sup>(3)</sup>	DESCRIPTION	TRACE (mils) <sup>(4)</sup>
NAME	NO.						
<b>MICROMIRROR RESET CONTROL</b>							
RESET_ADDR(0)	X9	I	LVCMOS		Pulldown	Reset driver address select	
RESET_ADDR(1)	X8	I				Reset driver address select	
RESET_ADDR(2)	Z8	I				Reset driver address select	
RESET_ADDR(3)	Z7	I				Reset driver address select	
RESET_MODE(0)	W11	I				Reset driver mode select	
RESET_MODE(1)	Z10	I				Reset driver mode select	
RESET_SEL(0)	Y10	I				Reset driver level select	
RESET_SEL(1)	Y9	I				Reset driver level select	
RESET_STROBE	Y7	I				Reset address, mode, and level latched on rising-edge	
<b>ENABLES AND INTERRUPTS</b>							
PWRDNZ	D2	I	LVCMOS		Pulldown	Active-low device reset	
RESET_OEZ	W7	I			Pulldown	Active-low output enable for DMD reset driver circuits	
RESETZ	Z6	I			Pulldown	Active-low sets reset circuits in known VOFFSET state	
RESET_IRQZ	Z5	O				Active-low, output interrupt to ASIC	
<b>VOLTAGE REGULATOR MONITORING</b>							
PG_BIAS	E11	I	LVCMOS		Pullup	Active-low fault from external VBIAS regulator	
PG_OFFSET	B10	I				Active-low fault from external VOFFSET regulator	
PG_RESET	D11	I				Active low from external VRESET regulator	
EN_BIAS	D9	O			Active-high enable for external VBIAS regulator		
EN_OFFSET	C9	O			Active-high enable for external VOFFSET regulator		
EN_RESET	E9	O			Active-high enable for external VRESET regulator		

**Table 5-1. Pin Functions (continued)**

PIN <sup>(1)</sup>		TYPE <sup>(5)</sup>	SIGNAL	DATA RATE <sup>(2)</sup>	INTERNAL TERM <sup>(3)</sup>	DESCRIPTION	TRACE (mils) <sup>(4)</sup>		
NAME	NO.								
<b>LEAVE PIN UNCONNECTED</b>									
MBRST(0)	C2	O	Analog		Pulldown	For proper DMD operation, do not connect.			
MBRST(1)	C3	O							
MBRST(2)	C5	O							
MBRST(3)	C4	O							
MBRST(4)	E5	O							
MBRST(5)	E4	O							
MBRST(6)	E3	O							
MBRST(7)	G4	O							
MBRST(8)	G3	O							
MBRST(9)	G2	O							
MBRST(10)	J4	O							
MBRST(11)	J3	O							
MBRST(12)	J2	O							
MBRST(13)	L4	O							
MBRST(14)	L3	O							
MBRST(15)	L2	O							
<b>LEAVE PIN UNCONNECTED</b>									
RESERVED_PFE	E7	I	LVCMOS		Pulldown	For proper DMD operation, do not connect.			
RESERVED_TM	D13	I							
RESERVED_XI1	E13	I							
RESERVED_TP0	W12	I	Analog						
RESERVED_TP1	Y11	I							
RESERVED_TP2	X11	I							
<b>LEAVE PIN UNCONNECTED</b>									
RESERVED_BA	Y12	O	LVCMOS			For proper DMD operation, do not connect.			
RESERVED_BB	C12	O							
RESERVED_TS	D5	O							
<b>LEAVE PIN UNCONNECTED</b>									
NO CONNECT	B11					For proper DMD operation, do not connect.			
NO CONNECT	C11								
NO CONNECT	C13								
NO CONNECT	E12								
NO CONNECT	E14								
NO CONNECT	E23								
NO CONNECT	H4					For proper DMD operation, do not connect.			
NO CONNECT	N2								
NO CONNECT	N3								
NO CONNECT	N4								
NO CONNECT	R2								
NO CONNECT	R3								
NO CONNECT	R4								
NO CONNECT	T4								

**Table 5-1. Pin Functions (continued)**

PIN <sup>(1)</sup>		TYPE <sup>(5)</sup>	SIGNAL	DATA RATE <sup>(2)</sup>	INTERNAL TERM <sup>(3)</sup>	DESCRIPTION	TRACE (mils) <sup>(4)</sup>
NAME	NO.						
NO CONNECT	U2					For proper DMD operation, do not connect.	
NO CONNECT	U3						
NO CONNECT	U4						
NO CONNECT	W3						
NO CONNECT	W4						
NO CONNECT	W5						
NO CONNECT	W13						
NO CONNECT	W14						
NO CONNECT	W23						
NO CONNECT	X4					For proper DMD operation, do not connect.	
NO CONNECT	X5						
NO CONNECT	X13						
NO CONNECT	Y2						
NO CONNECT	Y3						
NO CONNECT	Y4						
NO CONNECT	Y5						
NO CONNECT	Z11						

- (1) The following power supplies are required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected.
- (2) DDR = Double Data Rate. SDR = Single Data Rate. Refer to [Section 6.7](#) for specifications and relationships.
- (3) Internal term—CMOS level internal termination. Refer to [Section 6.4](#) for differential termination specification.
- (4) Dielectric Constant for the DMD FYE package is approximately 9.6. For the package trace lengths shown: Propagation Speed =  $11.8 / \sqrt{9.6} = 3.808$  in/ns. Propagation Delay =  $0.262$  ns/in =  $262$  ps/in =  $10.315$  ps/mm.
- (5) I = Input, O = Output, G = Ground



**Table 5-2. Power Pin Functions**

PIN		TYPE (I/O/P) <sup>(2)</sup>	SIGNAL	DESCRIPTION
NAME <sup>(1)</sup>	NO.			
VBIAS	A6, A7, A8, AA6, AA7, AA8	P	Analog	Supply voltage for positive Bias level of micromirror reset signal
VOFFSET	A3, A4, A25		Analog	Supply voltage for HVCMOS logic
	B26, L26, M26		Analog	Supply voltage for stepped high voltage at micromirror address electrodes
	N26, Z26, AA3, AA4		Analog	Supply voltage for positive Offset level of micromirror reset signal
VRESET	G1, H1, J1, R1, T1, U1		Analog	Supply voltage for negative Reset level of micromirror reset signal
VCC	A9, B3, B5, B12, C1, C6, C10, D4, D6, D8, E1, E2, E10, E15, E16, E17, F3, H2, K1, K3, M4, P1, P3, T2, V3, W1, W2, W6, W9, W10, W15, W16, W17, X3, X6, Y1, Y8, Y13, Z1, Z3, Z12, AA2, AA9, AA10		Analog	Supply voltage for LVCMOS core logic. Supply voltage for normal high level at micromirror address electrodes. Supply voltage for positive Offset level of micromirror reset signal during power-down sequence
VCCI	A16, A17, A18, A20, A21, A23, AA16, AA17, AA18, AA20, AA21, AA23		Analog	Supply voltage for LVDS receivers
VSS	A5, A10, A11, A19, A22, A24, B2, B4, B9, B13, B17, B20, B21, B24, C7, C15, C18, C21, C22, C26, D1, D3, D7, D10, D12, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D26, E6, E8, E18, E19, E20, E21, E22, E26, F1, F2, F4, F23, F26, G23, G26, H3, H26, J26, K2, K4, K26, L1, M1, M2, M3, M23, M24, M25, N1, P2, P4, P26, R26, T3, T26, U23, U26, V1, V2, V4, V23, V26, W8, W18, W19, W20, W21, W22, W26, X1, X2, X7, X10, X12, X14, X15, X16, X17, X18, X19, X20, X21, X22, X23, X26, Y6, Y15, Y18, Y21, Y22, Y26, Z2, Z4, Z9, Z13, Z17, Z20, Z21, Z24, AA5, AA11, AA19, AA22, AA24	Analog	Device ground. Common return for all power	

(1) The following power supplies are required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected.

(2) P = Power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

		MIN	MAX	UNIT
<b>SUPPLY VOLTAGES</b>				
VCC	Supply voltage for LVCMOS core logic <sup>(1)</sup>	-0.5	4	V
VCCI	Supply voltage for LVDS receivers <sup>(1)</sup>	-0.5	4	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode <sup>(1) (2)</sup>	-0.5	9	V
VBIAS	Supply voltage for micromirror electrode <sup>(1)</sup>	-0.5	17	V
VRESET	Supply voltage for micromirror electrode <sup>(1)</sup>	-11	0.5	V
VCC – VCCI	Supply voltage change (absolute value) <sup>(3)</sup>		0.3	V
VBIAS – VOFFSET	Supply voltage change (absolute value) <sup>(4)</sup>		8.75	V
<b>INPUT VOLTAGES</b>				
	Input voltage for all other LVCMOS input pins <sup>(1)</sup>	-0.5	VCC + 0.15	V
	Input voltage for all other LVDS input pins <sup>(1) (5)</sup>	-0.5	VCCI + 0.15	V
V <sub>ID</sub>	Input differential voltage (absolute value) <sup>(6)</sup>		700	mV
I <sub>ID</sub>	Input differential current <sup>(6)</sup>		7	mA
<b>CLOCKS</b>				
f <sub>clock</sub>	Clock frequency for LVDS interface, DCLK (all channels)		460	MHz
<b>ENVIRONMENTAL</b>				
T <sub>ARRAY</sub> and T <sub>WINDOW</sub>	Temperature, operating <sup>(7)</sup>	0	90	°C
	Temperature: non-operating <sup>(7)</sup>	-40	90	°C
T <sub>DELTA</sub>	Absolute Temperature delta between any point on the window edge and the ceramic test point TP1 <sup>(8)</sup>		30	°C
T <sub>DP</sub>	Dew Point temperature, operating and non-operating (non-condensing)		81	°C

- (1) All voltages are referenced to common ground VSS. Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
- (2) VOFFSET supply transients must fall within specified voltages.
- (3) To prevent excess current, the supply voltage change |VCCI – VCC| must be less than specified limit.
- (4) To prevent excess current, the supply voltage change |VBIAS – VOFFSET| must be less than specified limit. Refer to [Section 8](#) for additional information.
- (5) This maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential.
- (6) LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors
- (7) The highest temperature of the active array (as calculated by [Section 7.6](#)) or of any point along the Window Edge as defined in [Figure 7-1](#). The locations of thermal test points TP2, TP3, TP4 and TP5 in [Figure 7-1](#) are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, add a test point to that location.
- (8) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in [Figure 7-1](#). The window test points TP2, TP3, TP4, and TP5 in [Figure 7-1](#) are intended to result in the worst-case delta. If a particular application causes another point on the window edge to result in a larger delta temperature, that point should be used.

### 6.2 Storage Conditions

Applicable for the DMD as a component or non-operational in a system.

		MIN	MAX	UNIT
T <sub>DMD</sub>	DMD storage temperature	-40	80	°C
T <sub>DP-AVG</sub>	Average dew point temperature (non-condensing) <sup>(1)</sup>		28	°C
T <sub>DP-ELR</sub>	Elevated dew point temperature range (non-condensing) <sup>(2)</sup>	28	36	°C

## 6.2 Storage Conditions (continued)

Applicable for the DMD as a component or non-operational in a system.

		MIN	MAX	UNIT
CT <sub>ELR</sub>	Cumulative time in elevated dew point temperature range		24	Months

- (1) The average over time (including storage and operating) that the device is not in the "elevated dew point temperature range."
- (2) Limit exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of CT<sub>ELR</sub>.

## 6.3 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

## 6.4 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
<b>SUPPLY VOLTAGES<sup>(1) (2)</sup></b>					
VCC	Supply voltage for LVCMOS core logic	3.15	3.3	3.45	V
VCCI	Supply voltage for LVDS receivers	3.15	3.3	3.45	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrodes <sup>(2)</sup>	8.25	8.5	8.75	V
VBIAS	Supply voltage for micromirror electrodes	15.5	16	16.5	V
VRESET	Supply voltage for micromirror electrodes	-9.5	-10	-10.5	V
VCCI-VCC	Supply voltage change (absolute value) <sup>(3)</sup>		0	0.3	V
VBIAS-VOFFSET	Supply voltage change (absolute value) <sup>(4)</sup>			8.75	V
<b>LVCMOS PINS</b>					
V <sub>IH</sub>	High level Input voltage <sup>(5)</sup>	1.7	2.5	VCC + 0.15	V
V <sub>IL</sub>	Low level Input voltage <sup>(5)</sup>	-0.3		0.7	V
I <sub>OH</sub>	High level output current at V <sub>OH</sub> = 2.4 V			-20	mA
I <sub>OL</sub>	Low level output current at V <sub>OL</sub> = 0.4 V			15	mA
t <sub>PWRDNZ</sub>	PWRDNZ pulse width <sup>(6)</sup>	10			ns
<b>SCP INTERFACE</b>					
f <sub>SCPCLK</sub>	SCP clock frequency <sup>(7)</sup>			500	kHz
t <sub>SCP_DS</sub>	SCPDI clock setup time (before SCPCLK falling-edge) <sup>(8)</sup>	800			ns
t <sub>SCP_DH</sub>	SCPDI hold time (after SCPCLK falling-edge) <sup>(8)</sup>	900			ns
t <sub>SCP_BYTE_INTERVAL</sub>	Time between consecutive bytes	1			µs
t <sub>SCP_NEG_ENZ</sub>	Time between falling edge of SCPENZ and the first rising edge of SCPCLK	30			ns
t <sub>SCP_PW_ENZ</sub>	SCPENZ inactive pulse width (high level)	1			µs
t <sub>SCP_OUT_EN</sub>	Time required for SCP output buffer to recover after SCPENZ (from tristate)			1.5	ns
f <sub>clock</sub>	SCP circuit clock oscillator frequency <sup>(9)</sup>	9.6		11.1	MHz

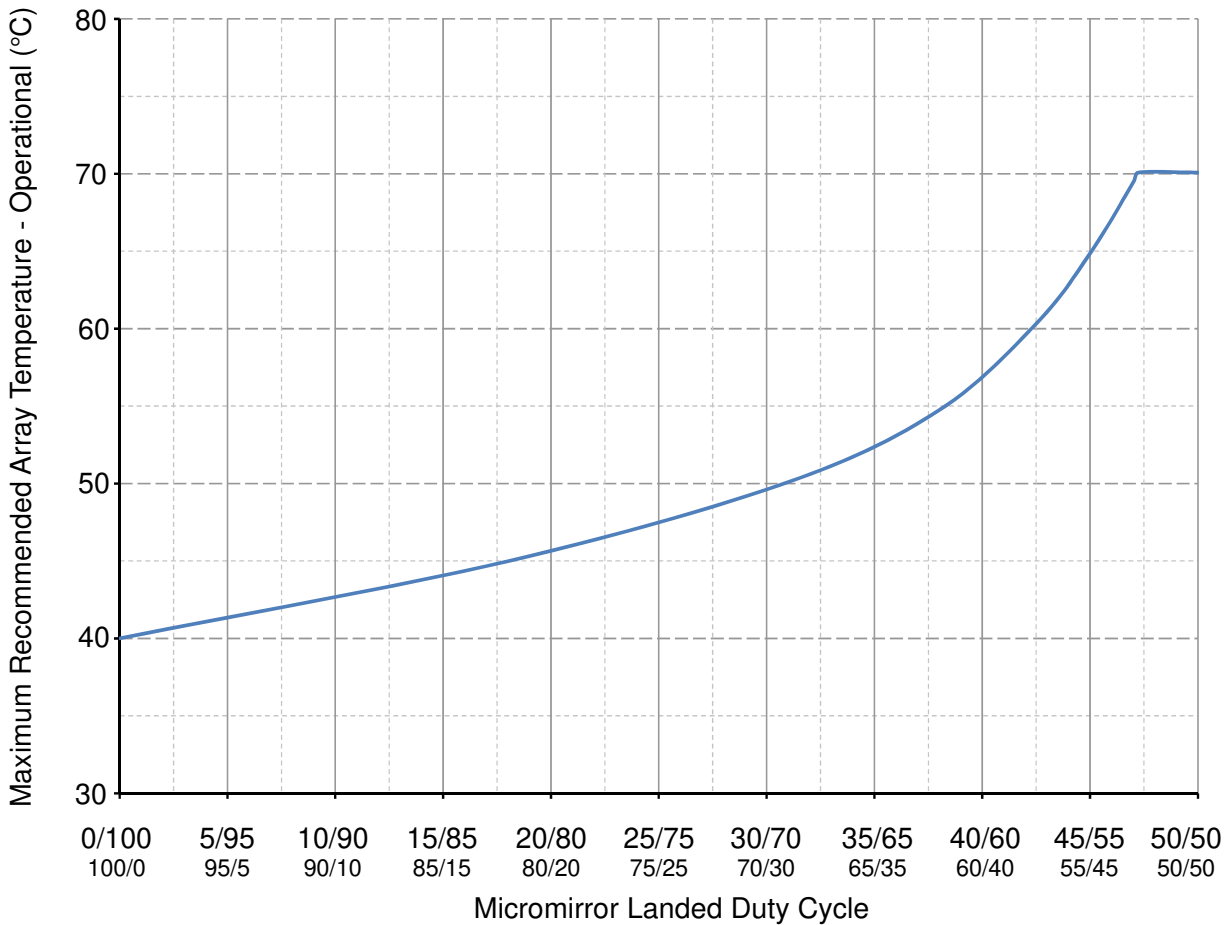
## 6.4 Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device within the limits defined by this table. No level of performance is implied when operating the device above or below these limits.

		MIN	NOM	MAX	UNIT
<b>LVDS INTERFACE</b>					
$f_{\text{clock}}$	Clock frequency for LVDS interface, DCLK (all channels)			400	MHz
$ V_{\text{ID}} $	Input differential voltage (absolute value) <sup>(10)</sup>	100	400	600	mV
$V_{\text{CM}}$	Common mode <sup>(10)</sup>		1200		mV
$V_{\text{LVDS}}$	LVDS voltage <sup>(10)</sup>	0		2000	mV
$t_{\text{LVDS\_RSTZ}}$	Time required for LVDS receivers to recover from PWRDNZ			10	ns
$Z_{\text{IN}}$	Internal differential termination resistance	95		105	$\Omega$
$Z_{\text{LINE}}$	Line differential impedance (PWB/trace)	90	100	110	$\Omega$
<b>ENVIRONMENTAL</b>					
$T_{\text{ARRAY}}$	Array temperature, long-term operational <sup>(11) (12) (13)</sup>	10		40 to 70 <sup>(14)</sup>	$^{\circ}\text{C}$
	Array temperature, short-term operational <sup>(12) (15)</sup>	0		10	
$T_{\text{WINDOW}}$	Window temperature – operational <sup>(16)</sup>			85	$^{\circ}\text{C}$
$T_{\text{DELTA}}$	Absolute temperature delta between any point on the window edge and the ceramic test point TP1. <sup>(17) (18)</sup>			26	$^{\circ}\text{C}$
$T_{\text{DP-AVG}}$	Average dew point temperature (non-condensing) <sup>(19)</sup>			28	$^{\circ}\text{C}$
$T_{\text{DP-ELR}}$	Elevated dew point temperature range (non-condensing) <sup>(20)</sup>	28		36	$^{\circ}\text{C}$
$CT_{\text{ELR}}$	Cumulative time in elevated dew point temperature range			24	Months
$L$	Operating system luminance <sup>(18)</sup>			4200	lm
$ILL_{\text{UV}}$	Illumination, wavelength < 395 nm <sup>(11)</sup>		0.68	2.0	mW/cm <sup>2</sup>
$ILL_{\text{VIS}}$	Illumination, wavelength between 395 nm and 800 nm			Thermally Limited	
$ILL_{\text{IR}}$	Illumination, wavelength > 800 nm			10	mW/cm <sup>2</sup>

- (1) Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
- (2) VOFFSET supply transients must fall within specified max voltages.
- (3) To prevent excess current, the supply voltage change  $|V_{\text{CCI}} - V_{\text{CC}}|$  must be less than specified limit.
- (4) To prevent excess current, the supply voltage change  $|V_{\text{BIAS}} - V_{\text{OFFSET}}|$  must be less than specified limit. Refer to [Section 8](#) for additional information.
- (5) Tester conditions for  $V_{\text{IH}}$  and  $V_{\text{IL}}$ :  
Frequency = 60 MHz. Maximum Rise Time = 2.5 ns at (20% to 80%)  
Frequency = 60 MHz. Maximum Fall Time = 2.5 ns at (80% to 20%)
- (6) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tri-states the SCPDO output pin.
- (7) The SCP clock is a gated clock. Duty cycle shall be 50%  $\pm$  10%. SCP parameter is related to the frequency of DCLK.
- (8) Refer to [Figure 6-2](#).
- (9) SCP internal oscillator is specified to operate all SCP registers. For all SCP operations, DCLK is required.
- (10) Refer to [Figure 6-3](#), [Figure 6-4](#), and [Figure 6-5](#).
- (11) Simultaneous exposure of the DMD to the maximum [Section 6.4](#) for temperature and UV illumination reduces device lifetime.
- (12) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in [Figure 7-1](#) and the package [Section 6.5](#) using the calculation in [Section 7.6](#).
- (13) Long-term is defined as the average over the usable life.
- (14) Per [Figure 6-1](#), the maximum operational array temperature should be derated based on the micromirror landed duty cycle that the DMD experiences in the end application. See [Section 7.7](#).
- (15) Array temperatures beyond those specified as long-term are recommended for short-term conditions only (power-up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours.
- (16) The locations of thermal test points TP2, TP3, TP4 and TP5 in [Figure 7-1](#) are intended to measure the highest window edge temperature. For most applications, the locations shown are representative of the highest window edge temperature. If a particular application causes additional points on the window edge to be at a higher temperature, test points should be added to those locations.
- (17) Temperature delta is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in [Figure 7-1](#). The window test points TP2, TP3, TP4, and TP5 shown in [Figure 7-1](#) are intended to result in the worst-case delta temperature. If a particular application causes another point on the window edge to result in a larger delta in temperature, that point should be used.

- (18) DMD is qualified at the combination of the maximum temperature and maximum lumens specified. Operation of the DMD outside of these limits has not been tested.
- (19) The average over time (including storage and operating) that the device is not in the 'elevated dew point temperature range'.
- (20) Exposure to dew point temperatures in the elevated range during storage and operation should be limited to less than a total cumulative time of CT<sub>ELR</sub>.



**Figure 6-1. Recommended Maximum DMD Temperature—Derating Curve**

### 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>	DLP650NE	UNIT
	FYE Package	
	350 PINS	
Thermal resistance from active array to test point 1 (TP1)	0.6	°C/W

- (1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the temperature range specified in the [Recommended Operating Conditions](#). The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Optical systems should be designed to minimize the light energy falling outside the window clear aperture since any additional thermal load in this area can significantly degrade the reliability of the device.

## 6.6 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT	
V <sub>OH</sub>	High-level output voltage	VCC = 3.3 V, I <sub>OH</sub> = -20 mA	2.4			V	
V <sub>OL</sub>	Low-level output voltage	VCC = 3.45 V, I <sub>OL</sub> = 15 mA	0.4			V	
I <sub>IH</sub>	High-level input current <sup>(2) (3)</sup>	VCC = 3.45 V, V <sub>I</sub> = VCC	250			μA	
I <sub>IL</sub>	Low-level input current	VCC = 3.45 V, V <sub>I</sub> = 0	-250			μA	
I <sub>OZ</sub>	High-impedance output current	VCC = 3.45 V	10			μA	
I <sub>CC</sub>	Supply current <sup>(4)</sup>	VCC = 3.45 V	1100			mA	
I <sub>CCI</sub>		VCCI = 3.45 V	500				
I <sub>OFFSET</sub>	Supply current <sup>(5)</sup>	V <sub>OFFSET</sub> = 8.75 V	10			mA	
I <sub>BIAS</sub>		V <sub>BIAS</sub> = 16.5 V	10				
I <sub>RESET</sub>	Supply current	V <sub>RESET</sub> = -10.5 V	10			mA	
I <sub>TOTAL</sub>		Total Sum	1650				
C <sub>I</sub>	Input capacitance	f = 1 MHz	10			pF	
C <sub>O</sub>	Output capacitance	f = 1 MHz	10			pF	
C <sub>M</sub>	Reset group capacitance MBRST(14:0)	f = 1 MHz all inputs interconnected, (1920 x 1080) array	330			390	pF

- (1) All voltages are referenced to common ground VSS. Supply voltages VCC, VCCI, V<sub>OFFSET</sub>, V<sub>BIAS</sub>, and V<sub>RESET</sub> are all required for proper DMD operation. VSS must also be connected.
- (2) Applies to LVCMOS input pins only; excludes the LVDS pins and MBRST pins
- (3) LVCMOS input pins utilize an internal 18000-Ω passive resistor for pullup and pulldown configurations. Refer to [Section 5](#) to determine the pullup or pulldown configuration used.
- (4) To prevent excess current, the supply voltage change |VCCI – VCC| must be less than specified limit.
- (5) To prevent excess current, the supply voltage change |V<sub>BIAS</sub> – V<sub>OFFSET</sub>| must be less than specified limit.

## 6.7 Timing Requirements

Over Recommended Operating Conditions (Section 6.4) unless otherwise noted.<sup>(5)</sup>

DESCRIPTION <sup>(1)</sup>			MIN	TYP	MAX	UNIT	
<b>SCP INTERFACE<sup>(2)</sup></b>							
$t_r$	Rise time	20% to 80% reference points			200	ns	
$t_f$	Fall time	80% to 20% reference points			200	ns	
<b>LVDS INTERFACE<sup>(2)</sup></b>							
$t_r$	Rise time	20% to 80%	100		400	ps	
$t_f$	Fall time	80% to 20%	100		400	ps	
<b>LVDS CLOCKS<sup>(3)</sup></b>							
$t_c$	Cycle time	DCLK_A, 50% to 50%	2.5			ns	
		DCLK_B, 50% to 50%	2.5				
$t_w$	Pulse duration	DCLK_A, 50% to 50%	1.19	1.25		ns	
		DCLK_B, 50% to 50%	1.19	1.25			
<b>LVDS INTERFACE<sup>(3)</sup></b>							
$t_{su}$	Setup time	D_A(15:0) before rising or falling edge of DCLK_A	0.1			ns	
		D_B(15:0) before rising or falling edge of DCLK_B	0.1				
$t_{su}$	Setup time	SCTRL_A before rising or falling edge of DCLK_A	0.1			ns	
		SCTRL_B before rising or falling edge of DCLK_B	0.1				
$t_h$	Hold time	D_A(15:0) after rising or falling edge of DCLK_A	0.4			ns	
		D_B(15:0) after rising or falling edge of DCLK_B	0.4				
$t_h$	Hold time	SCTRL_A after rising or falling edge of DCLK_A	0.3			ns	
		SCTRL_B after rising or falling edge of DCLK_B	0.3				
<b>LVDS INTERFACE<sup>(4)</sup></b>							
$t_{skew}$	Skew time	Channel B relative to Channel A <sup>(4)</sup>	Channel A includes the following LVDS pairs: DCLK_AP and DCLK_AN SCTRL_AP and SCTRL_AN D_AP(15:0) and D_AN(15:0)	Channel B includes the following LVDS pairs: DCLK_BP and DCLK_BN SCTRL_BP and SCTRL_BN D_BP(15:0) and D_BN(15:0)	-1.25	1.25	ns

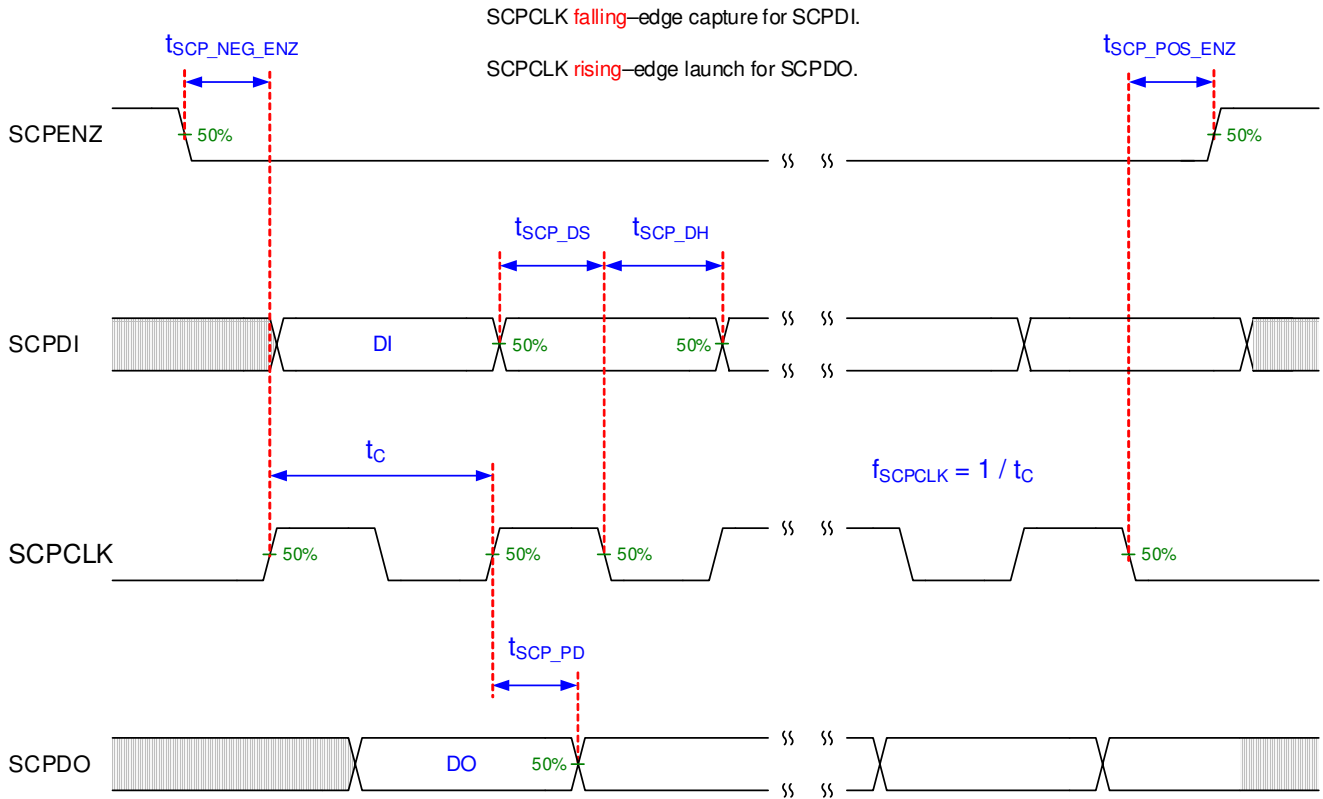
(1) Refer to Section 5 for pin details.

(2) Refer to Figure 6-6.

(3) Refer to Figure 6-8.

(4) Refer to Figure 6-9.

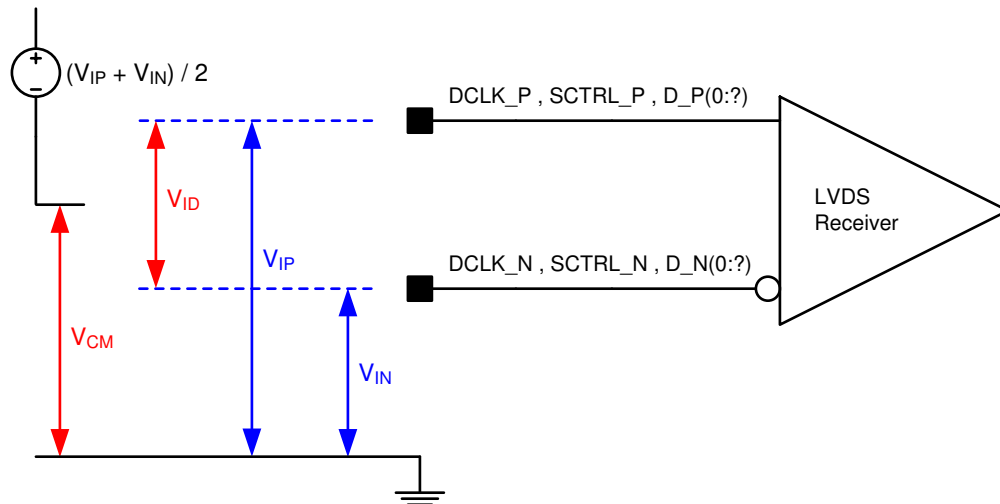
(5) Tested at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be considered.



Not to scale

Refer to the SCP Interface section of the *Recommended Operating Conditions* Section 6.4.

**Figure 6-2. SCP Timing Parameters**

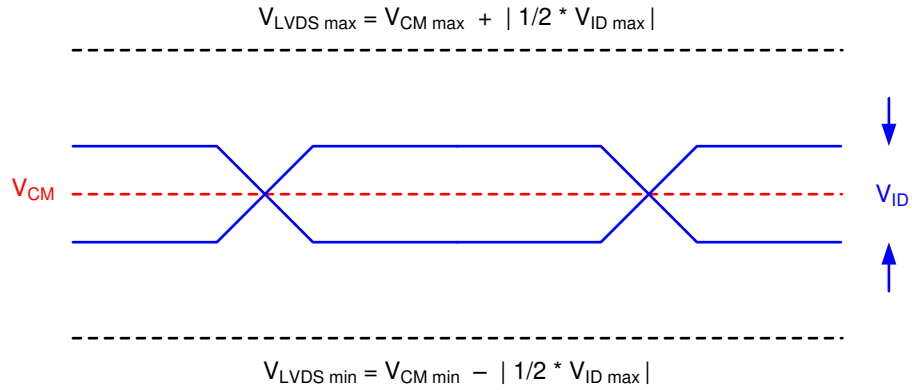


Refer to the LVDS Interface section of the *Recommended Operating Conditions* (Section 6.4).

Refer to the Pin Functions table for the list of LVDS pins.

**Figure 6-3. LVDS Voltage Definitions (References)**

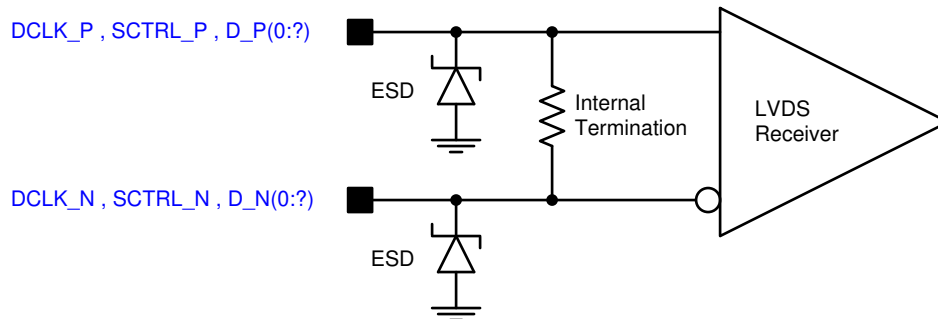




Not to scale

Refer to the LVDS Interface section of the *Recommended Operating Conditions* (Section 6.4).

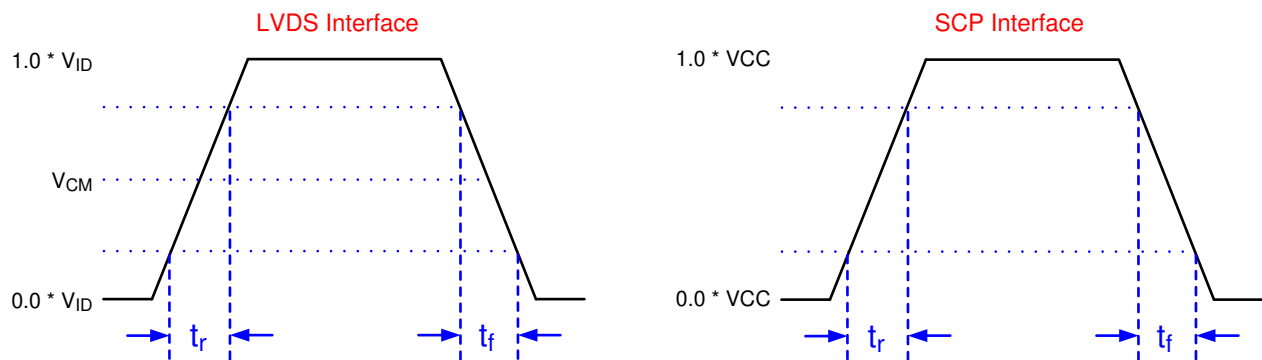
**Figure 6-4. LVDS Voltage Parameters**



Refer to the LVDS Interface section of the *Recommended Operating Conditions* (Section 6.4).

Refer to the Pin Functions table for the list of LVDS pins.

**Figure 6-5. LVDS Equivalent Input Circuit**

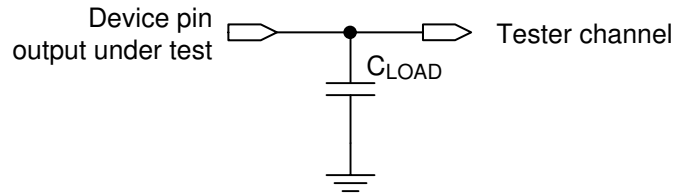


Not to scale

Refer to the timing requirements.

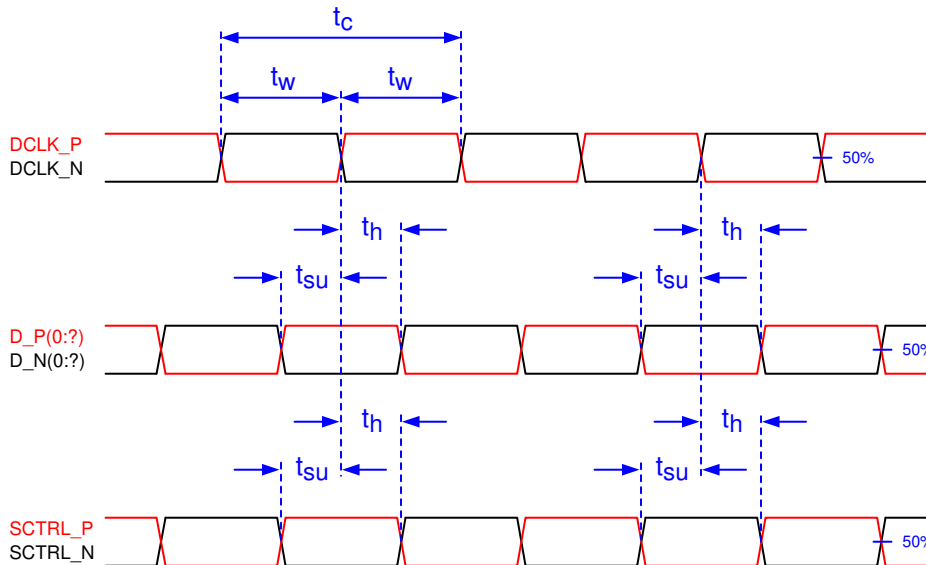
Refer to the Pin Functions table for the list of LVDS pins and SCP pins.

**Figure 6-6. Rise Time and Fall Time**



**Figure 6-7. Test Load Circuit for Output Propagation Measurement**

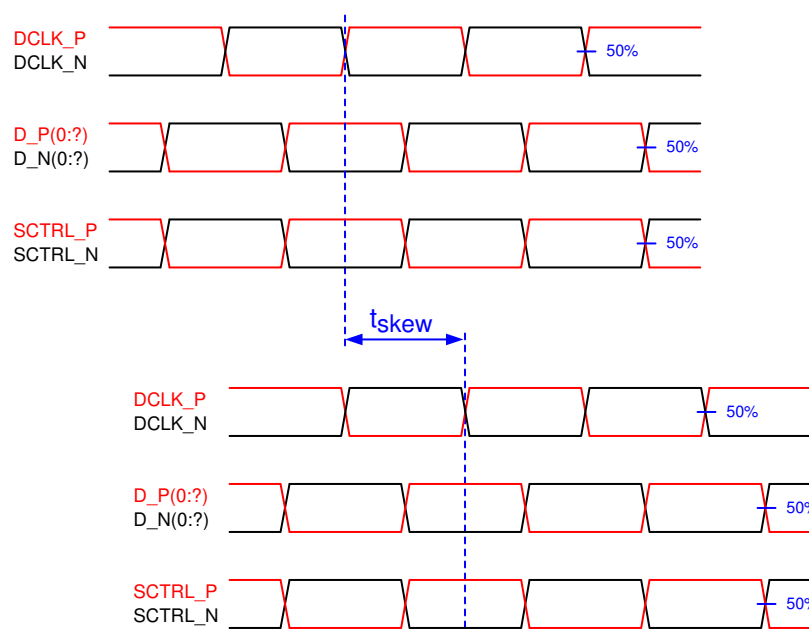
For output timing analysis, the tester pin electronics and its transmission line effects must be considered. System design should use IBIS or other simulation tools to correlate the timing reference load to a system environment. See [Figure 6-7](#).



Not to scale

Refer to the LVDS Interface section in the timing requirements.

**Figure 6-8. Timing Requirement Parameter Definitions**



Not to scale

Refer to the LVDS Interface section in the timing requirements.

**Figure 6-9. LVDS Interface Channel Skew Definition**

**6.8 Window Characteristics**

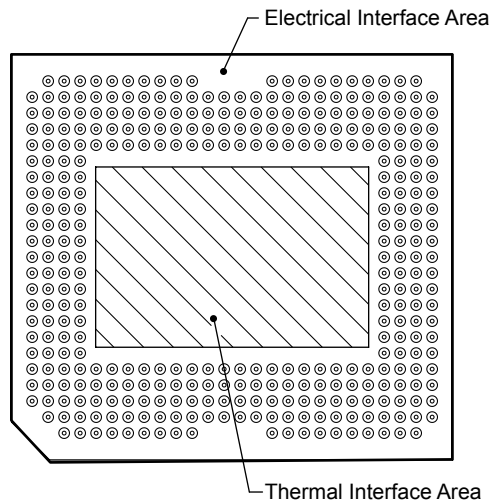
PARAMETER	MIN	NOM
Window material		Corning Eagle XG
Window refractive index at wavelength 546.1 nm		1.5119
Window Transmittance, minimum within the wavelength range 420–680 nm. Applies to all angles 0–30° AOI. <sup>(1)</sup> <sup>(2)</sup>	97%	
Window Transmittance, average over the wavelength range 420–680 nm. Applies to all angles 30–45° AOI. <sup>(1)</sup> <sup>(2)</sup>	97%	

- (1) Single-pass through both surfaces and glass
- (2) Angle of incidence (AOI) is the angle between an incident ray and the normal to a reflecting or refracting surface.

**6.9 System Mounting Interface Loads**

PARAMETER	MIN	NOM	MAX	UNIT
Condition 1: <sup>(1)</sup>				
• Thermal Interface area			11.3	kg
• Electrical Interface area			11.3	kg

- (1) Uniformly distributed within area shown in [Figure 6-10](#)



**Figure 6-10. System Mounting Interface Loads**

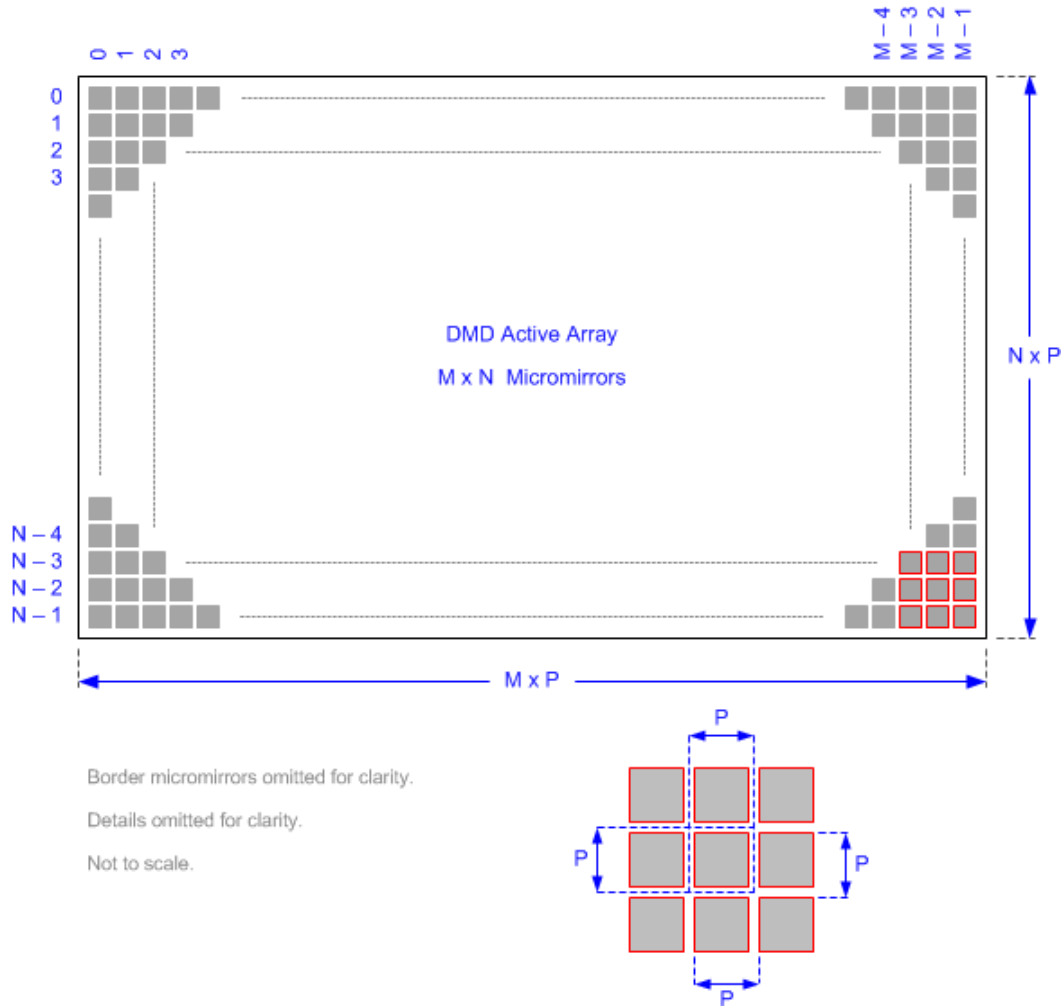
**6.10 Micromirror Array Physical Characteristics**

		VALUE	UNIT
Number of active columns <sup>(1)</sup>	M	1920	micromirrors
Number of active rows <sup>(1)</sup>	N	1080	micromirrors
Micromirror (pixel) pitch <sup>(1)</sup>	P	7.56	µm
Micromirror active array width <sup>(1)</sup>	Micromirror Pitch × number of active columns	14.5152	mm
Micromirror active array height <sup>(1)</sup>	Micromirror Pitch × number of active rows	8.1648	mm

### 6.10 Micromirror Array Physical Characteristics (continued)

		VALUE	UNIT
Micromirror active border <sup>(2)</sup>	Pond of micromirrors (POM)	14	micromirrors /side

- (1) See Figure 6-11.
- (2) The structure and qualities of the border around the active array includes a band of partially functional micromirrors referred to as the pond of micromirrors (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.



Refer to Section 6.10 for M, N, and P specifications.

**Figure 6-11. Micromirror Array Physical Characteristics**

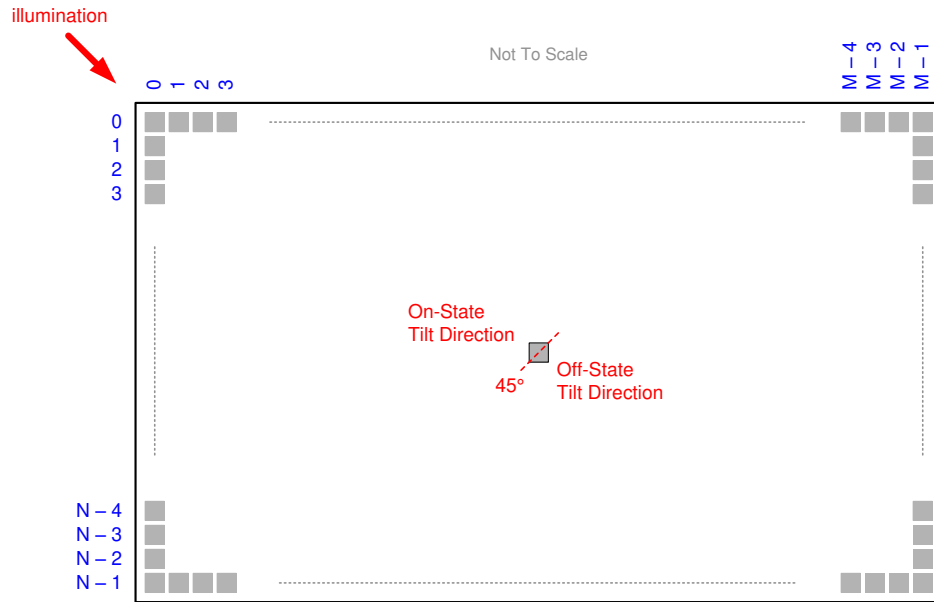
### 6.11 Micromirror Array Optical Characteristics

See Section 7.5 for important information.

PARAMETER		MIN	NOM	MAX	UNIT
Mirror tilt angle, variation device to device <sup>(1) (2) (3) (4)</sup>		11	12	13	°
Number of out-of-specification micromirrors <sup>(5)</sup>	Adjacent micromirrors			0	micromirrors
	Non-adjacent micromirrors			10	

- (1) Measured relative to the plane formed by the overall micromirror array
- (2) Variation can occur between any two individual micromirrors located on the same device or located on different devices.
- (3) Additional variation exists between the micromirror array and the package datums. See the package drawing.
- (4) See Figure 6-12.

- (5) An "out-of-specification micromirror" is defined as a micromirror that is unable to transition between the two landed states.



Refer to [Section 6.10](#) for M, N, and P specifications.

**Figure 6-12. Micromirror Landed Orientation and Tilt**

## 6.12 Chipset Component Usage Specification

The DLP650NE is a component of one or more DLP chipsets. Reliable function and operation of the DLP650NE require that it is used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology is the TI technology and devices for operating or controlling a DLP DMD.

## 7 Detailed Description

### 7.1 Overview

DLP650NE is a 0.65-inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. Pixel array size and square grid pixel arrangement are shown in [Figure 6-11](#).

The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is low voltage differential signaling (LVDS), double data rate (DDR).

DLP650NE DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of  $M$  memory cell columns by  $N$  memory cell rows. Refer to the [Section 7.2](#).

The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

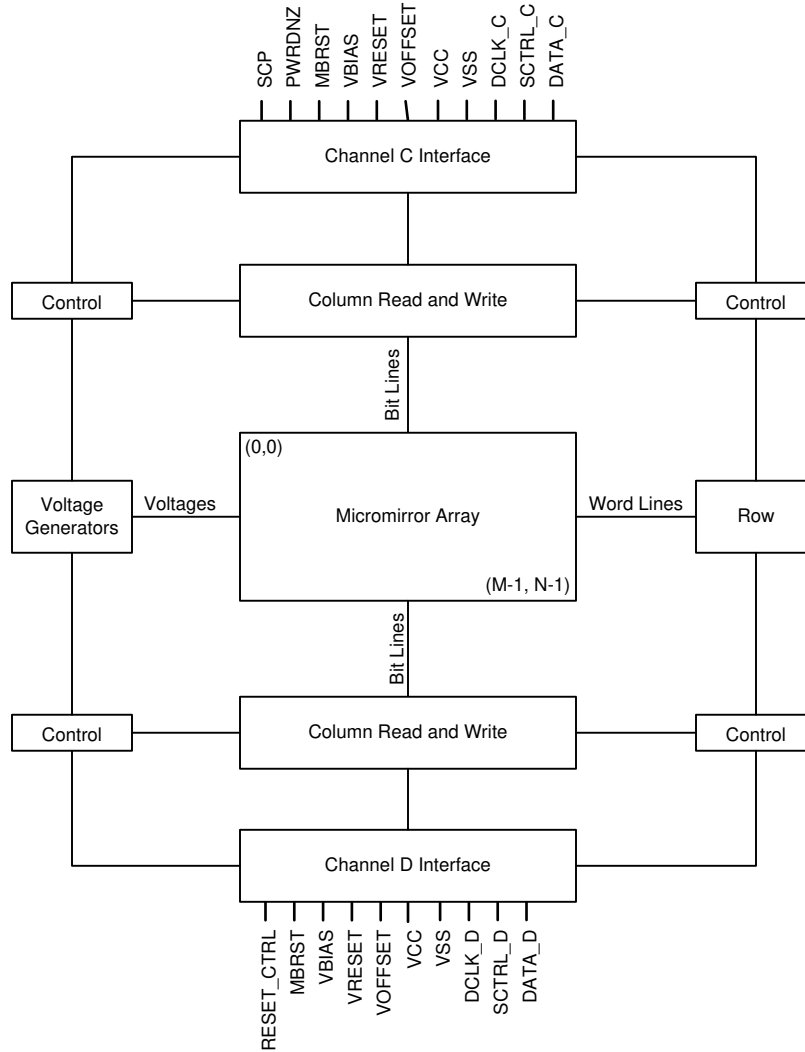
Each cell of the  $M \times N$  memory array drives its true and complement ('Q' and 'QB') data to two electrodes underlying one micromirror, one electrode on each side of the diagonal axis of rotation. Refer to [Section 6.11](#). The micromirrors are electrically tied to the micromirror reset signals (MBRST) and the micromirror array is divided into reset groups.

Electrostatic potentials between a micromirror and its memory data electrodes cause the micromirror to tilt toward the illumination source in a DLP projection system or away from it, thus reflecting its incident light into or out of an optical collection aperture. The positive (+) tilt angle state corresponds to an 'on' pixel, and the negative (–) tilt angle state corresponds to an 'off' pixel.

Refer to [Section 6.11](#) for the  $\pm$  tilt angle specifications. Refer to [Section 5](#) for more information on micromirror reset control.

### 7.2 Functional Block Diagram

The main LVDS lines going to the DMD are connected via channel A and B. However, the LVDS lines come from channel C and D off the DLPC4430. Please refer to the DLPC4430 data sheet for more information.



For pin details on Channels A, B, C, and D, refer to [Section 5](#) and LVDS Interface section of [Timing Requirements](#).

## 7.3 Feature Description

### 7.3.1 Power Interface

The DMD requires four DC voltage input signals.

- DMD\_P3P3V
- VOFFSET
- VRESET
- VBIAS

The DMD\_P3P3V signal is created by the power and motor driver of the DLPA100 device. It is used on the DMD board to create the other three DMD voltage inputs, as well as powering various peripherals (for example, TMP411, I<sup>2</sup>C, and TI level translators). The other signals (VOFFSET (8.5 V), VRESET (–10 V), and VBIAS (16.5 V)) are created by the TI PMIC TPS65145 device and are supplied to the DMD to control the micromirrors.

### 7.3.2 Timing

The data sheet provides a timing analysis as measured at the device pin. For an output timing analysis, the tester pin electronics and its transmission line effects must be considered. [Figure 6-7](#) shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. TI suggests that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

## 7.4 Device Functional Modes

DMD functional modes are controlled by the DLPC4430 digital display controller. See the [DLPC4430 DLP® Display Controller Data Sheet](#). Contact a TI applications engineer for more information.

## 7.5 Optical Interface and System Image Quality Considerations

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. System optical performance and image quality strongly relate to optical system design parameter trades offs. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

### 7.5.1 Numerical Aperture and Stray Light Control

The angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area are the same. This angle should not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The micromirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle (and vice versa), objectionable artifacts in the display's border and/or active area could occur.

### 7.5.2 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

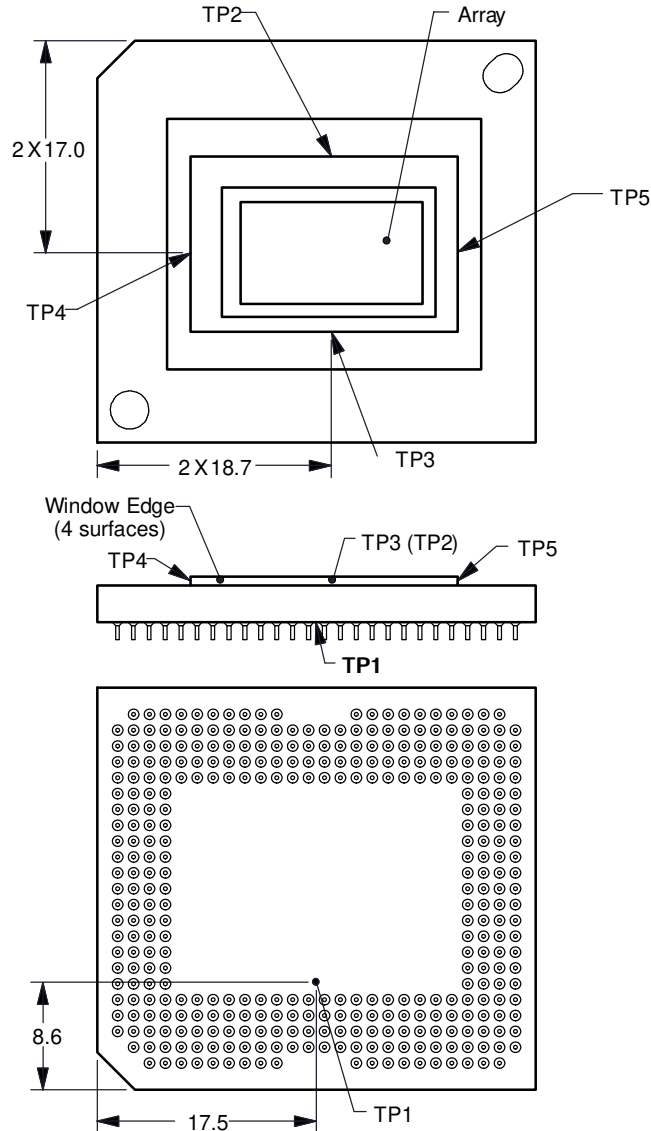
### 7.5.3 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD chip assembly from normal view. The aperture is sized to anticipate several optical



operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system’s optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

### 7.6 Micromirror Array Temperature Calculation



**Figure 7-1. DMD Thermal Test Points**

Micromirror array temperature cannot be measured directly, therefore it must be computed analytically from measurement points on the outside of the package, the package thermal resistance, the electrical power, and the illumination heat load. The relationship between array temperature and the reference ceramic temperature (thermal test TP1 in Figure 7-1) is provided by the following equations:

$$T_{\text{ARRAY}} = T_{\text{CERAMIC}} + (Q_{\text{ARRAY}} \times R_{\text{ARRAY-TO-CERAMIC}})$$

$$Q_{\text{ARRAY}} = Q_{\text{ELECTRICAL}} + Q_{\text{ILLUMINATION}}$$

$$Q_{\text{ILLUMINATION}} = (C_{\text{L2W}} \times \text{SL})$$

where

- $T_{\text{ARRAY}}$  = Computed array temperature ( $^{\circ}\text{C}$ )
- $T_{\text{CERAMIC}}$  = measured ceramic temperature ( $^{\circ}\text{C}$ ), TP1 location in [Figure 7-1](#)
- $R_{\text{ARRAY-TO-CERAMIC}}$  = thermal resistance of package (specified in [Section 6.5](#)) from array to ceramic TP1 ( $^{\circ}\text{C}/\text{W}$ )
- $Q_{\text{ARRAY}}$  = total DMD Power on array (W). (electrical + absorbed)
- $Q_{\text{ELECTRICAL}}$  = Nominal DMD electrical power dissipation (W)
- $C_{\text{L2W}}$  = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm) specified below
- $SL$  = Measured ANSI screen lumens (lm)

The electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. The nominal electrical power dissipation to use when calculating array temperature is 2.9 W. The absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. The equations shown above are valid for a 1-chip DMD system with total projection efficiency through the projection lens from DMD to the screen of 87%.

The conversion constant  $C_{\text{L2W}}$  is based on the DMD micromirror array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00293 W/lm.

Sample calculations:

$$T_{\text{CERAMIC}} = 55^{\circ}\text{C}$$

$$SL = 4200 \text{ lm}$$

$$Q_{\text{ELECTRICAL}} = 2.9 \text{ W}$$

$$C_{\text{L2W}} = 0.00293 \text{ W/lm}$$

$$Q_{\text{ARRAY}} = 2.9 \text{ W} + (0.00293 \times 4200) = 15.21 \text{ W}$$

$$T_{\text{ARRAY}} = 55^{\circ}\text{C} + (15.21 \text{ W} \times 0.6 \text{ C/W}) = 64.1^{\circ}\text{C}$$

## 7.7 Micromirror Landed-On or Landed-Off Duty Cycle

### 7.7.1 Definition of Micromirror Landed-On or Landed-Off Duty Cycle

The micromirror landed-on or landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON-state versus the amount of time the same micromirror is landed in the OFF-state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON-state 100% of the time (and in the OFF-state 0% of the time); whereas 0/100 would indicate that the pixel is in the OFF-state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

### 7.7.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example,

a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

Individual DMD mirror duty cycles vary by application as well as the mirror location on the DMD within any specific application. DMD mirror useful life are maximized when every individual mirror within a DMD approaches 50/50 (or 1/1) duty cycle. Therefore, for the DLPC4430 and DLP650NE chipset, it is recommended that the DMD Idle Mode be enabled as often as possible. Examples are whenever the system is idle, the illumination is disabled, between sequential pattern exposures (if possible), or when the exposure pattern sequence is stopped for any reason. This software mode provides a 50/50 duty cycle across the entire DMD mirror array, where the mirrors are continuously flipped between the on and off states. Refer to the DLPC4430 Software Programmer's Guide for a description of the DMD Idle Mode command. For the DLPC910 and DLP650NE chipset, it is recommended that the controlling applications processor provide a 50/50 pattern sequence to the DLPC910 for display on the DLP650NE as often as possible, similar to the above examples stated for the DLPC4430. The pattern provides a 50/50 duty cycle across the entire DMD mirror array, where the mirrors are continuously flipped between the ON and OFF states.

### 7.7.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the usable life of the DMD. This is quantified in the de-rating curve shown in [Figure 6-1](#). The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD temperature at a given long-term average Landed Duty Cycle.

### 7.7.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given time period, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in [Table 7-1](#).

**Table 7-1. Grayscale Value and Landed Duty Cycle**

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where *color cycle time* is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated in [Equation 1](#).

$$\text{Landed Duty Cycle} = (\text{Red\_Cycle\_}\% \times \text{Red\_Scale\_Value}) + (\text{Green\_Cycle\_}\% \times \text{Green\_Scale\_Value}) + (\text{Blue\_Cycle\_}\% \times \text{Blue\_Scale\_Value}) \quad (1)$$

where

- Red\_Cycle\_% represents the percentage of the frame time that Red is displayed to achieve the desired white point
- Green\_Cycle\_% represents the percentage of the frame time that Green is displayed to achieve the desired white point
- Blue\_Cycle\_%, represents the percentage of the frame time that Blue is displayed to achieve the desired white point

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities would be as shown in [Table 7-2](#).

**Table 7-2. Example Landed Duty Cycle for Full-Color**

CYCLE PERCENTAGE			Landed Duty Cycle
Red 50%	Green 20%	Blue 30%	
Red Scale Value	Green Scale Value	Blue Scale Value	
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

## Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

Texas Instruments DLP technology is a micro-electro-mechanical systems (MEMS) technology that modulates light using a digital micromirror device (DMD). The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, towards the projection optics or collection optics. The large micromirror array size and ceramic package provides great thermal performance for bright display applications. Typical applications using the DLP650NE include home theater, digital signage, interactive display, low-latency gaming display, portable smart displays.

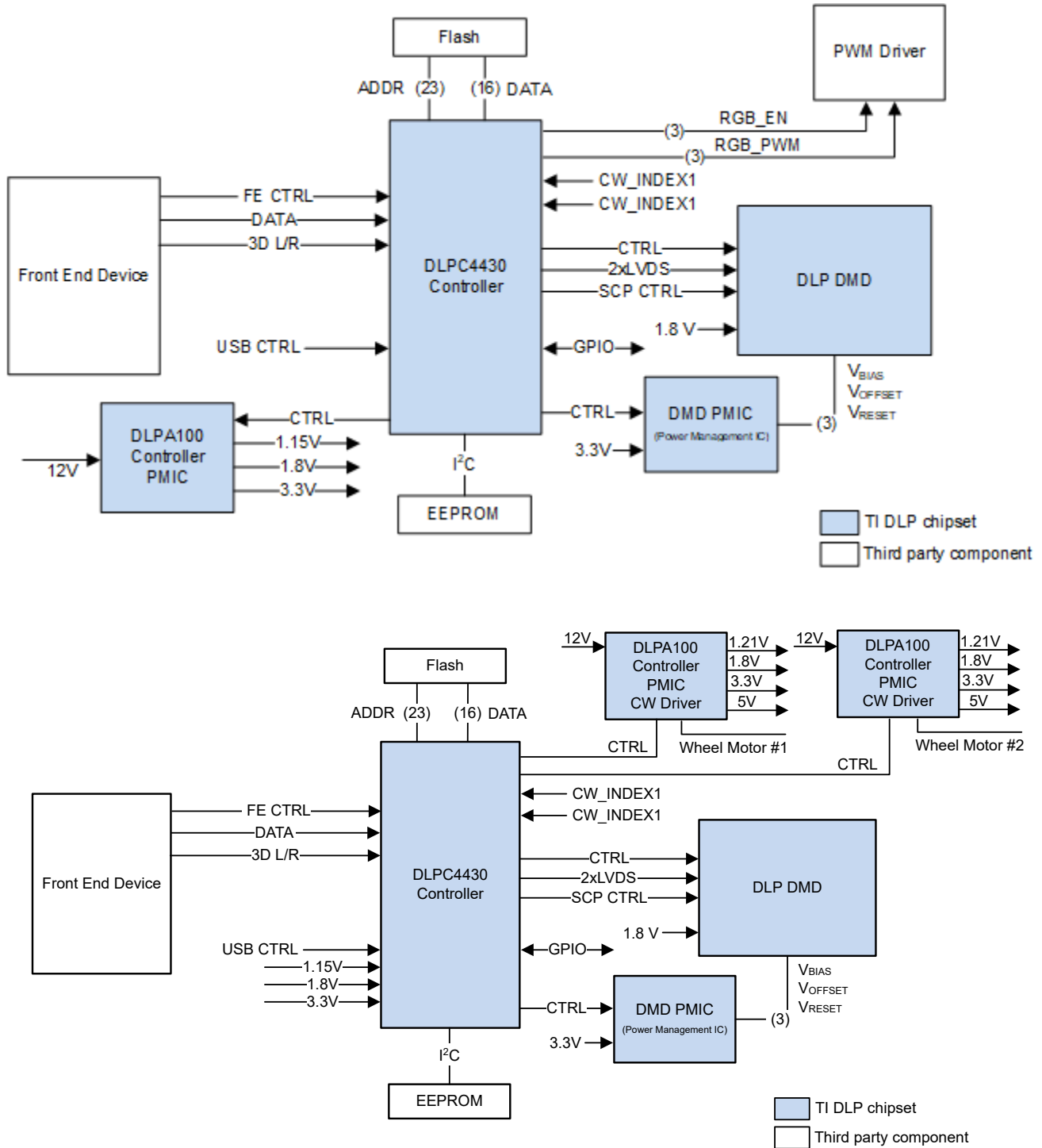
The following orderables have been replaced by the DLP650NE:

#### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)	MECHANICAL ICD
DLP650NET	FYE (350)	35.0 mm × 32.2 mm × 5.1 mm	2511543
1910-6232E	FYE (350)	35.0 mm × 32.2 mm × 5.1 mm	2511543
1910-6237E	FYE (350)	35.0 mm × 32.2 mm × 5.1 mm	2511543
1910-6239E	FYE (350)	35.0 mm × 32.2 mm × 5.1 mm	2511543
1910-623AE	FYE (350)	35.0 mm × 32.2 mm × 5.1 mm	2511543

### 8.2 Typical Application

The DLP650NE DMD combined with a DLPC4430 digital controller and DLPA100 power management device provides full HD resolution for bright, colorful display applications. A typical display system using the DLP650NE and additional system components can be seen in [Figure 8-1](#).



**Figure 8-1. Typical DLPC4430 Application (LED, Top; LPCW, Bottom)**

**8.2.1 Design Requirements**

A DLP650NE projection system is created by using the DMD chipset, including the DLP650NE, DLPC4430, and DLPA100. The DLP650NE DMD is the core imaging device in the display system and contains a 0.65-inch array of micromirrors. The DLPC4430 controller is the digital interface between the DMD and the rest of the system, taking digital input from front end receiver that converts the data from the source and using the converted

data for driving the DMD over a LVDS interface. The DLPA100 power management device provides voltage regulators for the DMD, controller, and illumination functionality.

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The illumination source options include lamp, LED, laser or laser phosphor. The type of illumination used and desired brightness affects the overall system design and size.

### **8.2.2 Detailed Design Procedure**

For a complete DLP system, an optical module or light engine is required that contains the DLP650NE DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DLP650NE DMD must always be used with the DLPC4430 display controllers and a DLPA100 PMIC driver.

## 8 Power Supply Requirements

### 8.1 DMD Power Supply Requirements

The following power supplies are all required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected. DMD power-up and power-down sequencing is strictly controlled by the DLPC4430 device.

#### CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. VCC, VCCI, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. VSS must also be connected. Failure to meet any of the below requirements results in a significant reduction in the DMD's reliability and lifetime. Refer to [Figure 8-1](#).

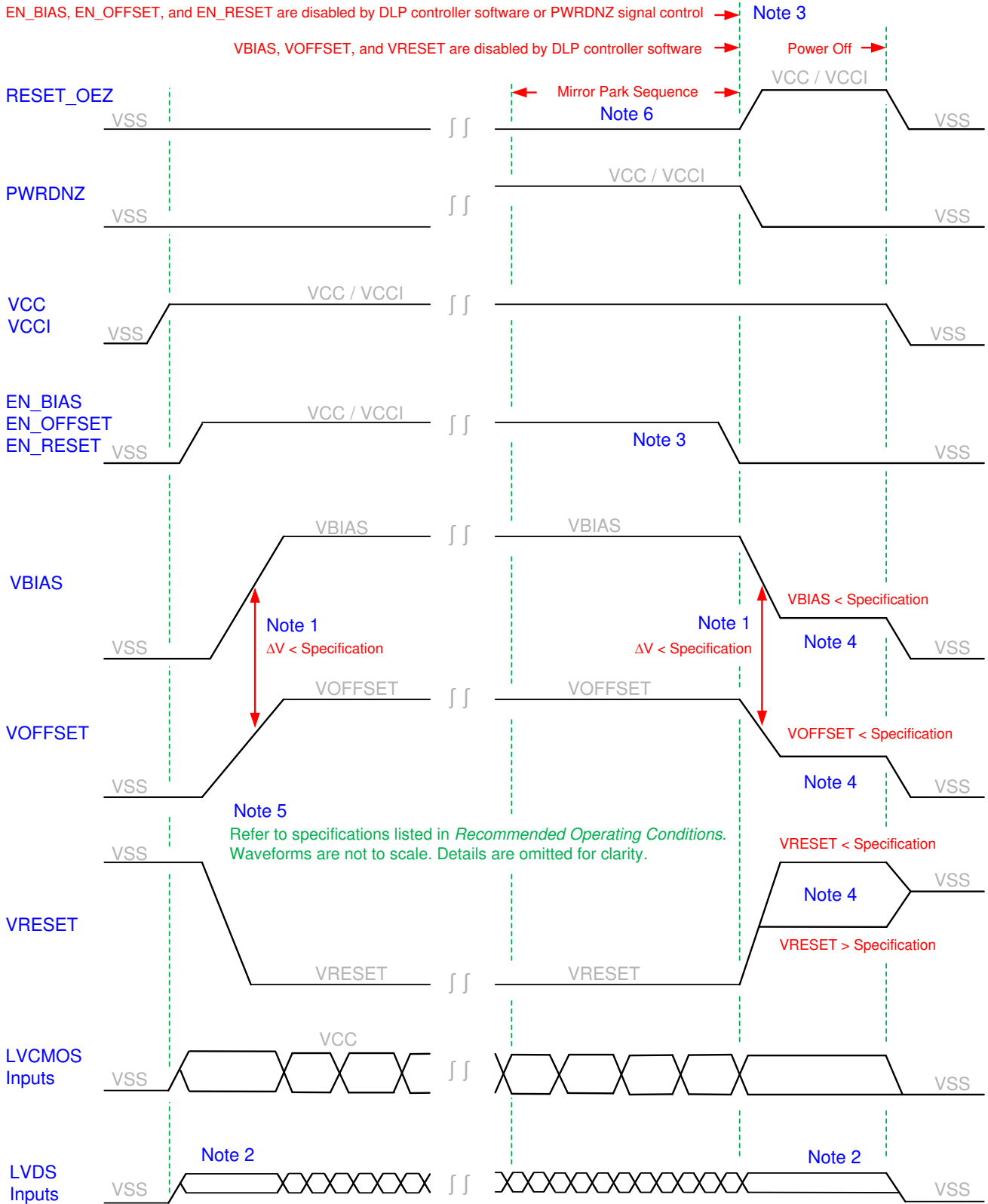
### 8.2 DMD Power Supply Power-Up Procedure

- During power-up, VCC and VCCI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the change between VBIAS and VOFFSET must be within the specified limit shown in [Recommended Operating Conditions](#). During power-up, VBIAS does not have to start after VOFFSET.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed in the [Absolute Maximum Ratings](#) table, in the [Recommended Operating Conditions](#) table, and in the [DMD Power Supply Sequencing Requirements](#) section.
- During power-up, LVCMOS input pins must not be driven high until after VCC and VCCI have settled at operating voltages listed in the [Recommended Operating Conditions](#) table.

### 8.3 DMD Power Supply Power-Down Procedure

- During power-down, VCC and VCCI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within the specified limit of ground. Refer to [Table 8-1](#).
- During power-down, it is a strict requirement that the change between VBIAS and VOFFSET must be within the specified limit shown in the [Section 6.4](#) table. During power-down, it is not mandatory to stop driving VBIAS prior to VOFFSET.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed in [Section 6.1](#), in [Section 6.4](#), and in [Figure 8-1](#).
- During power-down, LVCMOS input pins must be less than specified in the [Section 6.4](#) table.





**Figure 8-1. DMD Power Supply Sequencing Requirements**

- A. To prevent excess current, the supply voltage change  $|V_{BIAS} - V_{OFFSET}|$  must be less than specified in the [Section 6.4](#) table. OEMs may find that the most reliable way to ensure this is to power VOFFSET prior to VBIAS during power-up and to remove VBIAS prior to VOFFSET during power-down.

- B. LVDS signals are less than the input differential voltage (VID) maximum specified in the [Section 6.4](#) table. During power-down, LVDS signals are less than the high level input voltage (VIH) maximum specified in the [Section 6.4](#) table.
- C. When system power is interrupted, the DLP DLPC4430 initiates a hardware power-down that activates PWRDNZ and disables VBIAS, VRESET and VOFFSET after the micromirror park sequence. Software power-down disables VBIAS, VRESET, and VOFFSET after the micromirror park sequence through software control. For either case, enable signals EN\_BIAS, EN\_OFFSET, and EN\_RESET are used to disable VBIAS, VOFFSET, and VRESET, respectively.
- D. Refer to [Table 8-1](#).
- E. Figure not to scale. Details have been omitted for clarity. Refer to the [Section 6.4](#) table.
- F. EN\_BIAS, EN\_OFFSET, and EN\_RESET are disabled by DLP controller software or PWRDNZ signal control.
- G. VBIAS, VOFFSET, and VRESET are disabled by DLP controller software.

**Table 8-1. DMD Power-Down Sequence Requirements**

PARAMETER		MIN	MAX	UNIT
VBIAS	Supply voltage level during power-down sequence		4.0	V
VOFFSET			4.0	V
VRESET		-4.0	0.5	V

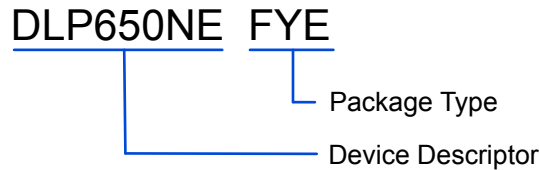
## 9 Device Documentation Support

### 9.1 Third-Party Products Disclaimer

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### 9.2 Device Support

#### 9.2.1 Device Nomenclature

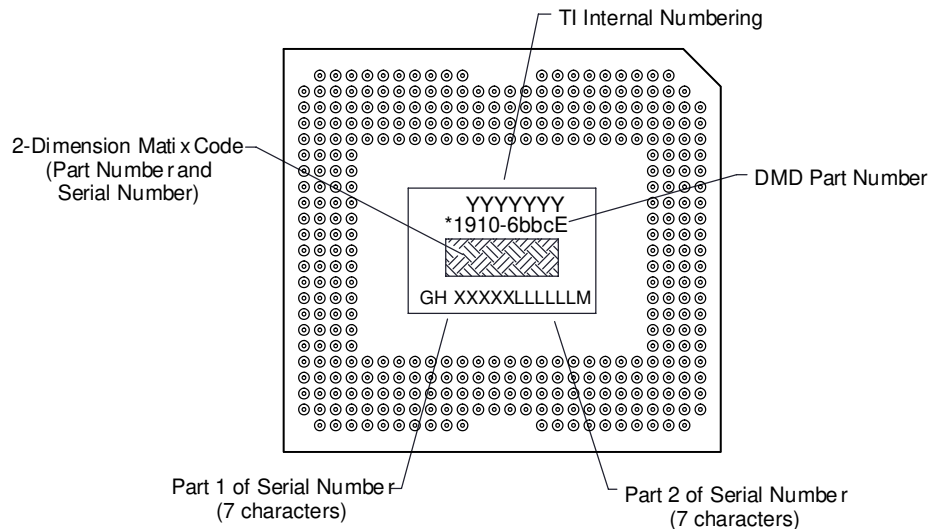


**Figure 9-1. Device Number Description**

#### 9.2.2 Device Markings

The device marking will include both human-readable information and a 2-dimensional matrix code. The human-readable information is described in [Figure 9-2](#). The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number. The first character of the DMD Serial Number (part 1) is the manufacturing year. The second character of the DMD Serial Number (part 1) is the manufacturing month. The last character of the DMD Serial Number (part 2) is the bias voltage bin letter.

Examples: \*1910-623AE GHXXXXX LLLLLLM



**Figure 9-2. DMD Marking**

## 9.3 Documentation Support

### 9.3.1 Related Documentation

The following documents contain additional information related to the use of the DLP650NE device.

- [DLPC4430 Digital Controller Data Sheet](#)
- [TPS65145 Triple output LCD Supply with Linear Regulator and Power Good](#)
- [DLPA100 Power Management and Motor Driver](#)
- [DMD101: Introduction to Digital Micromirror Device \(DMD\) Technology](#)

## 9.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.5 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 9.6 Trademarks

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DLP® is a registered trademark of Texas Instruments.

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## 9.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.8 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP650NEFYE	ACTIVE	CPGA	FYE	350	21	RoHS & Green	NI-PD-AU	N / A for Pkg Type	0 to 70		Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TRAY**



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

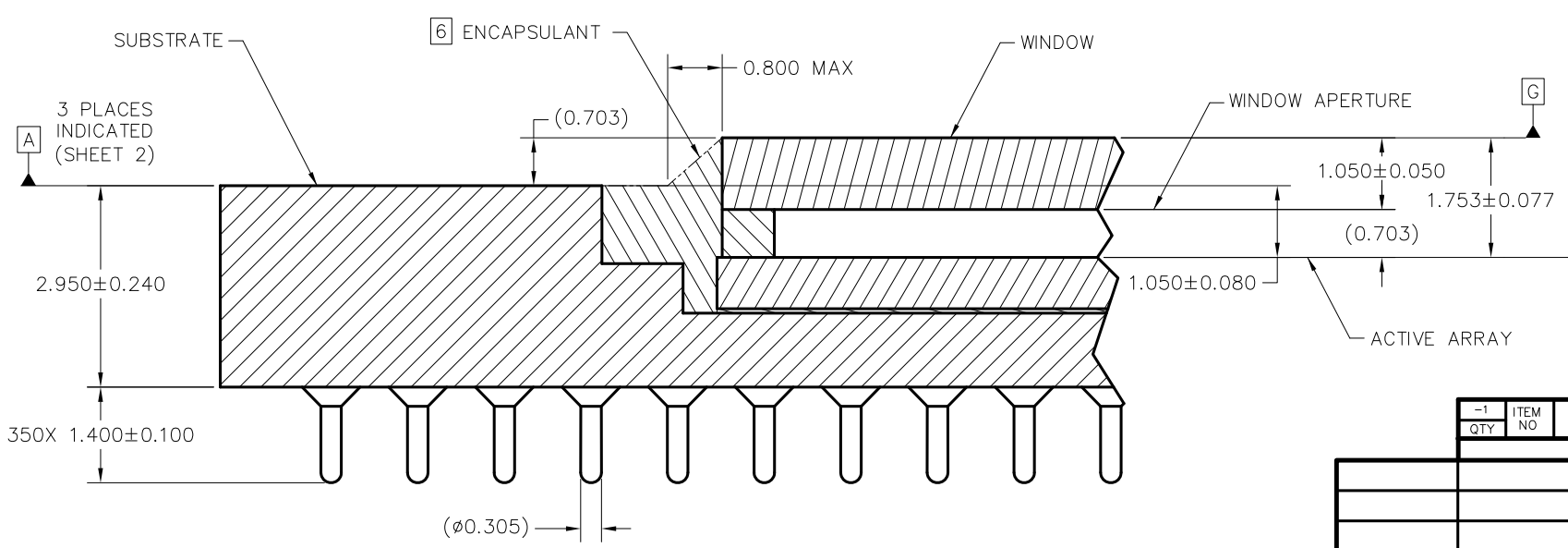
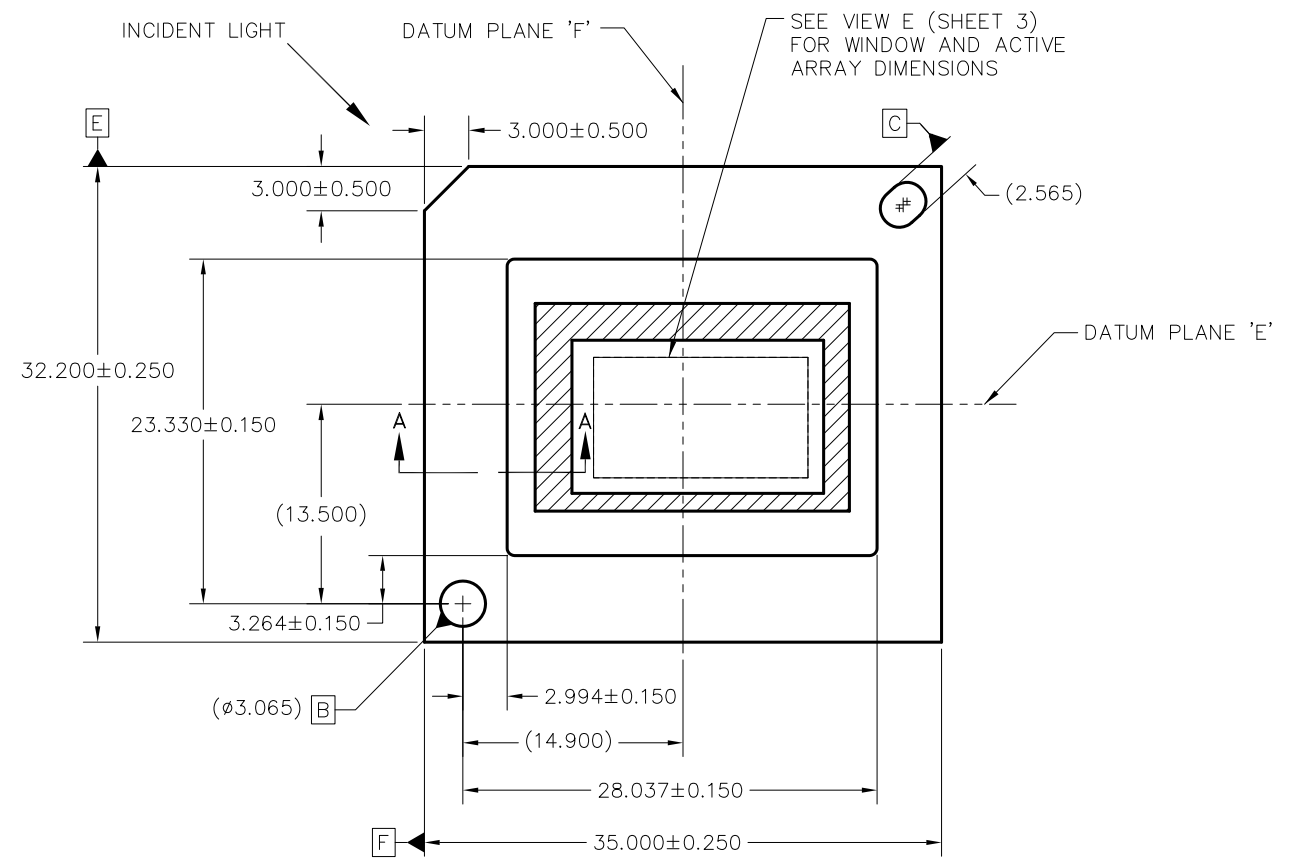
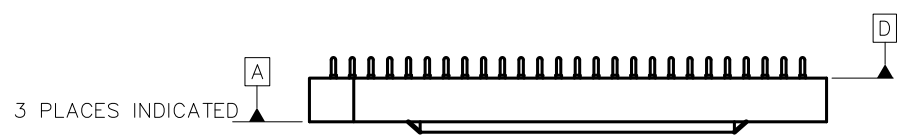
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DLP650NEFYE	FYE	CPGA	350	21	3 x 7	150	315	135.9	12190	43.9	25.8	26.85

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NOTES: UNLESS OTHERWISE SPECIFIED:

- 1 SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
- 2 DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
- 3 ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
- 4 SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES ARE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
- 5 BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
- 6 MAXIMUM ENCAPSULANT PROFILE SHOWN
- 7 ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
- 8 SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	ECO 2111739, INITIAL RELEASE	11/04/2010	F. ARMSTRONG
B	ECO 2112602, CHANGE TOLERANCES ON OUTSIDE DIMENSIONS TO ±0.250; CHANGE DATUM B, BACK SIDE PINS, AND DATUM PLANES 'E' AND 'F' TO REFERENCE CENTERLINE OF PART	12/10/2010	F. ARMSTRONG
C	ECO 2135107, ADD NOTE 8 TO SHEETS 1 & 4	08/02/2013	F. ARMSTRONG
D	ECO 2139887, CHG GLASS SIZE UPPER TOL TO +0.050 TO MATCH PROCESS CAPABILITY	02/14/2014	F. ARMSTRONG
E	ECO 2179962, ADD PKG REF DESIGNATOR FYE TO TITLE BLOCK	03/04/2019	F. ARMSTRONG



SECTION A-A  
SCALE 20/1

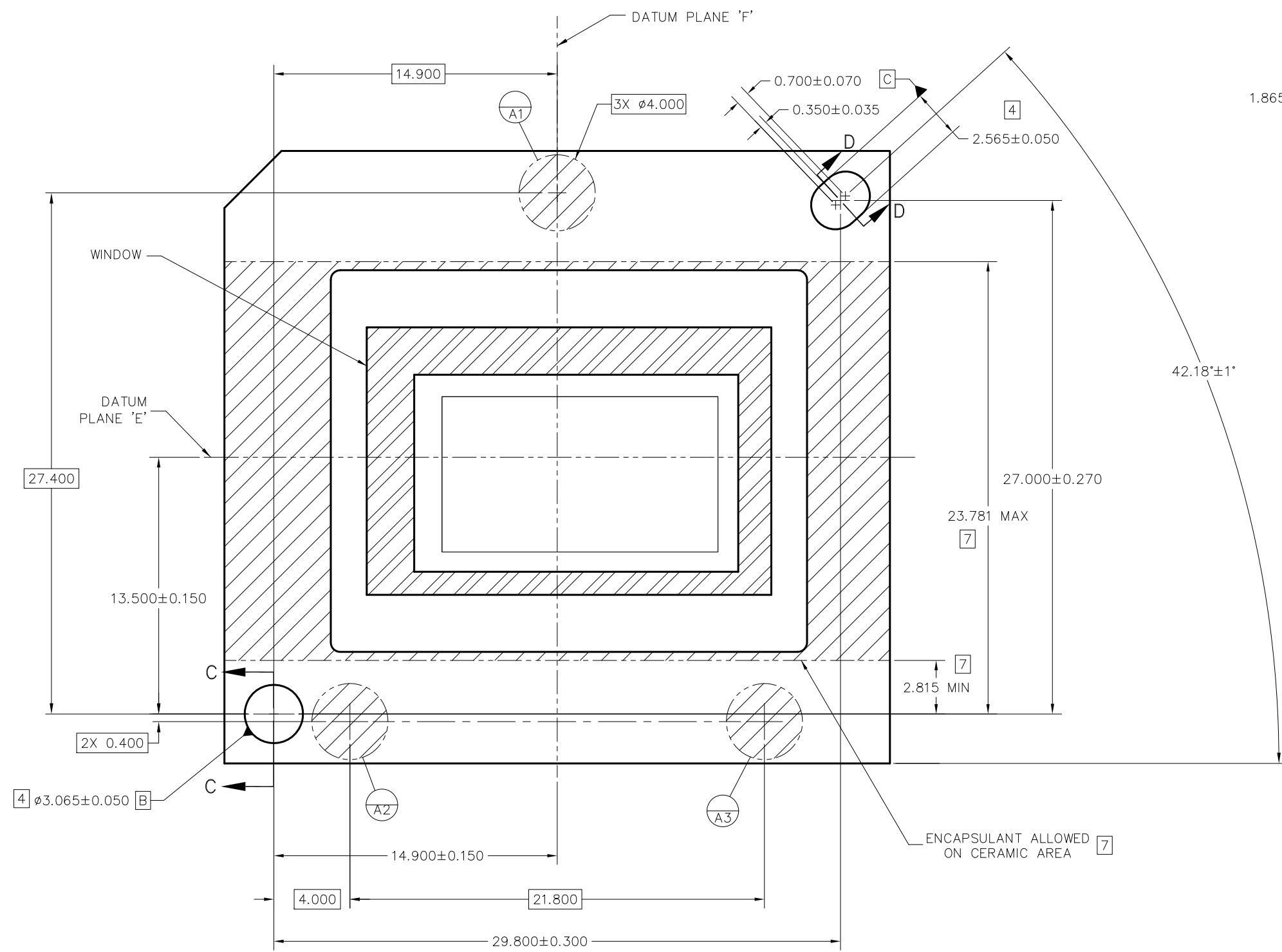
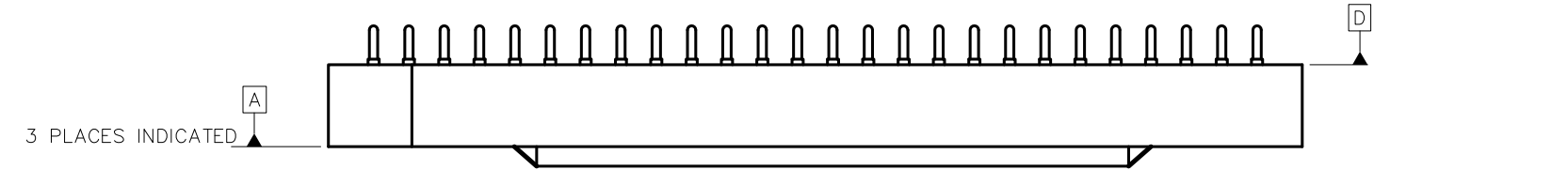
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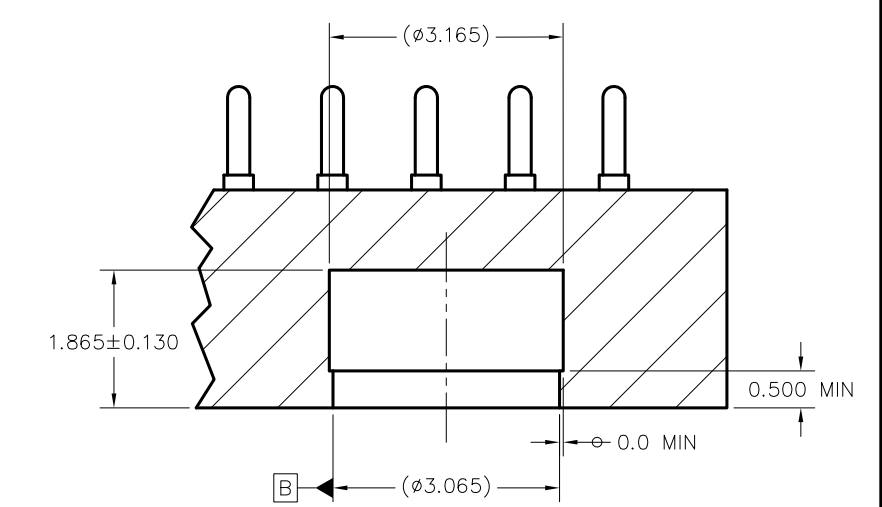
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QA	P. KONRAD	11/08/2010	
COE	M. DORAK	11/08/2010	

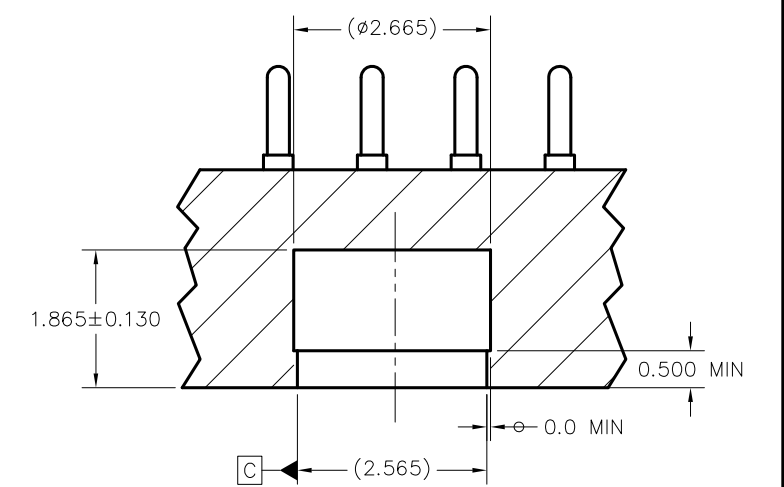
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS TOLERANCES: ANGLES ± 1° 2 PLACE DECIMALS ±0.25 3 PLACE DECIMALS ±0.50		TEXAS INSTRUMENTS Dallas, Texas	
REMOVE ALL BURRS AND SHARP EDGES INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5-1994 DIMENSIONAL LIMITS APPLY BEFORE PROCESSES PARENTHEICAL INFO FOR REF ONLY		ICD, MECHANICAL, DMD .65 1080p MVSP 2XLVDS SERIES 600 (FYE PACKAGE)	
THIRD ANGLE PROJECTION	NONE	0314DA	SIZE B
NEXT ASSY	USED ON	APPLICATION	DRAWING NO 2511543
			REV E
			SCALE 4/1
			SHEET 1 OF 4



VIEW B  
DATUMS AND ENCAPSULANT ALLOWABLE AREA  
SCALE 8/1

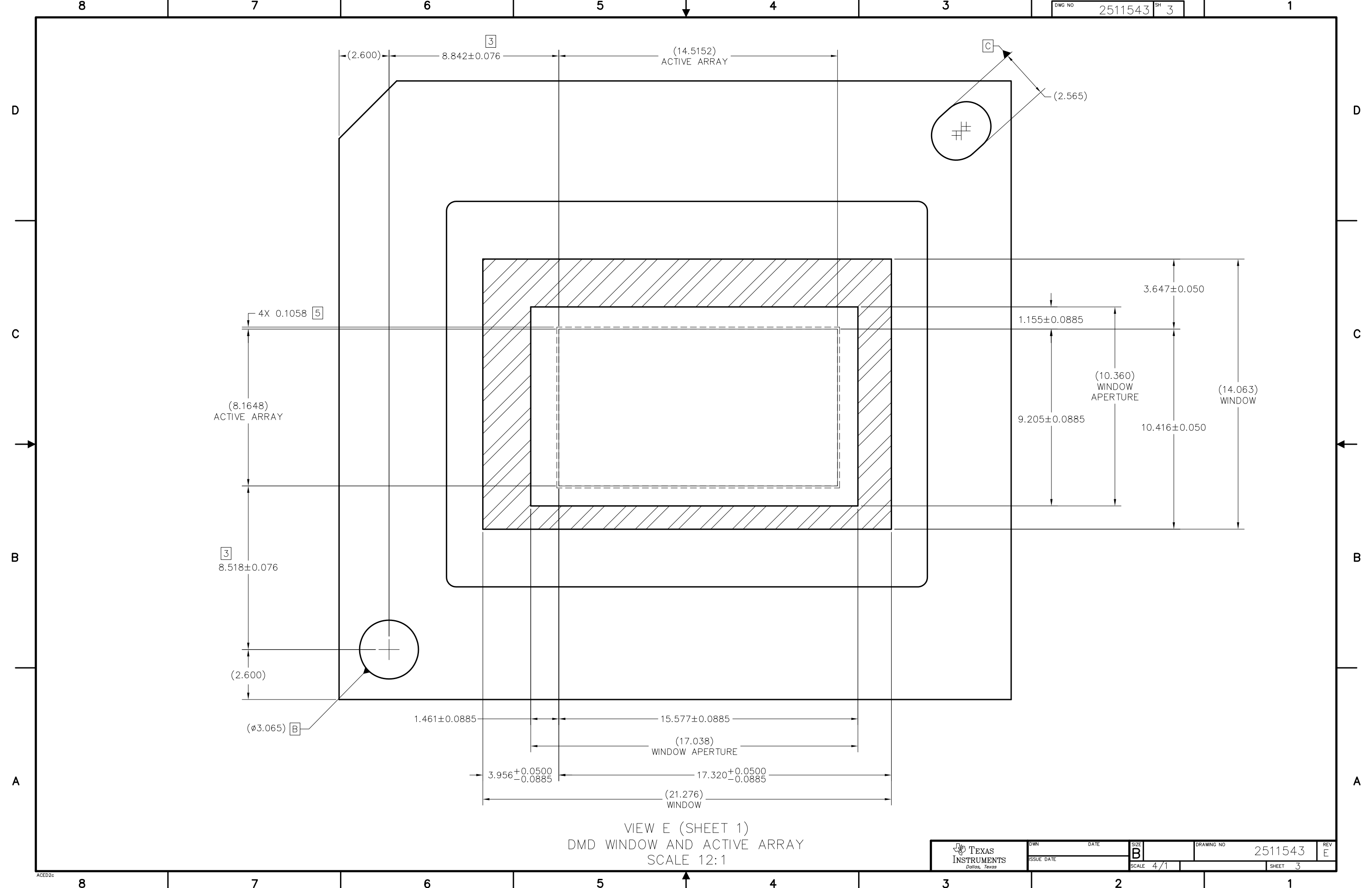


SECTION C-C  
DATUM B  
SCALE 16/1



SECTION D-D  
DATUM C  
SCALE 16/1





(2.600)

8.842±0.076

(14.5152)  
ACTIVE ARRAY

(2.565)

4X 0.1058

(8.1648)  
ACTIVE ARRAY

8.518±0.076

(2.600)

(∅3.065)

1.461±0.0885

15.577±0.0885

(17.038)  
WINDOW APERTURE

3.956<sup>+0.0500</sup><sub>-0.0885</sub>

17.320<sup>+0.0500</sup><sub>-0.0885</sub>

(21.276)  
WINDOW

1.155±0.0885

9.205±0.0885

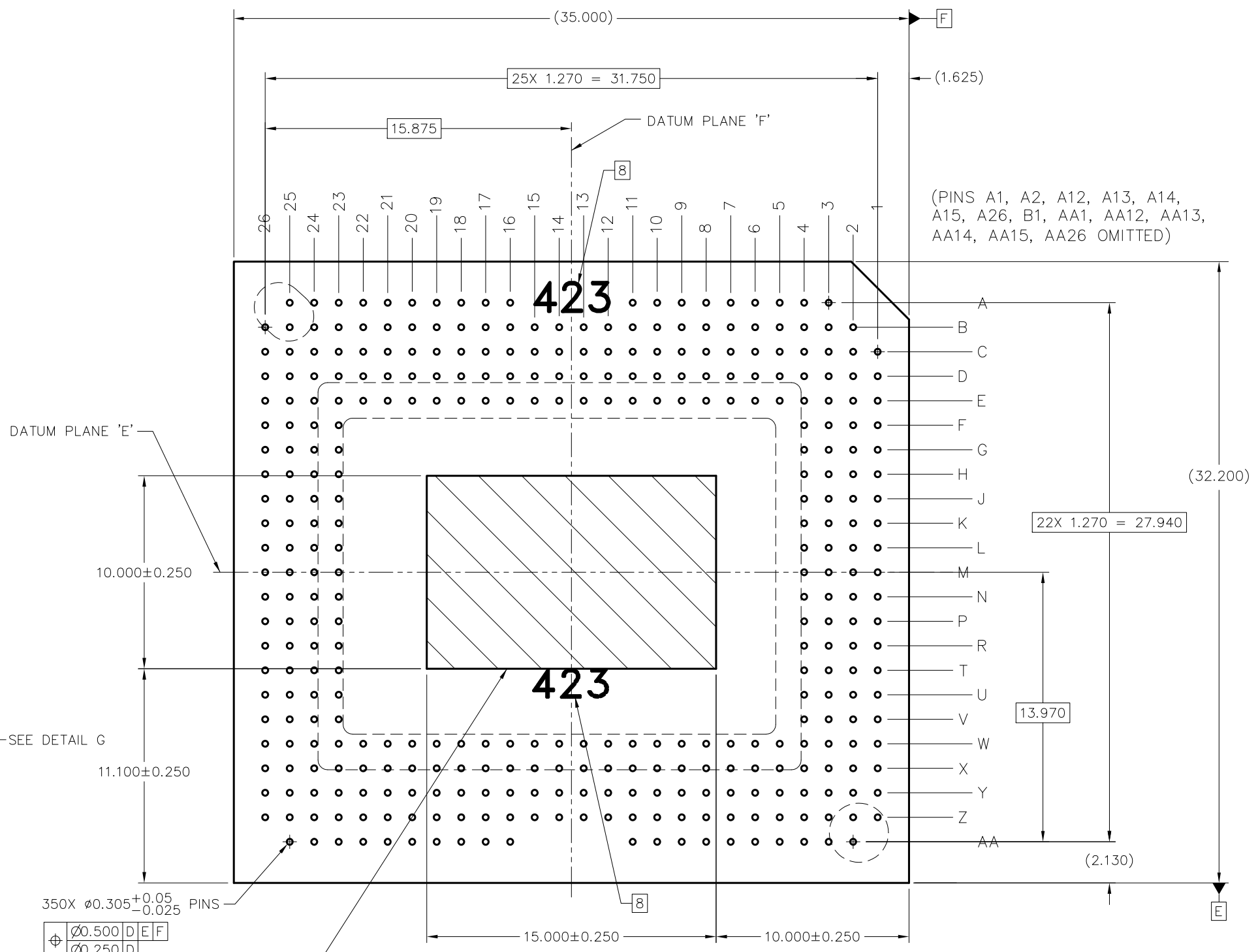
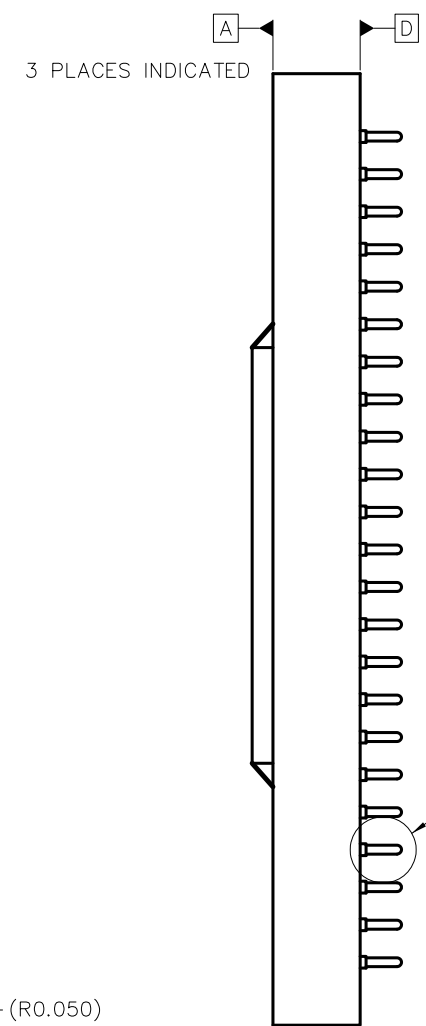
(10.360)  
WINDOW APERTURE

3.647±0.050

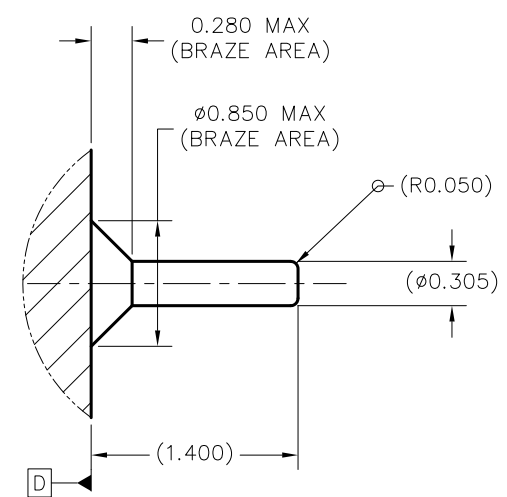
10.416±0.050

(14.063)  
WINDOW

VIEW E (SHEET 1)  
DMD WINDOW AND ACTIVE ARRAY  
SCALE 12:1



(PINS A1, A2, A12, A13, A14, A15, A26, B1, AA1, AA12, AA13, AA14, AA15, AA26 OMITTED)



DETAIL G (350 PLACES)  
PIN & BRAZE DIMENSIONS  
SCALE 40/1

VIEW F-F (SHEET 1)  
PINS AND SYMBOLIZATION PAD  
SCALE 8/1

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