ESD2CANxx36-Q1 Automotive 2-Channel, 36V ESD Protection Diode for In-Vehicle Networks

1 Features

- 36V working voltage
- IEC 61000-4-2 ESD protection:
  - ±25kV contact and ±25kV air-gap discharge (ESD2CAN36-Q1)
  - ±18kV contact and ±18kV air-gap discharge (ESD2CANFD36-Q1)
- ISO 10605 (330pF, 330 Ω) ESD protection:
  - ±25kV contact and ±25kV air-gap discharge (ESD2CAN36-Q1)
  - ±18kV contact and ±18kV air-gap discharge (ESD2CANFD36-Q1)
- IEC 61000-4-5 surge protection (8/20µs):
  - 4.3A (ESD2CAN36-Q1)
  - 3.1A (ESD2CANFD36-Q1)
- Bidirectional ESD protection
- I/O capacitance = 2.8pF typical (ESD2CAN36-Q1)
- I/O capacitance = 2.6pF typical (ESD2CANFD36-Q1)
- Low clamping voltage protects downstream components
- AEC-Q101 qualified
- SOT-23 (DBZ) small, standard footprint
- Leaded packages to allow for automatic optical inspection (AOI)

2 Applications

- Automotive in-vehicle networks:
  - Controller area network (CAN)
  - Controlled area network flexible data-rate (CAN-FD)
  - Low, fault tolerant CAN
  - High-speed CAN
- Industrial control networks:
  - DeviceNet IEC 62026-3
  - CANopen – CiA 301/302-2 and EN 50325-4

3 Description

The ESD2CANxx36-Q1 is a bidirectional ESD protection diode for controller area network (CAN) interface protection. The ESD2CANxx36-Q1 is rated to dissipate contact ESD strikes specified in the ISO 10605 automotive standard. The low dynamic resistance and low clamping voltage enables system level protection against transient events. This protection is key as automotive systems require a high level of robustness and reliability for safety applications.

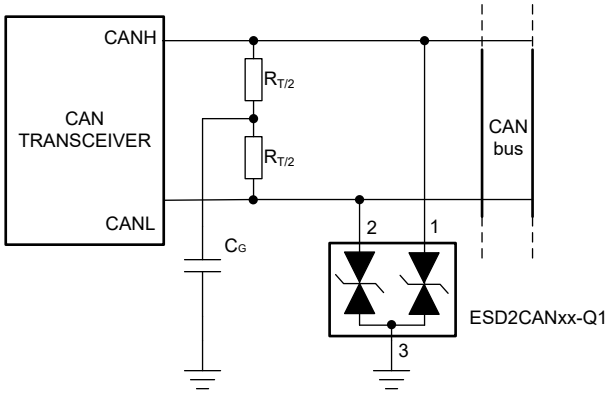
This device features a low IO capacitance per channel and a pin-out to suit two automotive CAN bus lines (CANH and CANL) from the damage caused by electrostatic discharge (ESD) and other transients. Additionally, the 2.8pF (typical) or less line capacitance of the ESD2CANxx36-Q1 is an excellent choice for CAN, CAN-FD, and CAN SiC applications.

The ESD2CANxx36-Q1 is offered in the 3-pin SOT-23 leaded package for easy flow through routing.

Device Information

PART NUMBER	CHANNEL COUNT	PACKAGE(1)
ESD2CAN36-Q1	2 Channels	DBZ (SOT-23, 3)
ESD2CANFD36-Q1		

(1) For more information, see Section 9



ESD2CANxx36-Q1 Typical Application

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4 Pin Configuration and Functions

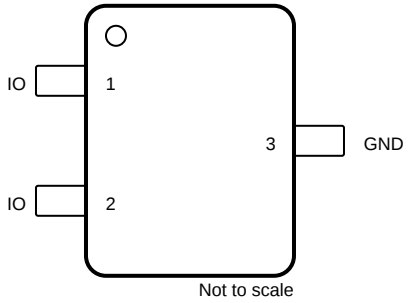


Figure 4-1. DBZ Package, 3-Pin SOT-23 (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
IO	1, 2	I/O	ESD protected IO
GND	3	G	Connect to ground.

(1) I/O = Input or Output, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		DEVICE	MIN	MAX	UNIT
P_{PP}	IEC 61000-4-5 Power (t_p – 8/20 µs) at 25°C	ESD2CAN36-Q1		233	W
		ESD2CANFD36-Q1		175	
I_{PP}	IEC 61000-4-5 current (t_p – 8/20 µs) at 25°C	ESD2CAN36-Q1		4.3	A
		ESD2CANFD36-Q1		3.1	
T_A	Operating free-air temperature		-55	150	°C
T_J	Junction temperature		-55	150	
T_{stg}	Storage temperature		-65	155	

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings—AEC Specification

PARAMETER		TEST CONDITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q101-001 (1)	± 2500	V
		Charged device model (CDM), per AEC Q101-005 (2)	± 1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings—IEC Specification

over TA = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	DEVICE	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, all pins	ESD2CAN36-Q1	±25000	V
			ESD2CANFD36-Q1	±18000	
		IEC 61000-4-2 Air-gap Discharge, all pins	ESD2CAN36-Q1	±25000	
			ESD2CANFD36-Q1	±18000	

5.4 ESD Ratings - ISO Specification

over TA = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	DEVICE	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Contact discharge	ISO 10605, 150pF, 330Ω, IO	ESD2CAN36-Q1	±25000	V
				ESD2CANFD36-Q1	±18000	
			ISO 10605, 330pF, 330Ω, IO	ESD2CAN36-Q1	±25000	
				ESD2CANFD36-Q1	±18000	
		Air-gap discharge	ISO 10605, 150pF, 330Ω, IO	ESD2CAN36-Q1	±25000	
				ESD2CANFD36-Q1	±18000	
			ISO 10605, 330pF, 330Ω, IO	ESD2CAN36-Q1	±25000	
				ESD2CANFD36-Q1	±18000	

5.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	-36		36	V
T_A	Operating free-air temperature	-55		150	°C

5.6 Thermal Information

THERMAL METRIC(1)		ESD2CAN36-Q1 DBZ (SOT-23) 3 PINS	ESD2CANFD36-Q1 DBZ (SOT-23) 3 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	293.4	313.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	148.9	162.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	133.0	151.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	32.9	43.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	132.0	150.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.7 Electrical Characteristics

over T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	DEVICE	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage			–36		36	V
V_{BRF}	Breakdown voltage(2)	I_{IO} = 10mA, IO to GND		37.8	40	44.2	V
V_{BRR}		I_{IO} = –10mA, IO to GND		–37.8	-40	–44.2	V
V_{CLAMP}	Clamping voltage(3)	I_{PP} = 1A, t_p = 8/20µs, IO to GND	ESD2CAN36-Q1		43		V
V_{CLAMP}		I_{PP} = 4.3A, t_p = 8/20µs, IO to GND	ESD2CAN36-Q1		61		V
V_{CLAMP}		I_{PP} = 1A, t_p = 8/20µs, IO to GND	ESD2CANFD36-Q1		47		V
V_{CLAMP}		I_{PP} = 3.1A, t_p = 8/20µs, IO to GND	ESD2CANFD36-Q1		61		V
V_{CLAMP}	Clamping voltage(4)	I_{PP} = 16 A, TLP, IO to GND or GND to IO	ESD2CAN36-Q1		63		V
V_{CLAMP}			ESD2CANFD36-Q1		64		V
I_{LEAK}	Leakage current	V_{IO} = ±24 V, IO to GND		-50	5	50	nA
R_{DYN}	Dynamic resistance(4)	IO to GND and GND to IO	ESD2CAN36-Q1		0.49		Ω
			ESD2CANFD36-Q1		0.49		Ω
C_L	Line capacitance(5)	V_{IO} = 0 V, f = 1MHz, V_{pp} = 30mV	ESD2CAN36-Q1		2.8	3.5	pF
			ESD2CANFD36-Q1		2.6	2.9	

(1) Measurements made on each IO channel
(2) V_{BRF} and V_{BRR} are defined as the voltage when ±10mA is applied in the positive and negative going direction respectively, before the device latches into the snapback state
(3) Device stressed with 8/20µs exponential decay waveform according to IEC 61000-4-5
(4) Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008
(5) Measured from IO to GND on each channel

5.8 Typical Characteristics – ESD2CAN36-Q1

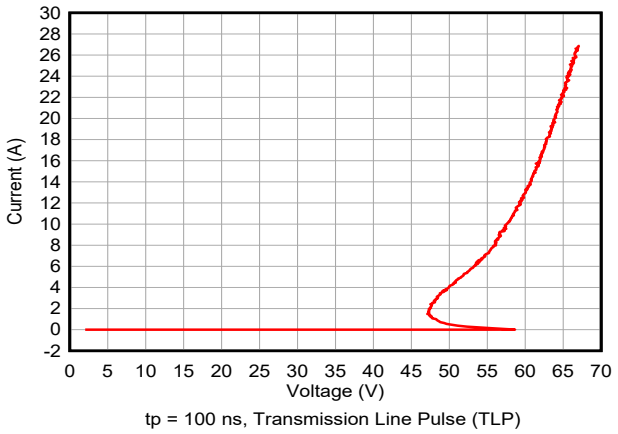


Figure 5-1. Positive TLP Curve

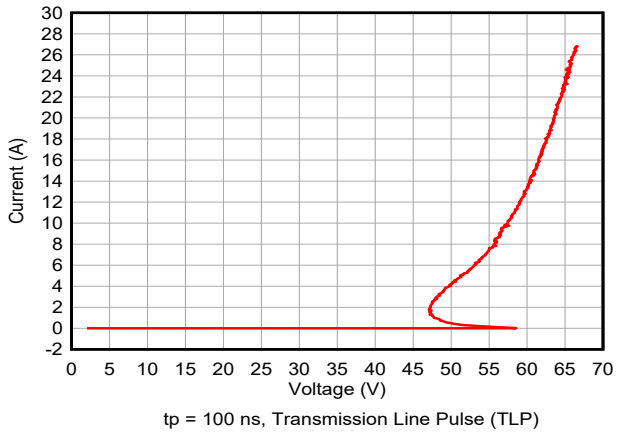


Figure 5-2. Negative TLP Curve

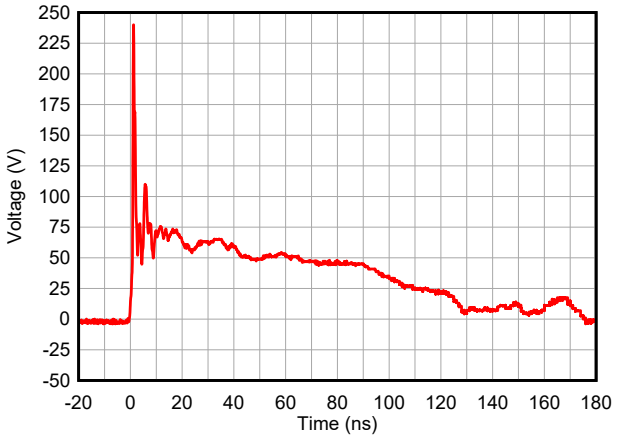


Figure 5-3. +8kV Clamped IEC Waveform

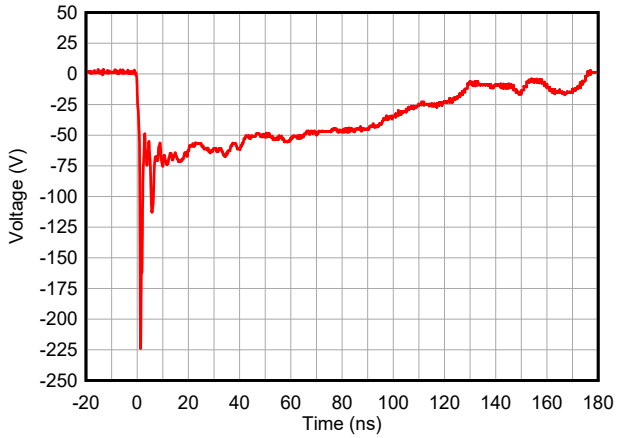


Figure 5-4. −8kV Clamped IEC Waveform

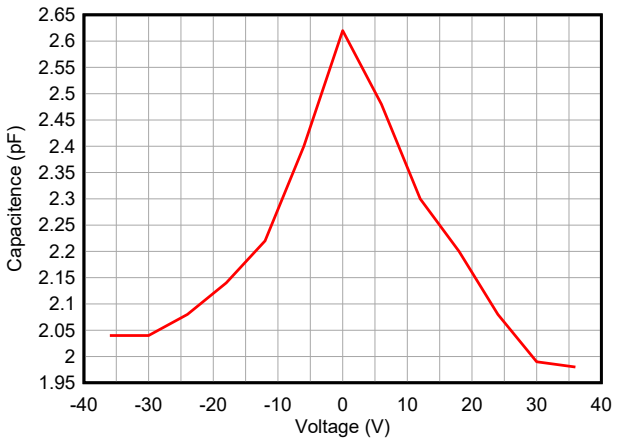


Figure 5-5. Capacitance vs. Bias Voltage

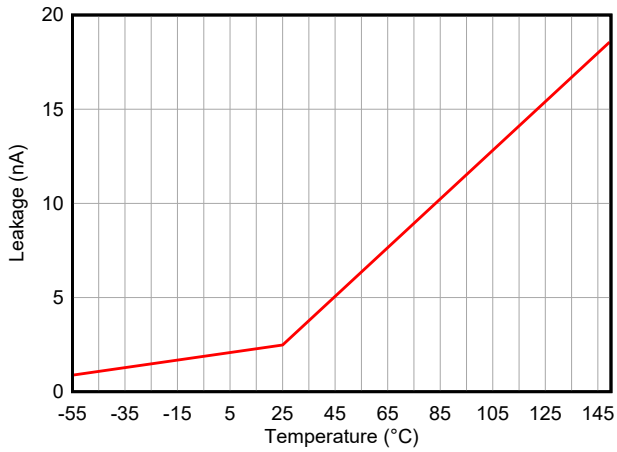


Figure 5-6. Leakage Current vs. Bias Voltage Across Temperature

5.9 Typical Characteristics- ESD2CANFD36-Q1

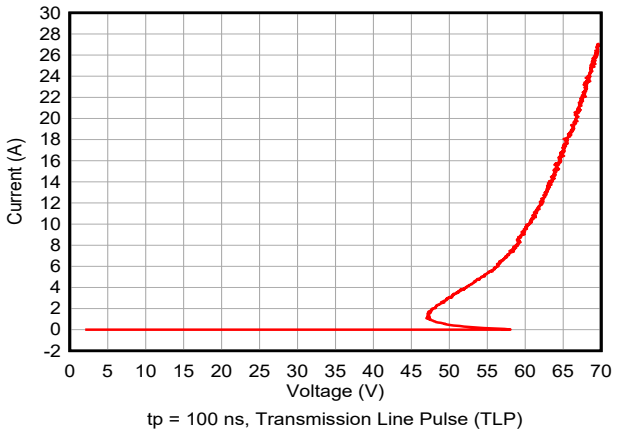


Figure 5-7. Positive TLP Curve

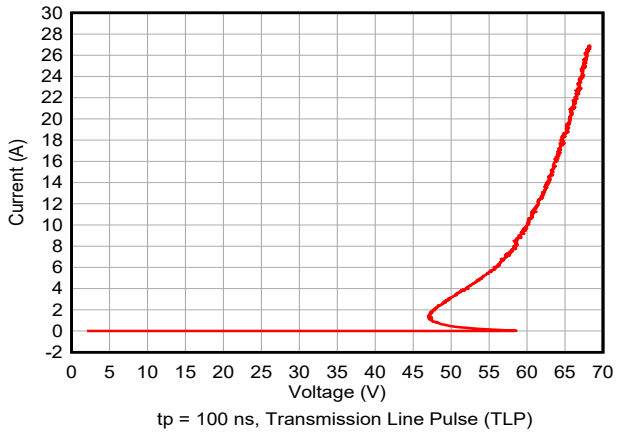


Figure 5-8. Negative TLP Curve

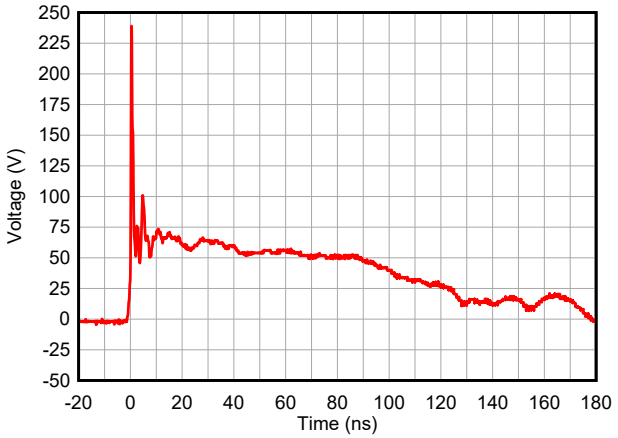


Figure 5-9. +8kV Clamped IEC Waveform

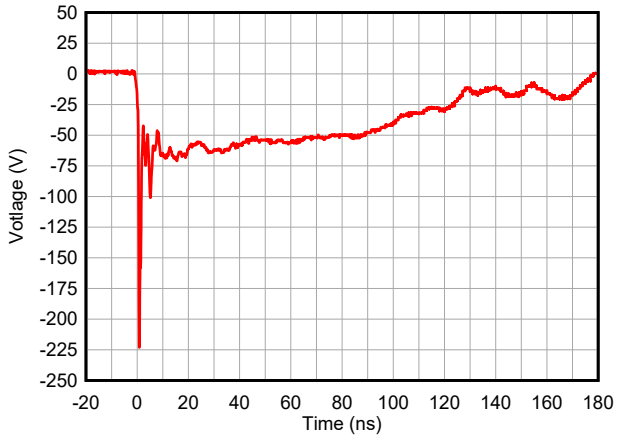


Figure 5-10. -8kV Clamped IEC Waveform

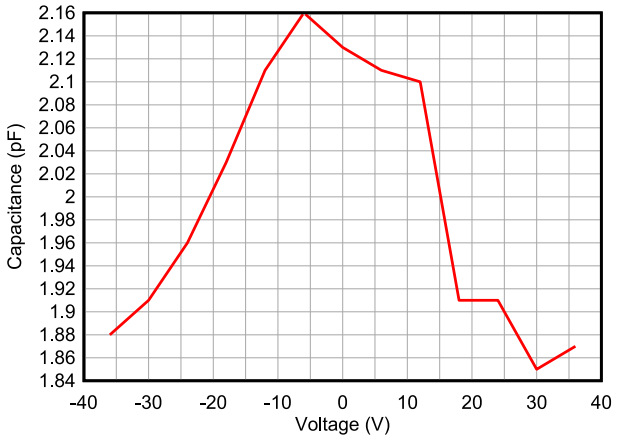


Figure 5-11. Capacitance vs. Bias Voltage

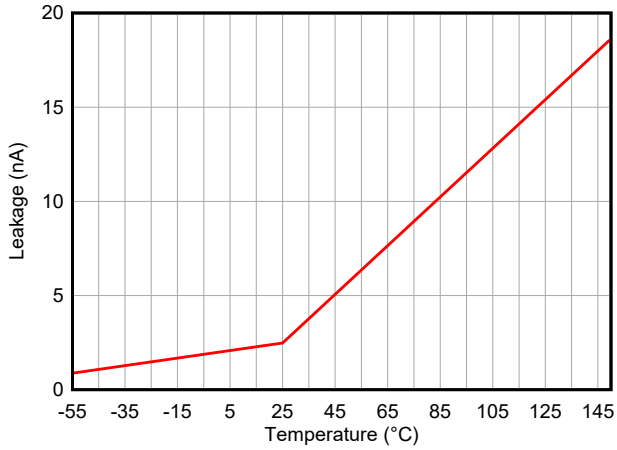


Figure 5-12. Leakage vs. Temperature

6 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The ESD2CANxx36-Q1 is a dual channel TVS diode that provides a path to ground for dissipating ESD events on differential CAN signal lines. The CAN signal lines are typically routed throughout the automobile to connect between the different ECUs. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC.

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 Documentation Support

7.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* user's guide
- Texas Instruments, *ESD Protection Diodes EVM* user's guide
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

7.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2024) to Revision A (March 2024)	Page
• Changed the status of data sheet from: *Advanced Information* to: *Production Data*	1

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD2CAN36DBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z18	Samples
ESD2CANFD36DBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	2Z58	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

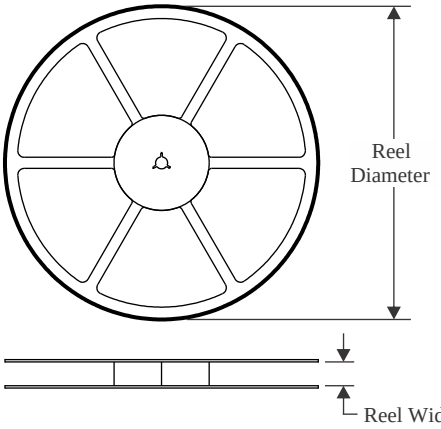
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

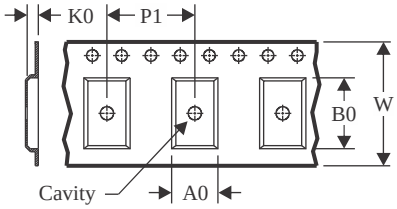
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

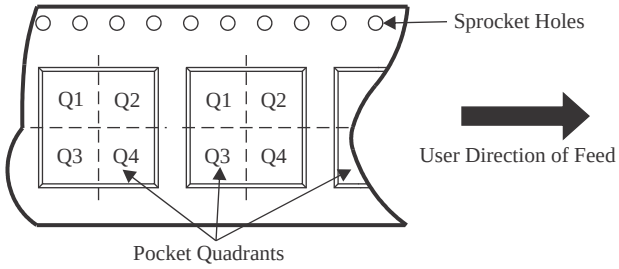


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

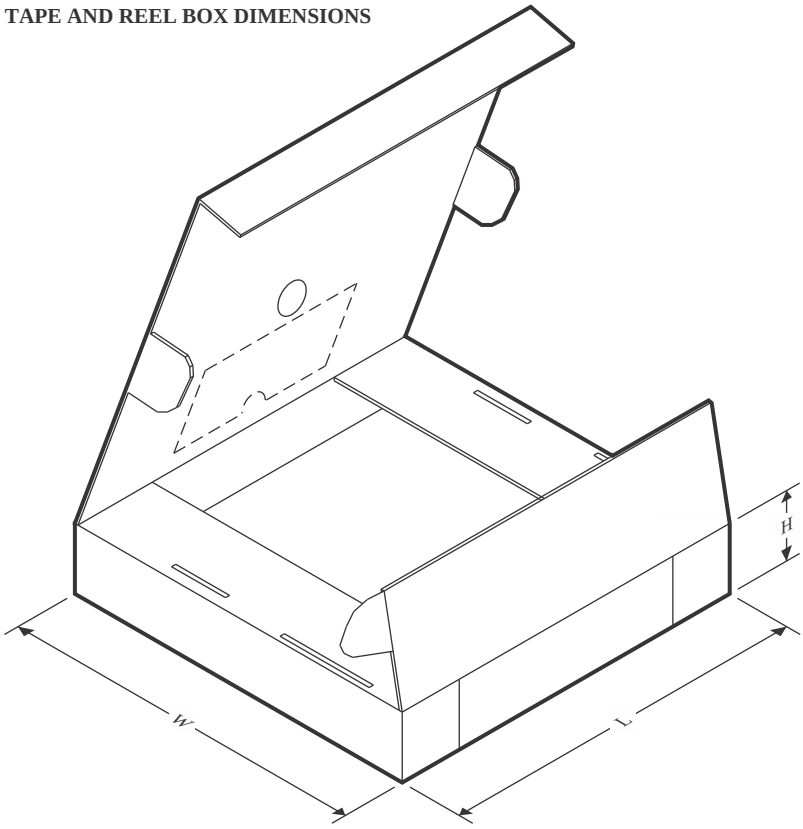
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD2CAN36DBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3
ESD2CANFD36DBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	2.9	3.35	1.35	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

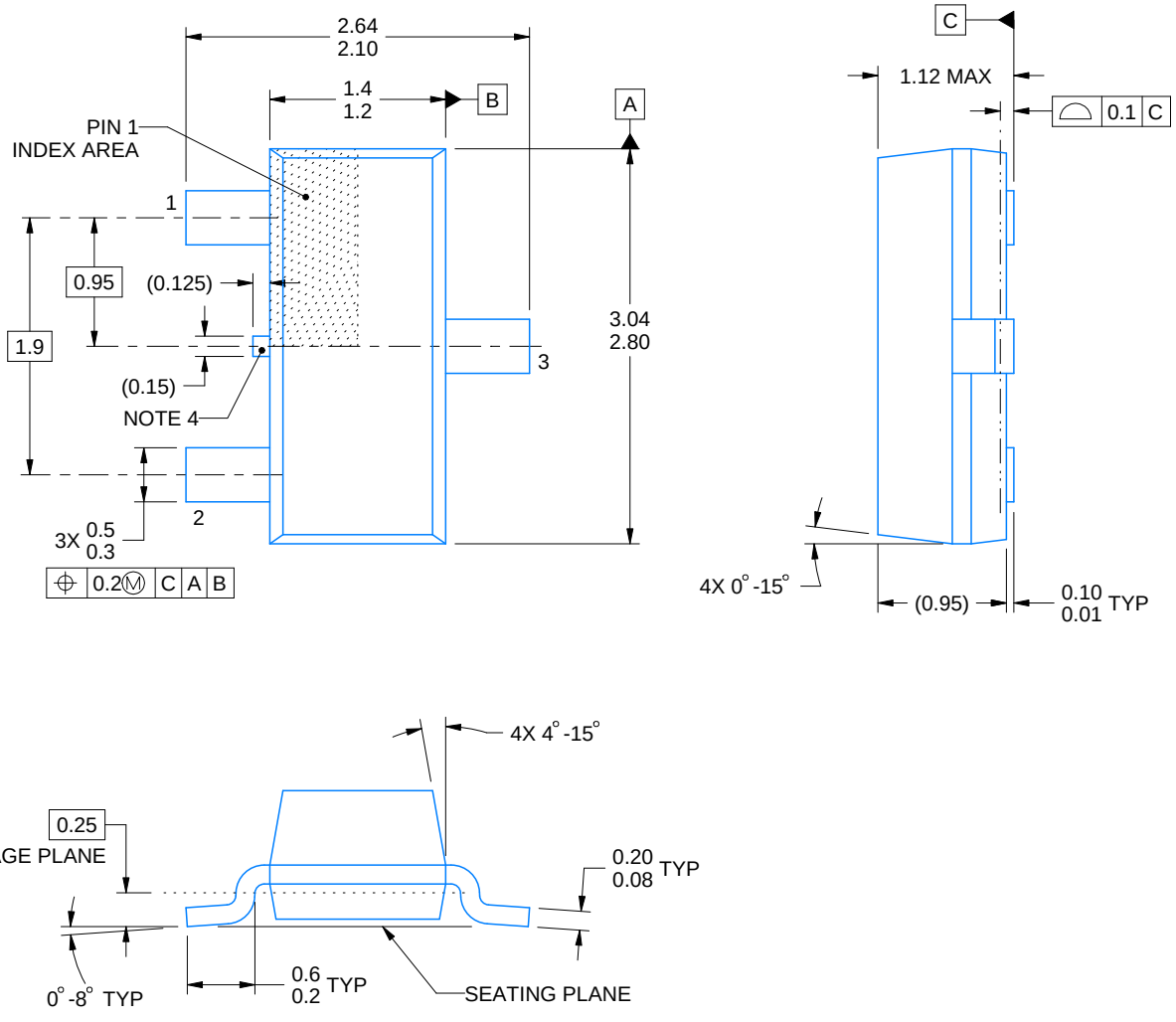
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD2CAN36DBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0
ESD2CANFD36DBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBZ0003A

SOT-23 - 1.12 mm max height

SMALL OUTLINE TRANSISTOR



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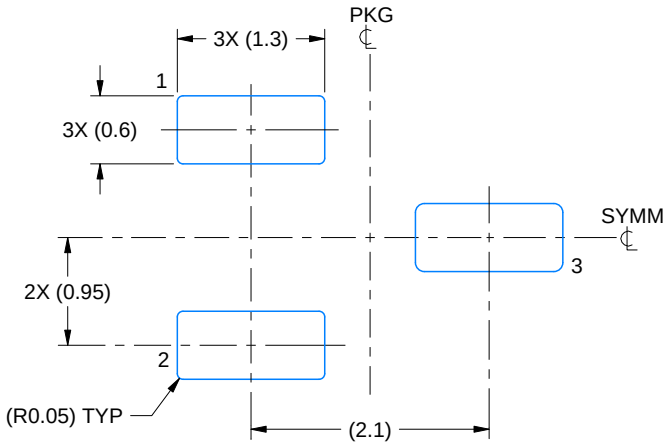
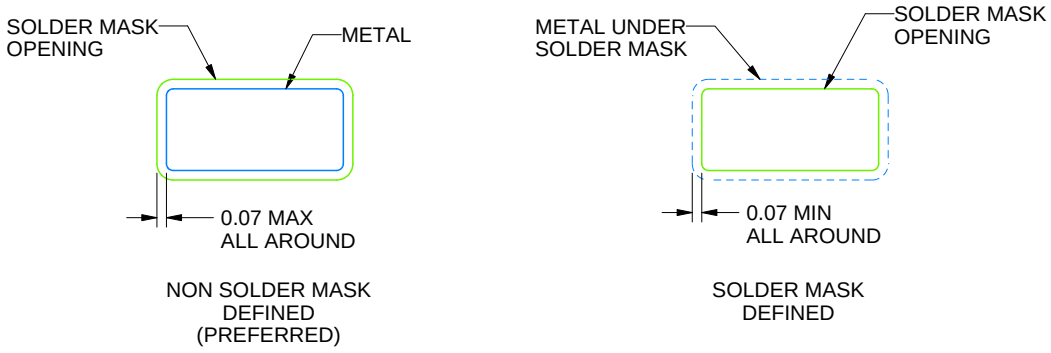
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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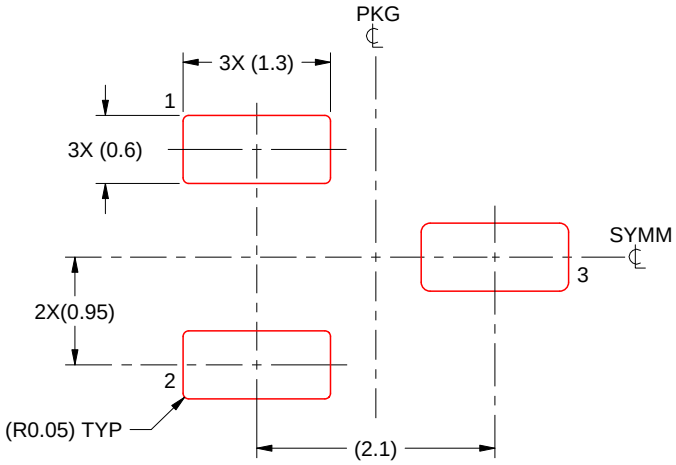
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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