LM21215A 2.95-V to 5.5-V,15-A, Voltage-Mode Synchronous Buck Converter With Frequency Synchronization

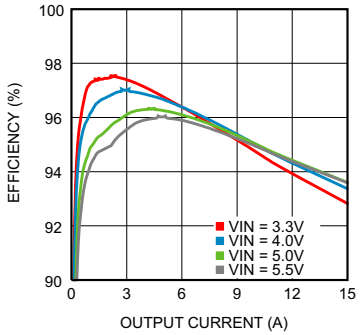
1 Features

- High-Efficiency Synchronous DC/DC Converter
  - Input Voltage Range of 2.95 V to 5.5 V
  - Adjustable Output Voltage From 0.6 V to V_{IN}
  - Output Current as High as 15 A
- Frequency Synchronization 300 kHz to 1.5 MHz
- Integrated 7-mΩ PMOS Buck Switch Supports 100% Duty Cycle for Low Dropout Voltage
- Integrated 4.3-mΩ NMOS Synchronous Rectifier Eliminates Schottky Diode
- Accurate ±1% Internal Voltage Reference
- Automatic Diode Emulation Mode for Improved Efficiency at Light Loads
- Monotonic Pre-Biased Startup
- Internal 0.5-ms or Externally Adjustable Soft Start
- Output Voltage Tracking Capability
- Ultra-Fast Line and Load Transient Response
  - Voltage-Mode PWM Control
  - Wide-Bandwidth Voltage Loop Error Amplifier
- Precision Enable with Hysteresis
- Integrated OVP, UVP, OCP, and UVLO
- Open-Drain Power Good Indicator
- Thermal Shutdown Protection With Hysteresis
- Thermally-Enhanced HTSSOP-20 Package
- Create a custom design using the LM21215A with the WEBENCH® Power Designer

2 Applications

- Telecommunications Infrastructure
- DSP and FPGA Core Voltage Supplies
- High Efficiency POL Conversion
- Embedded Computing, Servers and Storage

Efficiency at 2.5 V, 500 kHz



3 Description

The LM21215A is a synchronous buck DC-DC converter that delivers up to 15 A of output current at output voltages as low as 0.6 V. Operating over an input voltage range of 2.95 V to 5.5 V with ultra-high efficiency, the LM21215A suits a wide variety of low voltage systems. The voltage-mode control loop with high gain-bandwidth error amplifier provides high noise immunity, narrow duty cycle capability and is easily compensated for stable operation with any type of output capacitor, providing maximum flexibility and ease of use.

The LM21215A features internal overvoltage protection (OVP) and cycle-by-cycle overcurrent protection (OCP) for increased system reliability. A precision enable pin and integrated UVLO allow turn-on of the device to be tightly controlled and sequenced. Startup inrush currents are limited by an internally-fixed or externally-adjustable soft-start circuit. An integrated open-drain PGOOD indicator provides fault reporting and supply sequencing.

Other features include auxiliary voltage rail tracking, monotonic startup into pre-biased loads, and switching frequency synchronization to an external clock signal between 300 kHz and 1.5 MHz for beat-frequency sensitive and multi-regulator applications. The LM21215A is offered in a thermally-enhanced 20-pin HTSSOP package with an exposed pad that is soldered to the PCB to achieve a very low junction-to-board thermal impedance.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM21215A	HTSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit

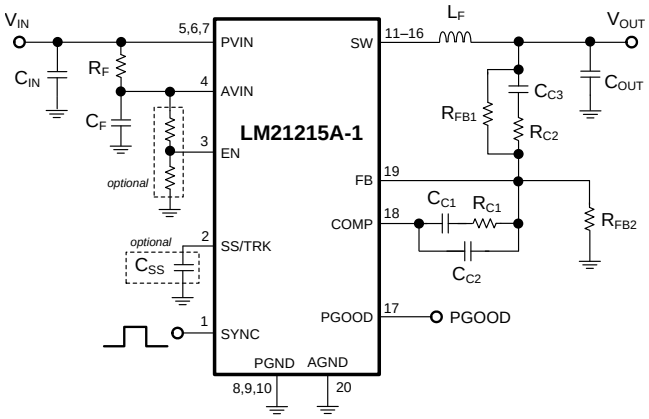


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2016) to Revision D — **Page**

- Editorial changes only, no technical revisions; add links for WEBENCH ... 1

Changes from Revision B (March 2013) to Revision C — **Page**

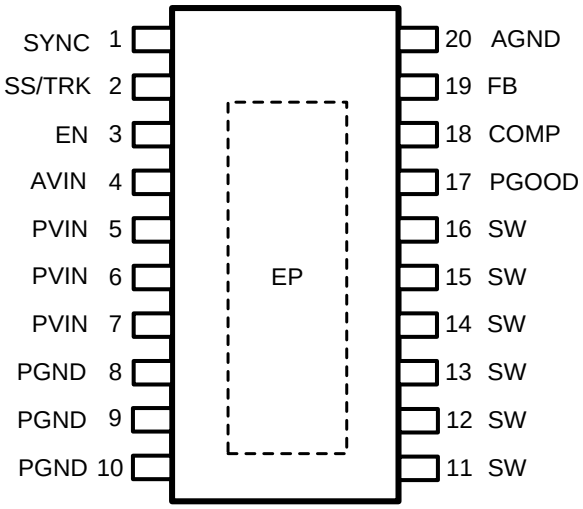
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (March 2013) to Revision B — **Page**

- Changed layout of National Data Sheet to TI format ... 27

5 Pin Configuration and Functions

PWP Package
20-Pin HTSSOP With Exposed Thermal Pad
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	SYNC	I	Frequency synchronization input pin. Applying a clock signal to this pin forces the device to switch at the clock frequency. If left unconnected, the frequency defaults to 500 kHz.
2	SS/TRK	I	Soft-start control pin. An internal 2-µA current source charges an external capacitor connected between this pin and AGND to set the output voltage ramp rate during startup. This pin can also be used to configure the tracking feature.
3	EN	I	Active high precision enable input. If not used, the EN pin can be left open, which will go high due to an internal pullup current source.
4	AVIN	P	Analog input voltage supply that generates the internal bias. Connect PVIN to AVIN through a low pass RC filter to minimize the influence of input rail ripple and noise on the analog control circuitry.
5–7	PVIN	P	Input voltage to the power switches inside the device. Connect these pins together at the device. Locate a low ESR input capacitance as close as possible to these pins.
8–10	PGND	G	Power ground pins for the internal power switches.
11–16	SW	P	Switch node pins. Tie these pins together locally and connect to the filter inductor.
17	PGOOD	O	Open-drain power good indicator.
18	COMP	O	Compensation pin is connected to the output of the voltage loop error amplifier.
19	FB	I	Feedback pin is connected to the inverting input of the voltage loop error amplifier.
20	AGND	G	Quiet analog ground for the internal reference and bias circuitry.
EP	Exposed Pad	P	Exposed metal pad on the underside of the package with an electrical and thermal connection to PGND. Connect this pad to the PC board ground plane to improve thermal dissipation.

(1) P = Power, G = Ground, I = Input, O = Output.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
PVIN(3) to GND, AVIN to GND	−0.3	6	V
SW(4) to GND	−0.3	V_{PVIN} + 0.3	V
EN, FB, COMP, PGOOD, SS/TRK to GND	−0.3	V_{PVIN} + 0.3	V
Storage temperature, T_{stg}	−65	150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The PVIN prin can tolerate transient voltages up to 6.5 V for a duration of up to 6 ns. These transients can occur during normal operation of the device.
(4) The SW pin can tolerate transient voltages up to 9 V for a duration of 6 ns and –1 V for a duration of 4 ns. These transients can occur during normal operation of the device.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input voltages	PVIN, AVIN to GND	2.95	5.5	V
Output current, I_{OUT}		−0.3	15	A
Junction temperature, T_J		−40	125	ºC

6.4 Thermal Information

THERMAL METRIC(1)		LM21215A PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	0.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	2.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise stated, the following conditions apply: V_{PVIN} = V_{AVIN}= 5 V, T_J = 25°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SYSTEM							
V_{FB}	Feedback voltage	V_{IN} = 2.95 V to 5.5 V	T_J = –40°C to 125°C	–1%		1%	V
			T_J = 25°C		0.6		
$\Delta V_{OUT}/\Delta I_{OUT}$	Load regulation				0.02%		V_{OUT}/A
$\Delta V_{OUT}/\Delta V_{IN}$	Line regulation				0.1%		V_{OUT}/V
$R_{DSON-HS}$	High-side switch on-resistance	I_{SW} = 12 A	T_J = –40°C to 125°C			9	mΩ
			T_J = 25°C		7		
$R_{DSON-LS}$	Low-side switch on-resistance	I_{SW} = 12 A	T_J = –40°C to 125°C			6	mΩ
			T_J = 25°C		4.3		
I_{CLR}	HS rising switch current limit	T_J = –40°C to 125°C		17.3		22.8	A
		T_J = 25°C			20		
I_{CLF}	LS falling switch current limit				14		A
V_{ZX}	Zero-cross voltage			–8	3	12	mV
I_Q	Operating quiescent current	T_J = –40°C to 125°C				3	mA
		T_J = 25°C			1.5		
I_{SD}	Shutdown quiescent current	V_{EN} = 0 V	T_J = –40°C to 125°C			70	µA
			T_J = 25°C		50		
V_{UVLO}	AVIN undervoltage lockout	AVIN rising	T_J = –40°C to 125°C	2.45		2.95	V
			T_J = 25°C		2.70		
$V_{UVLOHYS}$	AVIN undervoltage lockout hysteresis	T_J = –40°C to 125°C		140		280	mV
		T_J = 25°C			200		
$V_{TRACKOS}$	SS/TRACK accuracy ($V_{SS/TRK}$ – V_{FB})	0 < $V_{SS/TRK}$ < 0.55 V	T_J = –40°C to 125°C	–10		20	mV
			T_J = 25°C		6		
I_{SS}	Soft-start pin source current	T_J = –40°C to 125°C		1.3		2.5	µA
		T_J = 25°C			1.9		
t_{INTSS}	Internal soft-start ramp to Vref	SS/TRK open	T_J = –40°C to 125°C	350		675	µs
			T_J = 25°C		500		
$t_{RESETSS}$	Device reset to soft-start ramp	T_J = –40°C to 125°C		50		200	µs
		T_J = 25°C			110		
OSCILLATOR							
f_{SYNCR}	SYNC frequency range	T_J = –40°C to 125°C		300		1500	kHz
$f_{DEFAULT}$	Default (no SYNC signal) frequency	T_J = –40°C to 125°C		475		525	kHz
		T_J = 25°C			500		
t_{SY_SW}	Time from V_{SYNC} falling to V_{SW} rising				200		ns
t_{SY_MIN}	Minimum SYNC pulse width, high or low				100		ns
$t_{HSBLANK}$	HS OCP blanking time	Rising edge of SW to I_{CLR} comparison			55		ns
$t_{LSBLANK}$	LS OCP blanking time	Falling edge of SW to I_{CLF} comparison			400		ns
$t_{ZXBLANK}$	Zero cross blanking time	Falling edge of SW to V_{ZX} comparison			120		ns
t_{MINON}	Minimum HS on-time				140		ns
ΔV_{RAMP}	PWM ramp peak-peak voltage				0.8		V
ERROR AMPLIFIER							
V_{OL}	Error amplifier open-loop gain	I_{COMP} = –65 µA to 1 mA			95		dB
GBW	Error amplifier gain-bandwidth				11		MHz
I_{FB}	Feedback pin bias current	V_{FB} = 0.6 V			1		nA

Electrical Characteristics (continued)

Unless otherwise stated, the following conditions apply: V_{PVIN} = V_{AVIN}= 5 V, T_J = 25°C. Minimum and maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{COMPSRC}$	COMP output source current				1		mA
$I_{COMPSINK}$	COMP output sink current				65		µA
POWER GOOD							
V_{OVP}	Overvoltage protection rising threshold	V_{FB} rising	T_J = –40°C to 125°C	105%		120%	V_{FB}
			T_J = 25°C		112.5%		
V_{OVPHYS}	Overvoltage protection hysteresis	V_{FB} falling			2%		V_{FB}
V_{UVP}	Undervoltage protection rising threshold	V_{FB} rising	T_J = –40°C to 125°C	82%		97%	V_{FB}
			T_J = 25°C		90%		
V_{UVPHYS}	Undervoltage protection hysteresis	V_{FB} falling			2.5%		V_{FB}
t_{PGDGL}	PGOOD deglitch low	Time to PGOOD falling after OVP/UVP event			15		µs
t_{PGDGH}	PGOOD deglitch high	Minimum low pulse			12		µs
R_{PGOOD}	PGOOD pulldown resistance	T_J = –40°C to 125°C		10		40	Ω
		T_J = 25°C			20		
$I_{PGOODLEAK}$	PGOOD leakage current	V_{PGOOD} = 5 V			1		nA
LOGIC							
V_{IHSYNC}	SYNC pin logic high			2			V
V_{ILSYNC}	SYNC pin logic low					0.8	V
V_{IHENR}	EN pin rising threshold	V_{EN} Rising	T_J = –40°C to 125°C	1.2		1.45	V
			T_J = 25°C		1.35		
V_{ENHYS}	EN pin hysteresis	T_J = –40°C to 125°C		50		180	mV
		T_J = 25°C			110		
I_{EN}	EN pin pullup current	V_{EN} = 0 V			2		µA
THERMAL SHUTDOWN							
T_{TSD}	Thermal shutdown				165		°C
$T_{TSD-HYS}$	Thermal shutdown hysteresis				10		°C

6.6 Typical Characteristics

Unless otherwise specified: V_{IN} = 5 V, V_{OUT} = 1.2 V, L_F = 0.56 µH (1.8 mΩ R_{DCR}), C_{SS} = 33 nF, f_{SW} = 500 kHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

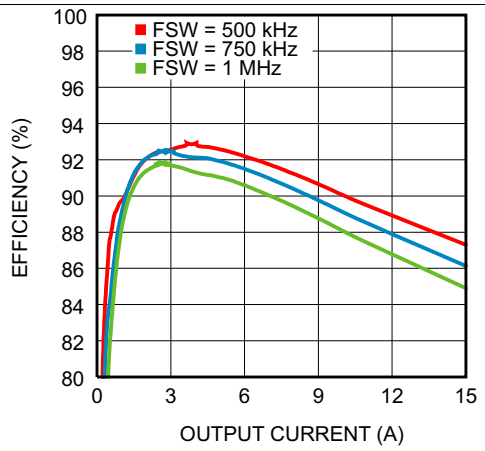


Figure 1. Efficiency

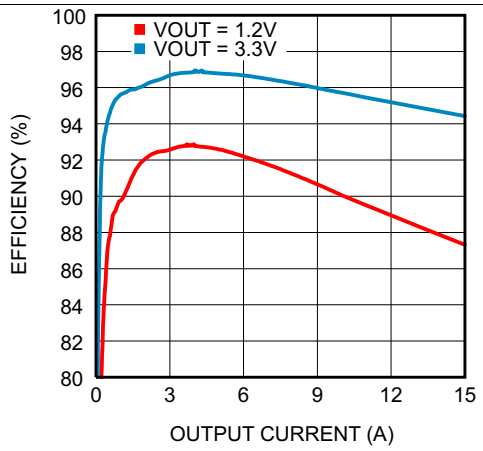


Figure 2. Efficiency

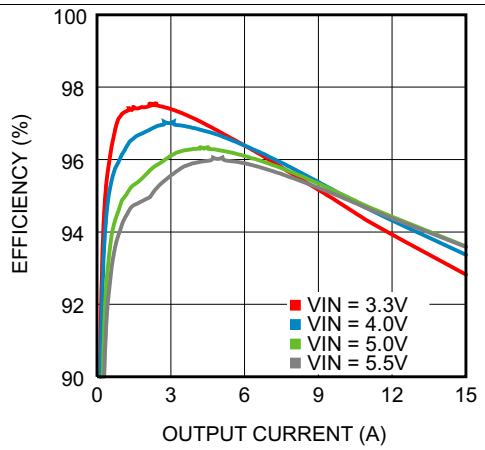


Figure 3. Efficiency (V_{OUT} = 2.5 V, F_{SW}= 500 kHz, Inductor P/N SER2010-601MLD)

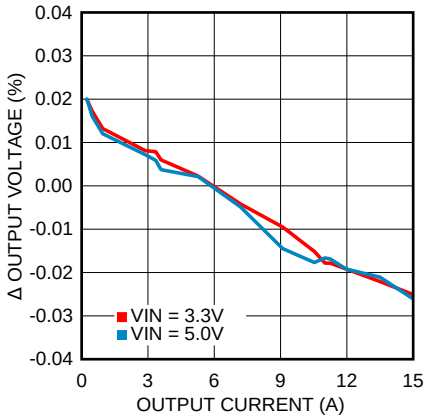


Figure 4. Load Regulation

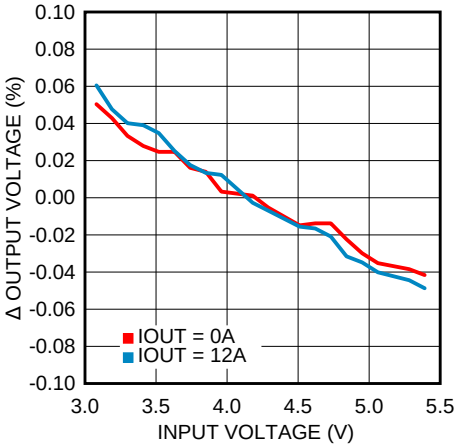


Figure 5. Line Regulation

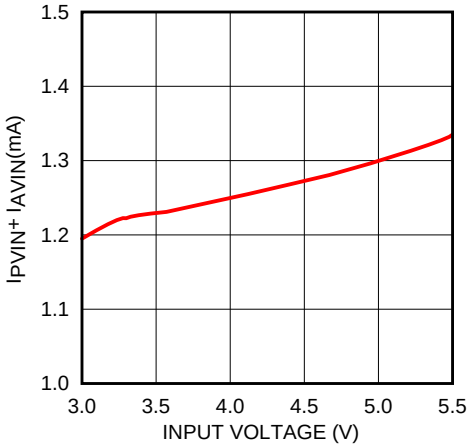


Figure 6. Non-Switching $I_{Q(TOTAL)}$ vs V_{IN}

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5 V, V_{OUT} = 1.2 V, L_F = 0.56 µH (1.8 mΩ R_{DCR}), C_{SS} = 33 nF, f_{SW} = 500 kHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

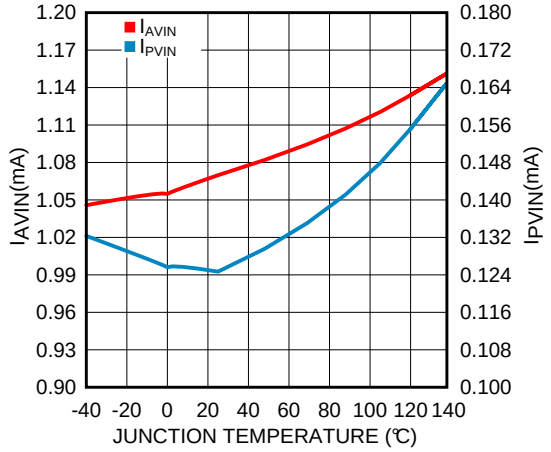


Figure 7. Non-Switching I_{AVIN} and I_{PVIN} vs Temperature

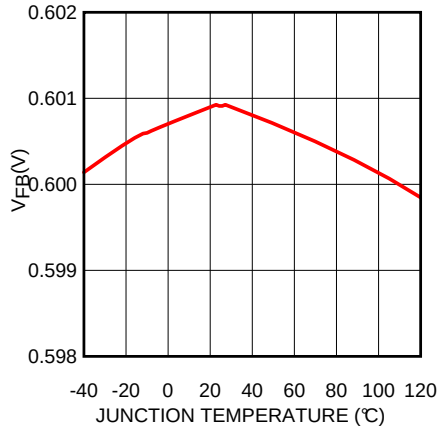


Figure 8. Feedback (FB) Voltage vs Temperature

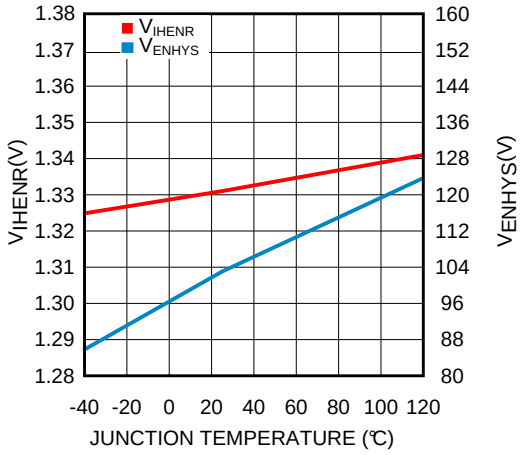


Figure 9. Enable Threshold and Hysteresis vs Temperature

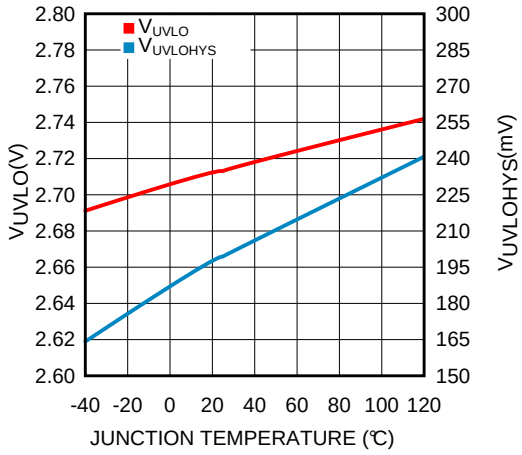


Figure 10. UVLO Threshold and Hysteresis vs Temperature

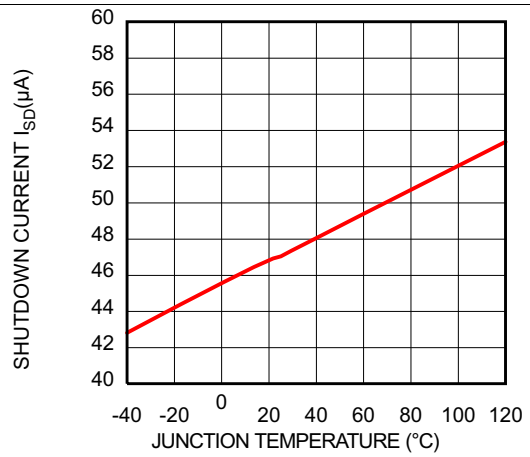


Figure 11. Enable Low Current vs Temperature

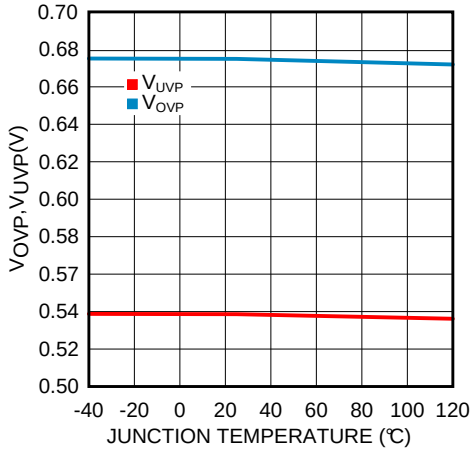


Figure 12. OVP/UVP Threshold vs Temperature

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5 V, V_{OUT} = 1.2 V, L_F = 0.56 µH (1.8 mΩ R_{DCR}), C_{SS} = 33 nF, f_{SW} = 500 kHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

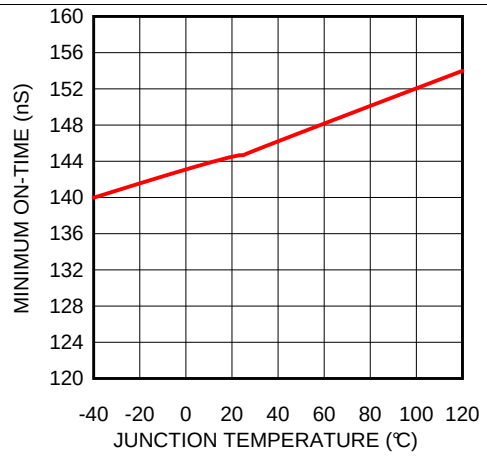


Figure 13. Minimum On-Time vs Temperature

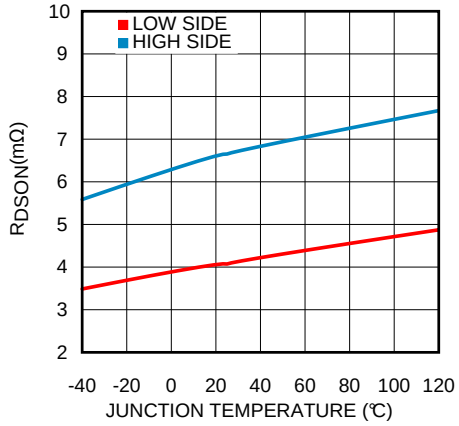


Figure 14. MOSFET On-State Resistance vs Temperature

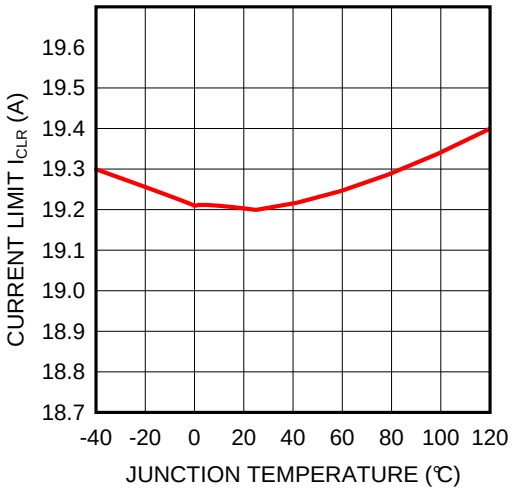


Figure 15. Peak Current Limit vs Temperature

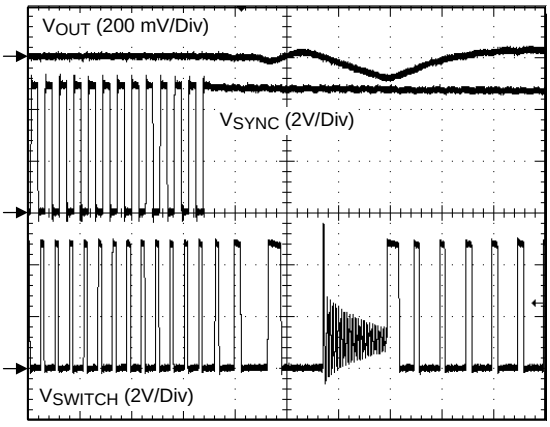


Figure 16. SYNC Signal Removed, 4 µs/Div

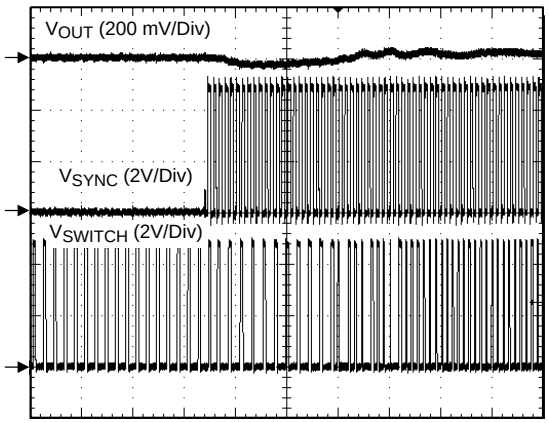


Figure 17. SYNC Signal Acquired, 10 µs/div

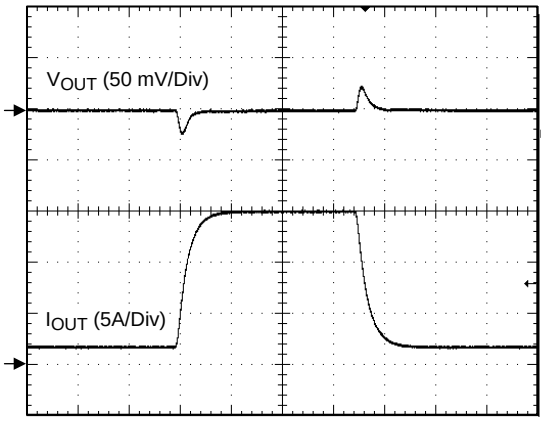


Figure 18. Load Transient Response, 100 µs/Div

Typical Characteristics (continued)

Unless otherwise specified: V_{IN} = 5 V, V_{OUT} = 1.2 V, L_F = 0.56 µH (1.8 mΩ R_{DCR}), C_{SS} = 33 nF, f_{SW} = 500 kHz, T_A = 25°C for efficiency curves, loop gain plots and waveforms, and T_J = 25°C for all others.

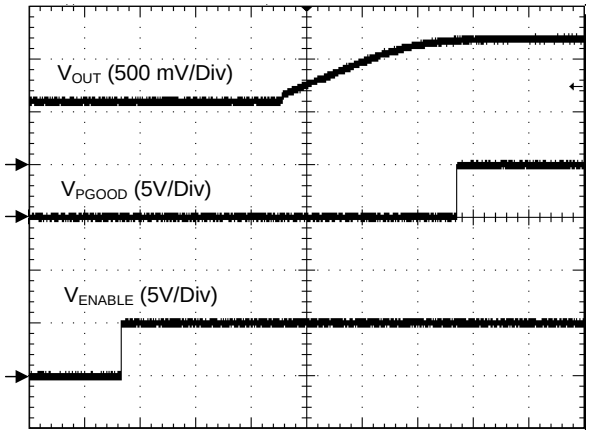


Figure 19. Startup with Prebiased Output, 2 ms/Div

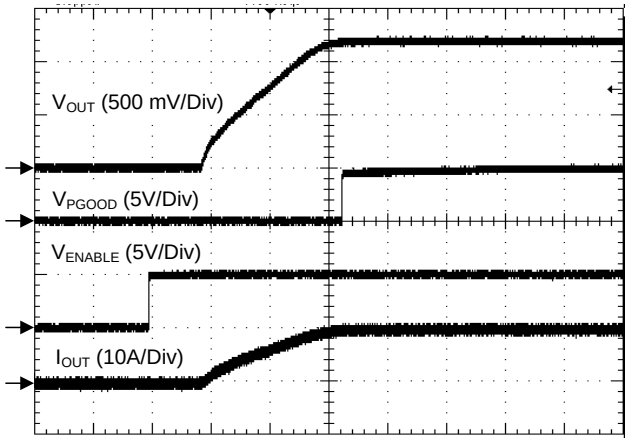


Figure 20. Startup with SS/TRK Open Circuit, 200 µs/Div

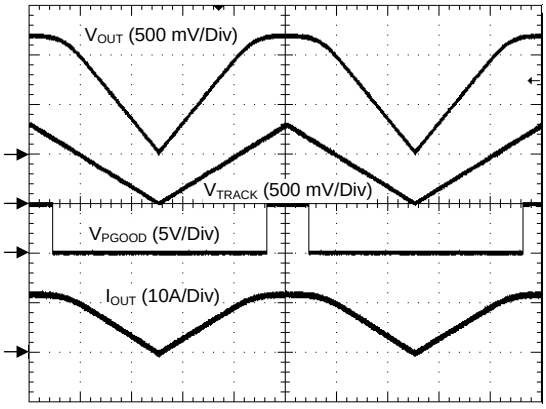


Figure 21. Startup with Tracking Signal Applied, 200 ms/Div

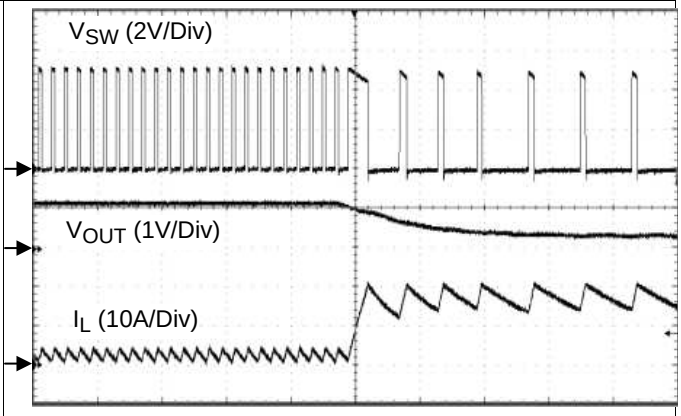


Figure 22. Output Overcurrent Condition, 10 µs/Div

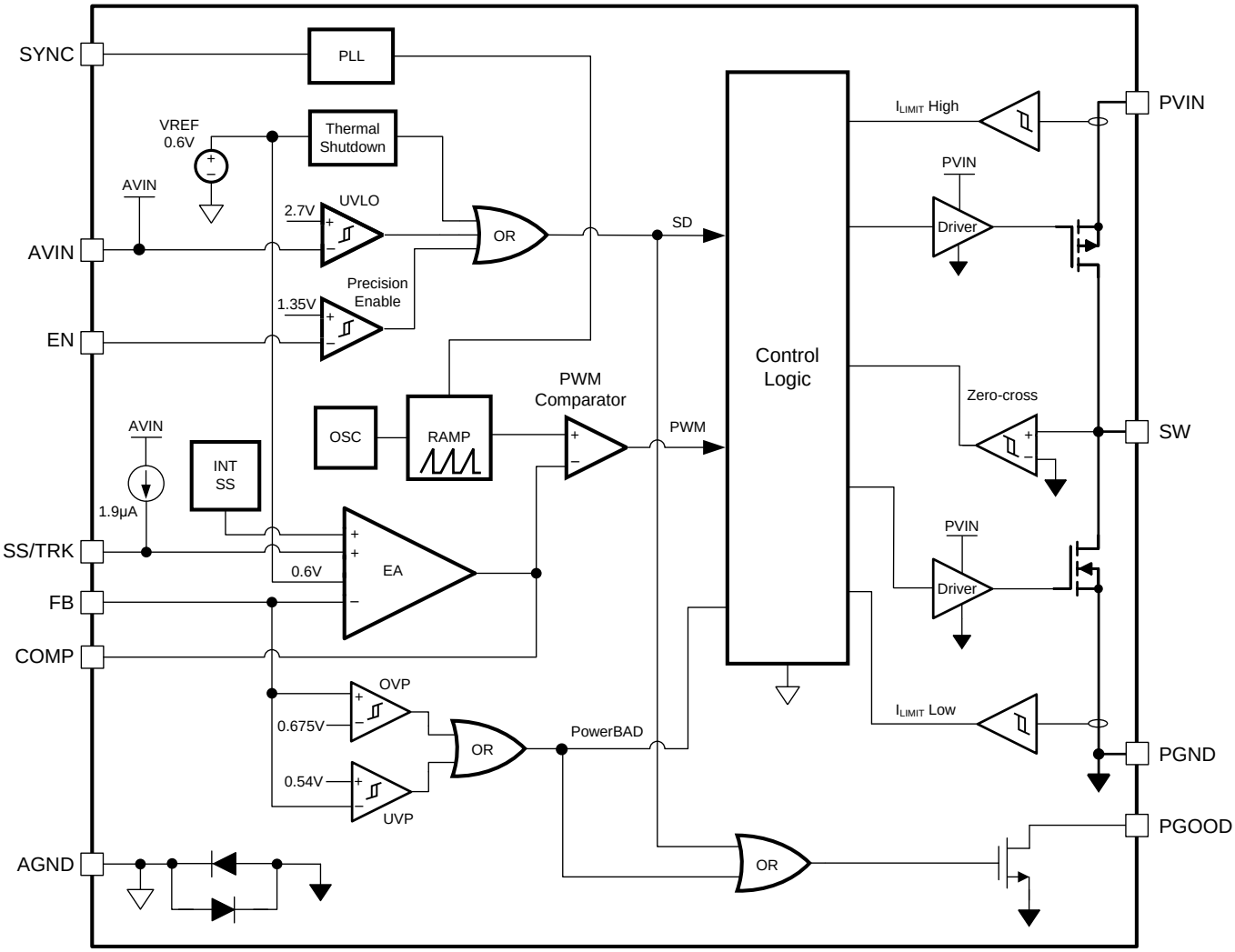
7 Detailed Description

7.1 Overview

The LM21215A synchronous buck regulator features all of the functions necessary to implement an efficient low-voltage converter using a minimum number of external components. This easy-to-use regulator features two integrated power MOSFET switches and is capable of supplying up to 15 A of continuous output current. Synchronous rectification yields high efficiency for low output voltage and high load current applications, whereas discontinuous conduction mode (DCM) with diode emulation mode (DEM) enables high-efficiency conversion with light load current conditions.

The regulator utilizes voltage-mode control with trailing-edge PWM modulation to optimize stability and transient response over the entire input voltage range. The device operates at high switching frequency, allowing the use of a small inductor yet still achieving high efficiency. The precision internal voltage reference allows output voltages as low as 0.6 V. Fault protection features include peak and valley current limiting, thermal shutdown, overvoltage protection, and undervoltage lockout. The device is available in the HTSSOP-20 package featuring an exposed pad to aid thermal dissipation. The LM21215A is ideal for numerous applications to efficiently step-down from a 5-V or 3.3-V bus.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Precision Enable

The EN pin allows the output of the device to be enabled or disabled with an external control signal. This pin is a precision analog input that enables the device when the voltage exceeds 1.35 V (typical). The EN pin has 110 mV of hysteresis and disables the output when the Enable voltage falls below 1.24 V (typical). If the EN pin is not used, it can be left open as it is pulled high by an internal 2-µA current source. Since the EN pin has a precise turn-on threshold, it can be used along with an external resistor divider network from VIN to configure the device to turn on at a precise input voltage.

7.3.2 Input Voltage UVLO

The LM21215A has a built-in undervoltage lockout protection circuit that prevents the device from switching until the input voltage reaches 2.7 V (typical). The UVLO threshold has 200 mV of hysteresis that prevents the device from responding to power-on glitches during startup. As mentioned above, adjust the turn-on threshold of the supply by using the precision enable pin and a resistor divider network connected to VIN. Please refer to Figure 30 of the *Detailed Design Procedure* section for more detail.

7.3.3 Soft-Start Capability

When EN exceeds 1.35 V and AVIN is above its UVLO threshold of 2.7 V, the LM21215A begins charging the output linearly to the voltage setpoint dictated by the feedback resistor network. The LM21215A employs a user-adjustable soft-start circuit to set the output voltage ramp time during startup. A capacitor from SS/TRK to GND sets the required soft-start time. Once the enable voltage exceeds 1.35 V, an internal 1.9-µA current source begins to charge the soft-start capacitor. This allows the user to limit inrush currents due to a high output capacitance and avoid an overcurrent condition. Adding a soft-start capacitor also reduces the stress on the input rail. Use Equation 1 to calculate the soft-start capacitance.

$$C_{SS} = \frac{t_{SS} \cdot I_{SS}}{0.6V} \quad (1)$$

where

- I_{SS} is nominally 1.9 µA
- t_{SS} is the desired startup time

If V_{IN} is higher than the UVLO level and Enable is toggled high, the soft-start sequence begins. There is a small delay between enable transitioning high and the beginning of the soft-start sequence. This delay allows the LM21215A to initialize its internal circuitry. Once the output has charged to 90% of the nominal output voltage, the PGOOD flag transitions high. This behavior is illustrated in Figure 23.

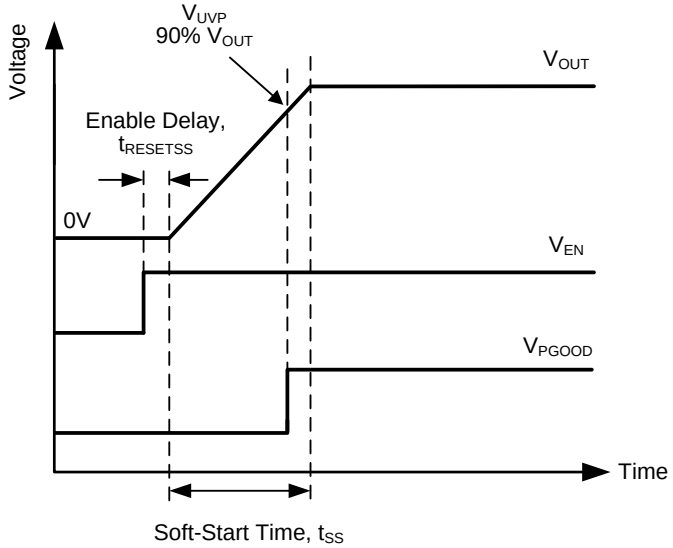


Figure 23. Soft-Start Timing

Feature Description (continued)

As shown above, the soft-start capacitance is set by the nominal feedback voltage level 0.6 V, the soft-start charging current I_{SS}, and the desired soft-start time. If a soft-start capacitor is not installed, the LM21215A defaults to a soft-start time of 500 µs. The LM21215A cannot startup faster than 500 µs. When Enable is cycled or the device enters UVLO, the soft-start capacitor is discharged to reset the startup process. This also occurs when the device enters short circuit mode following an overcurrent event.

7.3.4 PGOOD Indicator

The PGOOD flag provides the user with a way to monitor the status of the LM21215A. In order to use the PGOOD function, the application must provide a pullup resistor to a desired DC voltage, for example VIN. PGOOD responds to a fault condition by pulling PGOOD low with the open-drain output. PGOOD pulls low on the following conditions: 1) V_{FB} moves above or below the V_{OVP} or V_{UVP}, respectively; 2) The EN voltage is brought below the Enable turn-off threshold; 3) A pre-biased output condition exists ($V_{FB} > V_{SS/TRK}$). PGOOD has 12 µs and 15 µs of built-in deglitch time for rising and falling edges, respectively.

Figure 24 shows the conditions that cause PGOOD to respond.

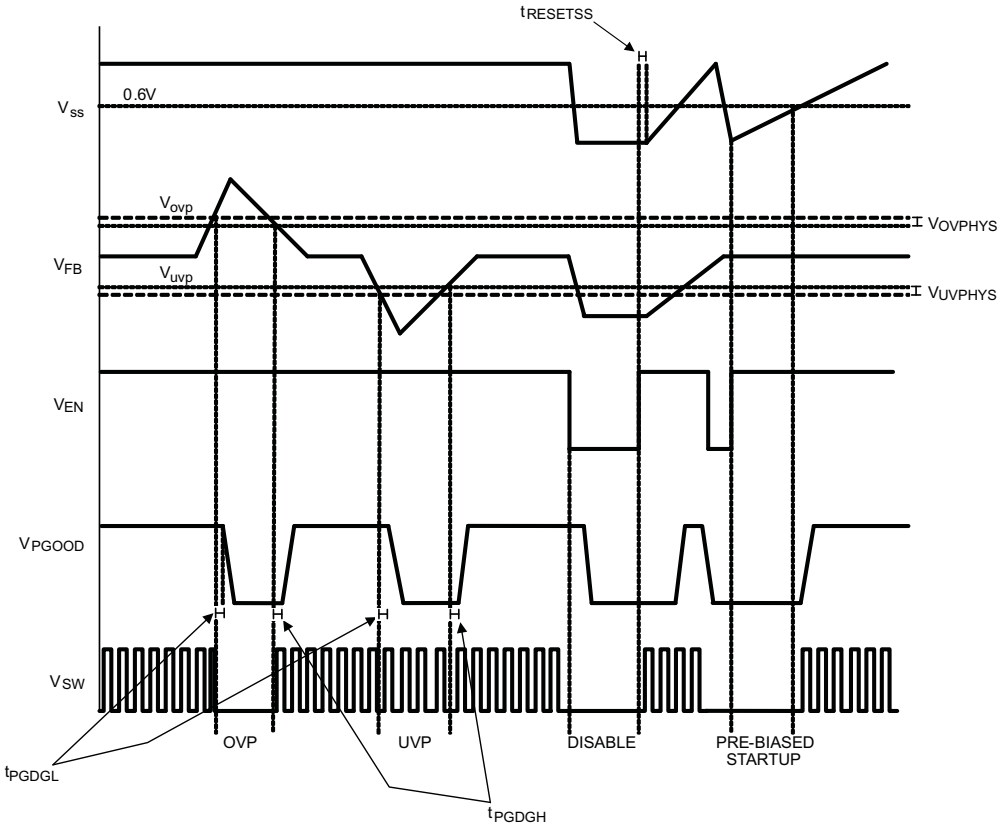


Figure 24. PGOOD Indicator Operation

7.3.5 Frequency Synchronization

The SYNC pin allows the LM21215A to be synchronized to an external clock frequency. When a clock signal within the allowable frequency range of 300 kHz to 1.5 MHz is present on SYNC, an internal PLL synchronizes the turn-on of the high-side MOSFET (SW voltage rising) to the negative edge of the clock signal, as seen in Figure 25.

The clock signal can be present on the SYNC pin before the device is powered on without loading of the clock signal. Alternatively, if a clock signal is not present while the device is powered up, the default switching frequency is 500 kHz. Once the clock signal is available, the device synchronizes to the clock frequency. The time required to achieve synchronization depends on the clock frequency.

Feature Description (continued)

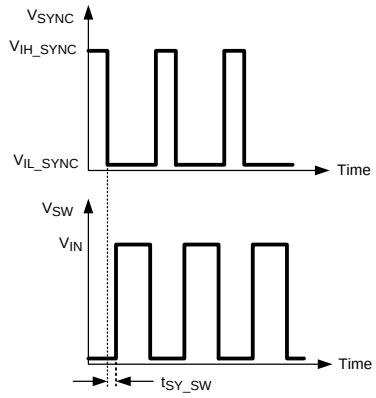


Figure 25. Frequency Synchronization

7.3.6 Current Limit

The LM21215A has overcurrent protection to avoid excessive current levels through the power MOSFETs and inductor. A current limit condition exists when the high-side MOSFET's current exceeds the rising current limit level, I_{CLR}. The control circuitry responds to this event by turning off the high-side MOSFET and turning on the low-side MOSFET. This forces a negative voltage on the inductor, thereby causing the inductor current to decrease. The high-side MOSFET does not conduct again until the lower current limit level, I_{CLF}, is sensed on the low-side MOSFET. At this point, the LM21215A resumes normal switching.

A current limit condition causes the internal soft-start voltage to ramp downward. After the internal soft-start ramps below the feedback (FB) voltage, nominally 0.6 V, FB begins to ramp downward, as well. This voltage foldback limits the power consumption in the device during a sustained overload. After the current limit condition is cleared, the internal soft-start voltage ramps up again. Figure 26 describes current limit behavior including V_{SS}, V_{FB}, V_{OUT} and V_{SW} waveforms.

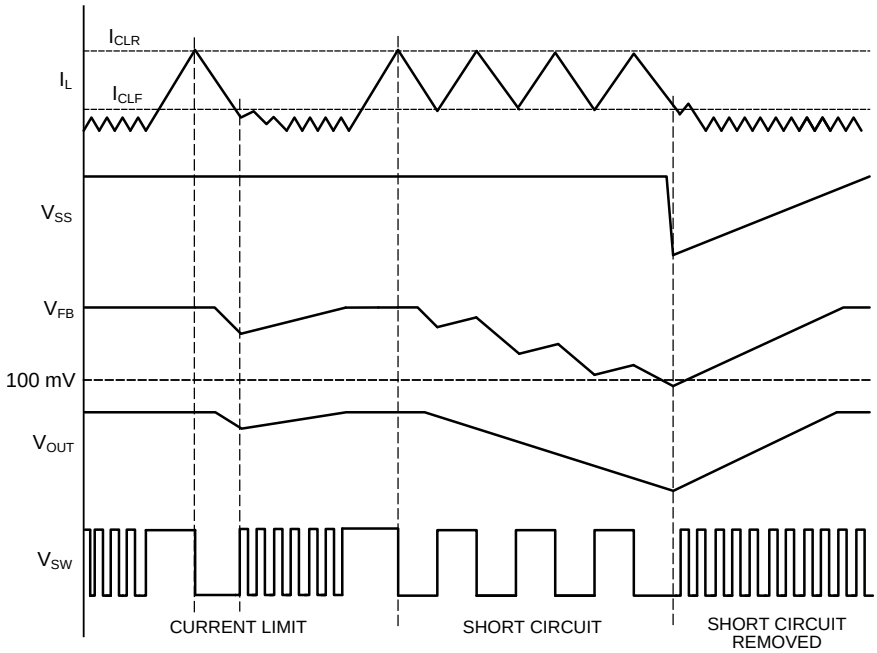


Figure 26. Current Limit Conditions

Feature Description (continued)

7.3.7 Short Circuit Protection

In an event that the output is shorted with a low impedance to ground, the LM21215A limits the current into the short by resetting the device. A short circuit condition is sensed as a current limit condition coinciding with a voltage on the FB pin that is lower than 100 mV. When this condition occurs, the device begins its reset sequence, turning off both power MOSFETs and discharging the soft-start capacitor after $t_{RESETSS}$ (nominally 110 µs). The device then attempts to restart. If the short circuit condition still exists, it resets again, repeating until the short circuit condition is cleared. The reset prevents excessive power MOSFET dissipation and limits thermal stress during a short circuit fault condition.

7.4 Device Functional Modes

7.4.1 Light-Load Operation

The LM21215A maintains high efficiency when operating at light loads. Whenever the load current is reduced to a level less than half the peak-to-peak inductor ripple current, the device enters discontinuous conduction mode (DCM) and prevents negative inductor current. The low-side MOSFET then operates in diode emulation mode (DEM), conducting only positive inductor current. Calculate the critical conduction boundary using Equation 2.

$$I_{BOUNDARY} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \cdot (1 - D)}{2 \cdot L_F \cdot F_{SW}} \quad (2)$$

Several diagrams are shown in Figure 27 illustrating continuous conduction mode (CCM), discontinuous conduction mode (DCM), and the boundary condition.

When the inductor current reaches zero, the SW node becomes high impedance. Resonant ringing occurs at SW as a result of the LC tank circuit formed by the filter inductor and the parasitic capacitance at the SW node. At very light loads, usually below 500 mA, several pulses may be skipped in between switching cycles, effectively reducing the switching frequency and further improving light-load efficiency.

7.4.2 Overvoltage and Undervoltage Handling

The LM21215A has built-in undervoltage protection (UVP) and overvoltage protection (OVP) using FB voltage comparators to control the power MOSFETs. The rising OVP threshold is typically set at 112.5% of the nominal voltage setpoint. Whenever excursions occur in the output voltage above the OVP threshold, the device terminates the present on-pulse, turns on the low-side MOSFET, and pulls PGOOD low. The low-side MOSFET remains on until either the FB voltage falls back into regulation or the inductor current zero-cross is detected. If the output reaches the falling UVP threshold, typically 90% of the nominal setpoint, the device continues switching and PGOOD is asserted and pulls low. As detailed in the *PGOOD Indicator* section, PGOOD has 15 µs of built-in deglitch time in response to a UVP or OVP condition to avoid false tripping during transient glitches.

7.4.3 Thermal Shutdown

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated, typically at 165°C, the LM21215A tri-states the power MOSFETs and resets soft start. After the junction temperature cools to approximately 155°C, the device starts up using the normal startup routine.

Device Functional Modes (continued)

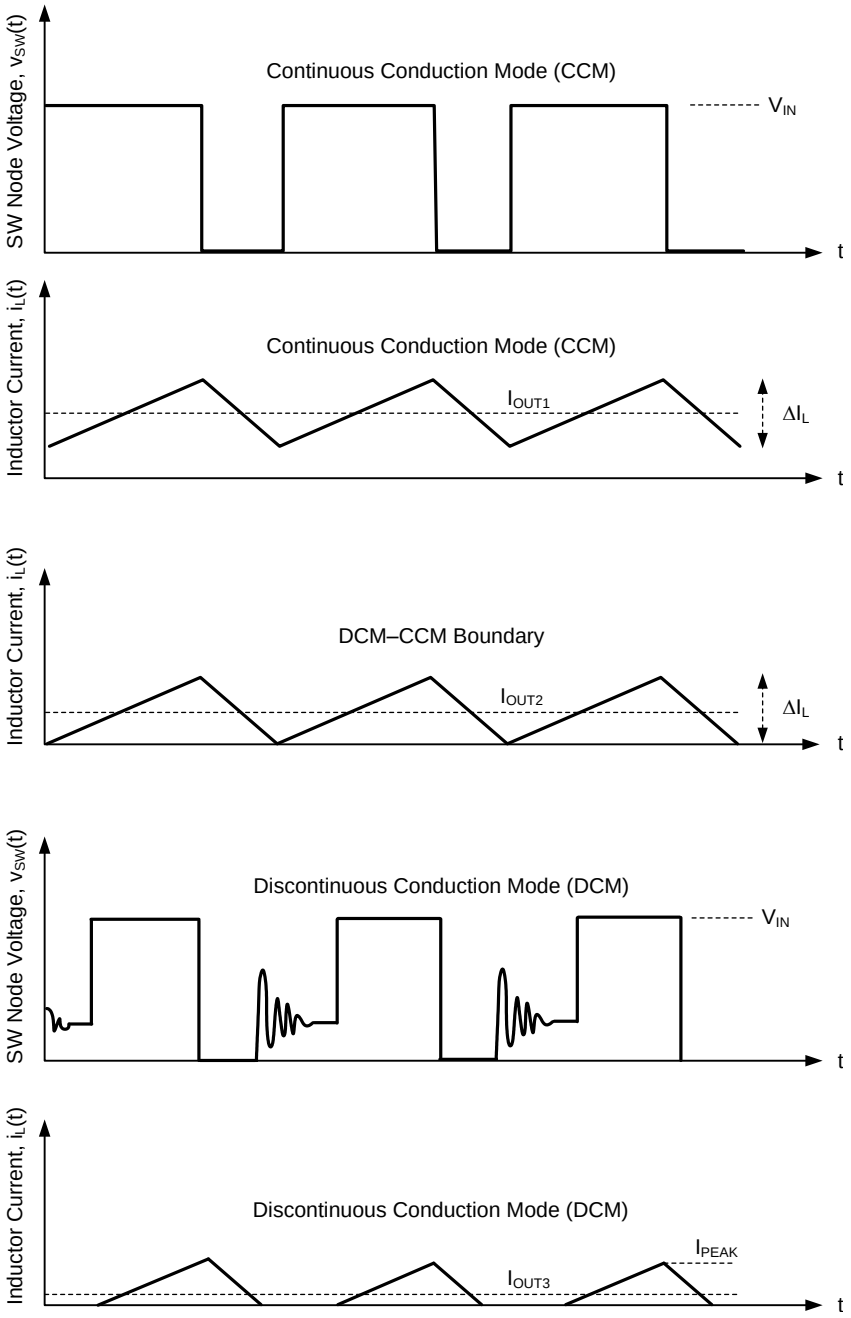


Figure 27. LM21215A Modes of Operation

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM21215A is a synchronous buck DC/DC converter with a maximum output current of 15 A. The following design procedure assists with component selection for the LM21215A. Alternately, the WEBENCH® Design Tool is available to generate a complete design. With access to a comprehensive component database, this tool uses an iterative design procedure to create an optimized design, allowing the user to experiment with various design options. As well as numerous LM21215 reference designs populated in the TI Designs reference design library, the *LM21215A Quickstart Design Calculator* is also available as a free download.

8.2 Typical Applications

8.2.1 Typical Application 1

The schematic diagram of a 15-A regulator is given in Figure 28. The target full-load efficiency in this example is 89% at an output voltage of 1.2 V and nominal input voltage of 5 V. The free-running switching frequency (with the SYNC pin open circuit) is 500 kHz. In terms of control loop performance, the target loop crossover frequency is 100 kHz with a phase margin in excess of 50°.

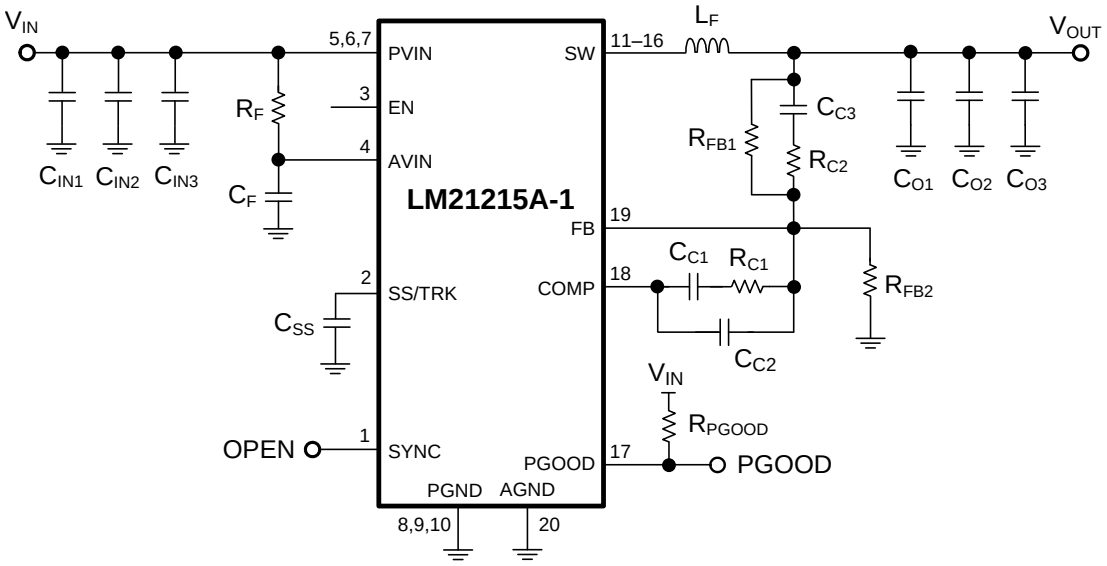


Figure 28. Typical Application Schematic 1

8.2.1.1 Design Requirements

An example of the step-by-step procedure to generate power stage and compensation component values using the typical application setup of Figure 28) is given in Table 1. The relevant design specifications are given in Table 1. Here, $f_{crossover}$ is the desired loop crossover frequency, which generally is less than one-fifth of the switching frequency, and $\Delta V_{OUT(pk-pk)}$ is the peak-to-peak output voltage ripple.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	5 V
V_{OUT}	1.2 V
I_{OUT}	15 A
F_{SW}	500 kHz
$f_{crossover}$	100 kHz
$\Delta V_{OUT(pk-pk)}$	10 mV

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM21215A device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Output Voltage Setpoint

The first step in designing an LM21215A application is to configure the output voltage setpoint by using a voltage divider between V_{OUT} and AGND, with the middle node connected to FB. When operating under steady state conditions, the LM21215A regulates V_{OUT} such that the FB voltage is driven to 0.6 V.

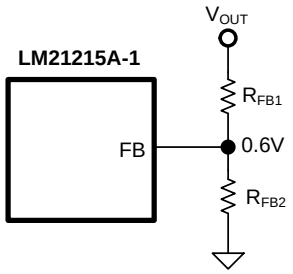


Figure 29. Setting the Output Voltage by Feedback Resistor Divider

A good starting point for the lower feedback resistor, R_{FB2}, is 10 kΩ. Calculate R_{FB1} using Equation 3.

$$V_{OUT} = 0.6V \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right) \quad (3)$$

8.2.1.2.3 Precision Enable

The Enable (EN) pin of the LM21215A allows the output to be toggled on and off. This pin is a precision analog input. When the voltage exceeds 1.35 V, the converter begins to regulate the output voltage as long as AVIN has exceeded the UVLO threshold voltage of 2.7 V. There is an internal pullup current source of 2 µA connected to EN. If enable is not used, the device turns on automatically. Also, if EN is not toggled directly, the device can be set to turn on at a certain input voltage higher than the internal UVLO rising threshold. This is achieved with an external resistor divider from AVIN to EN and EN to AGND as shown in Figure 30.

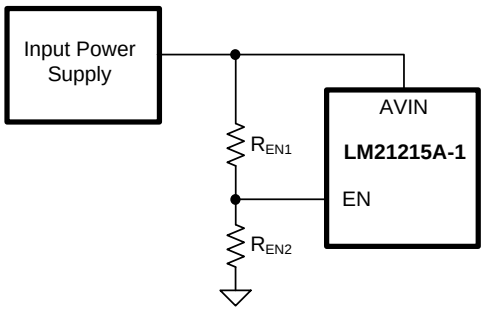


Figure 30. Input Voltage Turn-on Setpoint Configured by Enable Resistor Divider

The resistances of R_{EN1} and R_{EN2} are chosen to allow EN to reach its rising threshold voltage at the desired the input supply voltage. With the enable current source included, use Equation 4 to solve for R_{EN1}.

$$R_{EN1} = R_{EN2} \cdot \frac{V_{IN} - 1.35V}{1.35V - I_{EN} \cdot R_{EN2}} \quad (4)$$

where

- R_{EN1} is the resistor from V_{IN} to EN
- R_{EN2} is the resistor from EN to AGND
- I_{EN} is the internal enable pullup current (2 µA)
- 1.35 V is the precision enable rising threshold voltage

Typical values for R_{EN2} range from 10 kΩ to 100 kΩ.

8.2.1.2.4 Filter Inductor Selection

The filter inductor, designated L_F, chosen for the application influences the ripple current and the efficiency of the converter. The first selection criteria is to define the buck converter inductor ripple current ΔI_L, typically selected between 20% to 40% of the maximum output current. Figure 31 shows the ripple current in a conventional buck converter operating in continuous conduction mode. Larger ripple current results in a lower inductance, which leads to lower inductor DC resistance (DCR) and improved efficiency. However, larger ripple current causes the LM21215A to operate in DCM at a higher average output current.

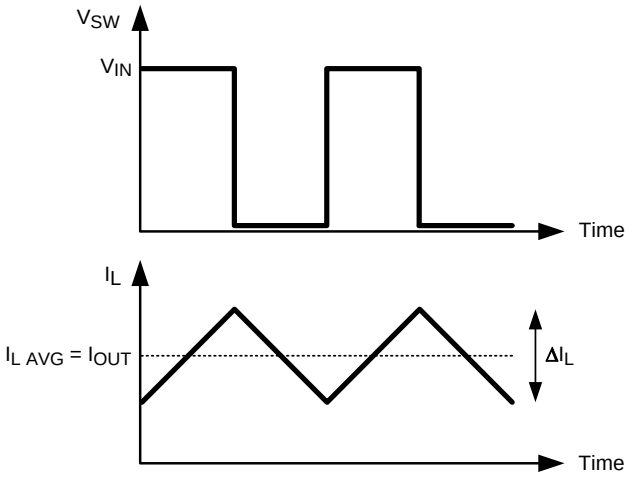


Figure 31. Switch (SW) Voltage and Inductor Current Waveforms

Once the ripple current has been determined, calculate the appropriate inductance using Equation 5.

$$L_F = \frac{V_{OUT} \cdot (1 - D)}{\Delta I_L \cdot F_{SW}} \tag{5}$$

A 0.56-µH inductor with 1.8-mΩ DCR meets the application requirements here. The peak inductor current at full load corresponds to the maximum output current plus the ripple current, as shown by Equation 6.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \tag{6}$$

Choose an inductor with a saturation current rating at maximum operating temperature that is higher than the overcurrent protection limit. In general, lower inductance is desirable in switching converters because it equates to faster transient response, lower inductor DCR, and reduced size for more compact designs. However, too low of an inductance implies large inductor ripple current such that the overcurrent protection circuit is falsely triggered at the full load. Larger inductor ripple current also implies higher output voltage ripple.

8.2.1.2.5 Output Capacitor Selection

The output capacitor, designated C_{OUT}, filters the inductor ripple current and provides a source of charge for transient load conditions. A wide range of output capacitors may be used with the LM21215A that provide various advantages. The best performance is typically obtained using ceramic, SP or OSCON type chemistries. Typical trade-offs are that the ceramic capacitor provides extremely low ESR to reduce the output ripple voltage and noise spikes, while the SP and OSCON capacitors provide a large bulk capacitance in a small volume for transient loading conditions.

When selecting an output capacitor, the two performance characteristics to consider are the output voltage ripple and load transient response. Approximate the output voltage ripple by using Equation 7.

$$\Delta V_{OUT} = \Delta I_L \sqrt{R_{ESR}^{\ 2} + \left(\frac{1}{8 \cdot F_{SW} \cdot C_{OUT}} \right)^2} \tag{7}$$

where

- ΔV_{OUT} is the peak-to-peak output voltage ripple
- R_{ESR} is the effective series resistance (ESR) of the output capacitor
- F_{SW} is the switching frequency
- C_{OUT} is the *effective* output capacitance

The amount of output voltage ripple is application specific. A general recommendation is to keep the output ripple less than 1% of the rated output voltage. Keep in mind that ceramic capacitors are sometimes preferred because they have very low ESR. However, depending on package and voltage rating of the capacitor, the effective in-circuit capacitance can drop significantly with applied voltage. The output capacitor selection also affects the output voltage droop during a load transient. The peak deviation of the output voltage during a load transient is dependent on many factors. An approximation of the transient dip ignoring loop bandwidth is obtained using Equation 8:

$$V_{DROOP} = \Delta I_{OUT-STEP} \cdot R_{ESR} + \frac{L_F \cdot \Delta I_{OUT-STEP}^{2}}{C_{OUT} \cdot \left(V_{IN} - V_{OUT}\right)}$$

where

- C_{OUT} is the minimum required output capacitance
- L_F is the filter inductance
- V_{DROOP} is the output voltage deviation ignoring loop bandwidth considerations
- $\Delta I_{OUT-STEP}$ is the load step change
- R_{ESR} is the output capacitor ESR
- V_{IN} is the input voltage
- V_{OUT} is the output voltage setpoint

(8)

Three 100-µF, 6.3-V ceramic capacitors with X5R dielectric and 1210 footprint are selected here based on a review of the capacitor's tolerance and voltage coefficient to meet output ripple specification.

8.2.1.2.6 Input Capacitor Selection

High quality input capacitors are necessary to limit the input voltage ripple while supplying switching-frequency AC current to the buck power stage. It is generally recommended to use X5R or X7R dielectric ceramic capacitors, thus providing low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the PVIN and PGND pins. A good approximation for the required ripple current rating is given by Equation 9.

$$I_{RMS-CIN} = I_{OUT} \cdot \frac{\sqrt{V_{OUT} \cdot \left(V_{IN} - V_{OUT}\right)}}{V_{IN}} \tag{9}$$

The highest input capacitor RMS current occurs at 50% duty cycle, at which point the RMS ripple current rating should be greater than half the output current. Place low ESR ceramic capacitors in parallel with higher value bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. One bulk capacitor of sufficiently high current rating and one or two 22-µF 10-V X7R ceramic decoupling capacitors are usually sufficient. Select the input bulk capacitor based on its ripple current rating and operating temperature.

When operating at low input voltages (3.3 V or lower), additional capacitance may be necessary to avoid triggering an undervoltage condition during an output current transient. This depends on the impedance between the input voltage supply and the LM21215A, as well as the magnitude and slew rate of the load transient.

The AVIN pin requires a 1-µF ceramic capacitor to AGND and a 1-Ω resistor to PVIN. This RC network filters inherent noise on PVIN from the sensitive analog circuitry connected to AVIN.

8.2.1.2.7 Control Loop Compensation

This section walks through the various steps in obtaining the open-loop transfer function. There are three main blocks of a voltage-mode buck converter that the power supply designer must consider when designing the control system: the power stage, the PWM modulator, and the compensated error amplifier. The control loop architecture of a voltage-mode buck converter is provided in Figure 32.

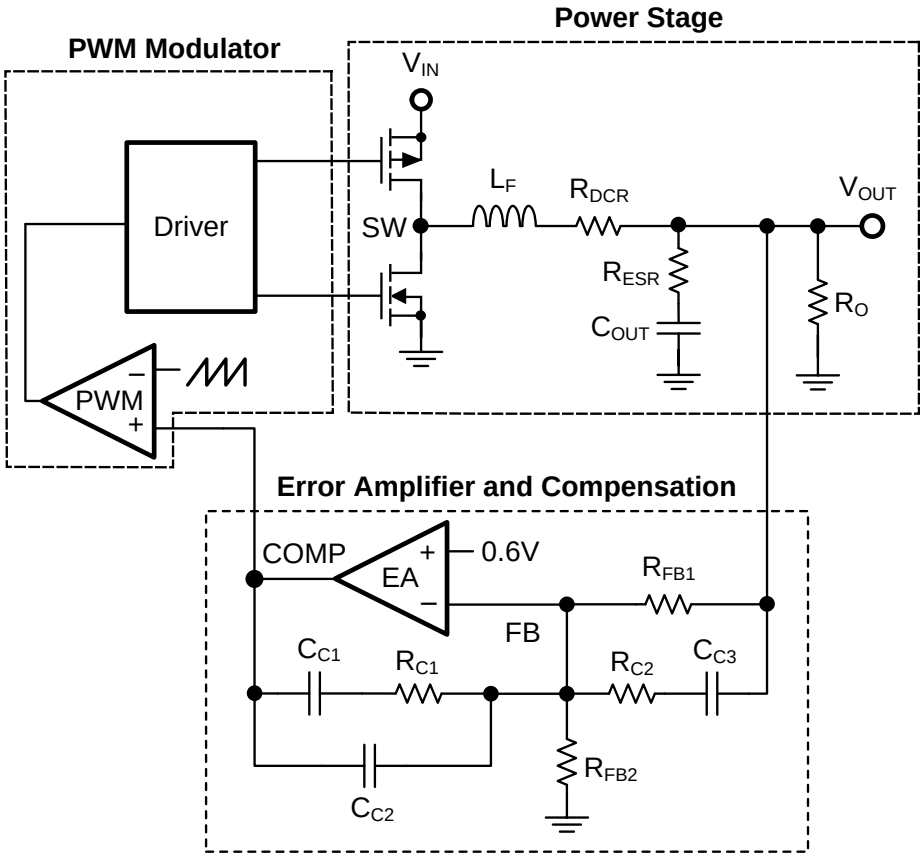


Figure 32. Voltage-mode Buck Converter Architecture

The power stage consists of the filter inductor (L_F) with DCR (DC resistance R_{DCR}), output capacitor (C_{OUT}) with ESR (effective series resistance R_{ESR}), and load resistance (R_O). The LM21215A incorporates a high-bandwidth error amplifier between the FB and COMP pins to achieve high loop bandwidth. The error amplifier (EA) constantly regulates FB to 0.6 V. The compensation component network around the error amplifier establish system stability. The modulator creates the duty cycle command by comparing the error amplifier output with an internally-generated PWM ramp set at the switching frequency.

There are three transfer functions that are taken into consideration when obtaining the total open-loop transfer function; COMP-to-duty cycle (modulator), duty cycle-to-V_{OUT} (power stage), and V_{OUT}-to-COMP (compensator). If ΔV_{RAMP} is the peak-to-peak ramp voltage (nominally 0.8 V), the COMP-to-duty cycle transfer function is simply the PWM modulator gain given by Equation 10.

$$G_{PWM} = \frac{1}{\Delta V_{RAMP}} \tag{10}$$

The duty cycle-to-output transfer function includes the filter inductor, output capacitor, and output load resistance. The inductor and capacitor create a pair of complex poles at the LC tank frequency expressed by Equation 11.

$$f_{LC} = \frac{1}{2 \cdot \pi} \cdot \sqrt{\frac{1}{L_F \cdot C_{OUT} \cdot \left(\frac{R_O + R_{ESR}}{R_O + R_{DCR}} \right)}} \tag{11}$$

In addition to two complex poles, a left half plane zero is created by the output capacitor ESR located at a frequency described by Equation 12.

$$f_{ESR} = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot R_{ESR}} \tag{12}$$

A Bode plot showing the –40dB/decade power stage response is shown in Figure 33

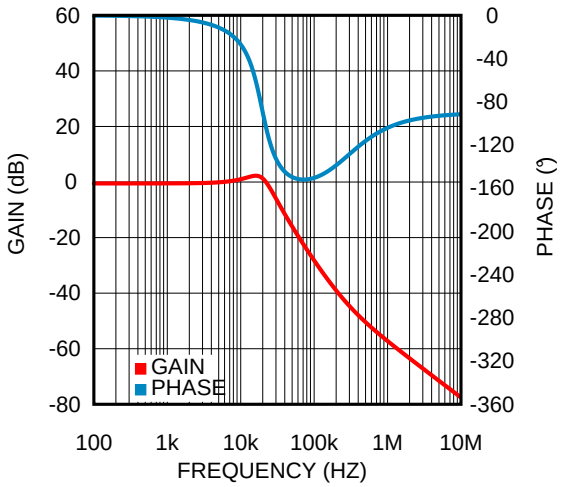


Figure 33. Power Stage Bode Plot

The complex poles created by the filter inductor and output capacitor cause a 180° phase lag. The phase is boosted back up to –90° by the output capacitor ESR zero. The compensator must provide sufficient phase boost to stabilize the loop response. The type-III compensation network shown around the error amplifier in Figure 32 creates two poles, two zeros and a pole at the origin. Placing these poles and zeros at the correct frequencies stabilizes the closed loop response. The compensator transfer function is given by Equation 13.

$$G_C(s) = K_{mid} \frac{\left(1 + \frac{2 \cdot \pi \cdot f_{Z1}}{s}\right) \cdot \left(1 + \frac{s}{2 \cdot \pi \cdot f_{Z2}}\right)}{\left(1 + \frac{s}{2 \cdot \pi \cdot f_{P1}}\right) \cdot \left(1 + \frac{s}{2 \cdot \pi \cdot f_{P2}}\right)} \quad (13)$$

where

- K_{mid} is the mid-band gain, R_{C1}/R_{FB1}

The pole located at the origin gives high open-loop gain at DC, translating into improved load regulation accuracy. This pole occurs at a very low frequency due to the finite gain of the error amplifier; however, its location is approximated at DC for the purposes of compensation. The other two poles and two zeros are located accordingly to stabilize the voltage-mode loop depending on the power stage complex poles and their quality factor, Q. Figure 34 illustrates a typical type-III compensator transfer function.

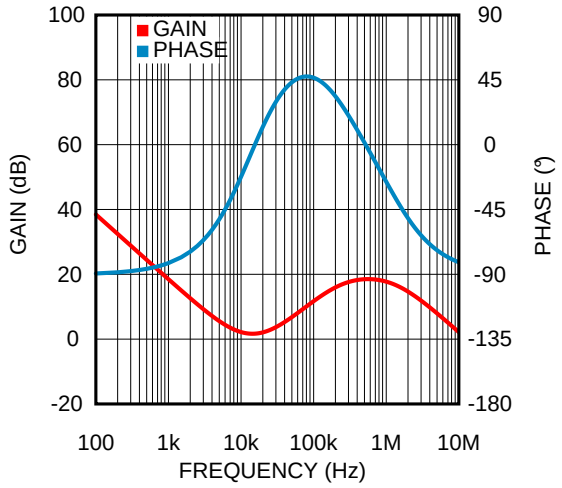


Figure 34. Type-III Compensation Network Bode Plot

As seen in Figure 34, the two compensator zeros located at (f_{LC}/2, f_{LC}) provide a phase boost. This mitigates the effect of the phase loss from the output filter. The compensation network also adds two poles to the system. One pole is located at the output capacitor ESR zero (f_{ESR}) and the other pole is at half the switching frequency (F_{SW}/2) to roll off the high frequency response.

The dependency of the pole and zero locations on the compensation components is described as follows:

$$f_{Z1} = \frac{f_{LC}}{2} = \frac{1}{2 \cdot \pi \cdot R_{C1} \cdot C_{C1}}$$

$$f_{Z2} = f_{LC} = \frac{1}{2 \cdot \pi \cdot \left(R_{C1} + R_{FB1}\right) \cdot C_{C3}}$$

$$f_{P1} = f_{ESR} = \frac{1}{2 \cdot \pi \cdot R_{C2} \cdot C_{C3}}$$

$$f_{P2} = \frac{F_{SW}}{2} = \frac{C_{C1} + C_{C2}}{2 \cdot \pi \cdot R_{C1} \cdot C_{C1} \cdot C_{C2}}$$

The output capacitance, C_{OUT}, depends on capacitor chemistry and bias voltage. For multi-layer ceramic capacitors (MLCC), the total capacitance degrades as the DC bias voltage is increased. To accurately calculate and optimize the compensation network, it is advisable to determine the effective capacitance of the output capacitors when biased at the output voltage.

The example given here is the total output capacitance using three MLCC output capacitors biased at 1.2 V, as seen in the typical application schematic of Figure 28. 50% capacitance derating is assumed.

NOTE

It is more conservative, from a stability standpoint, to err on the side of a lower output capacitance in the compensation calculations rather than a higher, as this will result in a lower bandwidth but increased phase margin.

First, choose a resistance for R_{FB1}, a typical value being 10 kΩ. From this, calculate the resistance of R_{C1} using Equation 14 to set the mid-band gain such that the desired crossover frequency is achieved.

$$R_{C1} = \frac{f_{crossover}}{f_{LC}} \cdot \frac{\Delta V_{RAMP}}{\Delta V_{IN}} \cdot R_{FB1} = \frac{100\,kHz}{17.4\,kHz} \cdot \frac{0.8\,V}{5\,V} \cdot 10\,k\Omega = 9.2\,k\Omega \quad (14)$$

Next, calculate the capacitance of C_{C1} by placing a zero at half of the LC double pole frequency (f_{LC}):

$$C_{C1} = \frac{1}{\pi \cdot f_{LC} \cdot R_{C1}} = 1.99\,nF \tag{15}$$

Now calculate C_{C2} to place a pole at half of the switching frequency and R_{C2} to place the second zero at the LC double pole frequency:

$$C_{C2} = \frac{C_{C1}}{\pi \cdot F_{SW} \cdot R_{C1} \cdot C_{C1} - 1} = 71\,pF \tag{16}$$

$$R_{C2} = \frac{R_{C2} \cdot f_{ESR}}{f_{ESR} - f_{LC}} = 166\,\Omega \tag{17}$$

Last, derive capacitance of C_{C3} to place a pole at the same frequency as the output capacitor ESR zero:

$$C_{C3} = \frac{1}{2 \cdot \pi \cdot f_{ESR} \cdot R_{C2}} = 898\,pF \tag{18}$$

An illustration of the total loop response is seen in Figure 35.

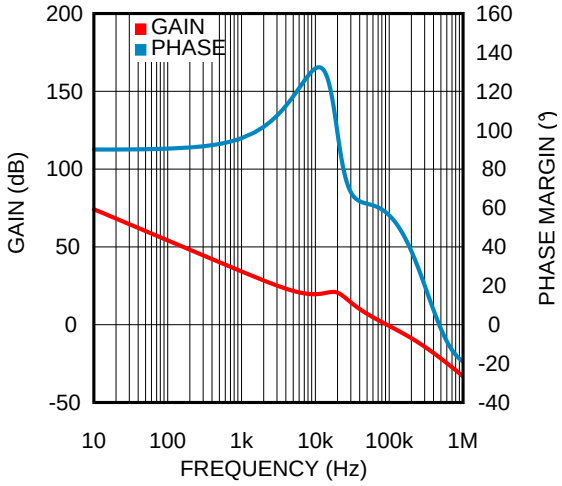


Figure 35. Loop Response

It is important to verify the stability either by observing the load transient response or by using a network analyzer. A phase margin between 45° and 70° is usually desired for voltage-mode converter circuits. Excessive phase margin causes slow system response to load transients whereas low phase margin leads to an oscillatory load transient response. If the peak deviation of the load transient response is larger than required, increasing $f_{crossover}$ and recalculating the compensation components may help but usually at the expense of phase margin.

Table 2. Bill of Materials (V_{IN} = 3.3 V to 5.5 V, V_{OUT} = 1.2 V, I_{OUT} = 15 A, f_{SW} = 500 kHz)

REF DES	DESCRIPTION	VENDOR	PART NUMBER	QUANTITY
C_F	CAP, CERM, 1 µF, 10 V, ±10%, X7R, 0603	MuRata	GRM188R71A105KA61D	1
C_{IN1}, C_{IN2}, C_{IN3}, C_{O1}, C_{O2}, C_{O3}	CAP, CERM, 100 µF, 6.3 V, ±20%, X5R, 1206	MuRata	GRM31CR60J107ME39L	6
C_{C1}	CAP, CERM, 1800 pF, 50 V, ±5%, C0G/NP0, 0603	TDK	C1608C0G1H182J	1
C_{C2}	CAP, CERM, 68 pF, 50 V, ±5%, C0G/NP0, 0603	TDK	C1608C0G1H680J	1
C_{C3}	CAP, CERM, 820 pF, 50 V, ±5%, C0G/NP0, 0603	TDK	C1608C0G1H821J	1
C_{SS}	CAP, CERM, 0.033 µF, 16 V, ±10%, X7R, 0603	MuRata	GRM188R71C333KA01D	1
L_F	Inductor, Powdered Iron, 560 nH, 27.5A, 1.8 mΩ, SMD	Vishay Dale	IHLP4040DZERR56M01	1
R_F	RES, 1 Ω, 5%, 0.1 W, 0603	Vishay Dale	CRCW06031R00JNEA	1
R_{C1}	RES, 9.31 kΩ, 1%, 0.1 W, 0603	Vishay Dale	CRCW06039K31FKEA	1
R_{C2}	RES, 165 Ω, 1%, 0.1 W, 0603	Vishay Dale	CRCW0603165RFKEA	1
R_{FB1}, R_{FB2}, R_{PGOOD}	RES, 10 kΩ, 1%, 0.1 W, 0603	Vishay Dale	CRCW060310K0FKEA	3
U_1	LM21215A Synchronous Buck Regulator	TI	LM21215AMH-1/NOPB	1

8.2.1.3 Application Curves

For additional details on the wavefroms shown in this section, please refer to application note *AN-2131 LM21215A Evaluation Board*, SNVA477.

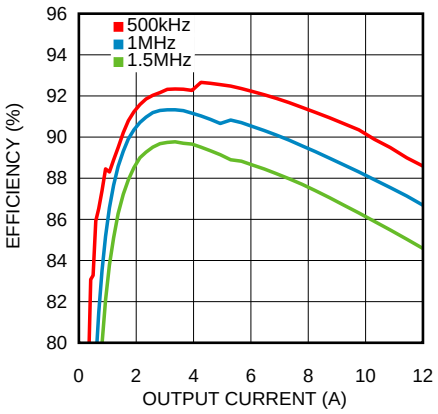


Figure 36. Efficiency vs Load Current, V_{OUT} = 1.2 V

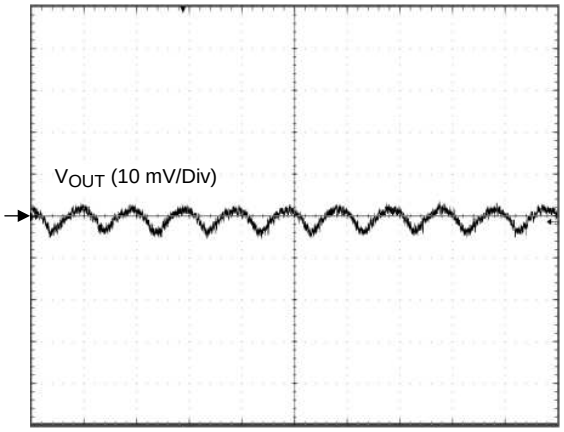


Figure 37. Output Ripple Voltage Waveform (1 µs/Div)

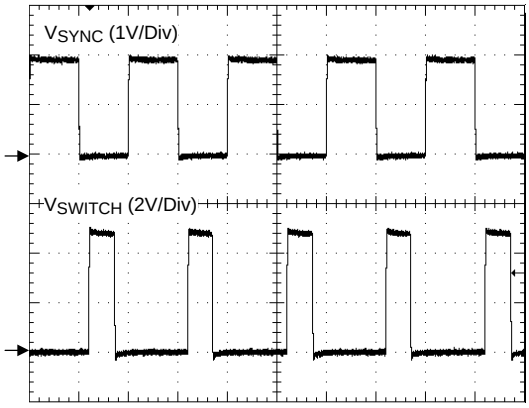


Figure 38. SW and SYNC Voltage Waveforms (1 µs/Div)

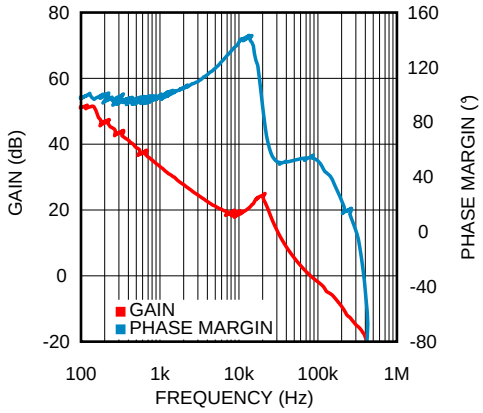


Figure 39. Bode Plot

8.2.2 Typical Application 2

The schematic diagram of a DC/DC regulator with 8-A output current is given by Figure 40.

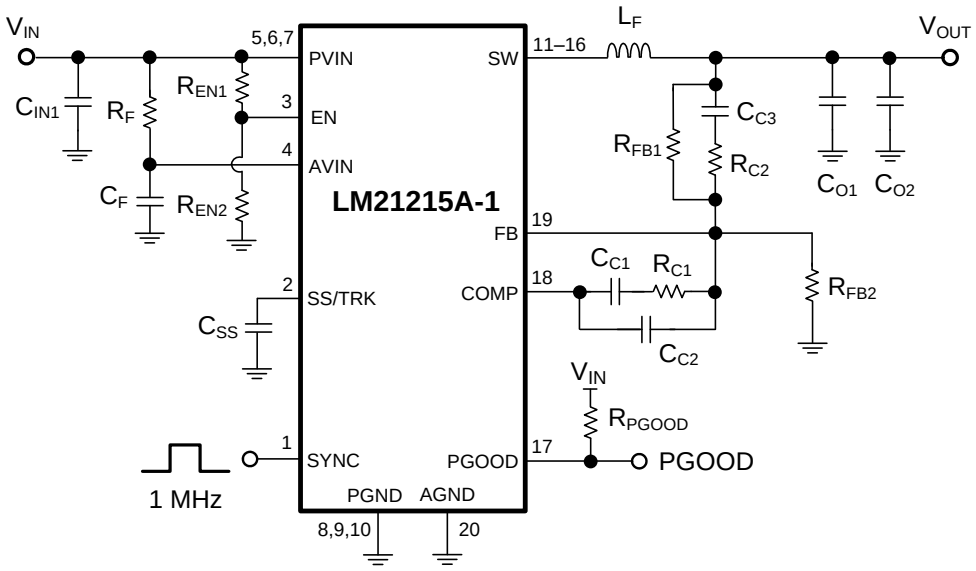


Figure 40. Typical Application Schematic 2

8.2.2.1 Design Requirements

Output voltage setpoint is 0.9 V and the input voltage ranges from 4 V to 5.5 V. The switching frequency is set by means of an external synchronization signal at 1 MHz. The output voltage soft-start time is 10 ms.

8.2.2.2 Detailed Design Procedure

Follow the detailed design procedure in *Typical Application 1*. The relevant power stage and small-signal components are listed in Table 3.

Table 3. Bill of Materials (V_{IN} = 4 V to 5.5 V, V_{OUT} = 0.9 V, I_{OUT} = 8 A, F_{SW} = 1 MHz)

REF DES	DESCRIPTION	VENDOR	PART NUMBER	QUANTITY
C_F	CAP, CERM, 1 µF, 10 V, ±10%, X7R, 0603	MuRata	GRM188R71A105KA61D	1
C_{IN1}, C_{O1}, C_{O2}	CAP, CERM, 100 µF, 6.3 V, ±20%, X5R, 1206	MuRata	GRM31CR60J107ME39L	3
C_{C1}	CAP, CERM, 1800 pF, 50 V, ±5%, C0G/NP0, 0603	MuRata	GRM1885C1H182JA01D	1
C_{C2}	CAP, CERM, 68 pF, 50 V, ±5%, C0G/NP0, 0603	TDK	C1608C0G1H680J	1
C_{C3}	CAP, CERM, 470 pF, 50 V, ±5%, C0G/NP0, 0603	TDK	C1608C0G1H471J	1
C_{SS}	CAP, CERM, 0.033 µF, 16 V, ±10%, X7R, 0603	MuRata	GRM188R71C333KA01D	1
L_F	Inductor, Shielded Core, 240 nH, 20 A, 1 mΩ, SMD	Würth	744314024	1
R_F	RES, 1 Ω, 5%, 0.1 W, 0603	Vishay Dale	CRCW06031R00JNEA	1
R_{C1}	RES, 4.87 kΩ, 1%, 0.1 W, 0603	Vishay Dale	CRCW06034K87FKEA	1
R_{C2}	RES, 210 Ω, 1%, 0.1 W, 0603	Vishay Dale	CRCW0603210RFKEA	1
R_{EN1}, R_{FB1}, R_{PGOOD}	RES, 10 kΩ, 1%, 0.1 W, 0603	Vishay Dale	CRCW060310K0FKEA	3
R_{EN2}	RES, 19.6 kΩ, 1%, 0.1 W, 0603	Vishay Dale	CRCW060319K6FKEA	1
R_{FB2}	RES, 20 kΩ, 1%, 0.1 W, 0603	Vishay Dale	CRCW060320K0FKEA	1
U_1	LM21215A Synchronous Buck Regulator	TI	LM21215AMH-1/NOPB	1

9 Power Supply Recommendations

The LM21215A converter is designed to operate from an input voltage supply range between 2.95 V and 5.5 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* tables. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with Equation 19, where η is the efficiency:

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \tag{19}$$

If the converter is connected to an input supply through long wires or PCB traces with large impedance, special care is required to achieve stable performance. The parasitic inductance and resistance of the input cables may have an adverse affect on converter operation. The parasitic inductance in combination with the low ESR ceramic input capacitors form an under-damped resonant circuit. This circuit can cause overvoltage transients at PVIN each time the input supply is cycled on and off. The parasitic resistance causes the PVIN voltage to dip during a load transient. If the regulator is operating close to the minimum input voltage, this dip can cause false UVLO fault triggering and a system reset. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 20 µF to 100 µF is usually sufficient to provide input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The user guide *Simple Success with Conducted EMI for DC-DC Converters*, SNVA489, provides helpful suggestions when designing an input filter for any switching regulator.

10 Layout

10.1 Layout Guidelines

PC board layout is an important and critical part of any DC-DC converter design. The performance of any switching converter depends as much upon the layout of the PCB as the component selection. Poor layout disrupts the performance of a switching converter and surrounding circuitry by contributing to EMI, ground bounce, conduction loss in the traces, and thermal problems. Erroneous signals can reach the DC-DC converter, possibly resulting in poor regulation or instability. There are several paths that conduct high slew-rate currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise and EMI or degrade the power-supply performance.

The following guidelines serve to help users to design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. Locate the input capacitors as close as possible to the PVIN and PGND pins, and place the inductor as close as possible to the SW pins and output capacitors. As described further in the *Compact PCB Layout for EMI Reduction* section, this placement is to minimize the area of switching current loops and reduce the resistive loss of the high current path. Ideally, use a ground plane on the top layer that connects the PGND pins, the exposed pad of the device, and the return terminals of the input and output capacitors in a small area near pins 10 and 11 of the device. For more details, refer to the board layout detailed in application note *AN-2131 LM21215A Evaluation Board*, SNVA477.
2. Minimize the copper area of the switch node. Route the six SW pins on a single top-layer plane to the inductor terminal using a wide trace to minimize conduction loss. The inductor can be placed on the bottom side of the PCB relative to the LM21215A, but take care to avoid any coupling of the inductor's magnetic field to sensitive feedback or compensation traces.
3. Use a solid ground plane on layer two of the PCB, particularly underneath the LM21215A and power stage components. This plane functions as a noise shield and also as a heat dissipation path.
4. Make input and output power bus connections as wide and short as possible to reduce voltage drops on the input and output of the converter and to improve efficiency. Use copper planes on top to connect the multiple PVIN pins and PGND pins together.
5. Provide enough PCB area for proper heat-sinking. As stated in the *Thermal Design* section, use enough copper area to ensure a low $R_{\theta JA}$ commensurate with the maximum load current and ambient temperature. Make the top and bottom PCB layers with two ounce copper thickness and no less than one ounce. Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers as recommended, connect these thermal vias to the inner layer heat-spreading ground planes.
6. Route the sense trace from the VOUT point of regulation to the feedback resistors away from the SW pins and inductor to avoid contaminating this feedback signal with switching noise. This routing is most important when high resistances are used to set the output voltage. Routing the feedback trace on a different layer than the inductor and SW node trace is recommended such that a ground plane exists between the sense trace and inductor or SW node polygon to provide further cancellation of EMI on the feedback trace.
7. If voltage accuracy at the load is important, ensure that the feedback voltage sense is made directly at the load terminals. Doing so corrects for voltage drops in the PCB planes and traces and provides optimal output voltage setpoint accuracy and load regulation. Place the feedback resistor divider closer to the FB node, rather than close to the load, because the FB node is the input to the error amplifier and is thus noise sensitive. COMP is a also noise-sensitive node and the compensation components must be located as close as possible to the device.
8. Place the AVIN bypass capacitor and the soft-start capacitor close to their respective pins.
9. See *Related Documentation* for additional important guidelines.

Layout Guidelines (continued)

10.1.1 Compact PCB Layout for EMI Reduction

Radiated EMI generated by high di/dt components relates to pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to reducing radiated EMI is to identify the pulsing current path and minimize the area of that path. The main switching loop of the LM21215A power stage is denoted by #1 in Figure 41. The topological architecture of a buck converter means that particularly high di/dt current flows in loop #1, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing its effective loop area. For loop #2 however, the di/dt through inductor L_F and capacitor C_{OUT} is naturally limited by the inductor. Keeping the area of loop #2 small is not nearly as important as that of loop #1. Also important are the gate drive loops of the low-side and high-side MOSFETs, which are inherently tight by virtue of the integrated power MOSFETs and gate drivers of the LM21215A

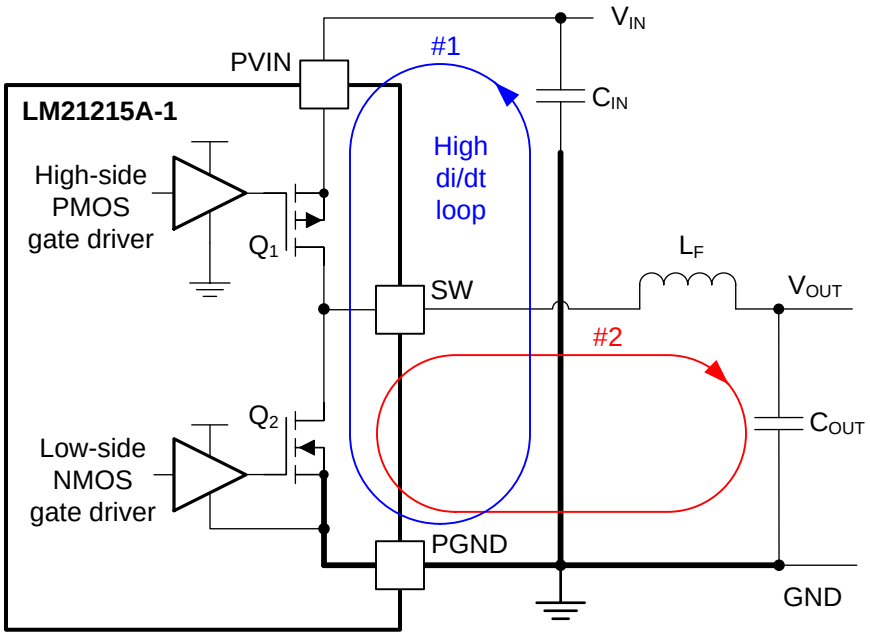


Figure 41. LM21215A Power Stage Circuit Switching Loops

High-frequency ceramic bypass capacitors at the input side provide the primary path for the high di/dt components of the pulsing current. Placing ceramic bypass capacitors as close as possible to the PVIN and PGND pins is the key to EMI reduction. Keep the SW trace connecting to the inductor as short as possible, and just wide enough to carry the load current without excessive heating. Use short, thick traces or copper pours (shapes) for current conduction path to minimize parasitic resistance. Place the output capacitors close to the VOUT side of the inductor and route the return using GND plane copper back to the PGND pins and the exposed pad of the LM21215A.

10.1.2 Thermal Design

As with any power conversion device, the LM21215A dissipates internal power while operating. The effect of this power dissipation is to raise the internal junction temperature of the LM21215A above ambient. The junction temperature (T_J) is a function of the ambient temperature (T_A), the power dissipation and the effective thermal resistance of the device and PCB combination ($R_{\theta JA}$). The maximum operating junction temperature for the LM21215A is 125°C, thus establishing a limit on the maximum device power dissipation and therefore the load current at high ambient temperatures. Equation 20 shows the relationships between these parameters.

$$I_{OUT} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \quad (20)$$

Layout Guidelines (continued)

High ambient temperatures and large values of $R_{\theta JA}$ reduce the maximum available output current. If the junction temperature exceeds 165°C, the LM21215A cycles in and out of thermal shutdown. Thermal shutdown may be a sign of inadequate heat-sinking or excessive power dissipation. Improve PCB heat-sinking by using more thermal vias, a larger board, or more heat-spreading layers within that board.

As stated in application note *Semiconductor and IC Package Thermal Metrics*, SPRA953, the values given in the *Thermal Information* table are not always valid for design purposes to estimate the thermal performance of the application. The values reported in the *Thermal Information* table are measured under a specific set of conditions that are seldom obtained in an actual application. The effective $R_{\theta JA}$ is a critical parameter and depends on many factors (such as power dissipation, air temperature, PCB area, copper heat-sink area, number of thermal vias under the package, air flow, and adjacent component placement). The LM21215A uses an advanced flip-chip-on-lead (FCOL) package and its exposed pad has a direct electrical and thermal connection to PGND. This pad must be soldered directly to the PCB copper ground plane to provide an effective heat-sink and proper electrical connection. Use the documents listed in *Related Documentation* as a guide for optimized thermal PCB design and estimating $R_{\theta JA}$ for a given application environment.

10.1.3 Ground Plane Design

As mentioned previously, using one of the middle layers as a solid ground plane is recommended. A ground plane offers shielding for sensitive circuits and traces and also provides a quiet reference potential for the control circuitry. Connect the AGND and PGND pins to the ground plane using an array of vias under the exposed pad. The PGND pins are connected to the source of the integrated low-side power MOSFET. Connect these pins directly to the return terminals of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce because of load current variations. The PGND trace, as well as PVIN and SW traces, must be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and is ideal for sensitive routes.

10.2 Layout Example

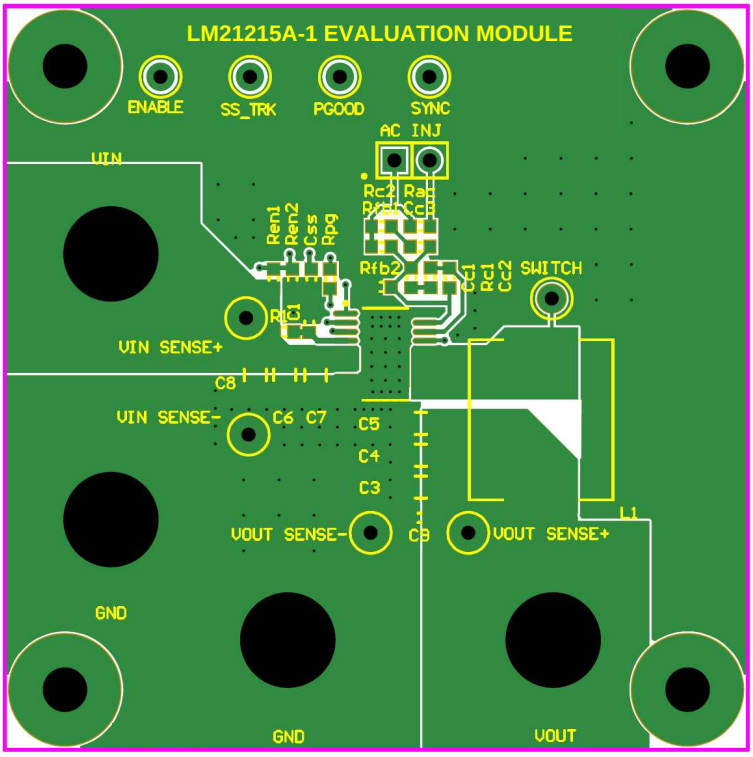


Figure 42. Layout Example Showing Top Layer Copper and Silkscreen

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

For the *LM21215A Quickstart Design Tool*, go to http://www.ti.com/product/LM21215A/toolssoftware#devtools.

For the PowerLab™, go to http://www.ti.com/powerlab.

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM21215A device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

- *AN-2131 LM21215A Evaluation Board*, SNVA477
- *AN-2130 LM21215 Evaluation Board*, SNVA476
- *AN-2107 LM21212-1 Evaluation Board*, SNVA467
- *AN-2140 LM21212-2 Evaluation Board*, SNVA480
- *AN-2162: Simple Success with Conducted EMI from DC-DC Converters*, SNVA489
- *6/4-Bit VID Programmable Current DAC for Point of Load Regulators with Adjustable Start-Up Current*, SNVS822
- *AN-1149 Layout Guidelines for Switching Power Supplies*, SNVA021
- *AN-1229 Simple Switcher PCB Layout Guidelines*, SNVA054
- *Constructing Your Power Supply – Layout Considerations*, SLUP230
- *Low Radiated EMI Layout Made SIMPLE with LM4360x and LM4600x*, SNVA721
- *AN-2020 Thermal Design By Insight, Not Hindsight*, SNVA419
- *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*, SNVA183
- *SPRA953B Semiconductor and IC Package Thermal Metrics*, SPRA953
- *SNVA719 Thermal Design made Simple with LM43603 and LM43602*, SNVA719
- *SLMA002 PowerPAD™ Thermally Enhanced Package*, SLMA002
- *SLMA004 PowerPAD Made Easy*, SLMA004
- *SBVA025 Using New Thermal Metrics*, SBVA025

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM21215AMH-1/NOPB	ACTIVE	HTSSOP	PWP	20	73	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21215 AMH-1	Samples
LM21215AMHE-1/NOPB	ACTIVE	HTSSOP	PWP	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21215 AMH-1	Samples
LM21215AMHX-1/NOPB	ACTIVE	HTSSOP	PWP	20	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM21215 AMH-1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

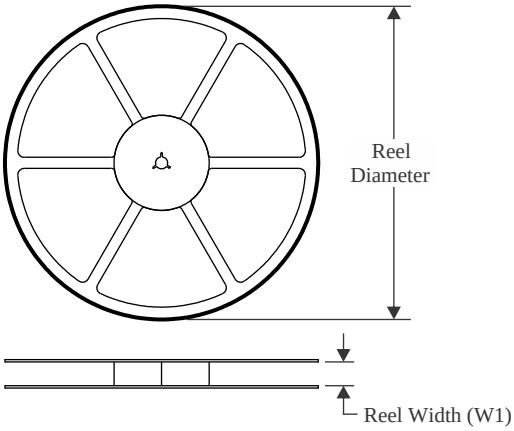
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

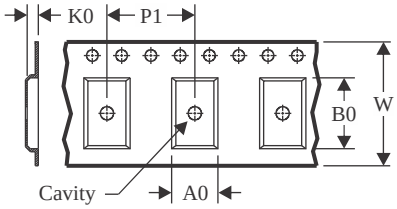
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

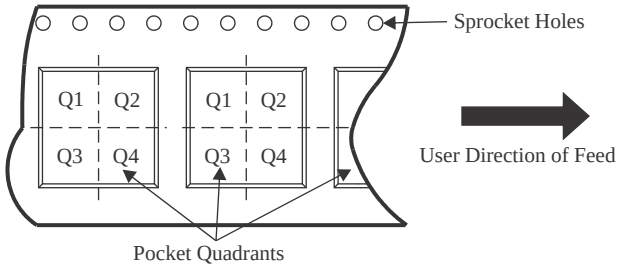


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

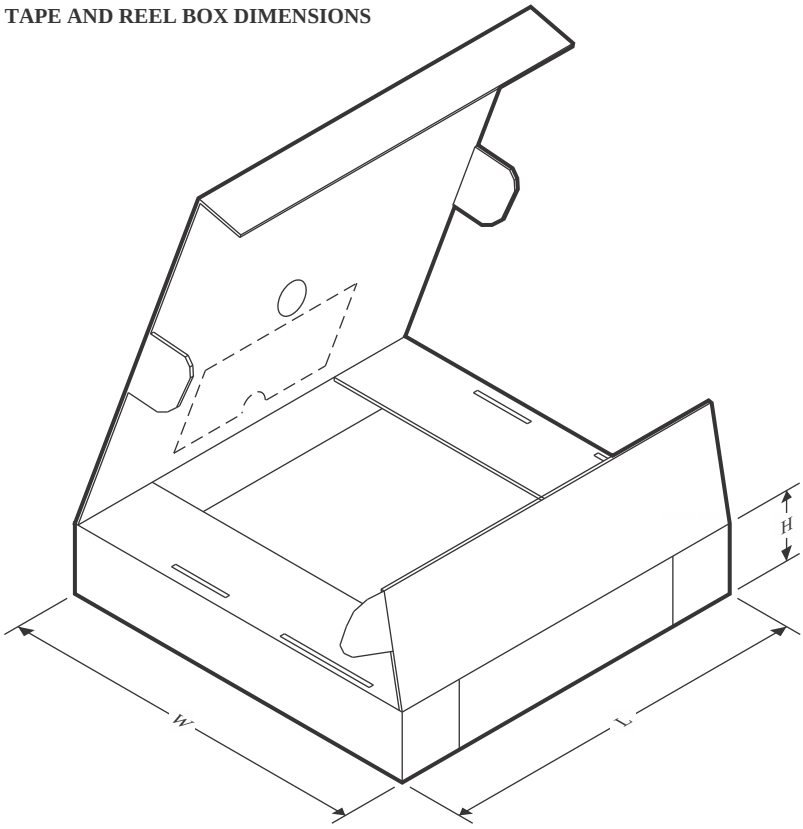
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM21215AMHE-1/NOPB	HTSSOP	PWP	20	250	178.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
LM21215AMHX-1/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

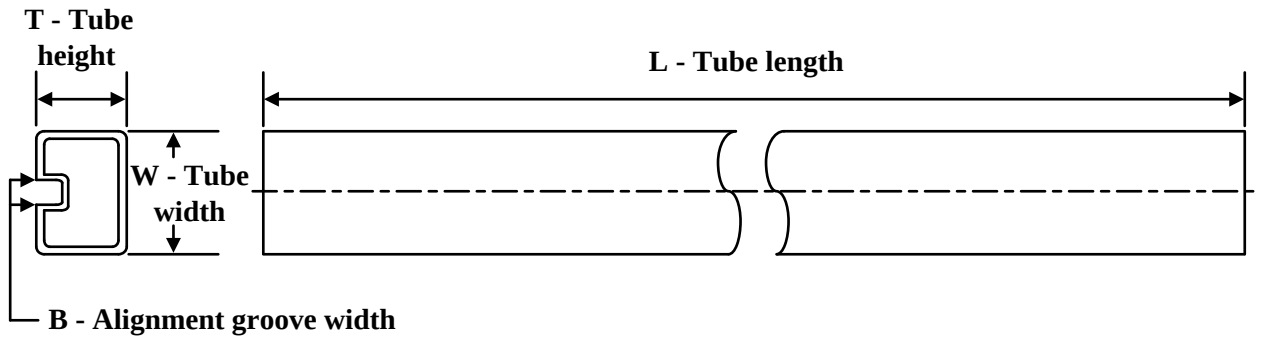
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM21215AMHE-1/NOPB	HTSSOP	PWP	20	250	210.0	185.0	35.0
LM21215AMHX-1/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0

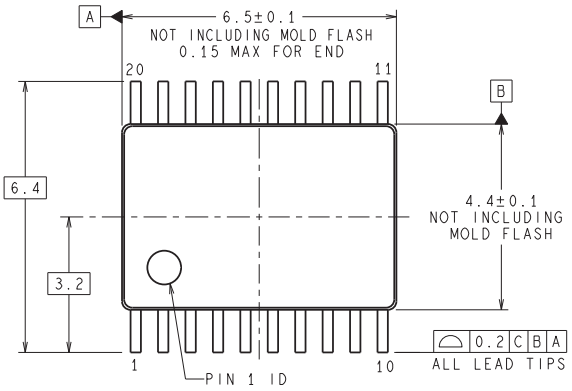
TUBE



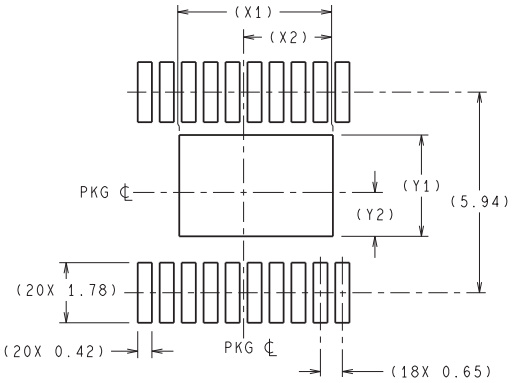
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM21215AMH-1/NOPB	PWP	HTSSOP	20	73	495	8	2514.6	4.06

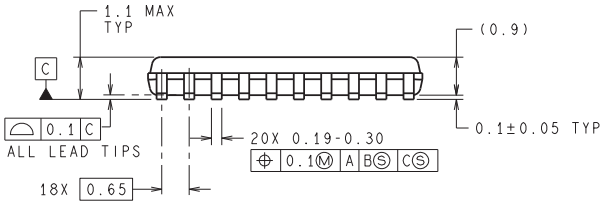
PWP0020AA

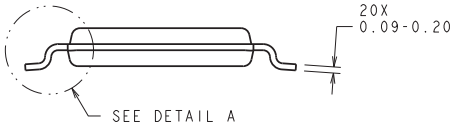


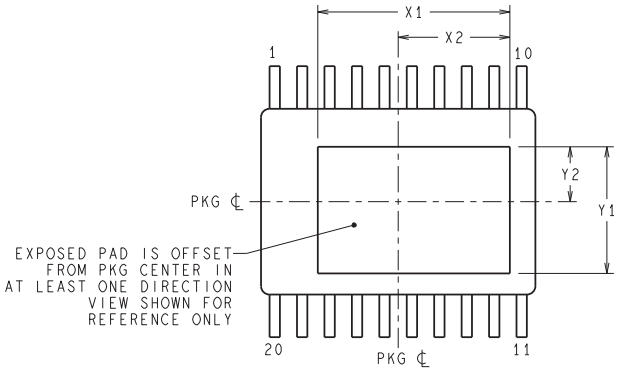
TOP VIEW



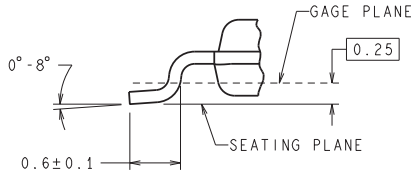
LAND PATTERN RECOMENDATION







BOTTOM VIEW



DETAIL A
TYPICAL

PAD SIZE CODE IN DWG No. (XX)	PAD SIZE		X2	Y2
	X1	Y1		
AA	4.55	3.32	2.645±0.1	1.66±0.1

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MYB20XX (REV E)

4214875/A 02/2013

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Reference JEDEC Registration MO-153, Variation ACT.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265