LM49370 Boomer® Audio Power Amplifier Series Audio Sub-System with an Ultra Low EMI, Spread Spectrum, Class D Loudspeaker Amplifier, a Dual-Mode Stereo Headphone Amplifier, and a Dedicated PCM Interface for Bluetooth Transceivers

Check for Samples: LM49370

FEATURES

- Spread Spectrum Class D Architecture Reduces EMI
- Mono Class D 8Ω Amplifier, 490 mW at 3.3V
- OCL or AC-Coupled Headphone Operation
- 33mW Stereo Headphone Amplifier at 3.3V
- 115 mW Earpiece Amplifier at 3.3V
- 18-bit Stereo DAC
- 16-bit Mono ADC
- 8 kHz to 192 kHz Stereo Audio Playback
- 8 kHz to 48 kHz Mono Recording
- Bidirectional I^2S Compatible Audio Interface
- Bidirectional PCM Compatible Audio Interface for Bluetooth Transceivers
- I^2S-PCM Bridge with Sample Rate Conversion
- Sigma-Delta PLL for Operation from Any Clock at Any Sample Rate
- Digital 3D Stereo Enhancement
- FIR Filter Programmability for Simple Tone Control
- Low Power Clock Network Operation if a 12 MHz or 13 MHz System Clock is Available
- Read/Write I^2C or SPI Compatible Control Interface
- Automatic Headphone & Microphone Detection
- Support for Internal and External Microphones
- Automatic Gain Control for Microphone Input
- Differential Audio I/O for External Cellphone Module
- Mono Differential Auxiliary Output
- Stereo Auxiliary Inputs
- Differential Microphone Input for Internal Microphone
- Flexible Audio Routing from Input to Output
- 32 Step Volume Control for Mixers in 1.5 dB Steps
- 16 Step Volume Control for Microphone in 2 dB Steps
- Programmable Sidetone Attenuation in 3 dB Steps
- Two Configurable GPIO Ports
- Multi-Function IRQ Output
- Micro-Power Shutdown Mode
- Available in the 4 x 4 mm 49 Bump DSBGA Package
- Key Specifications
  - $P_{HP\ (AC\text{-}COUP)}$ (A_V_{DD} = 3.3V, 32Ω, 1% THD) 33 mW
  - $P_{HP\ (OCL)}$ (A_V_{DD} = 3.3V, 32Ω, 1% THD) 31 mW
  - P_{LS} (LS_V_{DD} = 5V, 8Ω, 1% THD) 1.2 W
  - P_{LS} (LS_V_{DD} = 4.2V, 8Ω, 1% THD) 900 mW
  - P_{LS} (LS_V_{DD} = 3.3V, 8Ω, 1% THD) 490 mW
  - Shutdown Current 0.8 µA
  - $PSRR_{LS}$ (217 Hz, LS_V_{DD} = 3.3V) 70 dB
  - SNR_{LS} (AUX IN to Loudspeaker) 90 dB (typ)
  - SNR_{DAC} (Stereo DAC to AUXOUT) 85 dB (typ)
  - SNR_{ADC} (Mono ADC from Cell Phone In) 90 dB (typ)
  - SNR_{HP} (Aux In to Headphones) 98 dB (typ)

APPLICATIONS

- Smart Phones
- Mobile Phones and Multimedia Terminals
- PDAs, Internet Appliances and Portable Gaming
- Portable DVD/CD/AAC/MP3 Players
- Digital Cameras/Camcorders

DESCRIPTION

The LM49370 is an integrated audio subsystem that supports both analog and digital audio functions. The LM49370 includes a high quality stereo DAC, a mono ADC, a stereo headphone amplifier, which supports output cap-less (OCL) or AC-coupled (SE) modes of operation, a mono earpiece amplifier, and an ultra-low EMI spread spectrum Class D loudspeaker amplifier. It is designed for demanding applications in mobile phones and other portable devices.

The LM49370 features a bi-directional I^2S interface and a bi-directional PCM interface for full range audio on either interface. The LM49370 utilizes an I^2C or SPI compatible interface for control. The stereo DAC path features an SNR of 85 dB with an 18-bit 48 kHz input. In SE mode the headphone amplifier delivers at least 33 mW_{RMS} to a 32Ω single-ended stereo load with less than 1% distortion (THD+N) when A_V_{DD} = 3.3V. The mono earpiece amplifier delivers at least 115mW_{RMS} to a 32Ω bridged-tied load with less than 1% distortion (THD+N) when A_V_{DD} = 3.3V. The mono speaker amplifier delivers up to 490mW into an 8Ω load with less than 1% distortion when LS_V_{DD} = 3.3V and up to 1.2W when LS_V_{DD} = 5.0V.

The LM49370 employs advanced techniques to reduce power consumption, to reduce controller overhead, to speed development time, and to eliminate click and pop. Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components. It is therefore ideally suited for mobile phone and other low voltage applications where minimal power consumption, PCB area and cost are primary requirements.

LM49370 Overview

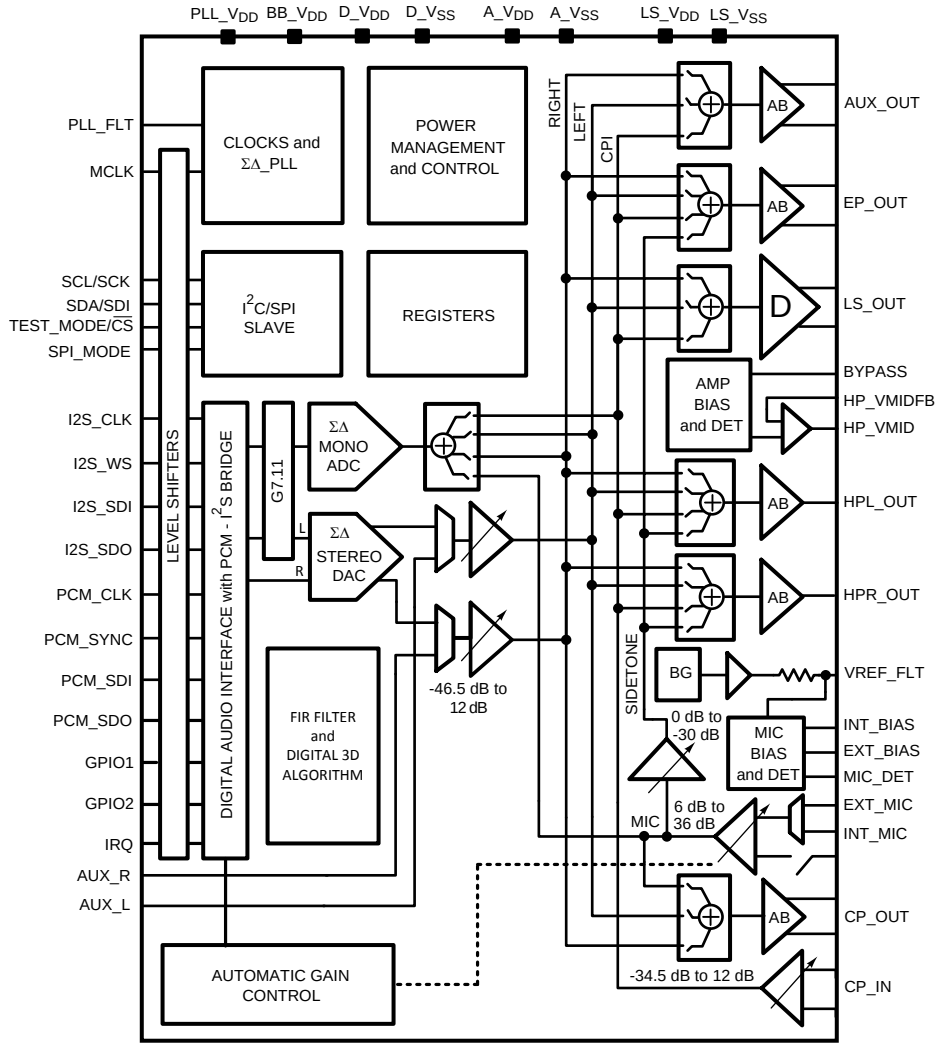


Figure 1. Conceptual Schematic

Typical Application

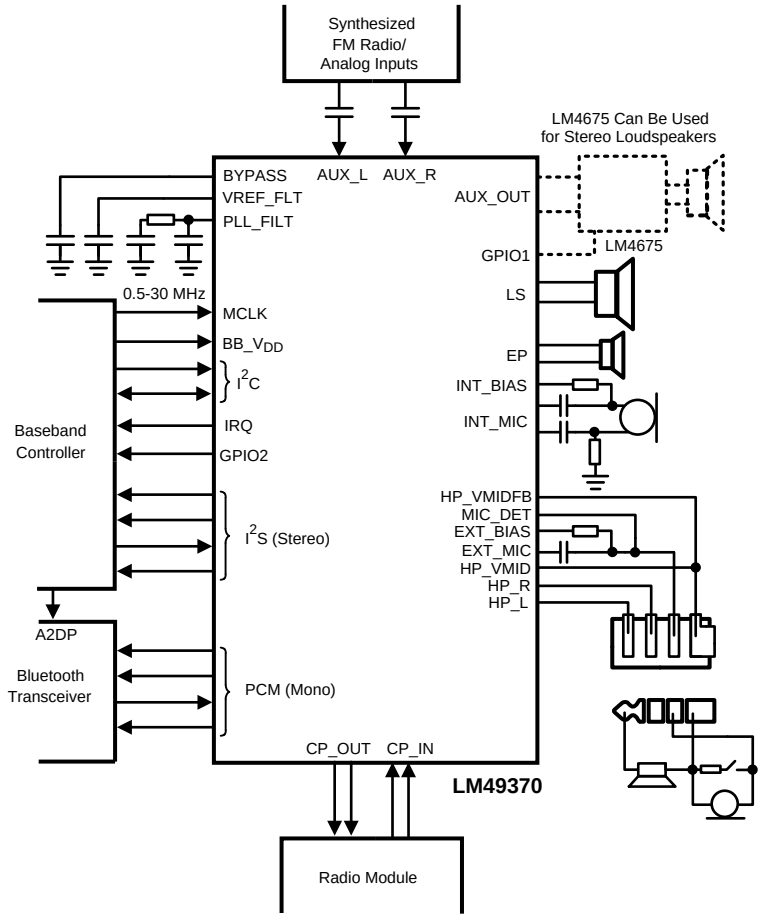


Figure 2. Example Application in Multimedia Mobile Phone

Connection Diagrams

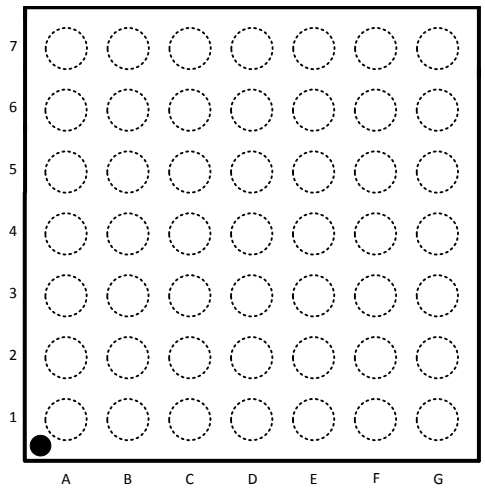


Figure 3. 49 Bump DSBGA
Top View (Bump Side Down)
See Package Number YPG0049UUA

Pin Descriptions

Pin	Pin Name	Type	Direction	Description
A1	EP_NEG	Analog	Output	Earpiece negative output
A2	A_V_{DD}	Supply	Input	Headphone and mixer V_{DD}
A3	INT_MIC_POS	Analog	Input	Internal microphone positive input
A4	PCM_SDO	Digital	Output	PCM Serial Data Output
A5	PCM_CLK	Digital	Inout	PCM clock signal
A6	PCM_SYNC	Digital	Inout	PCM sync signal
A7	PCM_SDI	Digital	Input	PCM Serial Data Input
B1	A_V_{SS}	Supply	Input	Headphone and mixer ground
B2	EP_POS	Analog	Output	Earpiece positive output
B3	INT_MIC_NEG	Analog	Input	Internal microphone negative input
B4	BYPASS	Analog	Input	A_V_{DD}/2 filter point
B5	TEST_MODE/$\overline{CS}$	Digital	Input	If SPI_MODE = 1, then this pin becomes $\overline{CS}$.
B6	PLL_FILT	Analog	Input	Filter point for PLL VCO input
B7	PLL_V_{DD}	Supply	Input	PLL V_{DD}
C1	HP_R	Analog	Output	Headphone Right Output
C2	EXT_BIAS	Analog	Output	External microphone supply (2.0/2.5/2.8/3.3V)
C3	INT_BIAS	Analog	Output	Internal microphone supply (2.0/2.5/2.8/3.3V)
C4	AUX_R	Analog	Input	Right Analog Input
C5	GPIO_2	Digital	Inout	General Purpose I/O 2
C6	SDA	Digital	Inout	Control Data, I2C_SDA or SPI_SDA
C7	SCL	Digital	Input	Control Clock, I2C_SCL or SPI_SCL
D1	HP_L	Analog	Output	Headphone Left Output
D2	VREF_FLT	Analog	Inout	Filter point for the microphone power supply
D3	EXT_MIC	Analog	Input	External microphone input
D4	SPI_MODE	Digital	Input	Control mode select 1 = SPI, 0 = I2C
D5	GPIO_1	Digital	Inout	General Purpose I/O 1
D6	BB_V_{DD}	Supply	Input	Baseband V_{DD} for the digital I/Os
D7	D_V_{DD}	Supply	Input	Digital V_{DD}
E1	HP_VMID	Analog	Inout	Virtual Ground for Headphones in OCL mode, otherwise 1st headset detection input
E2	MIC_DET	Analog	Input	Headset insertion/removal and microphone presence detection input.
E3	AUX_L	Analog	Input	Left Analog Input
E4	CPI_NEG	Analog	Input	Cell Phone analog input negative
E5	IRQ	Digital	Output	Interrupt request signal (NOT open drain)
E6	I2S_SDO	Digital	Output	I2S Serial Data Out

Pin Descriptions (continued)

Pin	Pin Name	Type	Direction	Description
E7	I2S_SDI	Digital	Input	I2S Serial Data Input
F1	HP_VMID_FB	Analog	Input	VMID Feedback in OCL mode, otherwise a 2nd headset detection input
F2	LS_V_{DD}	Supply	Input	Loudspeaker V_{DD}
F3	CPI_POS	Analog	Input	Cell Phone analog input positive
F4	CPO_NEG	Analog	Output	Cell Phone analog output negative
F5	AUX_OUT_NEG	Analog	Output	Auxiliary analog output negative
F6	I2S_WS	Digital	Inout	I2S Word Select Signal (can be master or slave)
F7	I2S_CLK	Digital	Inout	I2S Clock Signal (can be master or slave)
G1	LS_NEG	Analog	Output	Loudspeaker negative output
G2	LS_V_{SS}	Supply	Input	Loudspeaker ground
G3	LS_POS	Analog	Output	Loudspeaker positive output
G4	CPO_POS	Analog	Output	Cell Phone analog output positive
G5	AUX_OUT_POS	Analog	Output	Auxiliary analog output positive
G6	D_V_{SS}	Supply	Input	Digital ground
G7	MCLK	Digital	Input	Input clock from 0.5 MHz to 30 MHz

PIN TYPE DEFINITIONS

Analog Input— A pin that is used by the analog and is never driven by the device. Supplies are part of this classification.

Analog Output— A pin that is driven by the device and should not be driven by external sources.

Analog Inout— A pin that is typically used for filtering a DC signal within the device, Passive components can be connected to these pins.

Digital Input— A pin that is used by the digital but is never driven.

Digital Output— A pin that is driven by the device and should not be driven by another device to avoid contention.

Digital Inout— A pin that is either open drain (I2C_SDA) or a bidirectional CMOS in/out. In the later case the direction is selected by a control register within the LM49370.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

Analog Supply Voltage (A_V_{DD} & LS_V_{DD})		6.0V
Digital Supply Voltage (BB_V_{DD} & D_V_{DD} & PLL_V_{DD})		6.0V
Storage Temperature		−65°C to +150°C
Power Dissipation (3)		Internally Limited
ESD Susceptibility	Human Body Model (4)	2500V
	Machine Model (5)	200V
Junction Temperature		150°C
Thermal Resistance θ_{JA} – YPG49 (soldered down to PCB with $2in^2$ 1oz. copper plane)		60°C/W
Soldering Information		

(1) All voltages are measured with respect to the relevant V_{SS} pin unless otherwise specified. All grounds should be coupled as close as possible to the device.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(3) The maximum power dissipation must be de-rated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in Absolute Maximum Ratings, whichever is lower.
(4) Human body model: 100pF discharged through a 1.5kΩ resistor.
(5) Machine model: 220pF – 240pF discharged through all pins.

Operating Ratings

Temperature Range		−40°C to +85°C
Supply Voltage	D_V_{DD}/PLL_V_{DD}	2.5V to 4.5V
	BB_V_{DD}	1.8V to 4.5V
	$LS\_V_{DD} = A\_V_{DD}$ (1)	2.5V to 5.5V

(1) LS_V_{DD} must be equal to A_V_{DD} due to intend ESD diode structure. For proper operation, LS_V_{DD} and A_V_{DD} need to be the highest voltage than BB_V_{DD}, D_V_{DD}, and PLL_V_{DD} and must be applied first.

Electrical Characteristics (1)(2)

Unless otherwise stated **PLL_V_{DD} = 3.3V, D_V_{DD} = 3.3V, BB_V_{DD} = 1.8V, A_V_{DD} = 3.3V, LS_V_{DD} = 3.3V.** The following specifications apply for the circuit shown in Figure 2 unless otherwise stated. Limits apply for 25°C.

Symbol	Parameter	Conditions	LM49370		Units
			Typical (3)	Limit (4) (5)	
POWER					
DI_{SD}	Digital Shutdown Current (6)	Chip Mode '00', f_{MCLK} = 13MHz	0.7	2.2	µA (max)
DI_{ST}	Digital Standby Current	Chip Mode '01', f_{MCLK} = 13MHz	0.9	1.8	mA(max)
AI_{SD}	Analog Shutdown Current	Chip Mode '00'	0.1	1.2	µA(max)
AI_{ST}	Analog Standby Current	Chip Mode '01'	0.1	1.2	µA (max)

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional but do not ensure specific performance limits. Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
(2) All voltages are measured with respect to the relevant V_{SS} pin unless otherwise specified. All grounds should be coupled as close as possible to the device.
(3) Typical values are measured at 25°C and represent the parametric norm.
(4) Limits are specified to TI's AOQL (Average Outgoing Quality Level).
(5) Datasheet min/max specification limits are specified by design, test, or statistical analysis.
(6) Digital shutdown current is measured with system clock set for PLL output while the PLL is disabled.

Electrical Characteristics [1][2] (continued)

Unless otherwise stated **PLL_V_{DD} = 3.3V, D_V_{DD} = 3.3V, BB_V_{DD} = 1.8V, A_V_{DD} = 3.3V, LS_V_{DD} = 3.3V.** The following specifications apply for the circuit shown in Figure 2 unless otherwise stated. Limits apply for 25°C.

Symbol	Parameter	Conditions	LM49370		Units
			Typical[3]	Limit[4] [5]	
	Digital Playback Mode Digital Active Current	Chip Mode '10', f_{MCLK} = 12MHz, f_S = 48kHz, DAC on; PLL off	7.9		mA
		Chip Mode '10', f_{MCLK} = 13MHz, f_{PLLOUT} = 12MHz, f_S = 48kHz; DAC + PLL on	12.5	14.5	mA(max)
	Digital Playback Mode Analog Active Current	Chip Mode '10', HP On, SE mode, DAC inputs selected	9.0	13.5	mA(max)
		Chip Mode '10', HP On, OCL mode, DAC inputs selected	9.4	13.5	mA(max)
		Chip Mode '10', LS On, DAC inputs selected	11.5	15.5	mA(max)
	Analog Playback Mode Digital Active Current	Chip Mode '10', f_{MCLK} = 13MHz, DAC +ADC + PLL off	0.9	1.8	mA(max)
	Analog Playback Mode Analog Active Current	Chip Mode '10', HP On, SE mode, AUX inputs selected	5.9	9.5	mA(max)
		Chip Mode '10', HP On, OCL mode, AUX inputs selected	6.3	9.7	mA(max)
		Chip Mode '10', LS On, AUX inputs selected	8.4	12	mA(max)
	CODEC Mode Digital Active Current	Chip Mode '10', f_{MCLK} = 13MHz, f_S = 8kHz, DAC +ADC on; PLL Off	2.7	3.5	mA(max)
	CODEC Mode Analog Active Current	Chip Mode '10', EP On, DAC inputs selected	11.2	15.5	mA(max)
	Voice Module Mode Digital Active Current	Chip Mode '10', f_{MCLK} = 13MHz, DAC +ADC + PLL off	0.9	1.8	mA(max)
	Voice Module Mode Analog Active Current	Chip Mode '10', EP + CPOUT on, CPIN input selected	7.4	11	mA(max)
LOUDSPEAKER AMPLIFIER					
P_{LS}	Max Loudspeaker Power	8Ω load, LS_V_{DD} = 5V	1.2		W
		8Ω load, LS_V_{DD} = 4.2V	0.9		W
		8Ω load, LS_V_{DD} = 3.3V	0.5	0.43	W (min)
LS_{THD+N}	Loudspeaker Harmonic Distortion	8Ω load, LS_V_{DD} = 3.3V, P_O = 400mW	0.04		%
LS_{EFF}	Efficiency	0 dB Input MCLK = 12.000 MHz	84		%
$PSRR_{LS}$	Power Supply Rejection Ration (Loudspeaker)	AUX inputs terminated C_{BYPASS} = 1.0 µF V_{RIPPLE} = 200 mV_{P-P} f_{RIPPLE} = 217 Hz	70		dB
SNR_{LS}	Signal to Noise Ratio	From 0 dB Analog AUX input, A-weighted	90	80	dB(min)
e_N	Output Noise[7]	A-weighted	62		µV
V_{OS}	Loudspeaker Offset Voltage		12		mV

(7) Disabling or bypassing the PLL will usually result in an improvement in noise measurements.

Electrical Characteristics [1][2] (continued)

Unless otherwise stated **PLL_V_{DD} = 3.3V, D_V_{DD} = 3.3V, BB_V_{DD} = 1.8V, A_V_{DD} = 3.3V, LS_V_{DD} = 3.3V.** The following specifications apply for the circuit shown in Figure 2 unless otherwise stated. Limits apply for 25°C.

Symbol	Parameter	Conditions	LM49370		Units
			Typical[3]	Limit[4] [5]	
HEADPHONE AMPLIFIER					
P_{HP}	Headphone Power	32Ω load, 3.3V, SE	33	25	mW (min)
		16Ω load, 3.3V, SE	52		mW
		32Ω load, 3.3V, OCL, VCM = 1.5V	31		mW
		32Ω load, 3.3V, OCL, VCM = 1.2V	20		mW
		16Ω load, 3.3V, OCL, VCM = 1.5V	50		mW
		16Ω load, 3.3V, OCL, VCM = 1.2V	32		mW
$PSRR_{HP}$	Power Supply Rejection Ratio (Headphones)	AUX inputs terminated C_{BYPASS} = 1.0 µF V_{RIPPLE} = 200 mV_{P-P} f_{RIPPLE} = 217 Hz			
		SE Mode	60		dB
		OCL Mode VCM = 1.2V	68	55	dB(min)
		OCL Mode VCM = 1.5V	65		dB
SNR_{HP}	Signal to Noise Ratio	From 0dB Analog AUX input A-weighted			
		SE Mode	98		dB
		OCL Mode VCM = 1.2V	97		dB
		OCL Mode VCM = 1.5V	96		dB
HP_{THD+N}	Headphone Harmonic Distortion	32Ω load, 3.3V, P_O = 7.5mW	0.05		%
e_N	Output Noise	A-weighted	12		µV
ΔA_{CH-CH}	Stereo Channel-to-Channel Gain Mismatch		0.3		dB
X_{TALK}	Stereo Crosstalk	SE Mode	61		dB
		OCL Mode	71		dB
V_{OS}	Offset Voltage		8		mV
EARPIECE AMPLIFIER					
P_{EP}	Earpiece Power	32Ω load, 3.3V	115	100	mW (min)
		16Ω load, 3.3V	150		mW
$PSRR_{EP}$	Power Supply Rejection Ratio (Earpiece)	CP_IN terminated C_{BYPASS} = 1.0 µF V_{RIPPLE} = 200 mV_{P-P} F_{RIPPLE} = 217 Hz	76		dB
SNR_{EP}	Signal to Noise Ratio	From 0dB Analog AUX input, A-weighted	93		dB
EP_{THD+N}	Earpiece Harmonic Distortion	32Ω load, 3.3V, P_O = 50mW	0.04		%
e_N	Output Noise	A-weighted	41		µV
V_{OS}	Offset Voltage		8		mV
AUXOUT AMPLIFIER					
THD+N	Total Harmonic Distortion + Noise	V_O = 1V_{RMS}, 5kΩ load	0.02		%
PSRR	Power Supply Rejection Ratio	CP_IN terminated C_{BYPASS} = 1.0µF V_{RIPPLE} = 200mVPP f_{RIPPLE} = 217Hz	86		dB

Electrical Characteristics [1][2] (continued)

Unless otherwise stated **PLL_V_{DD} = 3.3V, D_V_{DD} = 3.3V, BB_V_{DD} = 1.8V, A_V_{DD} = 3.3V, LS_V_{DD} = 3.3V.** The following specifications apply for the circuit shown in Figure 2 unless otherwise stated. Limits apply for 25°C.

Symbol	Parameter	Conditions	LM49370		Units
			Typical[3]	Limit[4] [5]	
CP_OUT AMPLIFIER					
THD+N	Total Harmonic Distortion + Noise	V_O = 1V_{RMS}, 5kΩ load	0.02		%
PSRR	Power Supply Rejection Ratio	C_{BYPASS} = 1.0µF V_{RIPPLE} = 200mVPP f_{RIPPLE} = 217Hz	86		dB
MONO ADC					
R_{ADC}	ADC Ripple		±0.25		dB
PB_{ADC}	ADC Passband	Lower (HPF Mode 1), f_S = 8 kHz	300		Hz
		Upper	3470		Hz
SBA_{ADC}	ADC Stopband Attenuation	Above Passband	60		dB
		HPF Notch, 50 Hz/60 Hz (worst case)	58		dB
SNR_{ADC}	ADC Signal to Noise Ratio	From CPI, A-weighted	90		dB
ADC_{LEVEL}	ADC Full Scale Input Level		1		V_{RMS}
STEREO DAC					
R_{DAC}	DAC Ripple		0.1		dB
PB_{DAC}	DAC Passband		20		kHz
SBA_{DAC}	DAC Stopband Attenuation		70		dB
SNR_{DAC}	DAC Signal to Noise Ratio	A-weighted, AUXOUT	85		dB
DR_{DAC}	DAC Dynamic Range		96		dB
DAC_{LEVEL}	DAC Full Scale Output Level		1		V_{RMS}
PLL[8]					
F_{IN}	Input Frequency Range	Min		0.5	MHz
		Max		30	MHz
I2S/PCM					
f_{I2SCLK}	I2S CLK Frequency	f_S = 48kHz; 16 bit mode	1.536		MHz
		f_S = 48kHz; 25 bit mode	2.4		MHz
		f_S = 8kHz; 16 bit mode	0.256		MHz
		f_S = 8kHz; 25 bit mode	0.4		MHz
f_{PCMCLK}	PCM CLK Frequency	f_S = 48kHz; 16 bit mode	0.768		MHz
		f_S = 48kHz; 25 bit mode	1.2		MHz
		f_S = 8kHz; 16 bit mode	0.128		MHz
		f_S = 8kHz; 25 bit mode	0.2		MHz
DC_{I2S_CLK}	I2S_CLK Duty Cycle	Min		40	% (min)
		Max		60	% (max)
DC_{I2S_WS}	I2S_WS Duty Cycle		50		%
I2C					
T_{I2CSET}	I2C Data Setup Time	Refer to TRANSFERRING DATA for more details		100	ns (min)
$T_{I2CHOLD}$	I2C Data Hold Time	Refer to TRANSFERRING DATA for more details		300	ns (min)
SPI					
$T_{SPISETENB}$	Enable Setup Time			100	ns (min)
$T_{SPIHOLD-ENB}$	Enable Hold Time			100	ns (min)
$T_{SPISETD}$	Data Setup Time			100	ns (min)

(8) Disabling or bypassing the PLL will usually result in an improvement in noise measurements.

Electrical Characteristics [1][2] (continued)

Unless otherwise stated **PLL_V_{DD} = 3.3V, D_V_{DD} = 3.3V, BB_V_{DD} = 1.8V, A_V_{DD} = 3.3V, LS_V_{DD} = 3.3V.** The following specifications apply for the circuit shown in Figure 2 unless otherwise stated. Limits apply for 25°C.

Symbol	Parameter	Conditions	LM49370		Units
			Typical[3]	Limit[4] [5]	
$T_{SPIHOLDD}$	Data Hold Time			100	ns (min)
T_{SPICL}	Clock Low Time			500	ns (min)
T_{SPICH}	Clock High Time			500	ns (min)
VOLUME CONTROL					
VCR_{AUX}	AUX Volume Control Range	Minimum Gain w/ AUX_BOOST OFF	–46.5		dB
		Maximum Gain w/ AUX_BOOST OFF	0		dB
		Minimum Gain w/ AUX_BOOST ON	–34.5		dB
		Maximum Gain w/ AUX_BOOST ON	12		dB
VCR_{DAC}	DAC Volume Control Range	Minimum Gain w/ DAC_BOOST OFF	–46.5		dB
		Maximum Gain w/ DAC_BOOST OFF	0		dB
		Minimum Gain w/ DAC_BOOST ON	–34.5		dB
		Maximum Gain w/ DAC_BOOST ON	12		dB
VCR_{CPIN}	CPIN Volume Control Range	Minimum Gain	–34.5		dB
		Maximum Gain	12		dB
VCR_{MIC}	MIC Volume Control Range	Minimum Gain	6		dB
		Maximum Gain	36		dB
VCR_{SIDE}	SIDETONE Volume Control Range	Minimum Gain	–30		dB
		Maximum Gain	0		dB
SS_{AUX}	AUX VCR Stepsize		1.5		dB
SS_{DAC}	DAC VCR Stepsize		1.5		dB
SS_{CPIN}	CPIN VCR Stepsize		1.5		dB
SS_{MIC}	MIC VCR Stepsize		2		dB
SS_{SIDE}	SIDETONE VCR Stepsize		3		dB
AUDIO PATH GAIN W/ STEREO (bit 6 of 0x00h) ENABLED (AUX_L & AUX_R signals identical and selected onto mixer)					
	Loudspeaker Audio Path Gain	Minimum Gain from AUX input, BOOST OFF	–34.5		dB
		Maximum Gain from AUX input, BOOST OFF	12		dB
		Minimum Gain from CPI input	–22.5		dB
		Maximum Gain from CPI input	24		dB
	Headphone Audio Path Gain	Minimum Gain from AUX input, BOOST OFF	–52.5		dB
		Maximum Gain from AUX input, BOOST OFF	–6		dB
		Minimum Gain from CPI input	–40.5		dB
		Maximum Gain from CPI input	6		dB
		Minimum Gain from MIC input using SIDETONE path w/ VCR_{MIC} gain = 6dB	–30		dB
		Maximum Gain from MIC input using SIDETONE path w/ VCR_{MIC} gain = 6dB	0		dB

Electrical Characteristics [1][2] (continued)

Unless otherwise stated **PLL_V_{DD} = 3.3V, D_V_{DD} = 3.3V, BB_V_{DD} = 1.8V, A_V_{DD} = 3.3V, LS_V_{DD} = 3.3V.** The following specifications apply for the circuit shown in Figure 2 unless otherwise stated. Limits apply for 25°C.

Symbol	Parameter	Conditions	LM49370		Units
			Typical[3]	Limit[4] [5]	
	Earpiece Audio Path Gain	Minimum Gain from AUX input, BOOST OFF	–40.5		dB
		Maximum Gain from AUX input, BOOST OFF	6		dB
		Minimum Gain from CPI input	–28.5		dB
		Maximum Gain from CPI input	18		dB
		Minimum Gain from MIC input using SIDETONE path w/ VCR_{MIC} gain = 6dB	–18		dB
		Maximum Gain from MIC input using SIDETONE path w/ VCR_{MIC} gain = 6dB	12		dB
	AUXOUT Audio Path Gain	Minimum Gain from AUX input, BOOST OFF	–46.5		dB
		Maximum Gain from AUX input, BOOST OFF	0		dB
		Minimum Gain from CPI input	–34.5		dB
		Maximum Gain from CPI input	12		dB
	CPOUT Audio Path Gain	Minimum Gain from AUX input, BOOST OFF	–46.5		dB
		Maximum Gain from AUX input, BOOST OFF	0		dB
		Minimum Gain from MIC input	6		dB
		Maximum Gain from MIC input	36		dB
Total DC Power Dissipation					
	Digital Playback Mode Power Dissipation	DAC (f_S = 48kHz) and HP ON			
		f_{MCLK} = 12MHz, PLL OFF	56		mW
		f_{MCLK} = 13MHz, PLL ON f_{PLLOUT} = 12MHz	71		mW
	Analog Playback Mode Power Dissipation	AUX Inputs selected and HP ON			
		f_{MCLK} = 13MHz, PLL OFF	22		mW
	VOICE CODEC Mode Power Dissipation	PCM DAC (f_S = 8kHz) + ADC (f_S = 8kHz) and EP ON			
		f_{MCLK} = 13MHz, PLL OFF	46		mW
	VOICE Module Mode Power Dissipation	CP IN selected. EP and CPOUT ON			
		f_{MCLK} = 13MHz, PLL OFF	27		mW

System Control

Method 1. I²C Compatible Interface

I²C SIGNALS

In I²C mode the LM49370 pin SCL is used for the I²C clock SCL and the pin SDA is used for the I²C data signal SDA. Both these signals need a pull-up resistor according to I²C specification. The I²C slave address for LM49370 is **0011010_2**.

I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW.

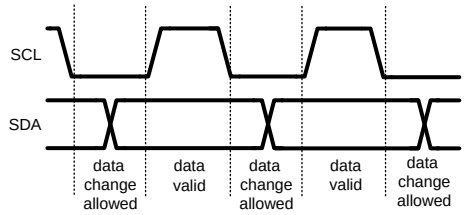
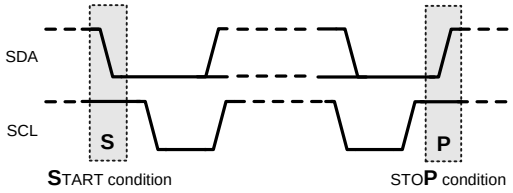


Figure 4. I²C Signals: Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eight bit which is a data direction bit (R/W). The LM49370 address is **0011010_2**. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

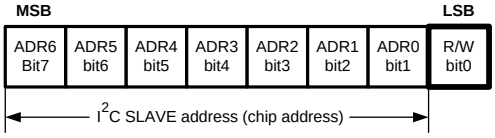
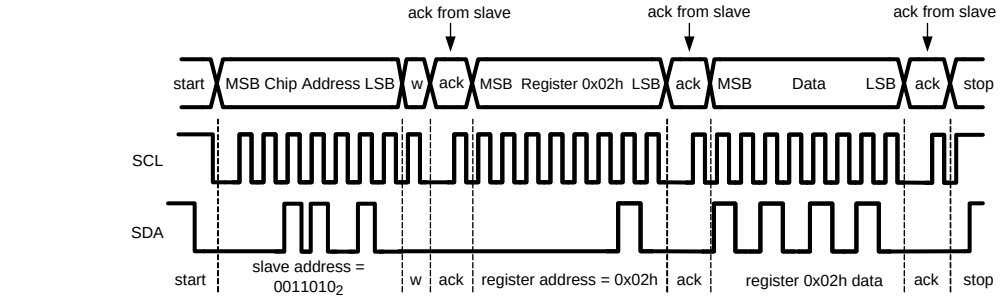


Figure 5. I²C Chip Address

Register changes take an effect at the SCL rising edge during the last ACK from slave.



w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled down by slave)
rs = repeated start

Figure 6. Example I^{2}C Write Cycle

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.

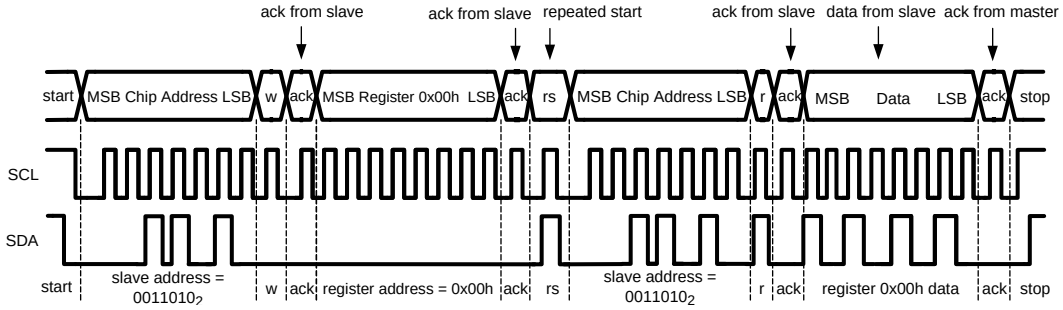


Figure 7. Example I^{2}C Read Cycle

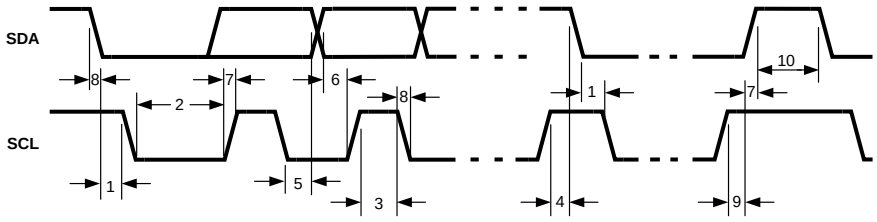


Figure 8. I^{2}C Timing Diagram

I^{2}C TIMING PARAMETERS

Symbol	Parameter[1]	Limit		Units
		Min	Max	
1	Hold Time (repeated) START Condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns

(1) Data specified by design

5	Data Hold Time (Output direction, delay generated by LM49370)	300	900	ns
5	Data Hold Time (Input direction, delay generated by the Master)	0	900	ns
6	Data Setup Time	100		ns
7	Rise Time of SDA and SCL	$20+0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15+0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condition	1.3		µs
C_b	Capacitive Load for Each Bus Line	10	200	pF

Method 2. SPI/Microwire Control/3–wire Control

The LM49370 can be controlled via a three wire interface consisting of a clock, data and an active low chip_select. To use this control method connect SPI_MODE to BB_V_{DD} and use TEST_MODE/$\overline{CS}$ as the chip_select as follows:

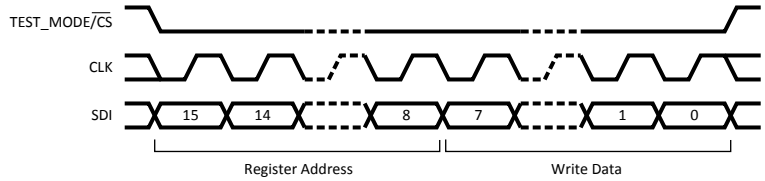


Figure 9. SPI Write Transaction

If the application requires read access to the register set; for example to determine the cause of an interrupt request, the GPIO2 pin can be configured as an SPI format serial data output by setting the GPIO_SEL in the GPIO configuration register (0x1Ah) to SPI_SDO. To perform a read rather than a write to a particular address the MSB of the register address field is set to a 1, this effectively mirrors the contents of the register field to read-only locations above 0x80h:

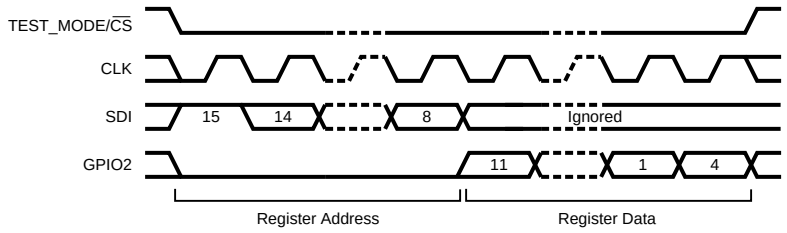


Figure 10. SPI Read Transaction

Figure 11. Three Wire Mode Write Bus Timing

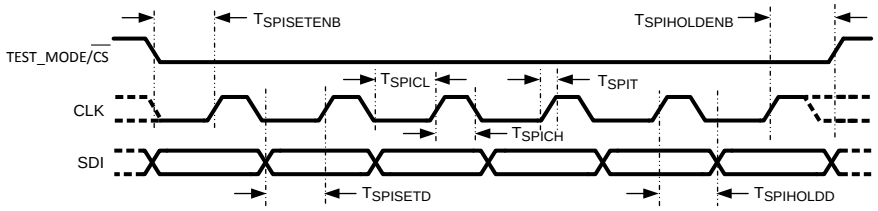


Figure 12. SPI Timing

Status & Control Registers

Table 1. Register Map(1)

Address	Register	7	6	5	4	3	2	1	0
0x00h	Table 2 BASIC	DAC_ MODE		CAP_SIZE		OSC_ENB	PLL_ENB	CHP_MODE	
0x01h	Table 3 CLOCKS	R_DIV						DAC_CLK_SEL	
0x02h		FORCERQ	PLL_M						
0x03h	PLL_N	PLL_N							
0x04h	PLL_P	VCOFATS	Q_DIV			PLL_P			
0x05h	PLL_MOD	PLLTEST	PLL_CLK_SEL		PLL_N_MOD				
0x06h	ADC_1	HPF_MODE		SAMPLE_RATE		RIGHT	LEFT	CPI	MIC
0x07h	ADC_2	NGZXDD	ADC_CLK_SEL		PEAKTIME			ADC MUTE	ADC _MODE
0x08h	AGC_1	NOISE_GATE_THRESHOLD			NG_ENB	AGC_TARGET			AGC_ENB
0x09h	AGC_2	AGC _TIGHT	AGC_DECAY			AGC_MAX_GAIN			
0x0Ah	AGC_3	AGC_ATTACK			AGC_HOLD_TIME				
0x0Bh	MIC_1		INT_EXT	SE_DIFF	MUTE	PREAMP_GAIN			
0x0Ch	MIC_2			BTN_DEBOUNCE_TIME		BTNTYPE	MIC_BIAS_VOLTAGE		VCMVOLT
0x0Dh	SIDETONE					SIDETONE_ATTEN			
0x0Eh	CP_INPUT			MUTE	CPI_LEVEL				
0x0Fh	AUX_LEFT	AUX_DAC	MUTE	BOOST	AUX_LEFT_LEVEL				
0x10h	AUX_RIGHT	AUX_DAC	MUTE	BOOST	AUX_RIGHT_LEVEL				
0x11h	DAC	USAXLVL	DACMUTE	BOOST	DAC_LEVEL				
0x12h	CP_OUTPUT				MICGATE	MUTE	LEFT	RIGHT	MIC
0x13h	AUX OUTPUT					MUTE	LEFT	RIGHT	CPI
0x14h	LS_OUTPUT					MUTE	LEFT	RIGHT	CPI
0x15h	HP_OUTPUT		OCL	STEREO	MUTE	LEFT	RIGHT	CPI	SIDE
0x16h	EP_OUTPUT				MUTE	LEFT	RIGHT	CPI	SIDE
0x17h	DETECT		HS_DBNC_TIME				TEMP_INT	BTN_INT	DET_INT
0x18h	STATUS		GPIN1	GPIN2	TEMP	BTN	MIC	STEREO	HEADSET
0x19h	3D	CUST _COMP	ATTENUATE	FREQ		LEVEL		MODE	3DENB
0x1Ah	I2SMODE	WORD_ ORDER	I2S_WS_GEN_MODE		WS_MS	STEREO REVERSE	I2S_MOD E	INENB	OUTENB
0x1Bh	I2SCLOCK	PCM_SYNC__WIDTH		I2S_CLOCK_GEN_MODE				CLKSCE	CLK_MS
0x1Ch	PCMMODE	ALAW/µLA W	COMPAND	SDO_ LSB_HZ	SYNC_MS	CLKSRCE	CLK_MS	INENB	OUTENB
0x1Dh	PCMCLOCK		PCM_SYNC_GEN_MODE			PCM_CLOCKGEN MODE			
0x1Eh	BRIDGE	MONO_SUM_MODE		MONO_ SUM_SEL	DAC_TX_SEL		I2S_TX_SEL		PCM_ TX_SEL
0x1Fh	GPIO	DAC_SRC_ MODE	ADC_SRC_ MODE	GPIO_2_SEL			GPIO_1_SEL		
0x20h	CMP_0_LSB	CMP_0_LSB							
0x21h	CMP_0_0SB	CMP_0_MSB							
0x22h	CMP_1_LSB	CMP_1_LSB							
0x23h	CMP_1_MSB	CMP_1_MSB							
0x24h	CMP_2_LSB	CMP_2_LSB							
0x25h	CMP_2_MSB	CMP_2_MSB							

(1) The default value of all I2C registers is 0x00h.

BASIC CONFIGURATION REGISTER

This register is used to control the basic function of the chip.

Table 2. BASIC (0x00h)

Bits	Field	Description		
1:0	CHIP_MODE	The LM49370 can be placed in one of four modes which dictate its basic operation. When a new mode is selected the LM49370 will change operation silently and will re-configure the power management profile automatically. The modes are described as follows:		
		CHIP MODE	Audio System	Typical Application
		00_2	Off	Power-down Mode
		01_2	Off	Stand-by mode with headset event detection
		10_2	On	Active without headset event detection
		11_2	On	Active with headset event detection
2	PLL_ENABLE	This enables the PLL.		
3	USE_OSC	If set the power management and control circuits will assume that no external clock is available and will resort to using an on-chip oscillator for headset detection and analog power management functions such as click and pop. The PLL, ADC, and DAC are not wired to use this low quality clock. This bit must be cleared for the part to be fully turned off power-down mode.		
5:4	CAP_SIZE	This programs the extra delays required to stabilize once charge/discharge is complete, based on the size of the bypass capacitor.		
		CAP_SIZE	Bypass Capacitor Size	Turn-off/on time
		00_2	0.1 µF	45 ms/75 ms
		01_2	1 µF	45 ms/140 ms
		10_2	2.2 µF	45 ms/260 ms
		11_2	4.7 µF	45 ms/500 ms
7:6	DAC_MODE	The DAC can operate in one of four modes. If an "fs*$2^{\Delta N}$" audio clock is available, then the DAC can be run in a slightly lower power mode. If such a clock is not available, the PLL can be used to generate a suitable clock.		
		DAC MODE	DAC OSR	Typical Application
		00_2	125	48kHz Playback from 12.000MHz
		01_2	128	48kHz Playback from 12.288MHz
		10_2	64	96kHz Playback from 12.288MHz
		11_2	32	192kHz Playback from 24.576MHz

For reliable headset / push button detection the following bits should be defined before enabling the headset detection system by setting bit 0 of CHIP_MODE:

The OCL-bit (Cap / Capless headphone interface; bit 6 of HP_OUTPUT (0x15h))

The headset insert/removal debounce settings (bits 6:3 of DETECT (0x17h))

The BTN_TYPE-bit (Parallel / Series push button type; bit 3 MIC_2 register (0x0Ch))

The parallel push button debounce settings (bits 5:4 of MIC_2 register (0x0Ch))

All register fields controlling the audio system should be defined before setting bit 1 of CHIP_MODE and should not be altered while the audio sub-system is active.

If the analog or digital levels are below −12dB then it is not necessary to set the stereo bit allowing greater output levels to be obtained for such signals.

CLOCKS CONFIGURATION REGISTER

This register is used to control the clocks throughout the chip.

Table 3. CLOCKS (0x01h)

Bits	Field	Description	
1:0	DAC_CLK	This selects the clock to be used by the audio DAC system.	
		DAC_CLK	DAC Input Source
		00_2	MCLK
		01_2	PLL_OUTPUT
		10_2	I2S_CLK_IN
		11_2	PCM_CLK_IN
7:2	R_DIV	This programs the R divider.	
		R_DIV	Divide Value
		0	Bypass
		1	Bypass
		2	1.5
		3	2
		4	2.5
		5	3
		6	3.5
		7	4
		8	4.5
		9	5
		10	5.5
		11	6
		12	6.5
		13 to 61	7 to 31
		62	31.5
		63	32

LM49370 CLOCK NETWORK

The audio ADC operates at 125*fs (or 128*fs), so it requires a 1.000 MHz (or 1.024MHz) clock to sample at 8 kHz (at point **C** as marked on the following diagram). If the stereo DAC is running at 125*fs (or128*fs), it requires a 12.000MHz (or 12.288MHz) clock (at point **B**) for 48 kHz data. It is expected that the PLL is used to drive the audio system operating at 125*fs unless a 12.000 MHz master clock is supplied or the sample rate is always a multiple of 8 kHz. In this case the PLL can be bypassed to reduce power, with clock division being performed by the Q and R dividers instead. The PLL can also be bypassed if the system is running at 128*fs and a 12.288MHz master clock is supplied and the sample rate is a multiple of 8kHz. The PLL can also use the I^2S clock input as a source. In this case, the audio DAC uses the clock from the output of the PLL and the audio ADC either uses the PLL output divided by $2*F_{S(DAC)}/F_{S(ADC)}$ or a system clock divided by Q, this allows n*8 kHz recording and 44.1 kHz playback.

MCLK must be less than or equal to 30 MHz. I2S_CLK and PCM_CLK should be below 6.144MHz.

When operating at 125*fs, the LM49370 is designed to work from a 12.000 MHz or 11.025 MHz clock at point **A**. When operating at 128*fs, the LM49370 is designed to work from a 12.288MHz or 11.2896 MHz clock at point A. This is used to drive the power management and control logic. Performance may not meet the electrical specifications if the frequency at this point deviates significantly beyond this range.

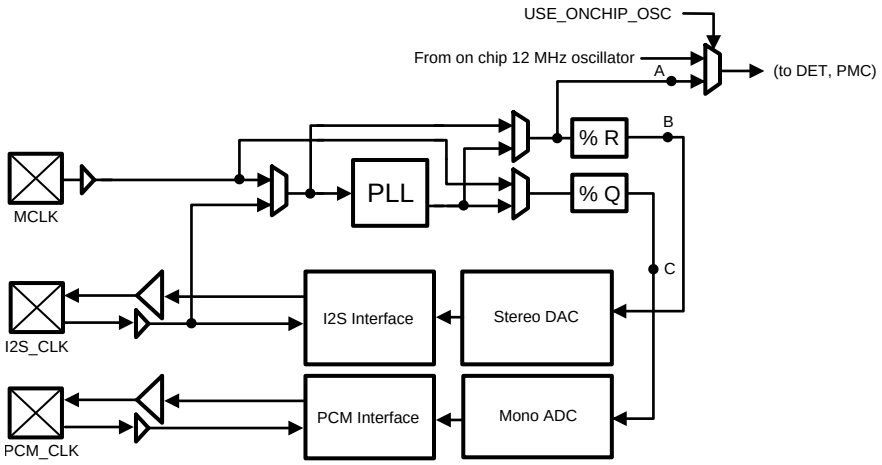


Figure 13. LM49370 Clock Network

COMMON CLOCK SETTINGS FOR THE DAC & ADC

When DAC_MODE = '00' (bits 7:6 of (0x00h)), the DAC has an over sampling ratio of 125 but requires a 250*fs clock at point **B**. This allows a simple clocking solution as it will work from 12.000 MHz (common in most systems with Bluetooth or USB) at 48 kHz exactly, the following table describes the clock required at point **B** for various clock sample rates in the different DAC modes:

Table 4. Common DAC Clock Frequencies

DAC Sample Rate (kHz)	Clock Required at B (OSR = 125)	Clock Required at B (OSR = 128)
8	2 MHz	2.048 MHz
11.025	2.75625 MHz	2.8224 MHz
12	3 MHz	3.072 MHz
16	4 MHz	4.096 MHz
22.05	5.5125 MHz	5.6448 MHz
24	6 MHz	6.144 MHz
32	8 MHz	8.192 MHz
44.1	11.025 MHz	11.2896 MHz
48	12 MHz	12.288 MHz

NOTE

When DAC_MODE = '01' with the I^2S or PCM interface operating as master, the stereo DAC operates at half the frequency of the clock at point B. This divided by two DAC clock is used as the source clock for the audio port.

The over sampling ratio of the ADC is set by ADC MODE (bit 0 of 0x07h)). The table below shows the required clock frequency at point **C** for the different ADC modes.

Table 5. Common ADC Clock Frequencies

ADC Sample Rate (kHz)	Clock Required at C (OSR = 125)	Clock Required at C (OSR = 128)
8	1 MHz	1.024 MHz
11.025	1.378125 MHz	1.4112 MHz
12	1.5 MHz	1.536 MHz
16	2 MHz	2.048 MHz
22.05	2.75625 MHz	2.8224 MHz
24	3 MHz	3.072 MHz

Methods for producing these clock frequencies are described in the PLL Section.

PLL M DIVIDER CONFIGURATION REGISTER

This register is used to control the input section of the PLL.

Table 6. PLL_M (0x02h)(1)

Bits	Field	Description	
0	RSVD	RESERVED	
6:0	PLL_M	PLL_M	Input Divider Value
		0	No Divided Clock
		1	1
		2	1.5
		3	2
		4	2.5
		...	3 to 63
		126	63.5
		127	64
7	FORCERQ	If set, the R and Q divider are enabled and the DAC and ADC clocks are propagated. This allows operation of the I^2S and PCM interfaces without the ADC or DAC being enabled, for example to act as a bridge or a clock master.	

(1) See Further Notes on PLL Programming for more detail.

The M divider should be set such that the output of the divider is between 0.5 MHz and 5 MHz.

The division of the M divider is derived from PLL_M such that:

M = (PLL_M + 1) / 2

PLL N DIVIDER CONFIGURATION REGISTER

This register is used to control the feedback divider of the PLL.

Table 7. PLL_N (0x03h)(1)

Bits	Field	Description	
7:0	PLL_N	This programs the PLL feedback divider as follows:	
		PLL_N	Feedback Divider Value
		0 to 10	10
		11	11
		12	12
		13	13
		14	14
		…	…
		249	249
		250 to 255	250

(1) See Further Notes on PLL Programming for further details.

The N divider should be set such that the output of the divider is between 0.5 MHz and 5 MHz. (Fin/M)*N will be the target resting VCO frequency, F_{VCO}. The N divider should be set such that 40 MHz < (Fin/M)*N < 60 MHz. Fin/M is often referred to as F_{comp} (comparison frequency) or F_{ref} (reference frequency), in this document F_{comp} is used.

The integer division of the N divider is derived from PLL_N such that:

For 9 < PLL_N < 251: N = PLL_N

PLL P DIVIDER CONFIGURATION REGISTER

This register is used to control the output divider of the PLL.

Table 8. PLL_P (0x04h)(1)

Bits	Field	Description	
3:0	PLL_P	This programs the PLL output divider as follows:	
		PLL_P	Output Divider Value
		0	No Divided Clock
		1	1
		2	1.5
		3	2
		4	2.5
		...	3 to 7
		14	7.5
		15	8
6:4	Q_DIV	This programs the Q Divider	
		Q_DIV	Divide Value
		000_2	2
		001_2	3
		010_2	4
		011_2	6
		100_2	8
		101_2	10
		110_2	12
		111_2	13
7	FAST_VCO	This programs the PLL VCO range:	
		FAST_VCO	PLL VCO Range
		0	40 to 60MHz
		1	60 to 80MHz

(1) See Further Notes on PLL Programming for more details.

The division of the P divider is derived from PLL_P such that:

P = (PLL_P + 1) / 2

PLL N MODULUS CONFIGURATION REGISTER

This register is used to control the modulation applied to the feedback divider of the PLL.

Table 9. PLL_N_MOD (0x05h)(1)

Bits	Field	Description	
4:0	PLL_N_MOD	This programs the PLL N divider's fractional component:	
		PLL_N_MOD	Fractional Addition
		0	0/32
		1	1/32
		2 to 30	2/32 to 30/32
		31	31/32
6:5	PLL_CLK_SEL	This selects the clock to be used as input for the audio PLL.	
		PLL_INPUT_CLK	
		00_2	MCLK
		01_2	I2S_CLK_IN
		10_2	PCM_CLK_IN
		11_2	—
7	RSVD	Reserved.	

(1) See Further Notes on PLL Programming for more details.

The complete N divider is a fractional divider as such:

$N = PLL\_N + PLL\_N\_MOD/32$

If the modulus input is zero then the N divider is simply an integer N divider. The output from the PLL is determined by the following formula:

$F_{out} = (F_{in}*N)/(M*P)$

FURTHER NOTES ON PLL PROGRAMMING

The sigma-delta PLL Is designed to drive audio circuits requiring accurate clock frequencies of up to 30MHz with frequency errors noise-shaped away from the audio band. The 5 bits of modulus control provide exact synchronization of 48kHz and 44.1kHz sample rates from any common system clock. In systems where an isochronous I^2S data stream is the source of data to the DAC a clock synchronous to the sample rate should be used as input to the PLL (typically the I^2S clock). If no isochronous source is available, then the PLL can be used to obtain a clock that is accurate to within 1Hz of the correct sample rate although this is highly unlikely to be a problem.

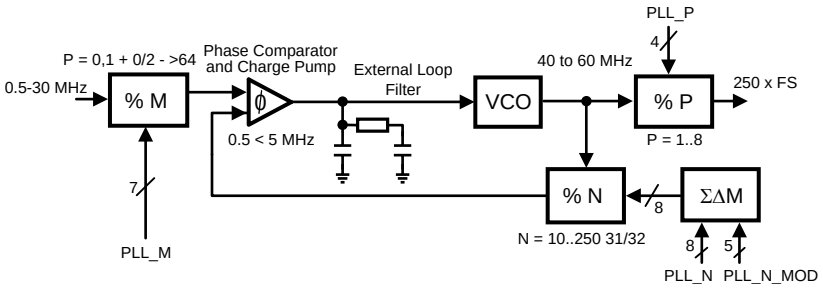


Figure 14. PLL Overview

Table 10. Example PLL Settings for 48 kHz and 44.1 kHz Sample Rates in DAC MODE 00

F_{in} (MHz)	F_S (kHz)	M	N	P	PLL_M	PLL_N	PLL_N_MOD	PLL_P	F_{out} (MHz)
11	48	11	60	5	21	60	0	9	12
12.288	48	4	19.53125	5	7	19	17	9	12
13	48	13	60	5	25	60	0	9	12
14.4	48	9	37.5	5	17	37	16	9	12
16.2	48	27	100	5	53	100	0	9	12
16.8	48	14	50	5	27	50	0	9	12
19.2	48	13	40.625	5	25	40	20	9	12
19.44	48	27	100	6	53	100	0	11	12
19.68	48	20.5	62.5	5	40	62	16	9	12
19.8	48	16.5	50	5	32	50	0	9	12
11	44.1	11	55.125	5	21	55	4	9	11.025
11.2896	44.1	8	39.0625	5	15	39	2	9	11.025
12	44.1	5	22.96875	5	9	22	31	9	11.025
13	44.1	13	55.125	5	25	55	4	9	11.025
14.4	44.1	12	45.9375	5	23	45	30	9	11.025
16.2	44.1	9	30.625	5	17	9	20	9	11.025
16.8	44.1	17	55.78125	5	33	30	25	9	11.025
19.2	44.1	16	45.9375	5	31	45	30	9	11.025
19.44	44.1	13.5	38.28125	5	26	38	9	9	11.025
19.68	44.1	20.5	45.9375	4	40	45	30	7	11.025
19.8	44.1	11	30.625	5	21	30	20	9	11.025

Table 11. Example PLL Settings for 48 kHz and 44.1 kHz Sample Rates in DAC MODE 01

F_{in} (MHz)	F_s (kHz)	M	N	P	PLL_M	PLL_N	PLL_N_MOD	PLL_P	F_{out} (MHz)
12	48	12.5	64	5	24	64	0	9	12.288
13	48	26.5	112.71875	4.5	52	112	23	8	12.288
14.4	48	37.5	128	4	74	128	0	7	12.288
16.2	48	37.5	128	4.5	74	128	0	8	12.288
16.8	48	12.53	32	3.5	24	32	0	6	12.288
19.2	48	12.5	32	4	24	32	0	7	12.288
19.44	48	40.5	128	58	80	128	0	9	12.288
19.68	48	20.5	64	5	40	64	0	9	12.288
19.8	48	37.5	128	5.5	74	128	0	10	12.288
12	44.1	35.5	133.59375	4	70	133	19	7	11.2896
13	44.1	37	144.59375	4.5	73	144	19	8	11.2896
14.4	44.1	37.5	147	5	74	147	0	9	11.2896
16.2	44.1	47.5	182.0625	5.5	94	182	2	10	11.2896
16.8	44.1	12.5	42	5	24	42	0	9	11.2896
19.2	44.1	12.5	36.75	5	24	36	24	9	11.2896
19.44	44.1	37.5	98	4.5	74	98	0	9	11.2896
19.68	44.1	44.5	114.875	4.5	88	114	28	8	11.2896
19.8	44.1	48	136.84375	5	95	136	27	9	11.2896

These tables cover the most common applications, obtaining clocks for derivative sample rates such as 22.05 kHz should be done by increasing the P divider value or using the R/Q dividers.

An example of obtaining 12.000 MHz from 1.536 MHz is shown below (this is typical for deriving DAC clocks from I2S datastreams).

Choose a small range of P so that the VCO frequency is swept between 40 MHz and 60 MHz (or 60–80 MHz if VCOFAST is used). Remembering that the P divider can divide by half integers, for a 12 MHz output, this gives possible P values of 3, 3.5, 4, 4.5, or 5. The M divider should be set such that the comparison frequency (Fcomp) is between 0.5 and 5 MHz. This gives possible M values of 1, 1.5, 2, 2.5, or 3. The most accurate N and N_MOD can be calculated by sweeping the P and M inputs of the following formulas:

N = FLOOR{[(Fout/Fin)*(P*M)],1}

N_MOD = ROUND{32*[((Fout)/Fin)*(P*M)-N],0}

This shows that setting M = 1, N = 39+1/16, P = 5 (i.e. PLL_M = 0, PLL_N = 39, PLL_N_MOD = 2, & PLL_P = 4) gives a comparison frequency of 1.536MHz, a VCO frequency of 60 MHz and an output frequency of 12.000 MHz. The same settings can be used to get 11.025 from 1.4112 MHz for 44.1 kHz sample rates.

Care must be taken when synchronization of isochronous data is not possible, i.e. when the PLL has to be used but an exact frequency match cannot be found. The I2S should be master on the LM49370 so that the data source can support appropriate SRC as required. This method should only be used with data being read on demand to eliminate sample rate mismatch problems.

Where a system clock exists at an integer multiple of the required ADC or DAC clock rate it is preferable to use this rather than the PLL. The LM49370 is designed to work in 8, 12, 16, 24, 48 kHz modes from a 12 MHz clock and 8 kHz modes from a 13 MHz clock without the use of the PLL. This saves power and reduces clock jitter which can affect SNR.

PLL Loop Filter

LM49370 requires a second or third order loop filter on PLL_FILT pin. LM49370 demoboard schematic has the recommended values to use for the second order filter. Please refer to the LM49370 demoboard schematic.

ADC_1 CONFIGURATION REGISTER

This register is used to control the LM49370's audio ADC.

Table 12. ADC_1 (0x06h)

Bits	Field	Description	
0	MIC_SELECT	If set the microphone preamp output is added to the ADC input signal.	
1	CPI_SELECT	If set the cell phone input is added to the ADC input signal.	
2	LEFT_SELECT	If set the left stereo bus is added to the ADC input signal.	
3	RIGHT_SELECT	If set the right stereo bus is added to the ADC input signal.	
5:4	ADC_SAMPLE_RATE	This programs the closest expected sample rate of the mono ADC, which is a variable required by the AGC algorithm whenever the AGC is in use. This does not set the sample rate of the mono ADC.	
		ADC_SAMPLE_RATE	Sample Rate
		00_2	8 kHz
		01_2	12 kHz
		10_2	16 kHz
		11_2	24 kHz
7:6	HPF_MODE	This sets the HPF of the ADC	
		HPF-MODE	HPF Response
		00_2	No HPF
		01_2	F_S = 8 kHz, −0.5 dB @ 300 Hz, Notch @ 55 Hz F_S = 12 kHz, −0.5 dB @ 450 Hz, Notch @ 82 Hz F_S = 16 kHz, −0.5 dB @ 600 Hz, Notch @ 110 Hz
		10_2	F_S = 8 kHz, −0.5 dB @ 150 Hz, Notch @ 27 Hz F_S = 12 kHz, −0.5 dB @ 225 Hz, Notch @ 41 Hz F_S = 16 kHz, −0.5 dB @ 300 Hz, Notch @ 55 Hz
		11_2	No HPF

ADC_2 CONFIGURATION REGISTER

This register is used to control the LM49370's audio ADC.

Table 13. ADC_2 (0x07h)

Bits	Field	Description	
0	ADC_MODE	This sets the oversampling ratio of the ADC	
		MODE	ADC OSR
		0	125fs
		1	128fs
1	ADC_MUTE	If set, the analog inputs to the ADC are muted.	

Table 13. ADC_2 (0x07h) (continued)

Bits	Field	Description	
4:2	AGC_FRAME_TIME	This sets the frame time to be used by the AGC algorithm. In a given frame, the AGC's peak detector determines the peak value of the incoming microphone audio signal and compares this value to the target value of the AGC defined by AGC_TARGET (bits [3:1] of register (0x08h)) in order to adjust the microphone preamplifier's gain accordingly. AGC_FRAME_TIME basically sets the sample rate of the AGC to adjust for a wide variety of speech patterns. (1)	
		AGC_FRAME_TIME	Time (ms)
		000_2	96
		001_2	128
		010_2	192
		011_2	256
		100_2	384
		101_2	512
		110_2	768
		111_2	1000
6:5	ADC_CLK	This selects the clock to be used by the audio ADC system.	
		ADC_CLK	Source
		00_2	MCLK
		01_2	PLL_OUTPUT
		10_2	I2S_CLK_IN
		11_2	PCM_CLK_IN
7	NGZXDD	If set, the noise gate will not wait for a zero crossing before mute/unmuting. This bit should be set if the ADC's HPF is disabled and if there is a large DC or low frequency component at the ADC input.	
		NGZXDD	Result
		0	Noise Gate operates on ZXD events
		1	Noise Gate operates on frame boundaries

(1) Refer to the AGC Overview for further detail.

AGC_1 CONFIGURATION REGISTER

This register is used to control the LM49370's Automatic Gain Control. (2)

Table 14. AGC_1 (0x08h)

Bits	Field	Description	
0	AGC_ENABLE	If set, the AGC controls the analog microphone preamplifier gain into the system. This feature is useful for microphone signals that are routed to the ADC.	
3:1	AGC_TARGET	This programs the target level of the AGC. This will depend on the expected transients and desired headroom. Refer to AGC_TIGHT (bit 7 of 0x09h) for more detail.	
		AGC_TARGET	Target Level
		000_2	−6 dB
		001_2	−8 dB
		010_2	−10 dB
		011_2	−12 dB
		100_2	−14 dB
		101_2	−16 dB
		110_2	−18 dB
		111_2	−20 dB
4	NOISE_GATE_ON	If set, signals below the noise gate threshold are muted. The noise gate is only activated after a set period of signal absence.	

(2) See the AGC Overview.

Table 14. AGC_1 (0x08h) (continued)

Bits	Field	Description	
7:5	NOISE_ GATE_ THRES	This field sets the expected background noise level relative to the peak signal level. The sole presence of signals below this level will not result in an AGC gain change of the input and will be gated from the ADC output if the NOISE_GATE_ON is set. This level must be set even if the noise gate is not in use as it is required by the AGC algorithm.	
		NOISE_GATE_THRES	Level
		000_2	−72 dB
		001_2	−66 dB
		010_2	−60 dB
		011_2	−54 dB
		100_2	−48 dB
		101_2	−42 dB
		110_2	−36 dB
		111_2	−30 dB

AGC_2 CONFIGURATION REGISTER

This register is used to control the LM49370's Automatic Gain Control.

Table 15. AGC_2 (0x09h)

Bits	Field	Description	
3:0	AGC_MAX_GAIN	This programs the maximum gain that the AGC algorithm can apply to the microphone preamplifier.	
		AGC_MAX_GAIN	Max Preamplifier Gain
		0000_2	6 dB
		0001_2	8 dB
		0010_2	10 dB
		0011_2	12 dB
		0100_2 to 1100_2	14 dB to 30 dB
		1101_2	32 dB
		1110_2	34 dB
		1111_2	36 dB
6:4	AGC_DECAY	This programs the speed at which the AGC will increase gains if it detects the input level is a quiet signal.	
		AGC_DECAY	Step Time (ms)
		000_2	32
		001_2	64
		010_2	128
		011_2	256
		100_2	512
		101_2	1024
		110_2	2048
		111_2	4096

Table 15. AGC_2 (0x09h) (continued)

Bits	Field	Description		
7	AGC_TIGHT	If set, the AGC algorithm controls the microphone preamplifier more exactly. (1)		
	AGC_TIGHT = 0	AGC_TARGET	Min Level	Max Level
		000_2	−6 dB	−3 dB
		001_2	−8 dB	−4 dB
		010_2	−10 dB	−5 dB
		011_2	−12 dB	−6 dB
		100_2	−14 dB	−7 dB
		101_2	−16 dB	−8 dB
		110_2	−18 dB	−9 dB
		111_2	−20 dB	−10 dB
	AGC_TIGHT = 1	000_2	−6 dB	−3 dB
		001_2	−8 dB	−5 dB
		010_2	−10 dB	−7 dB
		011_2	−12 dB	−9 dB
		100_2	−14 dB	−11 dB
		101_2	−16 dB	−13 dB
		110_2	−18 dB	−15 dB
		111_2	−20 dB	−17 dB

(1) The AGC can be used to control the analog path of the microphone to the output stages or to optimize the microphone path for recording on the ADC. When the analog path is used this bit should be set to ensure the target is tightly adhered to. If the ADC is the only destination of the microphone or the desired analog mixer level is line level then AGC_TIGHT should be cleared, allowing greater dynamic rage of the recorded signal. For further details see the AGC Overview.

AGC_3 CONFIGURATION REGISTER

This register is used to control the LM49370's Automatic Gain Control. (2)

Table 16. AGC_3 (0x0Ah)

Bits	Field	Description	
4:0	AGC_HOLDTIME	This programs the amount of delay before the AGC algorithm begins to adjust the gain of the microphone preamplifier.	
		AGC_HOLDTIME	No. of speech segments
		00000_2	0
		00001_2	1
		00010_2	2
		00011_2	3
		00100_2 to 11100_2	4 to 28
		11101_2	29
		11110_2	30
		11111_2	31

(2) See the AGC Overview.

Table 16. AGC_3 (0x0Ah) (continued)

Bits	Field	Description	
7:5	AGC_ATTACK	This programs the speed at which the AGC will reduce gains if it detects the input level is too large.	
		AGC_ATTACK	Step Time (ms)
		000_2	32
		001_2	64
		010_2	128
		011_2	256
		100_2	512
		101_2	1024
		110_2	2048
		111_2	4096

AGC OVERVIEW

The Automatic Gain Control (AGC) system can be used to optimize the dynamic range of the ADC for voice data when the level of the source is unknown. A target level for the output is set so that any transients on the input won't clip during normal operation. The AGC circuit then compares the output of the ADC to this level and increases or decreases the gain of the microphone preamplifier to compensate. If the audio from the microphone is to be output digitally through the ADC then the full dynamic range of the ADC can be used automatically. If the output is through the analog mixer then the ADC is used to monitor the microphone level. In this case, the analog dynamic range is less important than the absolute level, so *AGC_TIGHT* should be set to tie transients closely to the target level.

To ensure that the system doesn't reduce the quality of the speech by constantly modulating the microphone preamplifier gain, the ADC output is passed through an envelope detector. This frames the output of the ADC into time segments roughly equal to the phonemes found in speech *(AGC_FRAME_TIME)*. To calculate this, the circuit must also know the sample rate of the data from the ADC *(ADC_SAMPLERATE)*. If after a programmable number of these segments *(AGC_HOLDTIME)*, the level is consistently below target, the gain will be increased at a programmable rate *(AGC_DECAY)*. If the signal ever exceeds the target level (AGC_TARGET) then the gain of the microphone is reduced immediately at a programmable rate *(AGC_ATTACK)*. This is demonstrated below:

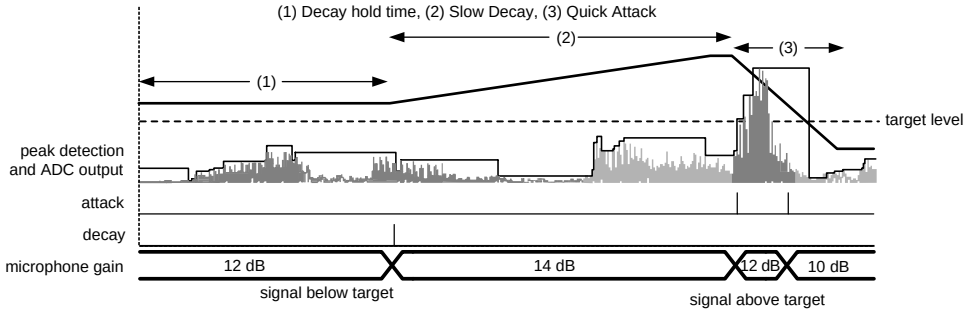


Figure 15. AGC Operation Example

The signal in the above example starts with a small analog input which, after the hold time has timed out, triggers a rise in the gain [(1) → (2)]. After some time the real analog input increases and it reaches the threshold for a gain reduction which decreases the gain at a faster rate [(2) → (3)] to allow the elimination of typical popping noises.

Only ADC outputs that are considered signal (rather than noise) are used to adjust the microphone preamplifier gain. The signal to noise ratio of the expected input signal is set by *NOISE_GATE_THRESHOLD*. In some situations it is preferable to remove audio considered to be consisting solely of background noise from the audio output; for example conference calls. This can be done by setting *NOISE_GATE_ON*. This does not affect the performance of the AGC algorithm.

The AGC algorithm should not be used where very large background noise is present. If the type of input data, application and microphone is known then the AGC will typically not be required for good performance, it is intended for use with inputs with a large dynamic range or unknown nominal level. When setting *NOISE_GATE_THRESHOLD* be aware that in some mobile phone scenarios the ADC SNR will be dictated by the microphone performance rather than the ADC or the signal. Gain changes to the microphone are performed on zero crossings. To eliminate DC offsets, wind noise, and pop sounds from the output of the ADC, the ADC's HPF should always be enabled.

MIC_1 CONFIGURATION REGISTER

This register is used to control the microphone configuration.

Table 17. MIC_1 (0x0Bh)

Bits	Field	Description	
3:0	PREAMP_GAIN	This programs the gain applied to the microphone preamplifier if the AGC is not in use.	
		PREAMP_GAIN	Gain
		0000_2	6 dB
		0001_2	8 dB
		0010_2	10 dB
		0011_2	12 dB
		0100_2 to 1100_2	14 dB to 30 dB
		1101_2	32 dB
		1110_2	34 dB
		1111_2	36 dB
4	MIC_MUTE	If set, the microphone preamplifier is muted.	
5	INT_SE_DIFF	If set, the internal microphone is assumed to be single ended and the negative connection is connected to the ADC common mode point internally. This allows a single-ended internal microphone to be used.	
6	INT_EXT	If set, the single ended external microphone is used and the negative microphone input is grounded internally, otherwise internal microphone operation is assumed. (1)	

(1) On changing INT_EXT from internal to external note that the dc blocking cap will not be charged so some time should be taken (300ms for a 1µF cap) between the detection of an external headset and the switching of the output stages and ADC to that input to allow the DC points on either side of this cap to stabilize. This can be accomplished by deselecting the microphone input from the audio outputs and ADC until the DC points stabilize. An active MIC path to CPOUT or the ADC may result in the microphone DC blocking caps causing audio pops under the following situations:1) Switching between internal and external microphone operation while in chip modes '10' or '11'.2) Toggling in and out of powerdown/standby modes.3) Toggling between chip modes '10' and '11' whenever external microphone operation is selected.4) The insertion/removal of a headset while in chip modes '10' or '11' whenever external microphone operation is selected. To avoid these potential pop issues, it is recommended to deselect the microphone input from CPOUT and ADC until the DC points stabilize.

MIC_2 CONFIGURATION REGISTER

This register is used to control the microphone configuration.

Table 18. MIC_2 (0x0Ch)

Bits	Field	Description	
0	OCL_ VCM_ VOLTAGE	This selects the voltage used as virtual ground (HP_VMID pin) in OCL mode. This will depend on the available supply and the power output requirements of the headphone amplifiers.	
		OCL_VCM_VOLTAGE	Voltage
		0	1.2V
		1	1.5V

Table 18. MIC_2 (0x0Ch) (continued)

Bits	Field	Description	
2:1	MIC_ BIAS_ VOLTAGE	This selects the voltage as a reference to the internal and external microphones. Only one bias pin is driven at once depending on the INT_EXT bit setting found in the MIC_1 (0x0Bh) register. MIC_BIAS_VOLTAGE should be set to '11' only if A_V_{DD} > 3.4V. In OCL mode, MIC_BIAS_VOLTAGE = '00' (EXT_BIAS = 2.0V) should not be used to generate the EXT_BIAS supply for a cellular headset external microphone. Please refer to Table 19 for more detail.	
		MIC_BIAS_VOLTAGE	EXT_BIAS/INT_BIAS
		00_2	2.0V
		01_2	2.5V
		10_2	2.8V
		11_2	3.3V
3	BUTTON_TYPE	If set, the LM49370 assumes that the button (if used) in the headset is in series (series push button) with the microphone, opening the circuit when pressed. The default is for the button to be in parallel (parallel push button), shorting out the microphone when pressed.	
5:4	BUTTON_ DEBOUNCE_ TIME	This sets the time used for debouncing the pushing of the button on a headset with a parallel push button.	
		BUTTON_DEBOUNCE_TIME	Time (ms)
		00_2	0
		01_2	8
		10_2	16
		11_2	32

In OCL mode there is a trade-off between the external microphone supply voltage (EXT_MIC_BIAS - OCL_VCM_ VOLTAGE) and the maximum output power possible from the headphones. A lower OCL_VCM_VOLTAGE gives a higher microphone supply voltage but a lower maximum output power from the headphone amplifiers due to the lower OCL_VCM_VOLTAGE - A_V_{SS}.

Table 19. External MIC Supply Voltages in OCL Mode

Available A_V_{DD}	Recommended EXT_MIC_BIAS	Supply to Microphone	
		OCL_VCM_VOLT = 1.5V	OCL_VCM_VOLT = 1.2V
> 3.4V	3.3V	1.8V	2.1V
2.9V to 3.4V	2.8V	1.3V	1.6V
2.8V to 2.9V	2.5V	1.0V	1.3V
2.7V to 2.8V	2.5V	-	1.3V

SIDETONE ATTENUATION REGISTER

This register is used to control the analog sidetone attenuation. (1)

Table 20. SIDETONE (0x0Dh)

Bits	Field	Description	
3:0	SIDETONE_ ATTEN	This programs the attenuation applied to the microphone preamp output to produce a sidetone signal.	
		SIDETONE_ATTEN	Attenuation
		0000_2	-Inf
		0001_2	−30 dB
		0010_2	−27 dB
		0011_2	−24 dB
		0100_2	−21 dB
		0101_2 to 1010_2	−18 dB to −3 dB
		1011_2 to 1111_2	0 dB

(1) An active SIDETONE path to an audio output may result in the microphone DC blocking caps causing audio pops under the following situations:1) Switching between internal and external microphone operation while in chip modes '10' or '11'.2) Toggling in and out of powerdown/standby modes.3) Toggling between chip modes '10' and '11' whenever external microphone operation is selected.4) The insertion/removal of a headset while in chip modes '10' or '11' whenever external microphone operation is selected.To avoid potential pop noises, it is recommended to set SIDETONE_ATTEN to '0000' until DC points have stabilized whenever the SIDETONE path is used.

CP_INPUT CONFIGURATION REGISTER

This register is used to control the differential cell phone input.

Table 21. CP_INPUT (0x0Eh)

Bits	Field	Description	
4:0	CPI_LEVEL	This programs the gain/attenuation applied to the cell phone input.	
		CPI_LEVEL	Level
		00000_2	−34.5 dB
		00001_2	−33 dB
		00010_2	−31.5 dB
		00011_2	−30 dB
		00100 to 11100_2	−28.5 dB to +7.5 dB
		11101_2	+9 dB
		11110_2	+10.5 dB
		11111_2	+12 dB
5	CPI_MUTE	If set, the CPI input is muted at source.	

AUX_LEFT CONFIGURATION REGISTER

This register is used to control the left aux analog input.

Table 22. AUX_LEFT (0x0Fh)

Bits	Field	Description		
4:0	AUX_ LEFT_ LEVEL	This programs the gain/attenuation applied to the AUX LEFT analog input to the mixer. (1)		
		AUX_LEFT_LEVEL	Level (With Boost)	Level (Without Boost)
		00000_2	−34.5 dB	−46.5 dB
		00001_2	−33 dB	−45 dB
		00010_2	−31.5 dB	−43.5 dB
		00011_2	−30 dB	−42 dB
		00100 to 11100_2	−28.5 dB to +7.5 dB	−40.5 dB to −4.5 dB
		11101_2	+9 dB	−3 dB
		11110_2	+10.5 dB	−1.5 dB
		11111_2	+12 dB	0 dB
5	AUX_ LEFT_ BOOST	If set, the gain of the AUX_LEFT input to the mixer is increased by 12 dB (see above).		
6	AUX_L_MUTE	If set, the AUX LEFT input is muted.		
7	AUX_OR_DAC_L	If set, the AUX LEFT input is passed to the mixer, the default is for the DAC LEFT output to be passed to the mixer.		

(1) The recommended mixer level is 1V RMS. The auxiliary analog inputs can be boosted by 12 dB if enough headroom is available. Clipping may occur if the analog power supply is insufficient to cater for the required gain.

AUX_RIGHT CONFIGURATION REGISTER

This register is used to control the right aux analog input.

Table 23. AUX_RIGHT (0x10h)

Bits	Field	Description		
4:0	AUX_ RIGHT_ LEVEL	This programs the gain/attenuation applied to the AUX RIGHT analog input to the mixer. (1)		
		AUX_RIGHT_LEVEL	Level (With Boost)	Level (Without Boost)
		00000_2	−34.5 dB	−46.5 dB
		00001_2	−33 dB	−45 dB
		00010_2	−31.5 dB	−43.5 dB
		00011_2	−30 dB	−42 dB
		00100 to 11100_2	−28.5 dB to +7.5 dB	−40.5 dB to −4.5 dB
		11101_2	+9 dB	−3 dB
		11110_2	+10.5 dB	−1.5 dB
		11111_2	+12 dB	0 dB
5	AUX_ RIGHT_BOOST	If set, the gain of the AUX_RIGHT input to the mixer is increased by 12 dB (see above).		
6	AUX_R_MUTE	If set, the AUX RIGHT input is muted.		
7	AUX_OR_DAC_R	If set, the AUX RIGHT input is passed to the mixer, the default is for the DAC RIGHT output to be passed to the mixer.		

(1) The recommended mixer level is 1V RMS. The auxiliary analog inputs can be boosted by 12 dB if enough headroom is available. Clipping may occur if the analog power supply is insufficient to cater for the required gain.

DAC CONFIGURATION REGISTER

This register is used to control the DAC levels to the mixer.

Table 24. DAC (0x11h)

Bits	Field	Description		
4:0	DAC_LEVEL	This programs the gain/attenuation applied to the DAC input to the mixer. (1)		
		DAC_LEVEL	Level (With Boost)	Level (Without Boost)
		00000_2	−34.5 dB	−46.5 dB
		00001_2	−33 dB	−45 dB
		00010_2	−31.5 dB	−43.5 dB
		00011_2	−30 dB	−42 dB
		00100 to 11100_2	−28.5 dB to +7.5 dB	−40.5 dB to −4.5 dB
		11101_2	+9 dB	−3 dB
		11110_2	+10.5 dB	−1.5 dB
		11111_2	+12 dB	0 dB
5	DAC_BOOST	If set, the gain of the DAC inputs to the mixer is increased by 12dB (see above).		
6	DAC_MUTE	If set, the stereo DAC input is muted on the next zero crossing.		
7	USE_AUX_ LEVELS	If set, the gain of the DAC inputs is controlled by the AUX_LEFT and AUX_RIGHT registers, allowing a stereo balance to be applied.		

(1) The output from the DAC is 1V RMS for a full scale digital input. This can be boosted by 12 dB if enough headroom is available. Clipping may occur if the analog power supply is insufficient to cater for the required gain.

CP_OUTPUT CONFIGURATION REGISTER

This register is used to control the differential cell phone output.(2)

Table 25. CP_OUTPUT (0x12h)

Bits	Field	Description
0	MIC_SELECT	If set, the microphone channel of the mixer is added to the CP_OUT output signal.
1	RIGHT_SELECT	If set, the right channel of the mixer is added to the CP_OUT output signal.
2	LEFT_SELECT	If set, the left channel of the mixer is added to the CP_OUT output signal.
3	CPO_MUTE	If set, the CPOUT output is muted.
4	MIC_NOISE_GAT E	If this is set and NOISE_GATE_ON (register 0x08h) is enabled, the MIC to CPO path will be gated if the signal is determined to be noise by the AGC (that is, if the signal is below the set noise threshold).

(2) The gain of cell phone output amplifier is 0 dB.

AUX_OUTPUT CONFIGURATION REGISTER

This register is used to control the differential auxiliary output. (1)

Table 26. AUX_OUTPUT (0x13h)

Bits	Field	Description
0	CPI_SELECT	If set, the cell phone input channel of the mixer is added to the AUX_OUT output signal.
1	RIGHT_SELECT	If set, the right channel of the mixer is added to the AUX_OUT output signal.
2	LEFT_SELECT	If set, the left channel of the mixer is added to the AUX_OUT output signal.
3	AUX_MUTE	If set, the AUX_OUT output is muted.

(1) The gain of the auxiliary output amplifier is 0 dB. If a second (external) loudspeaker amplifier is to be used its gain should be set to 12 dB to match the onboard loudspeaker amplifier gain.

LS_OUTPUT CONFIGURATION REGISTER

This register is used to control the loudspeaker output.(1)

Table 27. LS_OUTPUT (0x14h)

Bits	Field	Description
0	CPI_SELECT	If set, the cell phone input channel of the mixer is added to the loudspeaker output signal.
1	RIGHT_SELECT	If set, the right channel of the mixer is added to the loudspeaker output signal.
2	LEFT_SELECT	If set, the left channel of the mixer is added to the loudspeaker output signal.
3	LS_MUTE	If set, the loudspeaker output is muted.
4	RSVD	Reserved.

(1) The gain of the loudspeaker output amplifier is 12 dB.

HP_OUTPUT CONFIGURATION REGISTER

This register is used to control the stereo headphone output.(1)

Table 28. HP_OUTPUT (0x15h)

Bits	Field	Description
0	SIDETONE_SELECT	If set, the sidetone channel of the mixer is added to both of the headphone output signals.
1	CPI_SELECT	If set, the cell phone input channel of the mixer is added to both of the headphone output signals.
2	RIGHT_SELECT	If set, the right channel of the mixer is added to the headphone output. If the STEREO bit (0x00h) is set, the right channel is added to the right headphone output signal only. If the STEREO bit (0x00h) is cleared, it is added to both the right and left headphone output signals.
3	LEFT_SELECT	If set, the left channel of the mixer is added to the headphone output. If the STEREO bit (0x00h) is set, the left channel is added to the left headphone output signal only. If the STEREO bit (0x00h) is cleared, it is added to both the right and left headphone output signals.
4	HP_MUTE	If set, the headphone output is muted.
5	STEREO	If set, the mixers assume that the signals on the left and right internal busses are highly correlated and when these signals are combined their levels are reduced by 6dB to allow enough headroom for them to be summed.
6	OCL	If set, the part is placed in OCL (Output Capacitor Less) mode.

(1) The gain of the headphone output amplifier is –6 dB for the cell phone input channel and sidetone channel of the mixer. When the STEREO bit (0x00h) is set, headphone output amplifier gain is –6 dB for the left and right channel. When the STEREO bit (0x00h) is cleared, the headphone output amplifier gain is –12 dB for the left and right channel (to allow enough headroom for adding them and routing them to both headphone amplifiers).

EP_OUTPUT CONFIGURATION REGISTER

This register is used to control the mono earpiece output.(1)

Table 29. EP_OUTPUT (0x16h)

Bits	Field	Description
0	SIDETONE_SELECT	If set, the sidetone channel of the mixer is added to the earpiece output signal.
1	CPI_SELECT	If set, the cell phone input channel of the mixer is added to the earpiece output signal.
2	RIGHT_SELECT	If set, the right channel of the mixer is added to the earpiece output signal.
3	LEFT_SELECT	If set, the left channel of the mixer is added to the earpiece output signal.
4	EP_MUTE	If set, the earpiece output is muted.

(1) The gain of the earpiece output amplifier is 6 dB.

DETECT CONFIGURATION REGISTER

This register is used to control the headset detection system.

Table 30. DETECT (0x17h)

Bits	Field	Description	
0	DET_INT	If set, an IRQ is raised when a change is detected in the headset status. Clearing this bit will clear an IRQ that has been triggered by the headset detect.	
1	BTN_INT	If set, an IRQ is raised when the headset button is pressed. Clearing this bit will clear an IRQ that has been triggered by a button event.	
2	TEMP_INT	If set, an IRQ is raised during a temperature event. The LM49370 will still automatically cycle the class AB power amplifiers off if the internal temperature is too high. This bit should not be set whenever the class D amplifier is turned on. Clearing this bit will clear an IRQ that has been triggered by a temperature event.	
6:3	HS_ DBNC_TIME	This sets the time used for debouncing the analog signals from the detection inputs used to sense the insertion/removal of a headset.	
		HS_DBNC_TIME	Time (ms)
		0000_2	0
		0001_2	8
		0010_2	16
		0011_2	32
		0100_2	48
		0101_2	64
		0110_2	96
		0111_2	128
		1000_2	192
		1001_2	256
		1010_2	384
		1011_2	512
		1100_2	768
		1101_2	1024
		1110_2	1536
		1111_2	2048

HEADSET DETECT OVERVIEW

The LM49370 has built in monitors to automatically detect headset insertion or removal. The detection scheme can differentiate between mono, stereo, mono-cellular and stereo-cellular headsets. Upon detection of headset insertion or removal, the LM49370 updates read-only bit 0 - headset absence/presence, bit 1- mono/stereo headset and bit 2 - headset without mic / with mic, of the STATUS register (0x18h). Headset insertion/removal and headset type can also be detected in standby mode; this consumes no analog supply current when the headset is absent.

The LM49370 can be programmed to raise an interrupt (set the IRQ pin high) when headset insert/removal is sensed by setting bit 0 of DETECT (0x17h). When headset detection is enabled in active mode and a headset is not detected, the HPL_OUT and HPR_OUT amplifiers will be disabled (switched off for capless mode and muted for AC-coupled mode) and the EXT_BIAS pin will be disconnected from the MIC_BIAS amplifier, irrespective of control register settings.

The LM49370 also has the capability to detect button press, when a button is present on the headset microphone. Both parallel button-type (in parallel with the headset microphone, default value) and series button-type (in series with the headset microphone) can be detected; the button type used needs to be defined in bit 3 of MIC_2 (0x0Ch). Button press can also be detected in stand-by mode; this consumes 10 µA of analog supply current for a series type push button and 100 µA for a parallel type push button. Upon button press, the LM49370 updates bit 3 of STATUS (0x18h). In active OCL mode, with internal microphone selected (INT_EXT = 0; (reg 0x0Bh)), if a parallel pushbutton headset is inserted into the system, INT_EXT must be set high before BTN (bit 3 of STATUS (0x18h)) can be read. The LM49370 can also be programmed to raise an interrupt on the IRQ pin when button press is sensed by setting bit 1 of DETECT (0x17h).

The LM49370 provides debounce programmability for headset and button detect. Debounce programmability can be used to reject glitches generated, and hence avoid false detection, while inserting/removing a headset or pressing a button.

Headset insert/removal debounce time is defined by HS_DBNC_TIME; bits 6:3 of DETECT (0x17h). Parallel button press debounce time is defined by BTN_DBNC_TIME; bits 5:4 of MIC_2 (0x0Ch).

Note that since the first effect of a series button press (microphone disconnected) is indistinguishable from headset removal, the debounce time for series button press in defined by HS_DBNC_TIME.

Headset and push button detection can be enabled by setting CHIP_MODE 0; bit 0 of BASIC (0x00h). For reliable headset / push button detection all following bits should be defined before enabling the headset detection system:

1. the OCL-bit (AC-Coupled / Capless headphone interface (bit 6 of HP_OUTPUT (0x15h))
2. the headset insert/removal debounce settings (bit 6:3 of DETECT (0x17h))
3. the BTN_TYPE-bit (Parallel / Series push button type (bit 3 of MIC_2 (0x0Ch))
4. the parallel push button debounce settings (bit 5:4 of MIC_2 (0x0Ch))

Figure 16 shows terminal connections and jack configuration for various headsets. Care should be taken to avoid any DC path from the MIC_DET pin to ground when a headset is not inserted.

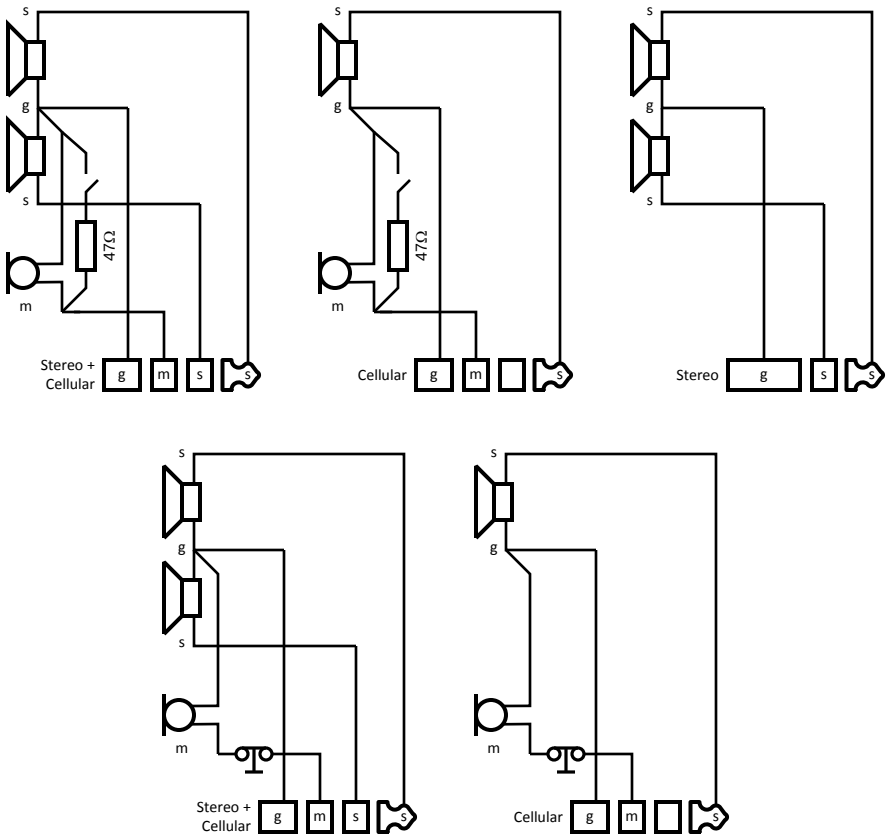


Figure 16. Headset Configurations Supported by the LM49370

The wiring of the headset jack to the LM49370 will depend on the intended mode of the headphone amplifier:

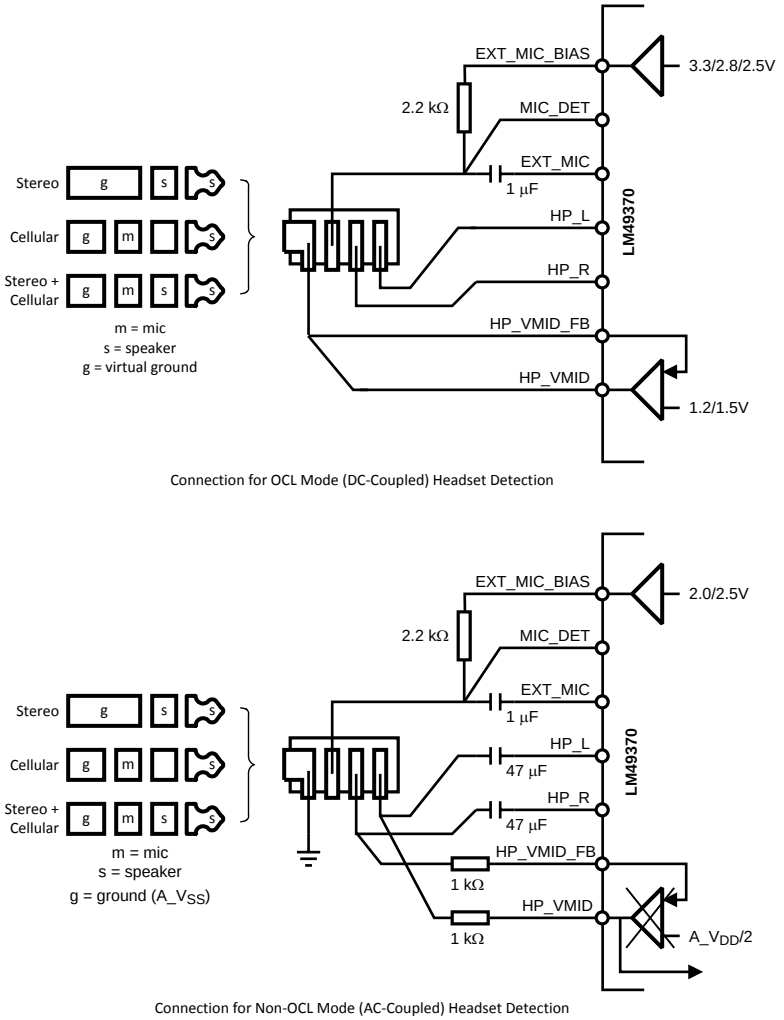


Figure 17. Connection of Headset Jack to LM49370 Depends on the Mode of the Headphone Amplifier.

In non-OCL mode, two 1kΩ resistors are optional and not needed if chip is active without headset event detection in Basic Register (0x00h) bits 1:0. If chip is active with headset event detection, these two resistors set an internal threshold voltage for a comparator that produces the headphone detect pulse. The value of these should be 1kΩ with tolerance of ±10% or better.

STATUS REGISTER

This register is used to report the status of the device.

Table 31. STATUS (0x18h)(1)(2)

Bits	Field	Description
0	HEADSET	This field is high when headset presence is detected (only valid if the detection system is enabled).(1)
1	STEREO_ HEADSET	This field is high when a headset with stereo speakers is detected (only valid if the detection system is enabled). (1)
2	MIC	This field is high when a headset with a microphone is detected (only valid if the detection system is enabled).(1)

(1) The detection IRQ is cleared when this register has been written to.
(2) This field is cleared whenever the STATUS (0x18h) register has been written to.

Table 31. STATUS (0x18h)(1)(2) (continued)

Bits	Field	Description
3	BTN	This field is high when the button on the headset is pressed (only valid if the detection system is enabled). IRQ is cleared when the button has been released **and** this register has been written to. (2)
4	TEMP	If this field is high then a temperature event has occurred (write to this register to clear IRQ). This field will stay high even when the IRQ is cleared so long as the event occurs. This bit is only valid whenever the loudspeaker amplifier is turned off. (2)
5	GPIN1	When GPIO_SEL is set to a readable configuration a digital input on GPIO1 can be read back here.
6	GPIN2	When GPIO_SEL is set to a readable configuration, a digital input on the relevant GPIO can be read back here.

3D CONFIGURATION REGISTER

This register is used to control the configuration of the 3D circuit.

Table 32. 3D (0x19h)

Bits	Field	Description	
0	3D_ENB	Setting this bit enables the 3D effect. When cleared to zero, the 3D effect is disabled and the 3D module then passes the I^2S left and right channel inputs to the DAC unchanged. The stereo AUX inputs are unaffected by the 3D module.	
1	3D_TYPE	This bit selects between type 1 and type 2 3D sound effect. Clearing this bit to zero selects type 1 effect and setting it to one selects type 2. Type1: Rout = Ri-G*Lout3d, Lout = Li-G*Rout3d Type2: Rout = -Ri-G*Lout3d, Lout = Li+G*Rout3d where, Ri = Right I^2S channel input Li = Left I^2S channel input G = 3D gain level (Mix ratio) Rout3d = Ri filtered through a high-pass filter with a corner frequency controlled by FREQ Lout3d = Li filtered through a high-pass filter with a corner frequency controlled by FREQ	
3:2	LEVEL	This programs the level of 3D effect that is applied.	
			LEVEL
		00_2	25%
		01_2	37.5%
		10_2	50%
		11_2	75%
5:4	FREQ	This programs the HPF rolloff (-3dB) frequency of the 3D effect.	
			FREQ
		00_2	0Hz
		01_2	300Hz
		10_2	600Hz
		11_2	900Hz
6	ATTENUATE	Clearing this bit to zero maintains the level of the left and right input channels at the output. Setting this bit to one attenuates the output level by 50%. This may be appropriate for high level audio inputs when type 2 3D effect is used. Type 2 effect involves adding the same polarity of left and right inputs to give the final outputs. Type 2 effect has the potential for creating a clipping condition, however this bit offers an alternative to clipping.	
7	CUST_COMP	If set, the DAC compensation filter may be programmed by the user through registers (0x20h) to(0x25h). Otherwise, the defaults are used.	

I2S PORT MODE CONFIGURATION REGISTER

This register is used to control the audio data interfaces.

Table 33. I2S Mode (0x1Ah)

Bits	Field	Description	
0	I2S_OUT_ENB	If set, the I^2S output bus is enabled. If cleared, the I^2S output will be tristate and all RX clocks will be gated.	
1	I2S_IN_ENB	If set, the I^2S input is enabled. If this bit cleared, the I^2S input is ignored and all TX clocks gated.	
2	I2S_MODE	This programs the format of the I^2S interface.	
			Definition
		0	Normal
		1	Left Justified
3	I2S_STEREO_REVERSE	If set, the left and right channels are reversed.	
			Operation
		0	Normal
		1	Reversed
4	I2S_WS_MS	If set, I2S_WS generation is enabled and is Master. If cleared, I2S_WS acts as slave.	
6:5	I2S_WS_GEN_MODE	This programs the I^2S word length.	
			Bits/Word
		00_2	16
		01_2	25
		10_2	32
		11_2	—
7	I2S_WORD_ORDER	This bit alters the RX phasing of left and right channels. If this bit is cleared: right then left. If this bit is set: left then right.	

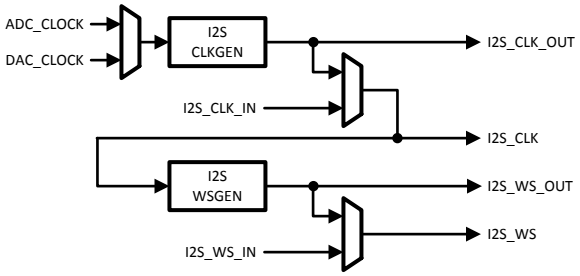


Figure 18. I2S Audio Port CLOCK/SYNC Options

I2S PORT CLOCK CONFIGURATION REGISTER

This register is used to control the audio data interfaces.

Table 34. I2S Clock (0x1Bh)

Bits	Field	Description	
0	I2S_CLOCK_MS	If set, then I^2S clock generation is enabled and is Master. If this bit is cleared, then the I^2S clock is driven by the device slave.	
1	I2S_CLOCK_SOURCE	This selects the source of the clock to be used by the I2S clock generator.	
		I2S_CLOCK_SOURCE	Clock is source from
		0	DAC (from R divider)
		1	ADC (from Q divider)

Table 34. I2S Clock (0x1Bh) (continued)

Bits	Field	Description		
5:2	I2S_CLOCK_GEN_MODE	This programs a clock divider that divides the clock defined by I2S_CLOCK_SOURCE. This divided clock is used to generate I2S_CLK in Master mode.(1)		
		Value	Divide By	Ratio
		0000_2	1	
		0001_2	2	
		0010_2	4	
		0011_2	6	
		0100_2	8	
		0101_2	10	
		0110_2	16	
		0111_2	20	—
		1000_2	2.5	2/5
		1001_2	3	1/3
		1010_2	3.90625	32/125
		1011_2	5	25/125
		1100_2	7.8125	16/125
		1101_2	—	—
		1110_2	—	—
		1111_2	—	—
7:6	PCM_SYNC_WIDTH	This programs the width of the PCM sync signal.		
			Generated SYNC Looks like:	
		00_2	1 bit (Used for Short PCM Modes)	
		01_2	4 bits (Used for Long PCM Modes)	
		10_2	8 bits (Used for Long PCM Modes)	
		11_2	15 bits (Used for Long PCM Modes) Should not be set if the bits/word is less than 16.	

(1) For DAC_MODE = '00', '10', '11', DAC_CLOCK is the clock at the output of the R divider. For DAC_MODE = '01', DAC_CLOCK is a divided by two version of the clock at the output of the R divider.

DIGITAL AUDIO DATA FORMATS

I^2S master mode can only be used when the DAC is enabled unless the FORCE_RQ bit is set. PCM Master mode can only be used when the ADC is enabled, unless the FORCE_RQ bit is set. If the PCM receiver interface is operated in slave mode the clock and sync should be enabled at the same time because the PCM receiver uses the first PCM frame to calculate the PCM interface format. This format can not be changed unless a soft reset is issued. Operating the LM49370 in master mode eliminates the risk of sample rate mismatch between the data converters and the audio interfaces.

In slave mode, the PCM and I^2S receivers only record the 1st 16 and 18 bits of the serial words respectively. The I^2S and PCM formats are as followed:

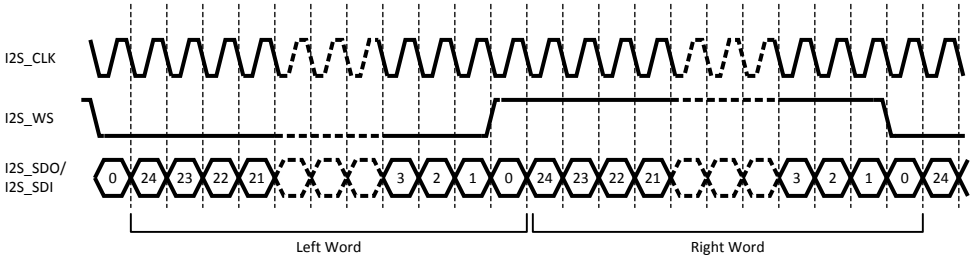


Figure 19. I^2S Serial Data Format (Default Mode)

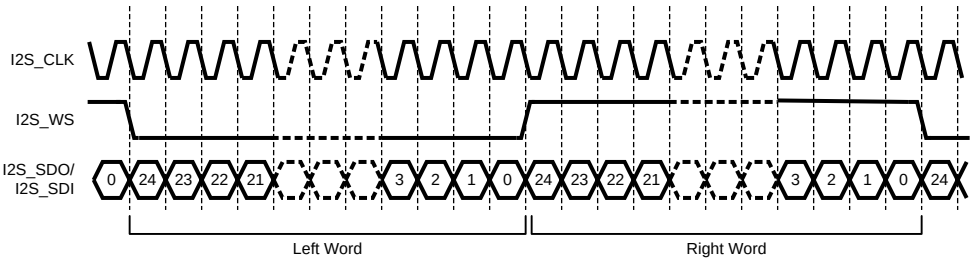


Figure 20. I²S Serial Data Format (Left Justified)

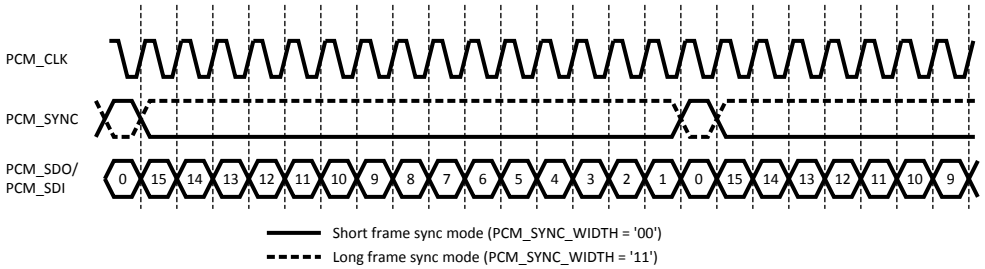


Figure 21. PCM Serial Data Format (16 bit Slave Example)

PCM PORT MODE CONFIGURATION REGISTER

This register is used to control the audio data interfaces.

Table 35. PCM MODE (0x1Ch)

Bits	Field	Description	
0	PCM_OUT_ENB	If set, the PCM output bus is enabled. If this bit is cleared, thr PCM output will be tristate and all RX clocks will be gated.	
1	PCM_IN_ENB	If set, the PCM input is enabled. If this bit is cleared, the PCM input is ignored and TX clocks are generated.	
3	PCM_CLOCK_SOURCE	DAC or ADC Clock 0 = DAC, 1 = ADC (1)	
4	PCM_SYNC_MS	If set, PCM_SYNC generation is enabled and is driven by the device (Master).	
5	PCM_SDO_LSB_HZ	If set, when the PCM port has run out of bits to transmit, it will tristate the SDO output.	
6	PCM_COMPAND	If set, the data sent to the PCM port is companded and the PCM data received by the PCM receiver is treated as companded data.	
7	PCM_ALAW_µLAW	If PCM_ COMPAND is set, then the data across the PCM interface to the DAC and from the ADC is companded as follows:	
		PCM_ALAW_µLAW	Commanding Type
		0	µ-LAW
		1	A-Law

(1) For DAC_MODE = '00', '10', '11', DAC_CLOCK is the clock at the output of the R divider. For DAC_MODE = '01', DAC_CLOCK is a divided by two version of the clock at the output of the R divider.

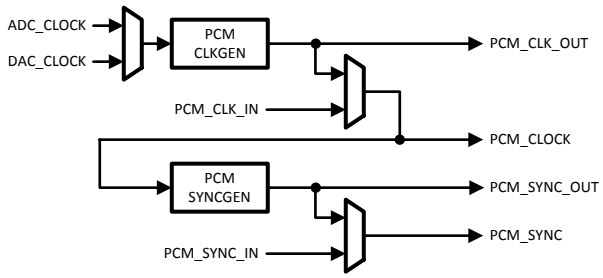


Figure 22. PCM Audio Port CLOCK/SYNC Options

PCM PORT CLOCK CONFIGURATION REGISTER

This register is used to control the configuration of audio data interfaces.

Table 36. PCM Clock (0x1Dh)

Bits	Field	Description		
3:0	PCM_CLOCK_ GEN_MODE	This programs a clock divider that divides the clock defined by PCM_CLOCK_SOURCE reg(0x1Ch). The divided clock is used to generate PCM_CLK in Master mode. (1)		
		Value	Divide By	Ratio
		0000_2	1	
		0001_2	2	
		0010_2	4	
		0011_2	6	
		0100_2	8	
		0101_2	10	
		0110_2	16	
		0111_2	20	—
		1000_2	2.5	2/5
		1001_2	3	1/3
		1010_2	3.90625	32/125
		1011_2	5	25/125
		1100_2	7.8125	16/125
		1101_2	—	—
		1110_2	—	—
		1111_2	—	—
6:4	PCM_SYNC_MODE	This programs a clock divider that divides PCM_CLK. The divided clock is used to generate PCM_SYNC.		
		Valve	**Divide By**	
		000_2	8	
		001_2	16	
		010_2	25	
		011_2	32	
		100_2	64	
		101_2	128	
		110_2	—	
		111_2	—	

(1) For DAC_MODE = '00', '10', '11', DAC_CLOCK is the clock at the output of the R divider. For DAC_MODE = '01', DAC_CLOCK is a divided by two version of the clock at the output of the R divider.

SRC CONFIGURATION REGISTER

This register is used to control the configuration of the Digital Routing interfaces. (2)

Table 37. Bridges (0x1Eh)

Bits	Field	Description	
0	PCM_TX_SEL	This controls the data sent to the PCM transmitter.	
		PCM_TX_SEL	**Source**
		0	ADC
		1	MONO SUM Circuit
2:1	I2S_TX_SEL	This controls the data sent to the I^2S transmitter.	
		I2S_TX_SEL	**Source**
		00_2	ADC
		01_2	PCM Receiver
		10_2	DAC Interpolator (oversampled)
		11_2	Disabled
4:3	DAC_INPUT_SEL	This controls the data sent to the DAC.	
		DAC_INPUT_SEL	**Source**
		00_2	I2S Receiver (In stereo)
		01_2	PCM Receiver (Dual Mono)
		10_2	ADC
		11_2	Disabled
5	MONO_SUM_SEL	This controls the data sent to the Stereo to Mono Converter	
		MONO_SUM_SEL	**Source**
		0	DAC Interpolated Output
		1	I2S Receiver Output
7:6	MONO_SUM_MODE	This controls the operation of the Stereo to Mono Converter.	
		MONO_SUM_ MODE	**Operation**
		00_2	(Left + Right)/2
		01_2	Left
		10_2	Right
		11_2	(Left + Right)/2

(2) Please refer to the Application Note AN-1591 (SNAA039) for the detailed discussion on how to use the I^2S to PCM Bridge.

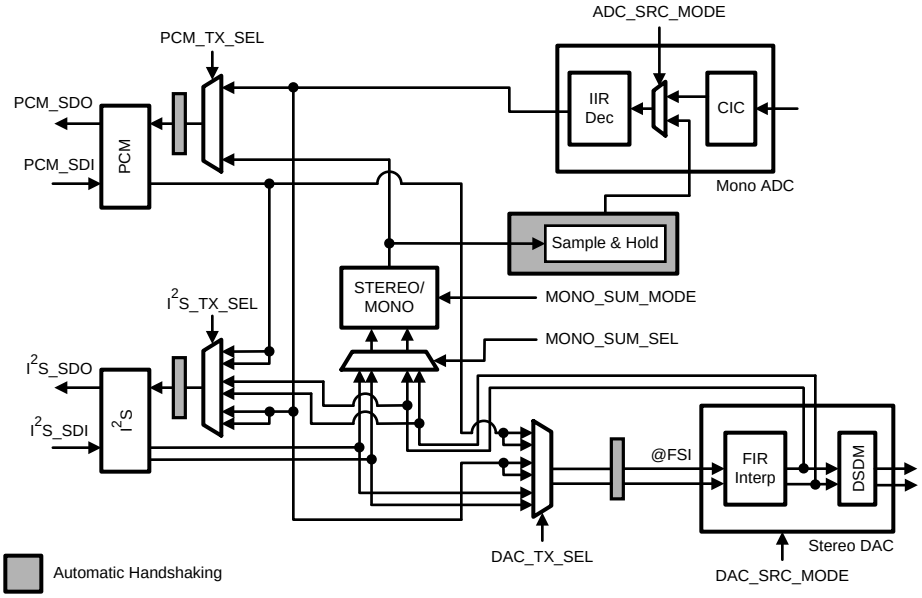


Figure 23. I^2S to PCM Bridge

GPIO CONFIGURATION REGISTER

This register is used to control the GPIOs and to control the digital signal routing when using the ADC and DAC to perform sample rate conversion.

Table 38. GPIO Control (0x1Fh)

Bits	Field	Description		
2:0	GPIO_1_SEL	This configures the GPIO_1 pin.		
		GPIO_1_SEL	**Does What?**	**Direction**
		000_2	Disable	HiZ
		001_2	SPI_SDO	Output
		010_2	Output 0	Output
		011_2	Output 1	Output
		100_2	Read	Input
		101_2	Class D Enable	Output
		110_2	AUX Enable	Output
		111_2	Dig_Mic_Data	Input
5:3	GPIO_2_SEL	This configures the GPIO_2 pin.		
		GPIO_2_SEL	**Does What?**	**Direction**
		000_2	Disable	HiZ
		001_2	SPI_SDO	Output
		010_2	Output 0	Output
		011_2	Output 1	Output
		100_2	Read	Input
		101_2	Class D Enable	Output
		110_2	Dig_Mic L Clock	Output
		111_2	Dig_Mic R Clock	Output
6	ADC_SRC_MODE	If set, the ADC analog is disabled and the digital is enabled, using the resampler input.		
7	DAC_SRC_MODE	This does not have to be set to use DAC in SRC mode, but should be set if the user wishes to disable the DAC analog to save power.		

DAC PATH COMPENSATION FIR CONFIGURATION REGISTERS

To allow for compensation of roll off in the DAC and analog filter sections an FIR compensation filter is applied to the DAC input data at the original sample rate. Since the DAC can operate at different over sampling ratios the FIR compensation filter is programmable. By default the filter applies approx 2dB of compensation at 20kHz. 5 taps is sufficient to allow passband equalization and ripple cancellation to around +/0.01dB.

The filter can also be used for precise digital gain and simple tone controls although a DSP or CPU should be used for more powerful tone control if required. As the FIR filter must always be phase linear, the coefficients are symmetrical. Coefficients C0, C1, and C2 are programmable, C3 is equal to C1 and C4 is equal to C0. The maximum power of this filter must not exceed that of the examples given below:

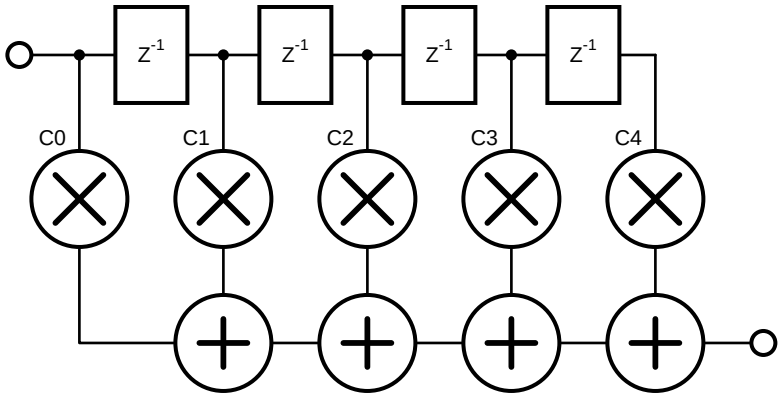


Figure 24. FIR Consumption Filter Taps

Sample Rate	DAC_MODE	C0	C1	C2	C3	C4
48kHz	00	334	–2291	26984	–2291	343
48kHz	01	61	–371	25699	–371	61

For DAC_MODE = '00 and '01', the defaults should be sufficient; but for DAC_MODE = '10' and '11', care should be taken to ensure the widest bandwidth is available without requiring such a large attenuation at DC that inband noise becomes audible.

Table 39. Compensation Filter C0 LSBs (0x20h)

Bits	Field	Description
7:0	C0_LSB	Bits 7:0 of C0[15:0]

Table 40. Compensation Filter C0 MSBs (0x21h)

Bits	Field	Description
7:0	C0_MSB	Bits 15:8 of C0[15:0]

Table 41. Compensation Filter C1 LSBs (0x22h)

Bits	Field	Description
7:0	C1_LSB	Bits 7:0 of C1[15:0]

Table 42. Compensation Filter C1 MSBs (0x23h)

Bits	Field	Description
7:0	C1_MSB	Bits 15:8 of C1[15:0]

Table 43. Compensation Filter C2 LSBs (0x24h)

Bits	Field	Description
7:0	C2_LSB	Bits 7:0 of C2[15:0]

Table 44. Compensation Filter C2 MSBs (0x25h)

Bits	Field	Description
7:0	C2_MSB	Bits 15:8 of C2[15:0]

Typical Performance Characteristics

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Stereo DAC Frequency Response
f_S = 8kHz

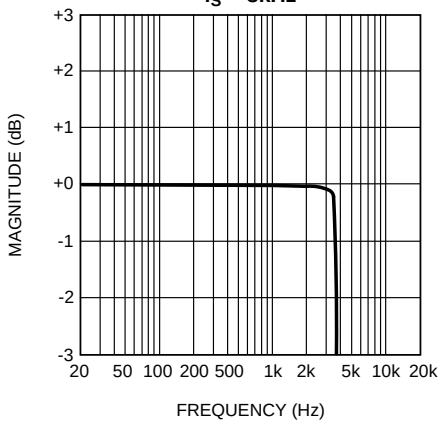


Figure 25.

Stereo DAC Frequency Response Zoom
f_S = 8kHz

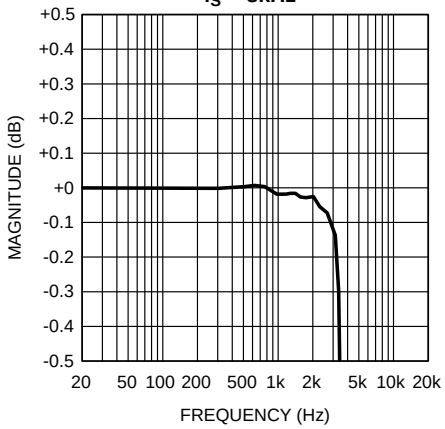


Figure 26.

Stereo DAC Frequency Response
f_S = 16kHz

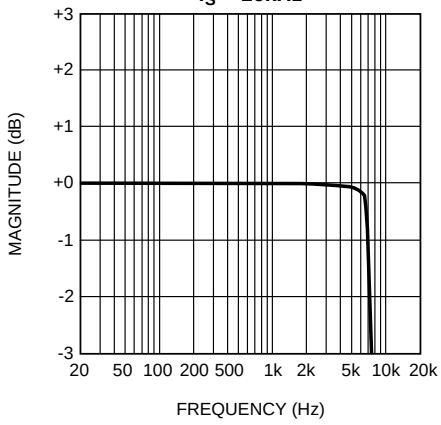


Figure 27.

Stereo DAC Frequency Response Zoom
f_S = 16kHz

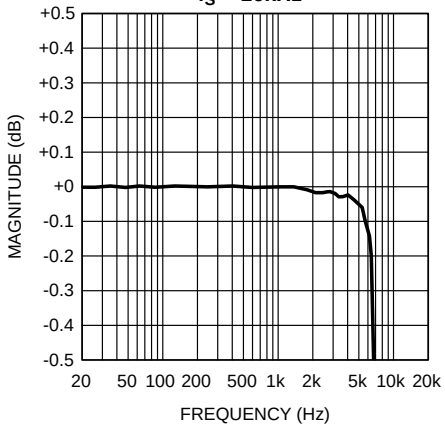


Figure 28.

Stereo DAC Frequency Response
f_S = 24kHz

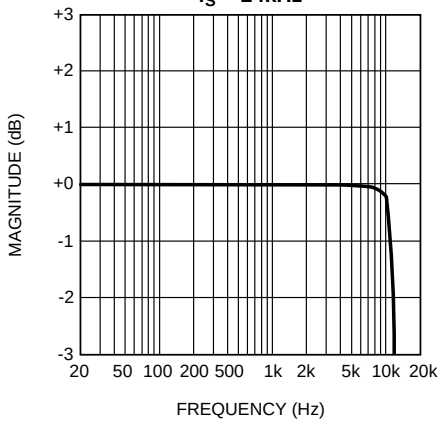


Figure 29.

Stereo DAC Frequency Response Zoom
f_S = 24kHz

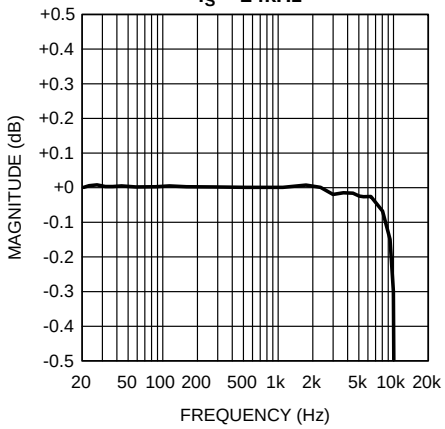


Figure 30.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Stereo DAC Frequency Response
f_S = 32kHz

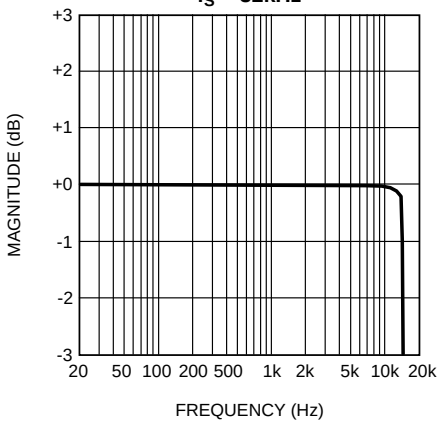


Figure 31.

Stereo DAC Frequency Response Zoom
f_S = 32kHz

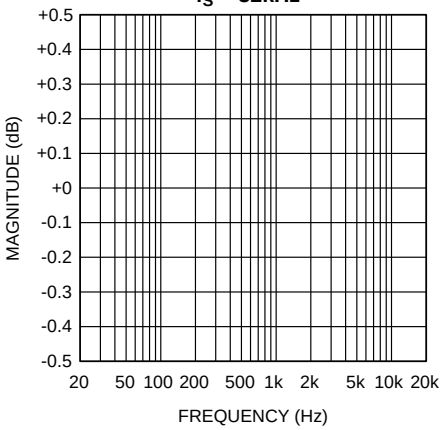


Figure 32.

Stereo DAC Frequency Response
f_S = 48kHz

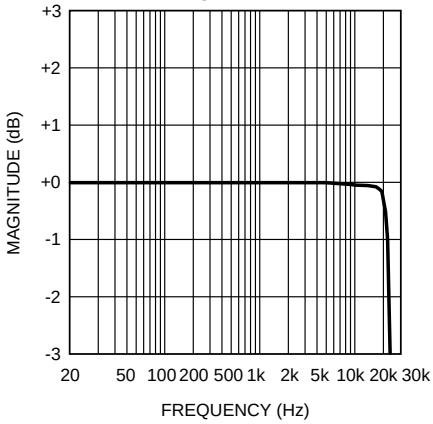


Figure 33.

Stereo DAC Frequency Response Zoom
f_S = 48kHz

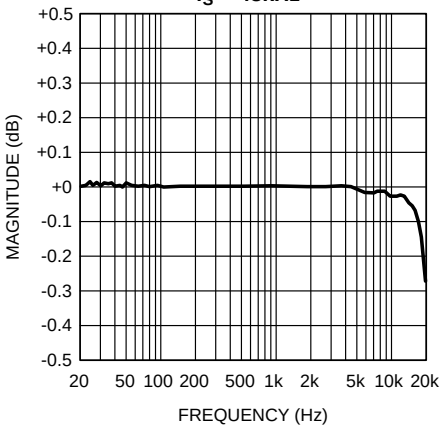


Figure 34.

THD+N
vs
Stereo DAC Input Voltage (0dB DAC, AUXOUT)

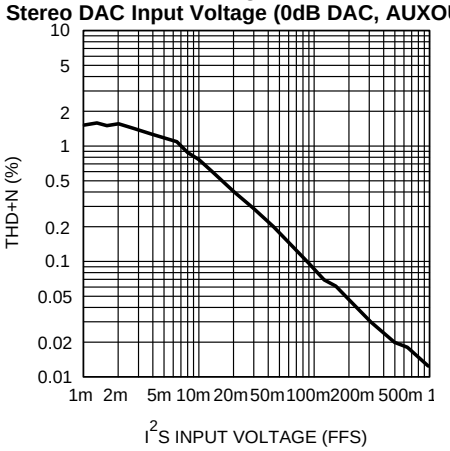


Figure 35.

Stereo DAC Crosstalk
(0dB, DAC, HP SE, 32Ω)

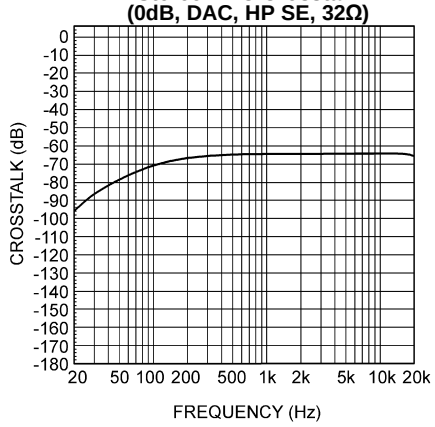


Figure 36.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

MONO ADC Frequency Response
f_S = 8kHz, 6dB MIC

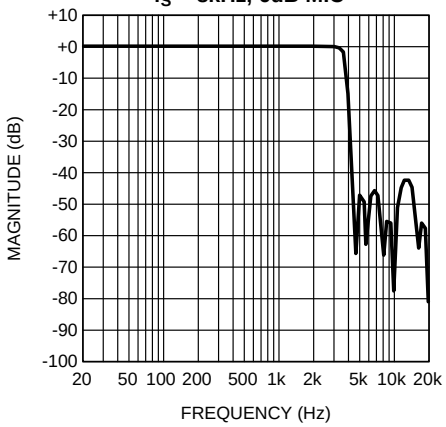


Figure 37.

MONO ADC Frequency Response Zoom
f_S = 8kHz, 6dB MIC

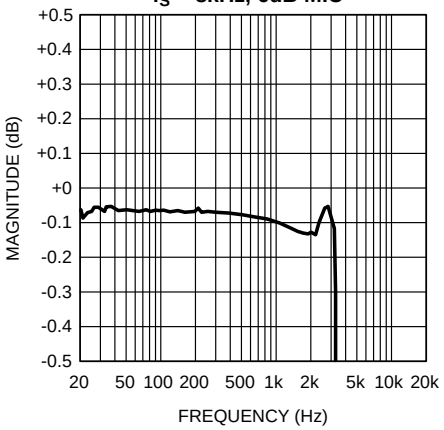


Figure 38.

MONO ADC Frequency Response
f_S = 8kHz, 36dB MIC

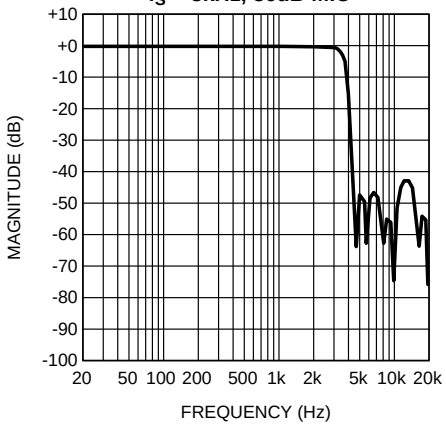


Figure 39.

MONO ADC Frequency Response Zoom
f_S = 8kHz, 36dB MIC

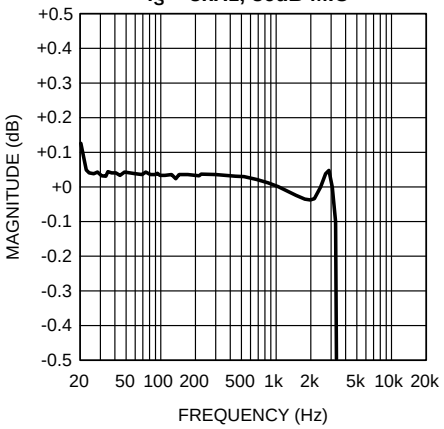


Figure 40.

MONO ADC Frequency Response
f_S = 16kHz, 6dB MIC

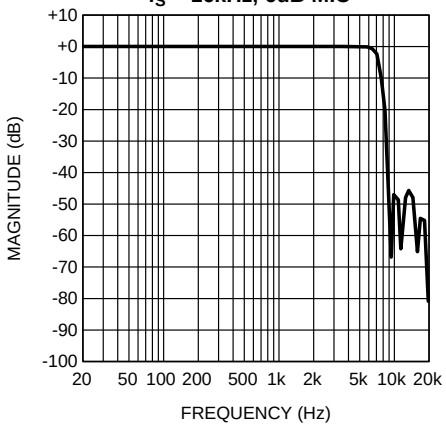


Figure 41.

MONO ADC Frequency Response Zoom
f_S = 16kHz, 6dB MIC

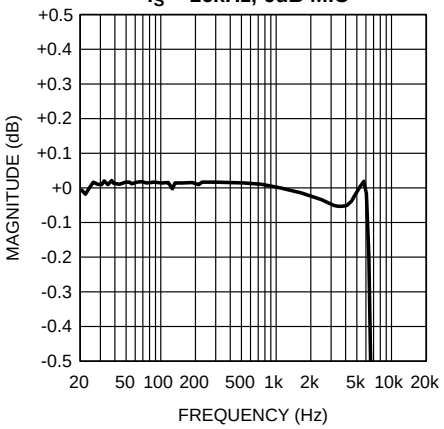


Figure 42.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

MONO ADC Frequency Response
f_S = 16kHz, 36dB MIC

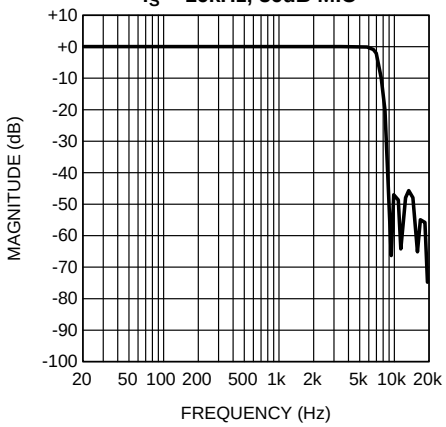


Figure 43.

MONO ADC Frequency Response Zoom
f_S = 16kHz, 36dB MIC

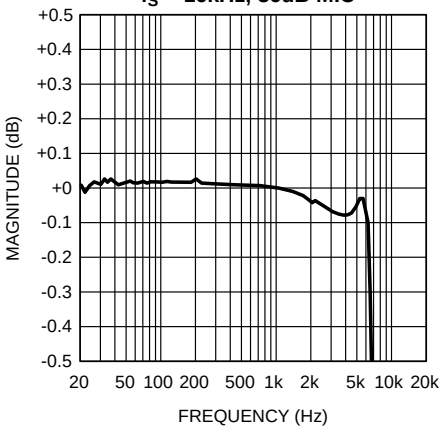


Figure 44.

MONO ADC Frequency Response
f_S = 24kHz, 6dB MIC

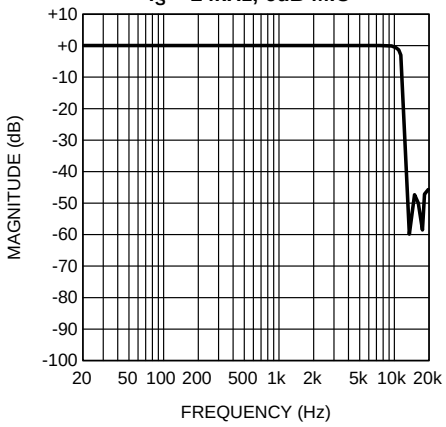


Figure 45.

MONO ADC Frequency Response Zoom
f_S = 24kHz, 6dB MIC

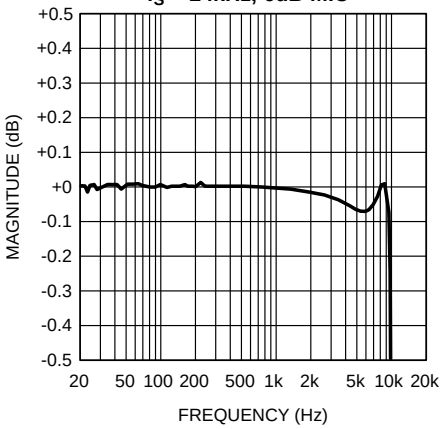


Figure 46.

MONO ADC Frequency Response
f_S = 24kHz, 36dB MIC

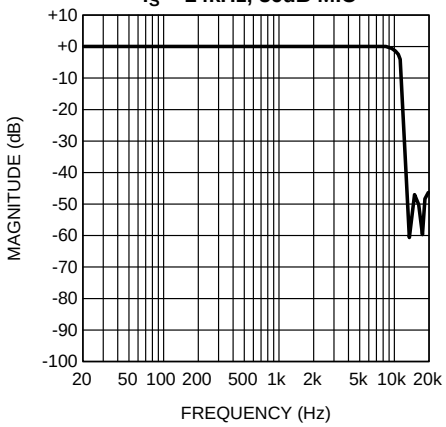


Figure 47.

MONO ADC Frequency Response Zoom
f_S = 24kHz, 36dB MIC

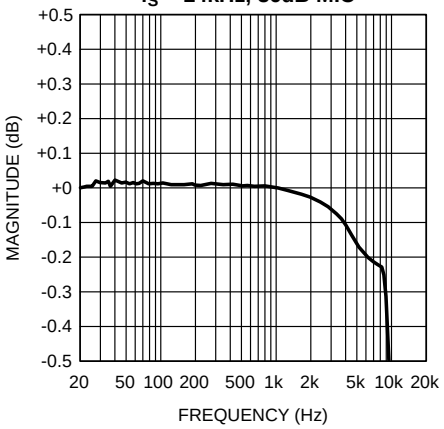


Figure 48.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

MONO ADC Frequency Response
f_S = 32kHz, 6dB MIC

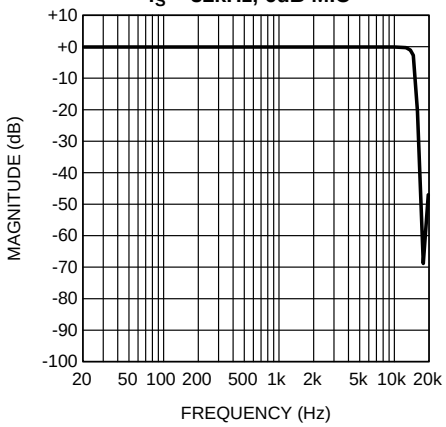


Figure 49.

MONO ADC Frequency Response Zoom
f_S = 32kHz, 6dB MIC

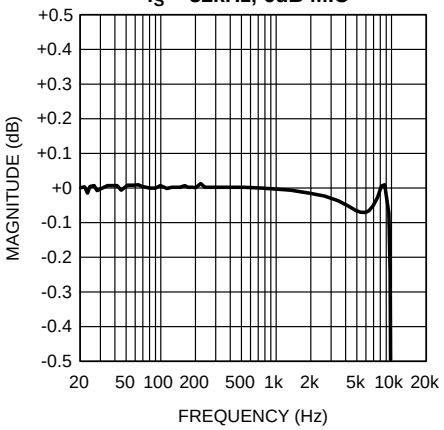


Figure 50.

MONO ADC Frequency Response
f_S = 32kHz, 36dB MIC

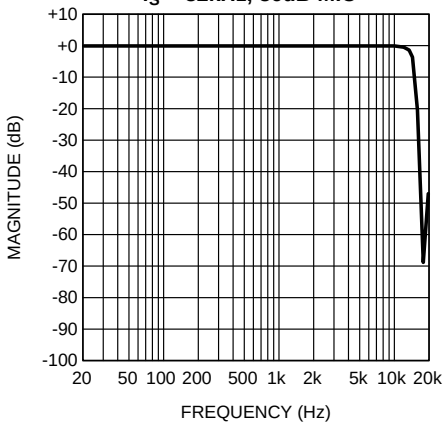


Figure 51.

MONO ADC Frequency Response Zoom
f_S = 32kHz, 36dB MIC

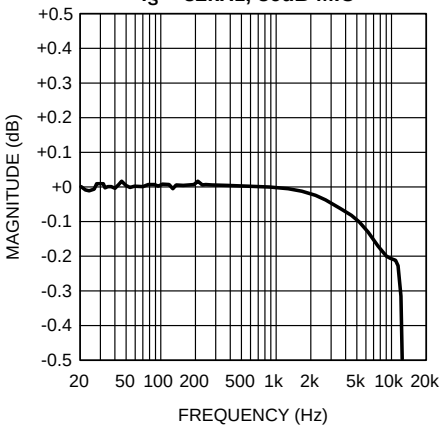


Figure 52.

MONO ADC HPF Frequency Response
f_S = 8kHz, 36dB MIC
(from left to right: HPF_MODE '00', '10', '01')

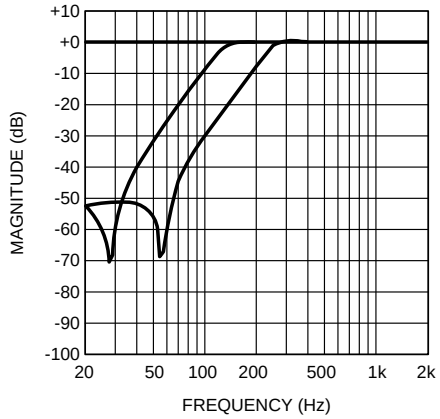


Figure 53.

MONO ADC HPF Frequency Response
f_S = 16kHz, 36dB MIC
(from left to right: HPF_MODE '00', '10', '01')

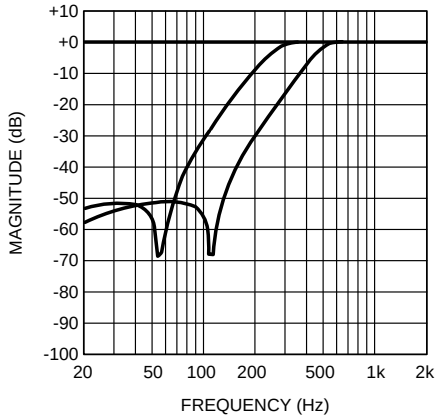


Figure 54.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

MONO ADC HPF Frequency Response
f_S = 24kHz, 36dB MIC
(from left to right: HPF_MODE '00', '10', '01')

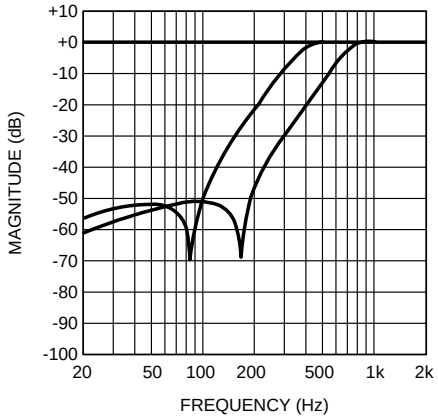


Figure 55.

MONO ADC HPF Frequency Response
f_S = 32kHz, 36dB MIC
(from left to right: HPF_MODE '00', '10', '01')

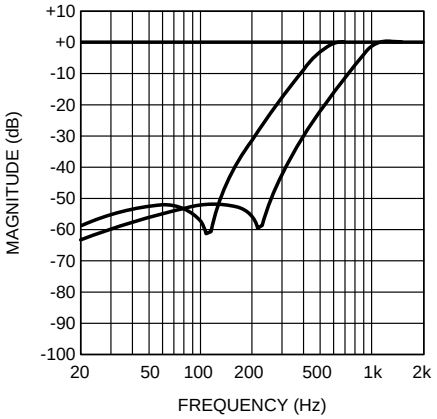


Figure 56.

MONO ADC THD+N
vs MIC Input Voltage
(f_S = 8kHz, 6dB MIC)

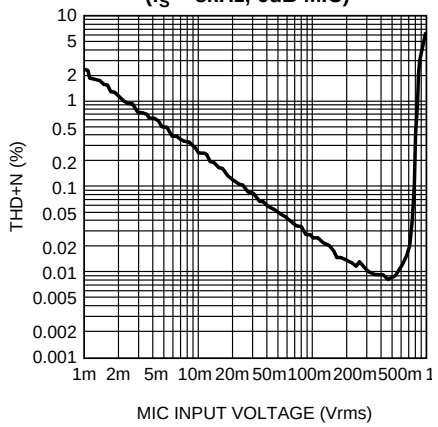


Figure 57.

MONO ADC THD+N
vs MIC Input Voltage
(f_S = 8kHz, 36dB MIC)

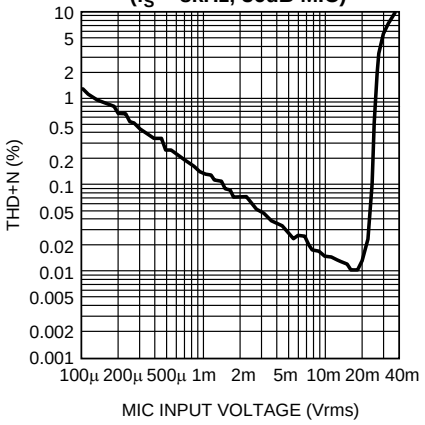


Figure 58.

MONO ADC PSRR
vs
Frequency
AV_{DD} = 3.3V, 6dB MIC

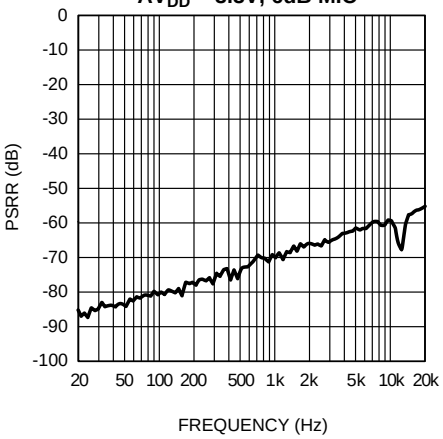


Figure 59.

MONO ADC PSRR
vs
Frequency
AV_{DD} = 5V, 6dB MIC

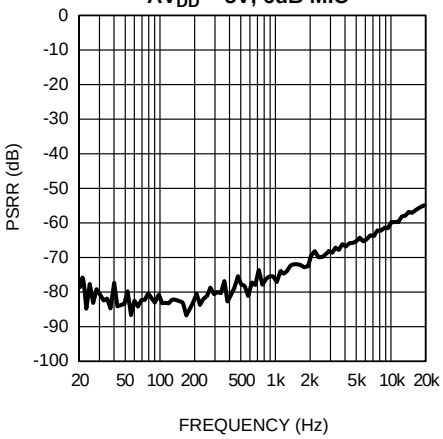


Figure 60.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

MONO ADC PSRR vs Frequency AV_{DD} = 3.3V, 36dB MIC

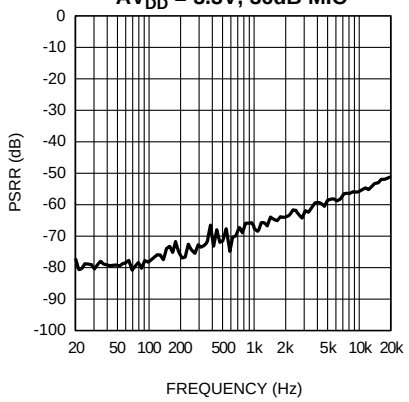


Figure 61.

MONO ADC PSRR vs Frequency AV_{DD} = 5V, 36dB MIC

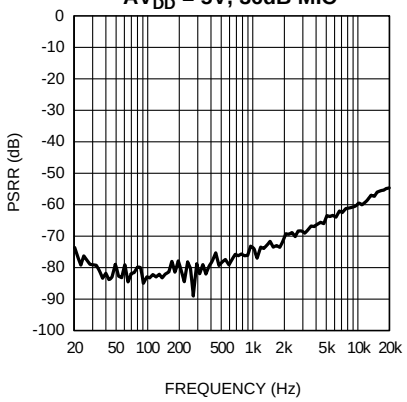


Figure 62.

AUXOUT PSRR vs Frequency AV_{DD} = 3.3V, 0dB AUX (AUX inputs terminated)

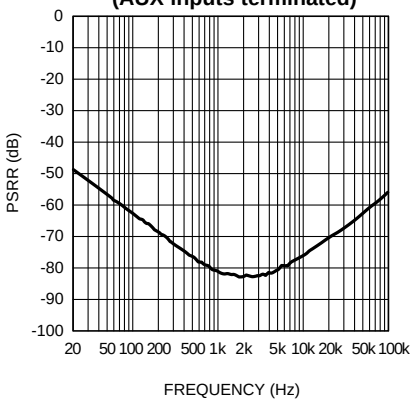


Figure 63.

AUXOUT PSRR vs Frequency AV_{DD} = 5V, 0dB AUX (AUX inputs terminated)

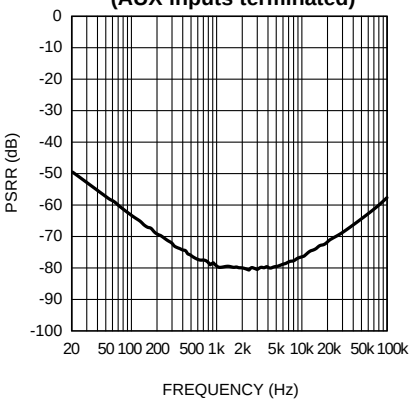


Figure 64.

AUXOUT PSRR vs Frequency AV_{DD} = 3.3V, 0dB CPI (CPI inputs terminated)

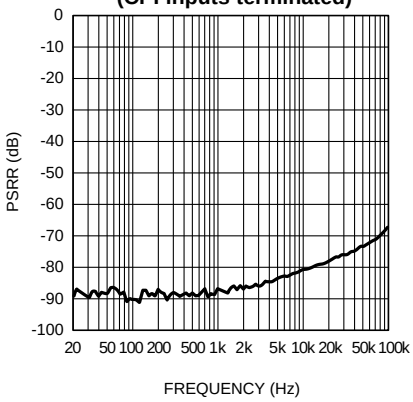


Figure 65.

AUXOUT PSRR vs Frequency AV_{DD} = 5V, 0dB CPI (CPI inputs terminated)

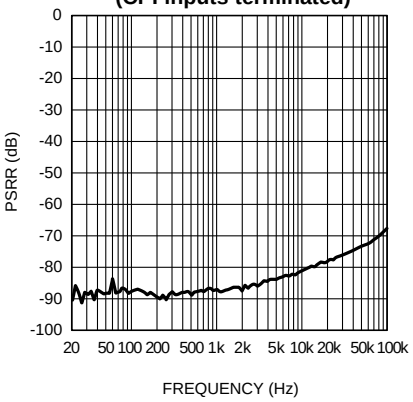


Figure 66.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

AUXOUT PSRR vs Frequency AV_{DD} = 3.3V, 0dB DAC (DAC inputs selected)

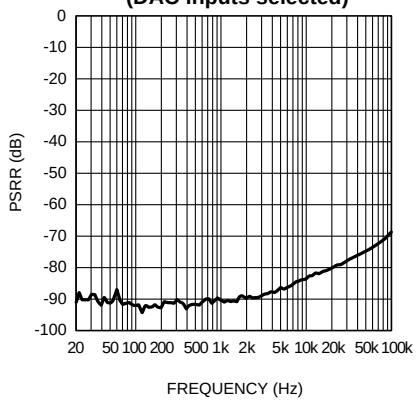


Figure 67.

AUXOUT PSRR vs Frequency AV_{DD} = 5V, 0dB DAC (DAC inputs selected)

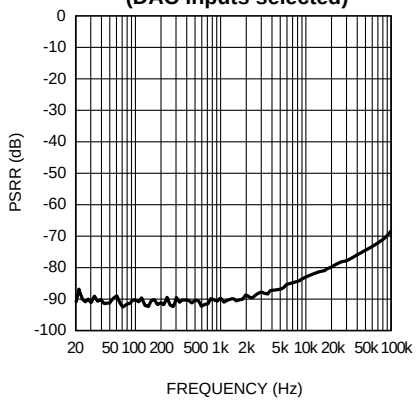


Figure 68.

CPOUT PSRR vs Frequency AV_{DD} = 3.3V, 0dB AUX (AUX inputs terminated)

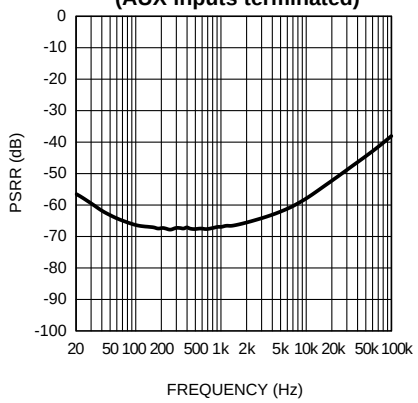


Figure 69.

CPOUT PSRR vs Frequency AV_{DD} = 5V, 0dB AUX (AUX inputs terminated)

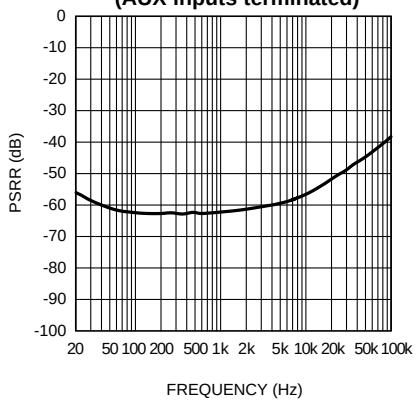


Figure 70.

CPOUT PSRR vs Frequency AV_{DD} = 3.3V, 0dB DAC (DAC inputs selected)

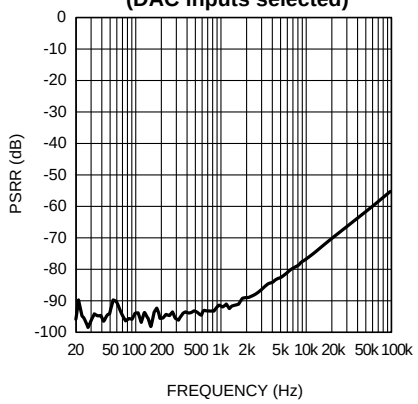


Figure 71.

CPOUT PSRR vs Frequency AV_{DD} = 5V, 0dB DAC (DAC inputs selected)

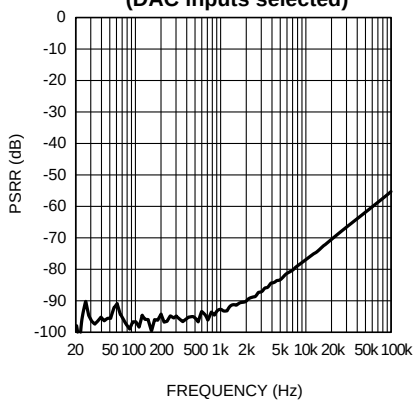


Figure 72.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Earpiece PSRR vs Frequency AV_{DD} = 3.3V, 0dB AUX (AUX inputs terminated)

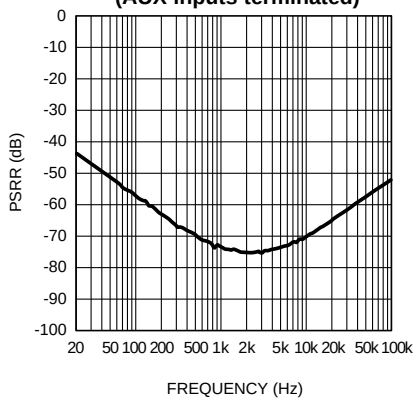


Figure 73.

Earpiece PSRR vs Frequency AV_{DD} = 5V, 0dB AUX (AUX inputs terminated)

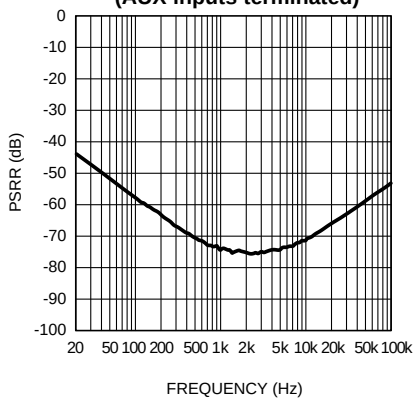


Figure 74.

Earpiece PSRR vs Frequency AV_{DD} = 3.3V, 0dB CPI (CPI input terminated)

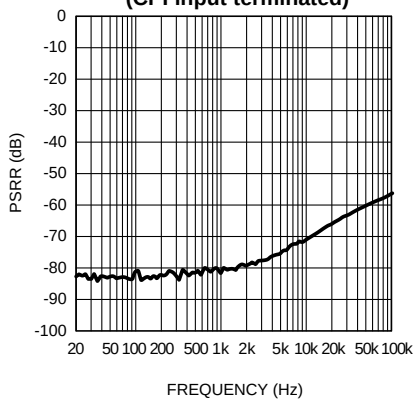


Figure 75.

Earpiece PSRR vs Frequency AV_{DD} = 5V, 0dB CPI (CPI input terminated)

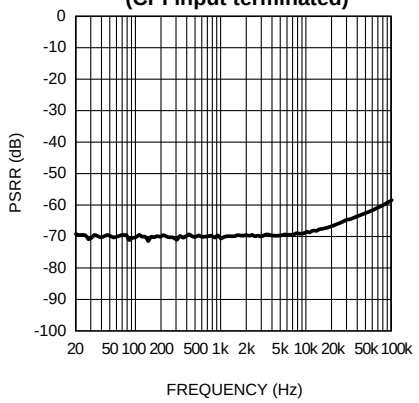


Figure 76.

Earpiece PSRR vs Frequency AV_{DD} = 3.3V, 0dB DAC (DAC input selected)

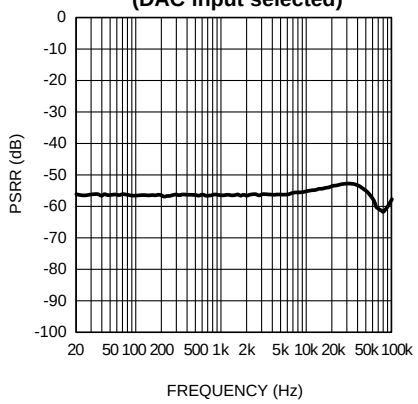


Figure 77.

Earpiece PSRR vs Frequency AV_{DD} = 5V, 0dB DAC (DAC input selected)

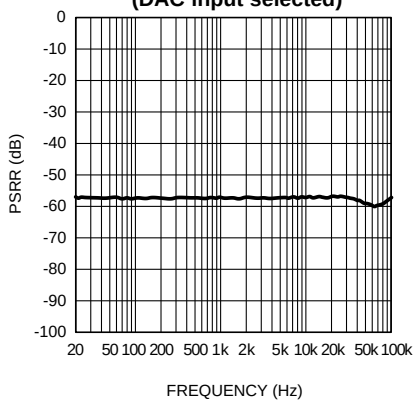


Figure 78.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone PSRR vs Frequency AV_{DD} = 3.3V, 0dB AUX, OCL 1.2V (AUX inputs terminated)

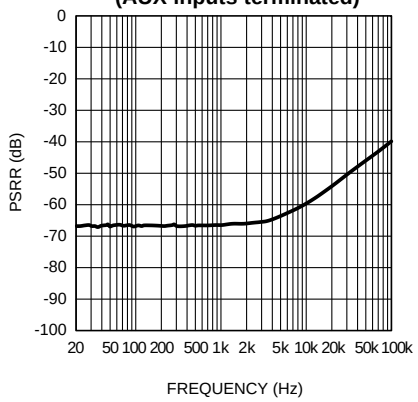


Figure 79.

Headphone PSRR vs Frequency AV_{DD} = 5V, 0dB AUX, OCL 1.2V (AUX inputs terminated)

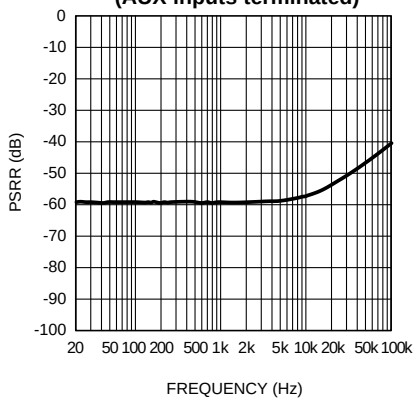


Figure 80.

Headphone PSRR vs Frequency AV_{DD} = 3.3V, 0dB CPI, OCL 1.2V (CPI input terminated)

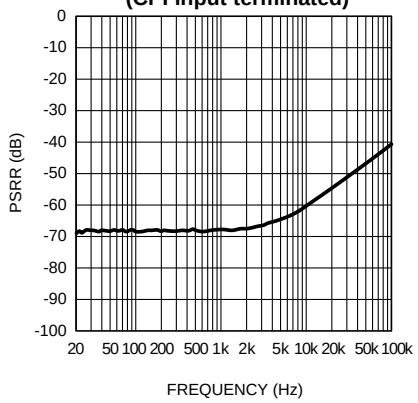


Figure 81.

Headphone PSRR vs Frequency AV_{DD} = 5V, 0dB CPI, OCL 1.2V (CPI input terminated)

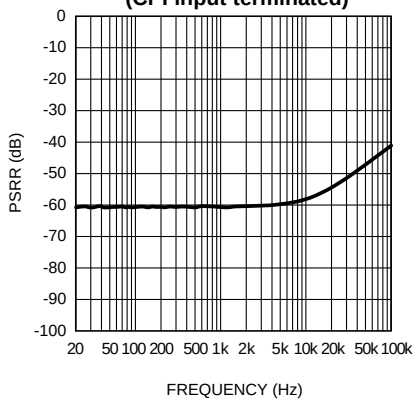


Figure 82.

Headphone PSRR vs Frequency AV_{DD} = 3.3V, 0dB ADC, OCL 1.2V (DAC input selected)

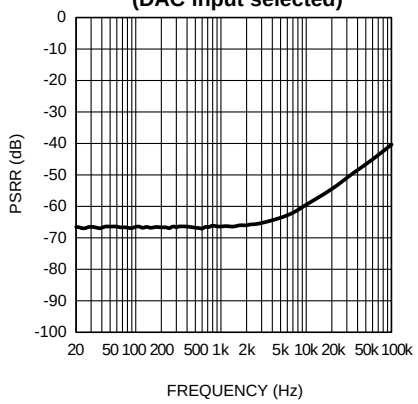


Figure 83.

Headphone PSRR vs Frequency AV_{DD} = 5V, 0dB ADC, OCL 1.2V (DAC input selected)

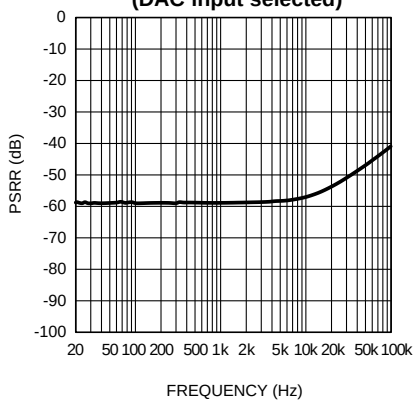


Figure 84.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone PSRR vs Frequency AV_{DD} = 3.3V, 0dB AUX, OCL 1.5V (AUX inputs terminated)

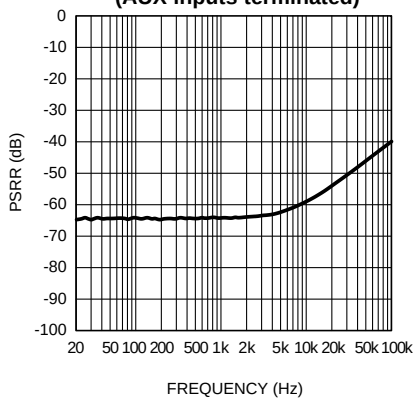


Figure 85.

Headphone PSRR vs Frequency AV_{DD} = 5V, 0dB AUX, OCL 1.5V (AUX inputs terminated)

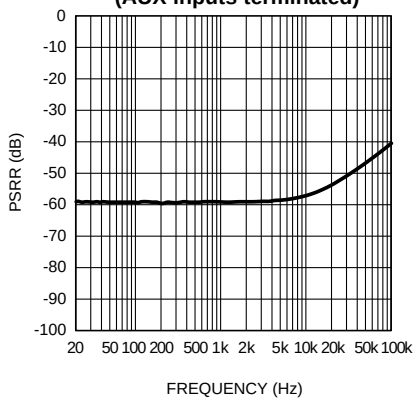


Figure 86.

Headphone PSRR vs Frequency AV_{DD} = 3.3V, 0dB CPI, OCL 1.5V (CPI input terminated)

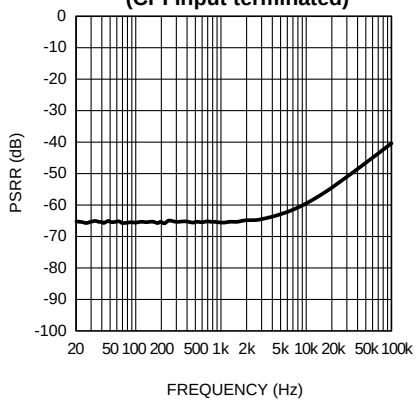


Figure 87.

Headphone PSRR vs Frequency AV_{DD} = 5V, 0dB CPI, OCL 1.5V (CPI input terminated)

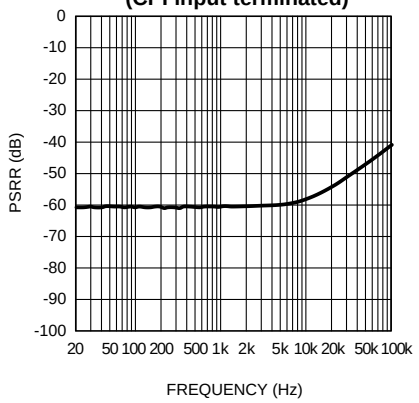


Figure 88.

Headphone PSRR vs Frequency AV_{DD} = 3.3V, 0dB DAC, OCL 1.5V (DAC input selected)

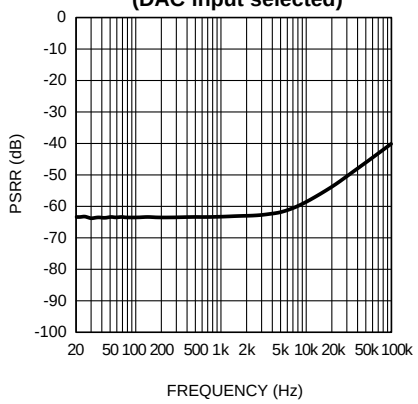


Figure 89.

Headphone PSRR vs Frequency AV_{DD} = 5V, 0dB DAC, OCL 1.5V (DAC input selected)

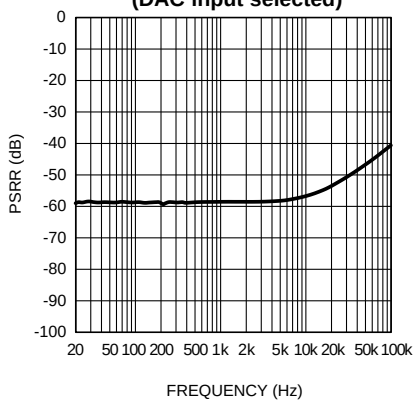


Figure 90.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone PSRR vs Frequency AV_{DD} = 3.3V, 0dB AUX, SE (AUX inputs terminated)

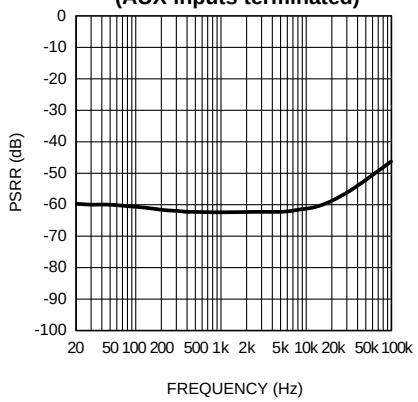


Figure 91.

Headphone PSRR vs Frequency AV_{DD} = 5V, 0dB AUX, SE (AUX inputs terminated)

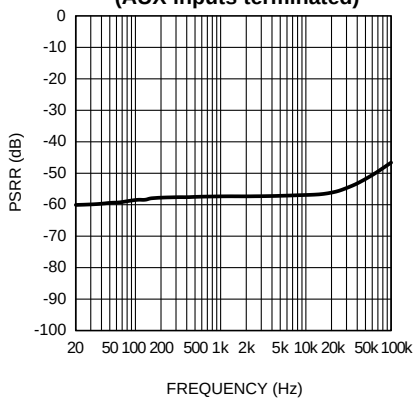


Figure 92.

Headphone PSRR vs Frequency AV_{DD} = 3.3V, 0dB CPI, SE (CPI input terminated)

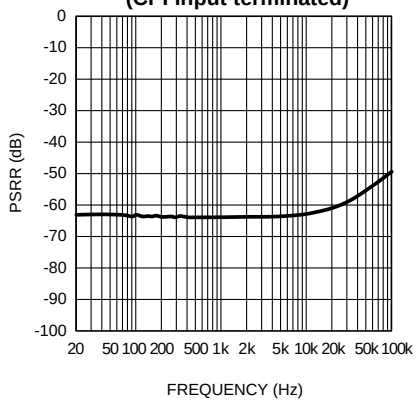


Figure 93.

Headphone PSRR vs Frequency AV_{DD} = 5V, 0dB CPI, SE (CPI input terminated)

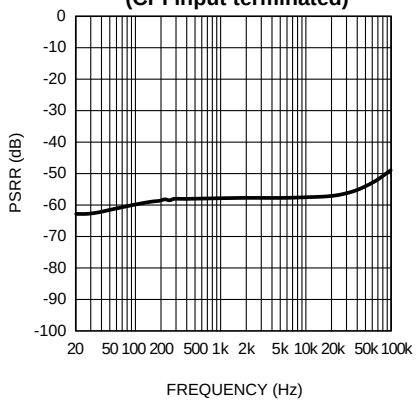


Figure 94.

Headphone PSRR vs Frequency AV_{DD} = 3.3V, 0dB DAC, SE (DAC input selected)

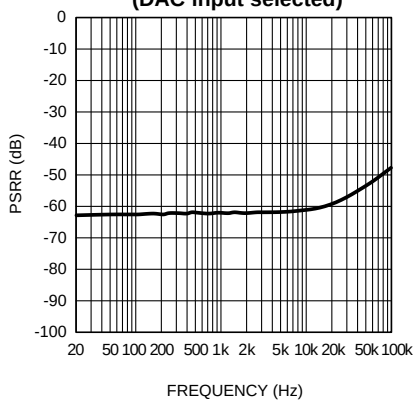


Figure 95.

Headphone PSRR vs Frequency AV_{DD} = 5V, 0dB DAC, SE (DAC input selected)

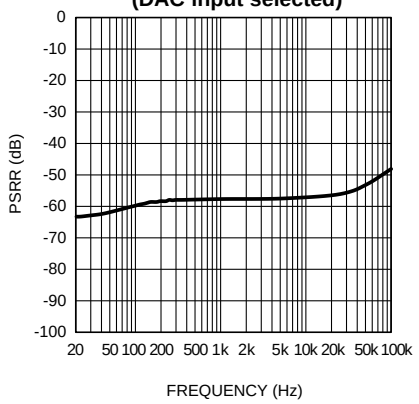


Figure 96.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Loudspeaker PSRR vs Frequency AV_{DD} = 3.3V, 0dB AUX (AUX inputs terminated)

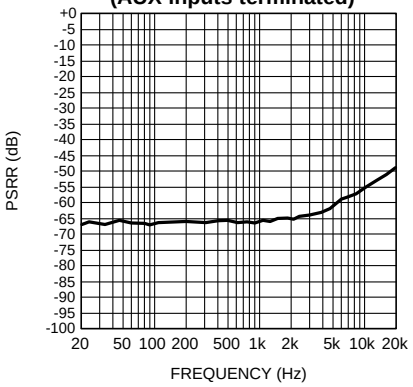


Figure 97.

Loudspeaker PSRR vs Frequency AV_{DD} = 5V, 0dB AUX (AUX inputs terminated)

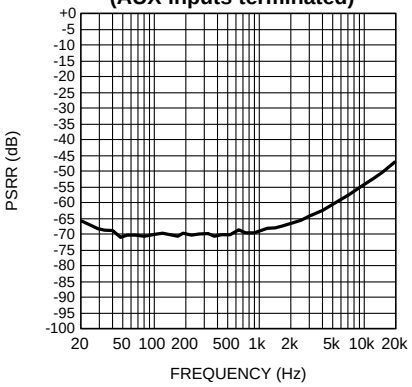


Figure 98.

Loudspeaker PSRR vs Frequency AV_{DD} = 3.3V, 0dB CPI (CPI input terminated)

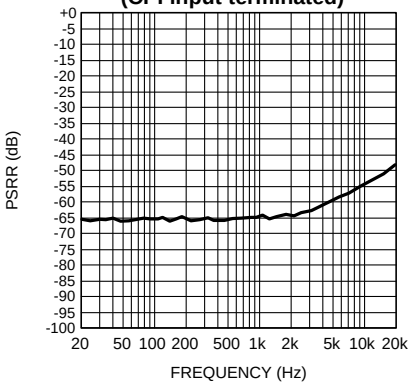


Figure 99.

Loudspeaker PSRR vs Frequency AV_{DD} = 5V, 0dB CPI (CPI input terminated)

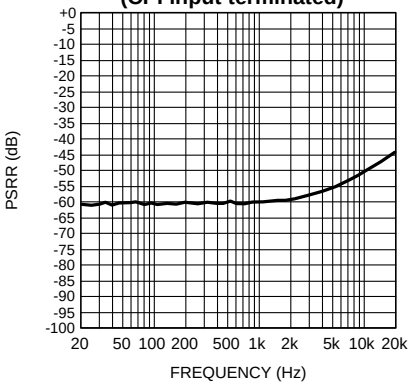


Figure 100.

Loudspeaker PSRR vs Frequency AV_{DD} = 3.3V, 0dB DAC (DAC input selected)

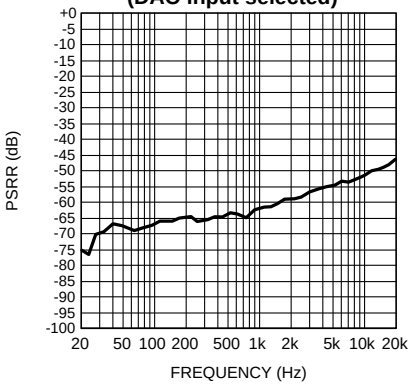


Figure 101.

Loudspeaker PSRR vs Frequency AV_{DD} = 5V, 0dB DAC (DAC input selected)

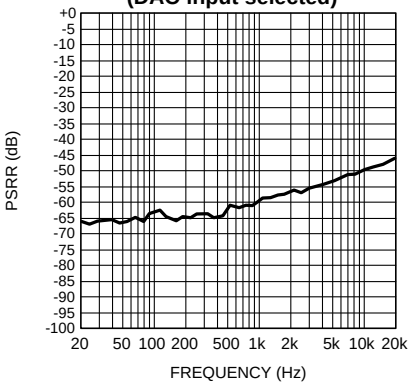


Figure 102.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

INT/EXT MICBIAS PSRR vs Frequency AV_{DD} = 3.3V, MICBIAS = 2.0V

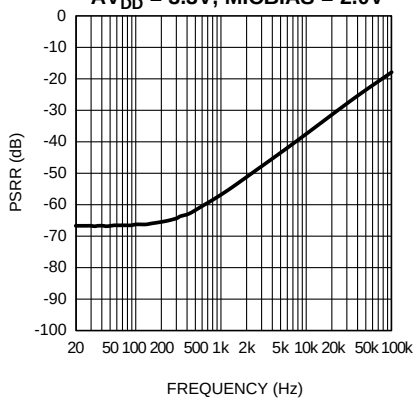


Figure 103.

INT/EXT MICBIAS PSRR vs Frequency AV_{DD} = 5V, MICBIAS = 2.0V

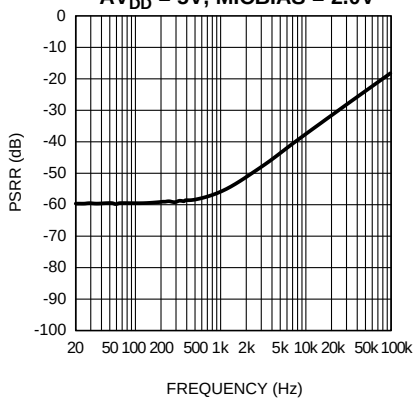


Figure 104.

INT/EXT MICBIAS PSRR vs Frequency AV_{DD} = 3.3V, MICBIAS = 2.5V

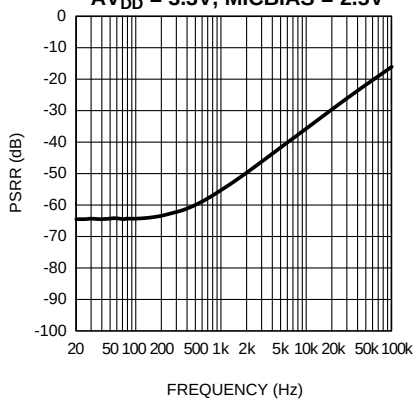


Figure 105.

INT/EXT MICBIAS PSRR vs Frequency AV_{DD} = 5V, MICBIAS = 2.5V

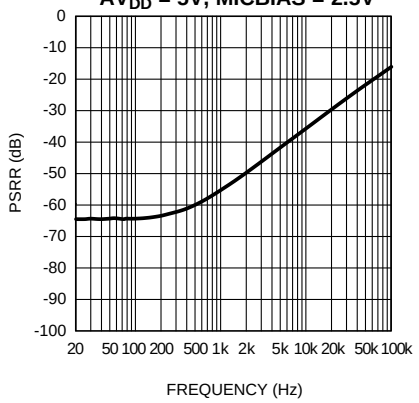


Figure 106.

INT/EXT MICBIAS PSRR vs Frequency AV_{DD} = 3.3V, MICBIAS = 2.8V

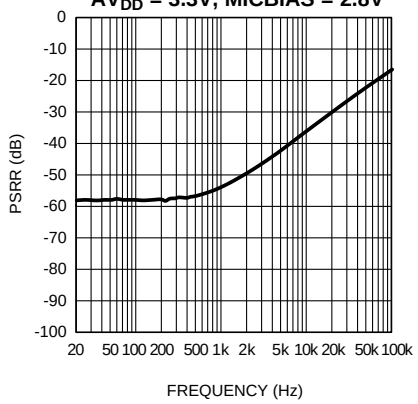


Figure 107.

INT/EXT MICBIAS PSRR vs Frequency AV_{DD} = 5V, MICBIAS = 2.8V

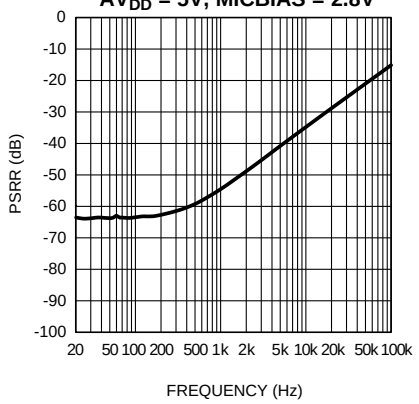


Figure 108.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

INT/EXT MICBIAS PSRR vs Frequency
AV_{DD} = 5V, MICBIAS = 3.3V

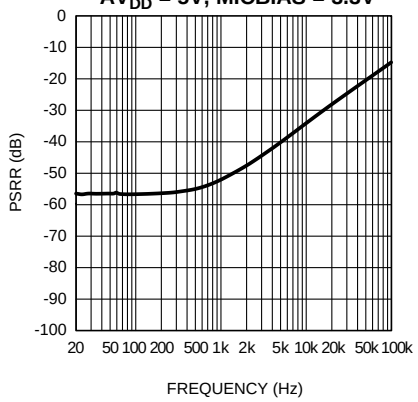


Figure 109.

AUXOUT THD+N vs Frequency
AV_{DD} = 3.3V, 0dB, V_{OUT} = 1V_{RMS}, 5kΩ

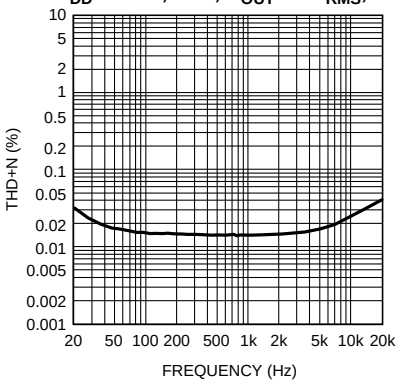


Figure 110.

AUXOUT THD+N vs Frequency
AV_{DD} = 5V, 0dB, V_{OUT} = 1V_{RMS}, 5kΩ

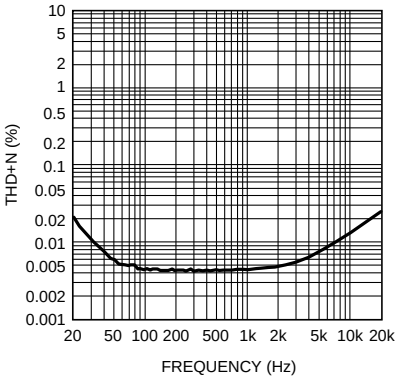


Figure 111.

CPOUT THD+N vs Frequency
AV_{DD} = 3.3V, 0dB, V_{OUT} = 1V_{RMS}, 5kΩ

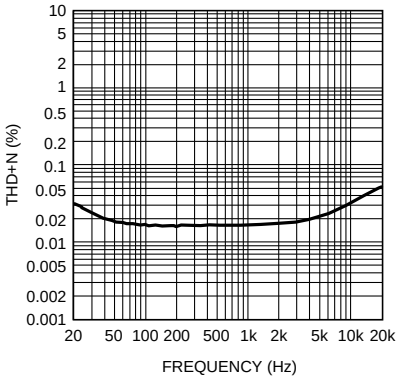


Figure 112.

CPOUT THD+N vs Frequency
AV_{DD} = 5V, 0dB, V_{OUT} = 1V_{RMS}, 5kΩ

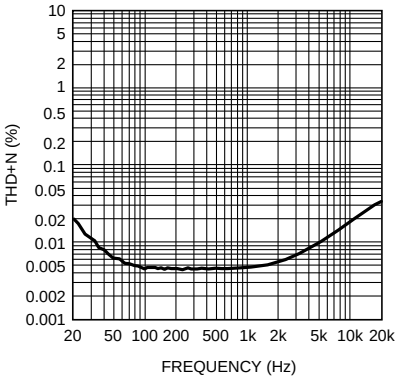


Figure 113.

Earpiece THD+N vs Frequency
AV_{DD} = 3.3V, 0dB, P_{OUT} = 500mW, 32Ω

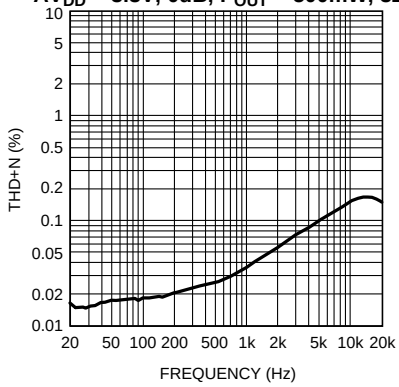


Figure 114.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Earpiece THD+N vs Frequency AV_{DD} = 5V, 0dB, P_{OUT} = 50mW, 32Ω

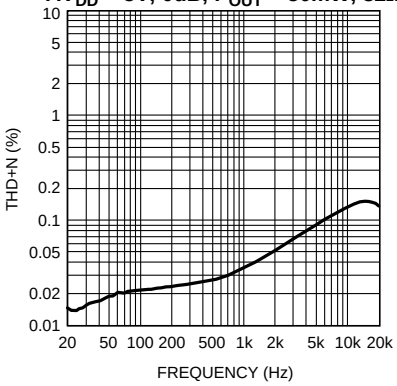


Figure 115.

Headphone THD+N vs Frequency AV_{DD} = 3.3V, OCL 1.5V, 0dB P_{OUT} = 7.5mW, 32Ω

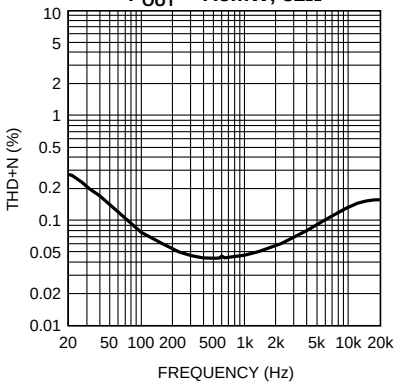


Figure 116.

Headphone THD+N vs Frequency AV_{DD} = 5V, OCL 1.5V, 0dB P_{OUT} = 10mW, 32Ω

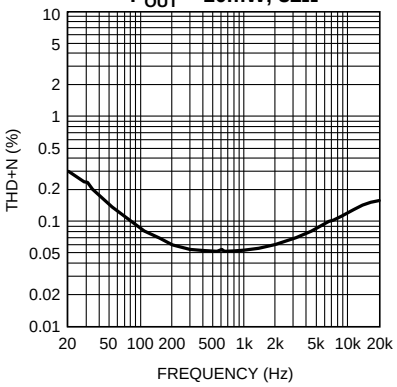


Figure 117.

Headphone THD+N vs Frequency AV_{DD} = 3.3V, OCL 1.2V, 0dB P_{OUT} = 7.5mW, 32Ω

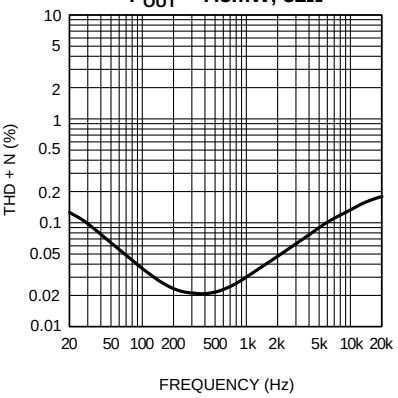


Figure 118.

Headphone THD+N vs Frequency AV_{DD} = 5V, OCL 1.2V, 0dB P_{OUT} = 10mW, 32Ω

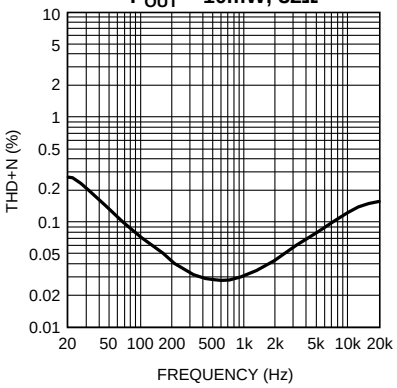


Figure 119.

Headphone THD+N vs Frequency AV_{DD} = 3.3V, SE, 0dB P_{OUT} = 7.5mW, 32Ω

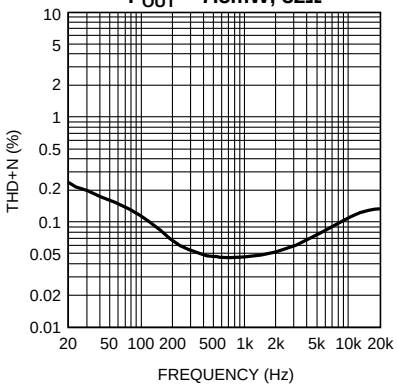


Figure 120.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone THD+N vs Frequency AV_{DD} = 5V, SE, 0dB P_{OUT} = 10mW, 32Ω

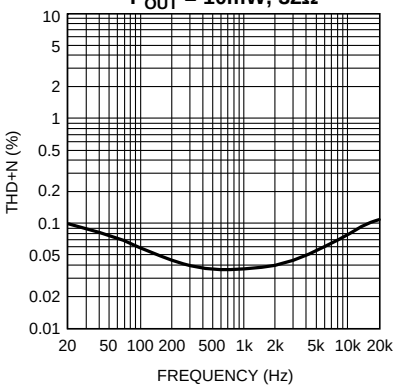


Figure 121.

Loudspeaker THD+N vs Frequency AV_{DD} = 3.3V, P_{OUT} = 400mW 15µH+8Ω+15µH

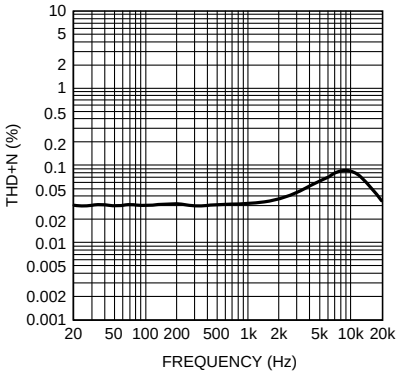


Figure 122.

Loudspeaker THD+N vs Frequency AV_{DD} = 5V, P_{OUT} = 400mW 15µH+8Ω+15µH

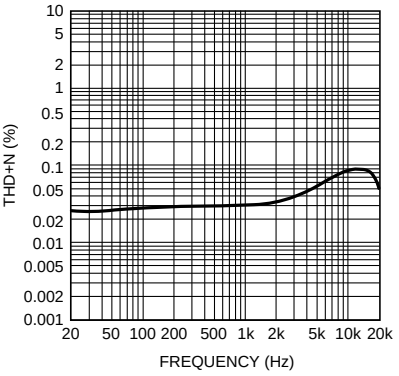


Figure 123.

Earpiece THD+N vs Output Power AV_{DD} = 3.3V, 0dB AUX f_{OUT} = 1kHz, 16Ω

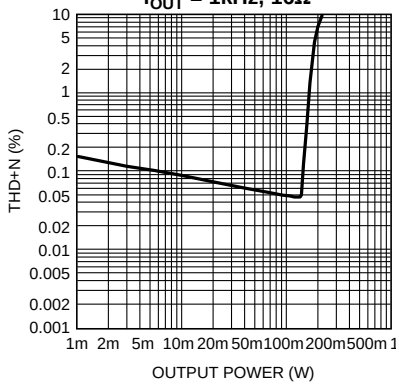


Figure 124.

Earpiece THD+N vs Output Power AV_{DD} = 5V, 0dB AUX f_{OUT} = 1kHz, 16Ω

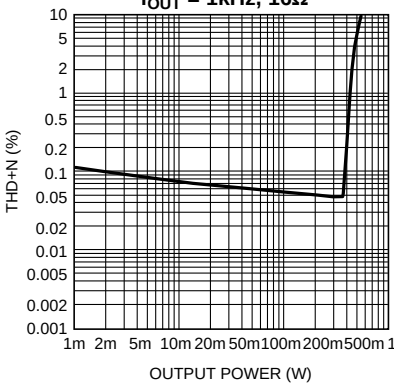


Figure 125.

Earpiece THD+N vs Output Power AV_{DD} = 3.3V, 0dB AUX f_{OUT} = 1kHz, 32Ω

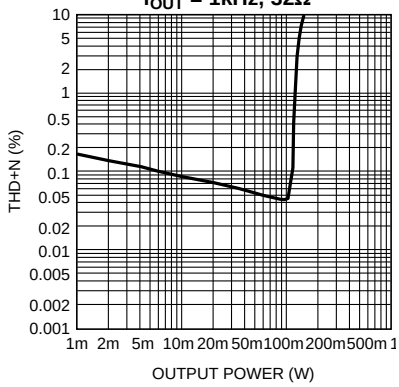


Figure 126.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Earpiece THD+N vs Output Power AV_{DD} = 5V, 0dB AUX f_{OUT} = 1kHz, 32Ω

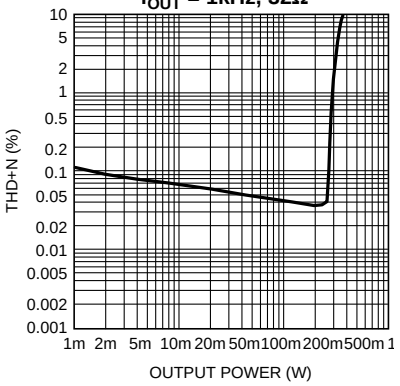


Figure 127.

Earpiece THD+N vs Output Power AV_{DD} = 3.3V, 0dB CPI f_{OUT} = 1kHz, 16Ω

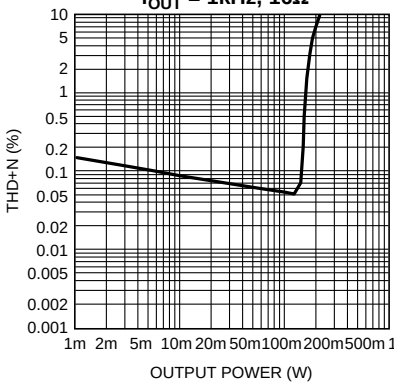


Figure 128.

Earpiece THD+N vs Output Power AV_{DD} = 5V, 0dB CPI f_{OUT} = 1kHz, 16Ω

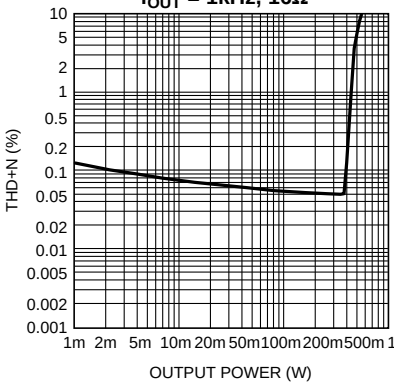


Figure 129.

Earpiece THD+N vs Output Power AV_{DD} = 3.3V, 0dB CPI f_{OUT} = 1kHz, 32Ω

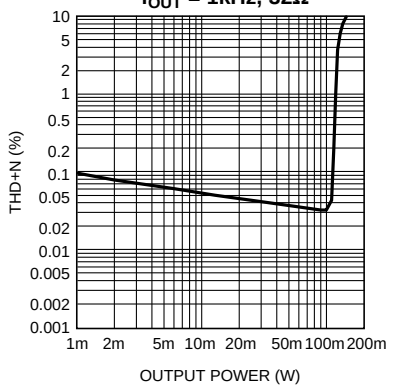


Figure 130.

Earpiece THD+N vs Output Power AV_{DD} = 5V, 0dB CPI f_{OUT} = 1kHz, 32Ω

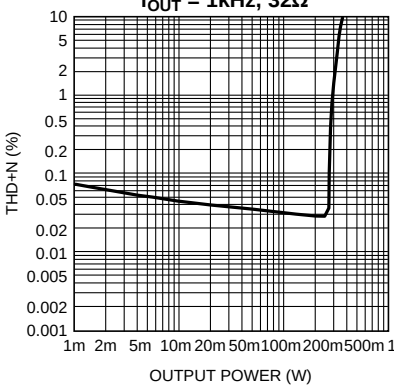


Figure 131.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 0dB DAC f_{OUT} = 1kHz, 16Ω

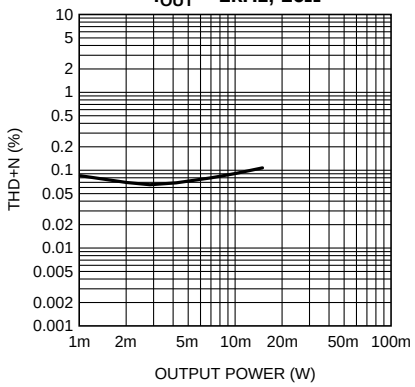


Figure 132.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 0dB DAC f_{OUT} = 1kHz, 16Ω

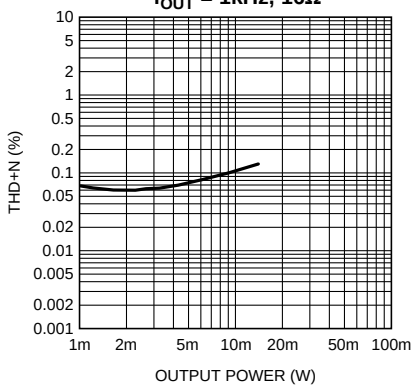


Figure 133.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 0dB DAC f_{OUT} = 1kHz, 32Ω

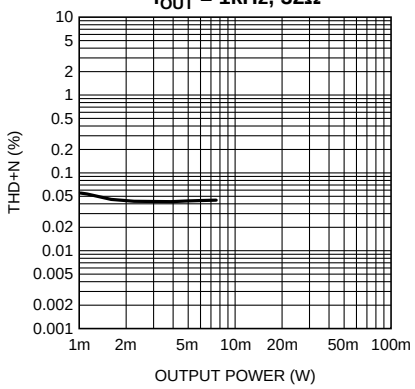


Figure 134.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 0dB DAC f_{OUT} = 1kHz, 32Ω

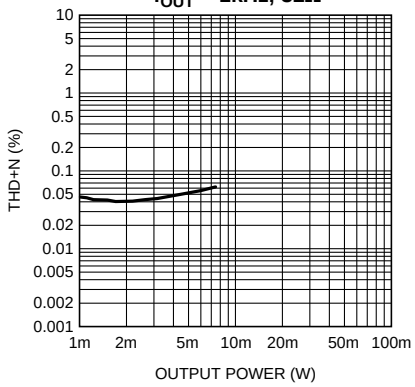


Figure 135.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 12dB DAC f_{OUT} = 1kHz, 16Ω

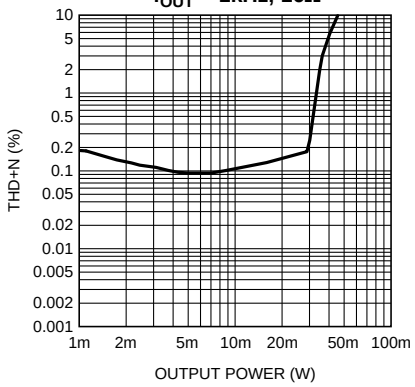


Figure 136.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 12dB DAC f_{OUT} = 1kHz, 16Ω

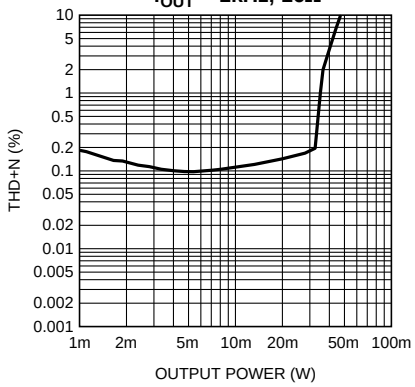


Figure 137.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 12dB DAC f_{OUT} = 1kHz, 32Ω

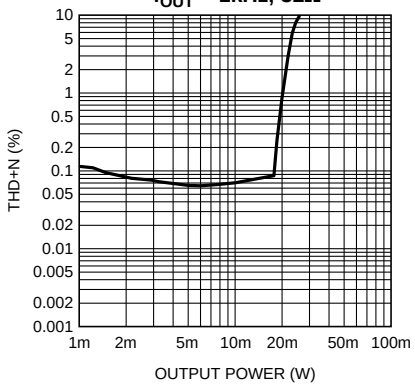


Figure 138.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 12dB DAC f_{OUT} = 1kHz, 32Ω

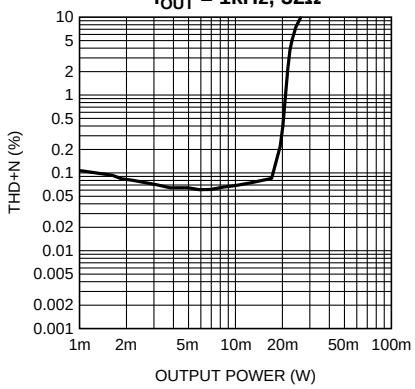


Figure 139.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 0dB DAC f_{OUT} = 1kHz, 16Ω

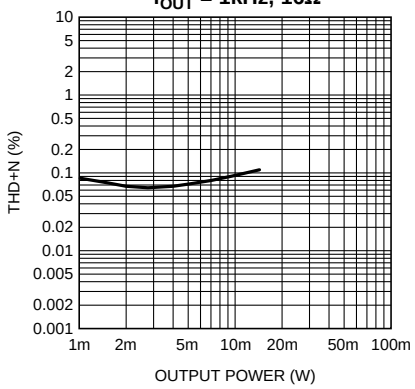


Figure 140.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 0dB DAC f_{OUT} = 1kHz, 16Ω

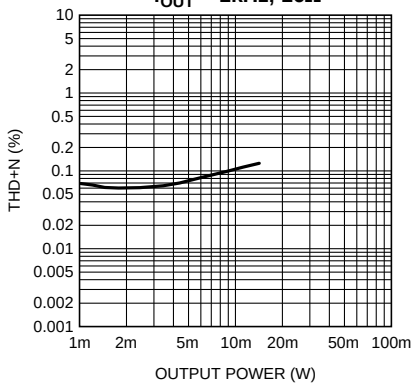


Figure 141.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 0dB DAC f_{OUT} = 1kHz, 32Ω

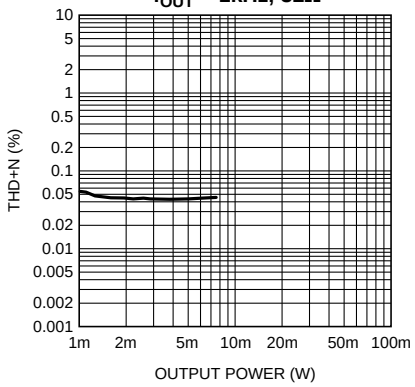


Figure 142.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 0dB DAC f_{OUT} = 1kHz, 32Ω

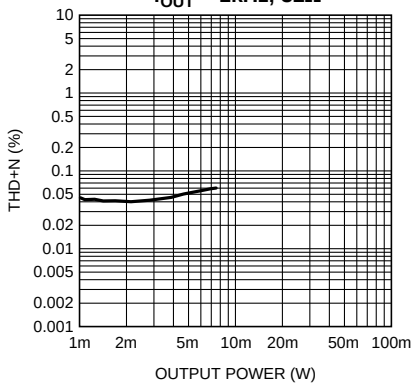


Figure 143.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 12dB DAC f_{OUT} = 1kHz, 16Ω

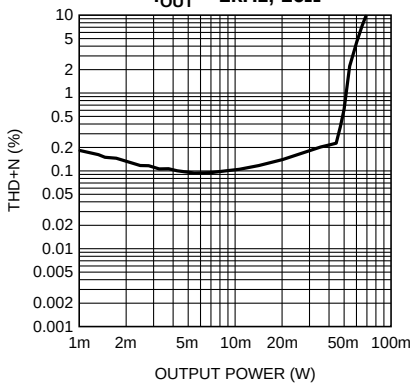


Figure 144.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 12dB DAC f_{OUT} = 1kHz, 16Ω

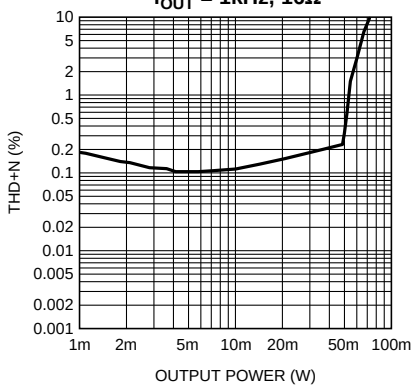


Figure 145.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 12dB DAC f_{OUT} = 1kHz, 32Ω

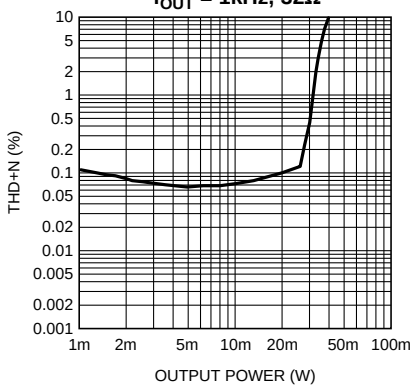


Figure 146.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 12dB DAC f_{OUT} = 1kHz, 32Ω

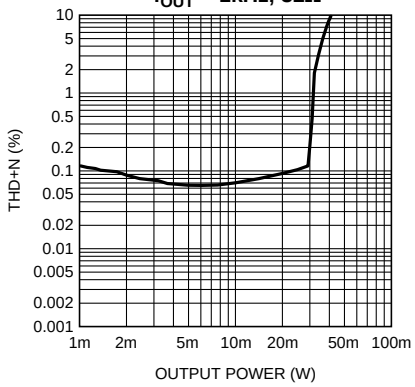


Figure 147.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 0dB DAC f_{OUT} = 1kHz, 16Ω

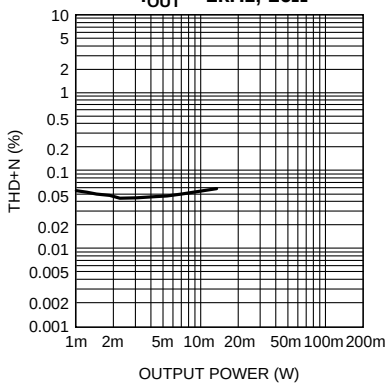


Figure 148.

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 0dB DAC f_{OUT} = 1kHz, 16Ω

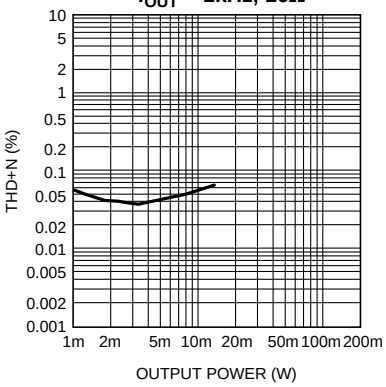


Figure 149.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 0dB DAC f_{OUT} = 1kHz, 32Ω

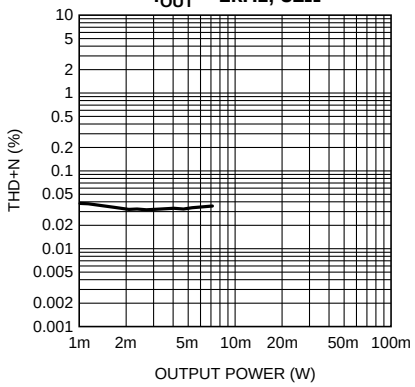


Figure 150.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 0dB DAC f_{OUT} = 1kHz, 32Ω

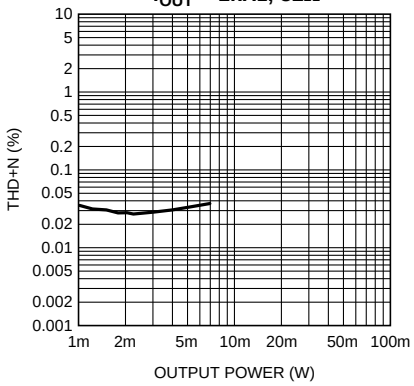


Figure 151.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 12dB DAC f_{OUT} = 1kHz, 16Ω

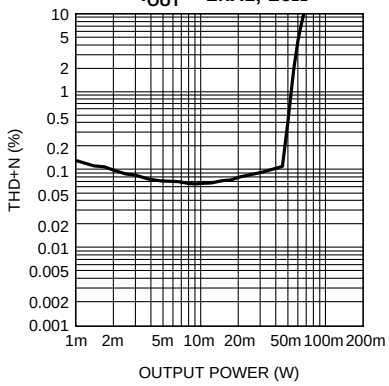


Figure 152.

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 12dB DAC f_{OUT} = 1kHz, 16Ω

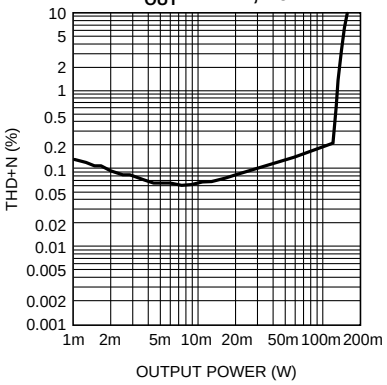


Figure 153.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 12dB DAC f_{OUT} = 1kHz, 32Ω

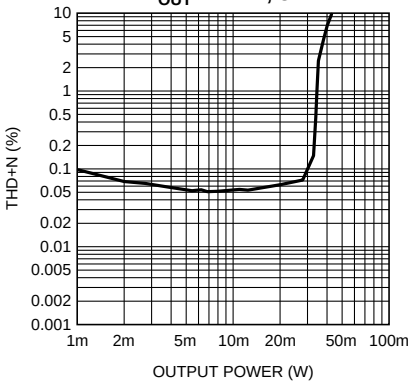


Figure 154.

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 12dB DAC f_{OUT} = 1kHz, 32Ω

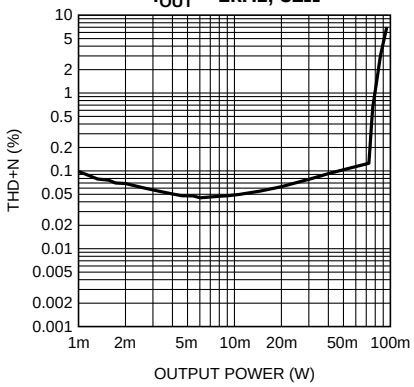


Figure 155.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 0dB AUX f_{OUT} = 1kHz, 16Ω

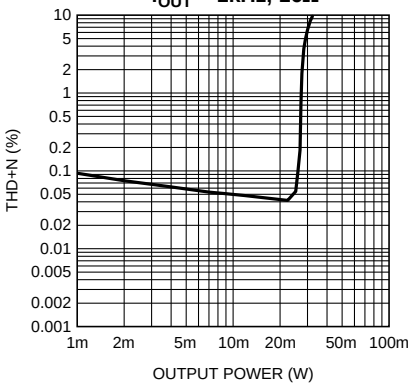


Figure 156.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 12dB AUX f_{OUT} = 1kHz, 16Ω

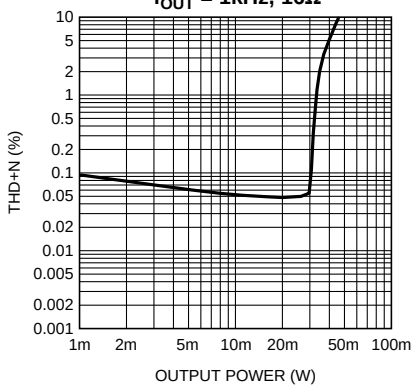


Figure 157.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 0dB AUX f_{OUT} = 1kHz, 16Ω

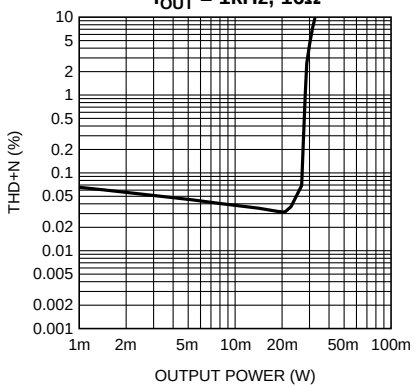


Figure 158.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 12dB AUX f_{OUT} = 1kHz, 16Ω

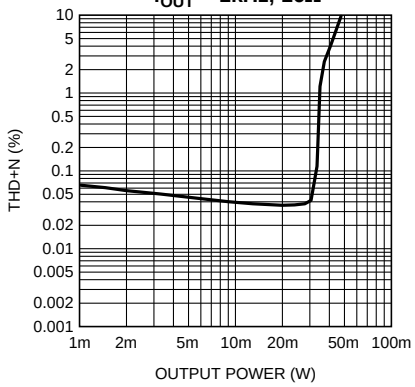


Figure 159.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 0dB AUX f_{OUT} = 1kHz, 32Ω

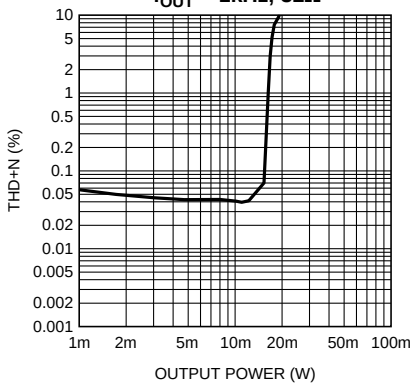


Figure 160.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 12dB AUX f_{OUT} = 1kHz, 32Ω

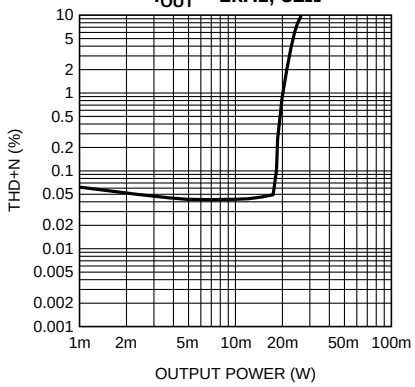


Figure 161.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 0dB AUX f_{OUT} = 1kHz, 32Ω

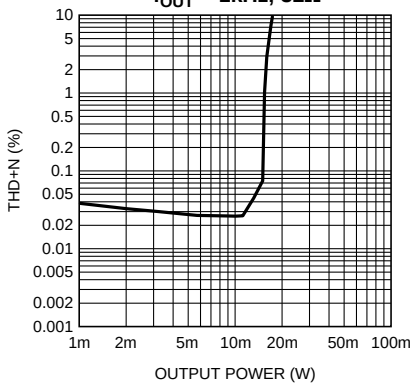


Figure 162.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 12dB AUX f_{OUT} = 1kHz, 32Ω

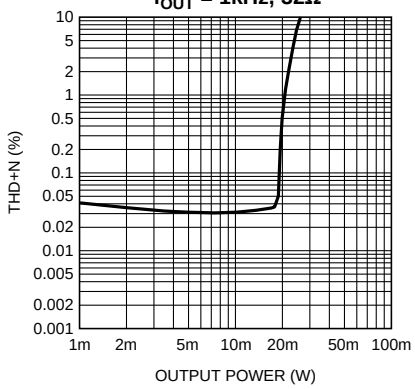


Figure 163.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 0dB CPI f_{OUT} = 1kHz, 16Ω

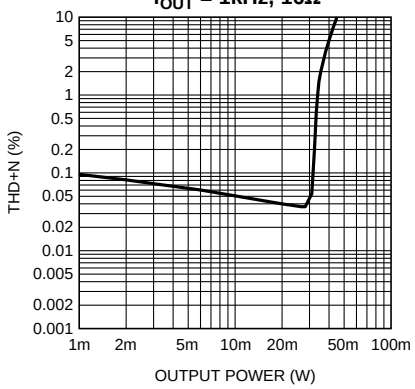


Figure 164.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 0dB CPI f_{OUT} = 1kHz, 16Ω

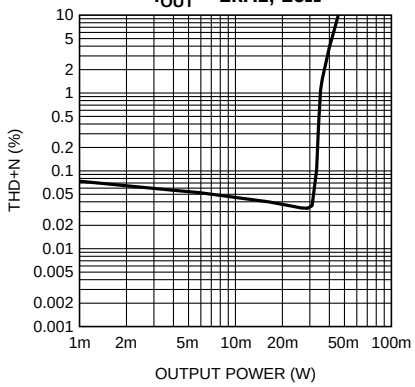


Figure 165.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.2V, 0dB CPI f_{OUT} = 1kHz, 32Ω

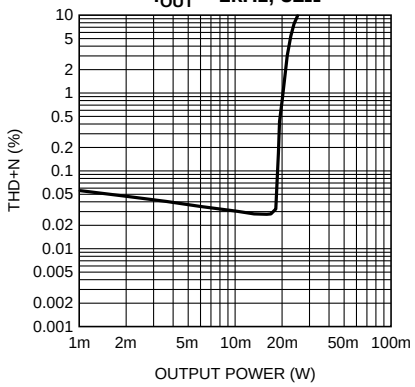


Figure 166.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.2V, 0dB CPI f_{OUT} = 1kHz, 32Ω

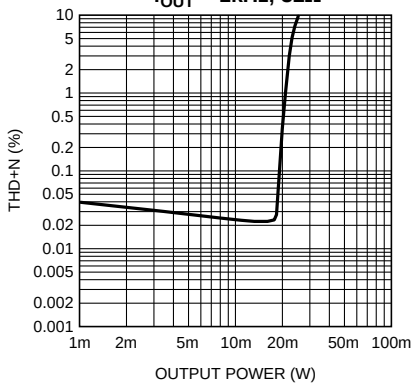


Figure 167.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 0dB AUX f_{OUT} = 1kHz, 16Ω

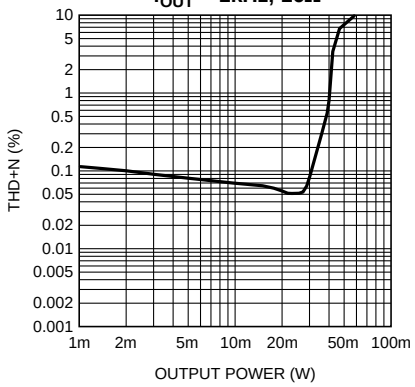


Figure 168.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 12dB AUX f_{OUT} = 1kHz, 16Ω

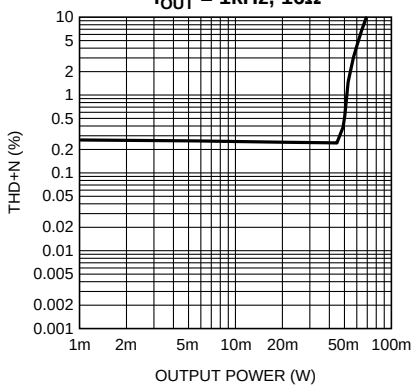


Figure 169.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 0dB AUX f_{OUT} = 1kHz, 16Ω

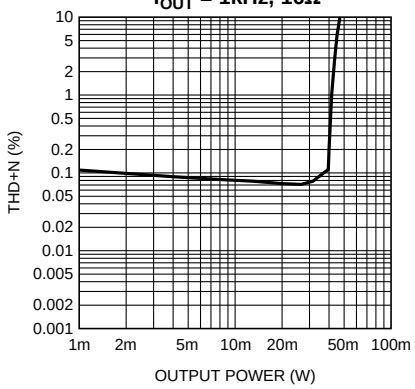


Figure 170.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 12dB AUX f_{OUT} = 1kHz, 16Ω

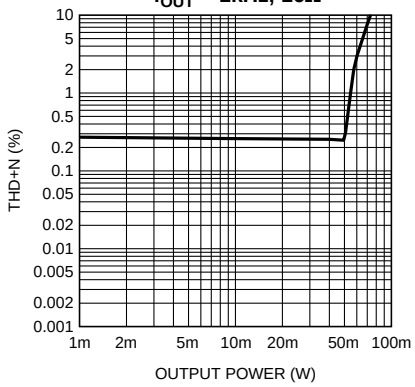


Figure 171.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 0dB AUX f_{OUT} = 1kHz, 32Ω

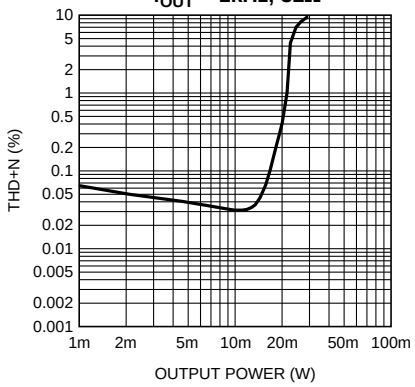


Figure 172.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 12dB AUX f_{OUT} = 1kHz, 32Ω

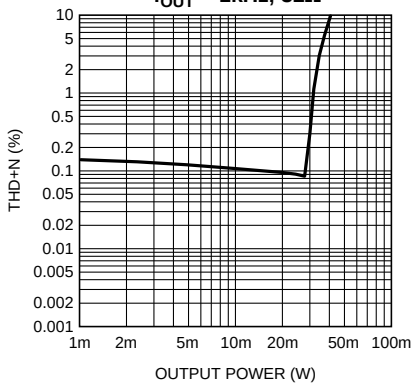


Figure 173.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 0dB AUX f_{OUT} = 1kHz, 32Ω

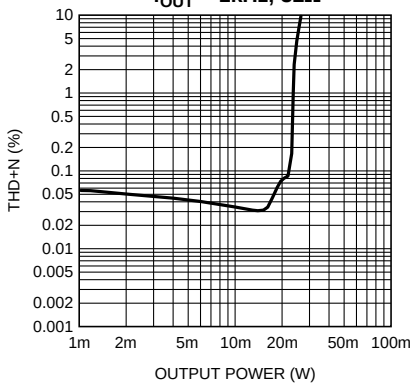


Figure 174.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 12dB AUX f_{OUT} = 1kHz, 32Ω

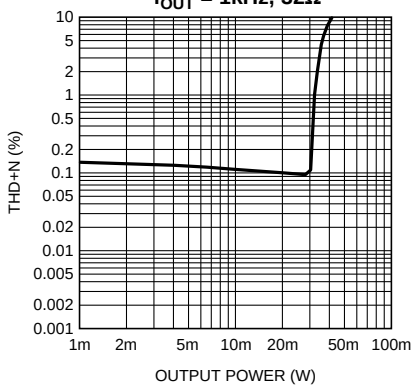


Figure 175.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 0dB CPI f_{OUT} = 1kHz, 16Ω

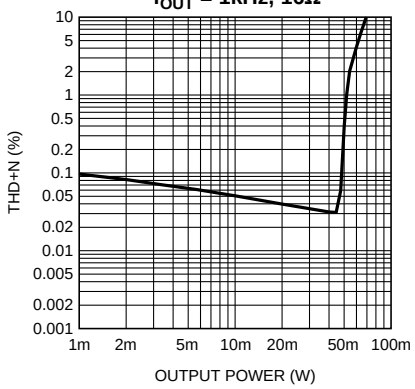


Figure 176.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 0dB CPI f_{OUT} = 1kHz, 16Ω

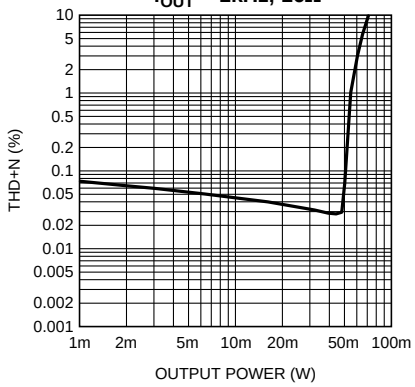


Figure 177.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, OCL 1.5V, 0dB CPI f_{OUT} = 1kHz, 32Ω

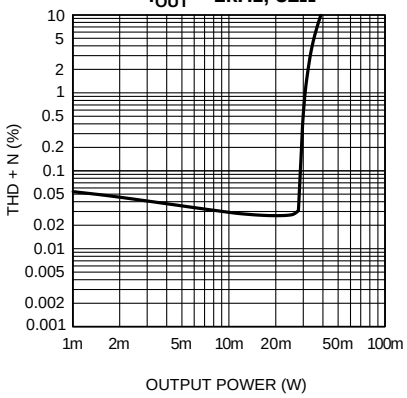


Figure 178.

Headphone THD+N vs Output Power AV_{DD} = 5V, OCL 1.5V, 0dB CPI f_{OUT} = 1kHz, 32Ω

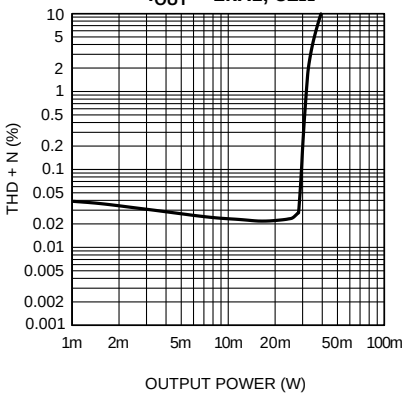


Figure 179.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 0dB AUX f_{OUT} = 1kHz, 16Ω

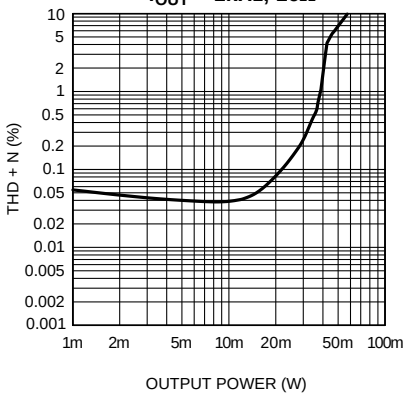


Figure 180.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 0dB AUX f_{OUT} = 1kHz, 16Ω

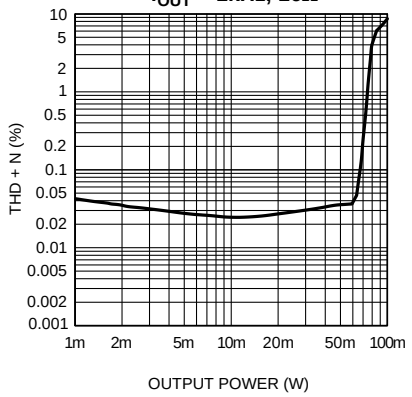


Figure 181.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 0dB AUX f_{OUT} = 1kHz, 32Ω

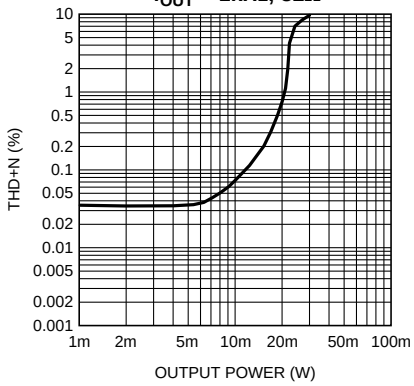


Figure 182.

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 0dB AUX f_{OUT} = 1kHz, 32Ω

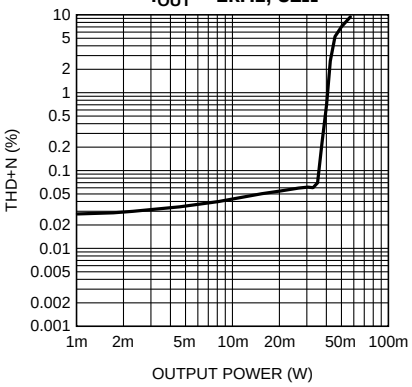


Figure 183.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 0dB CPI f_{OUT} = 1kHz, 16Ω

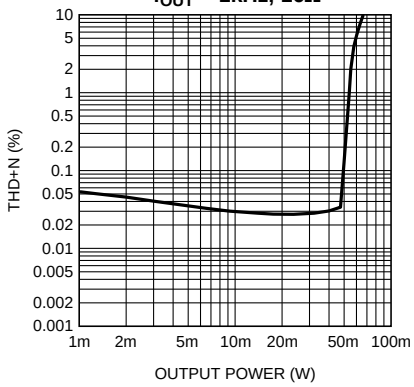


Figure 184.

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 0dB CPI f_{OUT} = 1kHz, 16Ω

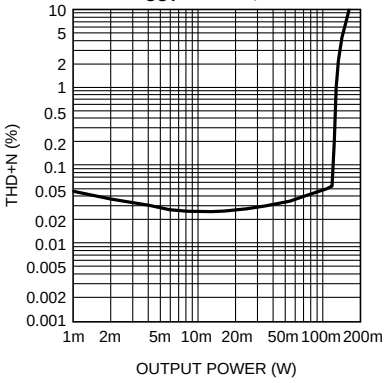


Figure 185.

Headphone THD+N vs Output Power AV_{DD} = 3.3V, SE, 0dB CPI f_{OUT} = 1kHz, 32Ω

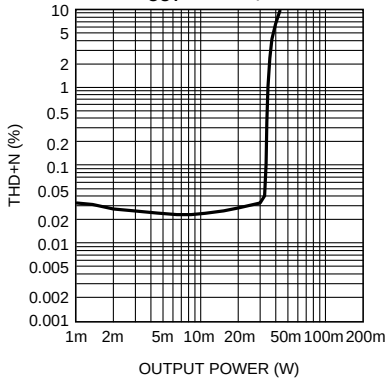


Figure 186.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone THD+N vs Output Power AV_{DD} = 5V, SE, 0dB CPI f_{OUT} = 1kHz, 32Ω

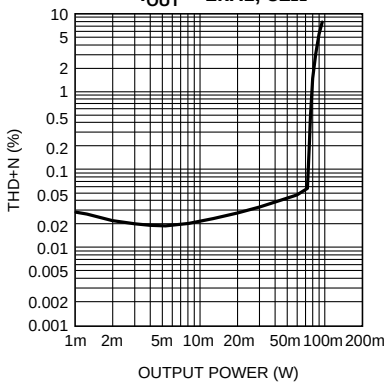


Figure 187.

Loudspeaker THD+N vs Output Power AV_{DD} = 3.3V, 0dB AUX f_{OUT} = 1kHz, 15µH+8Ω+15µH

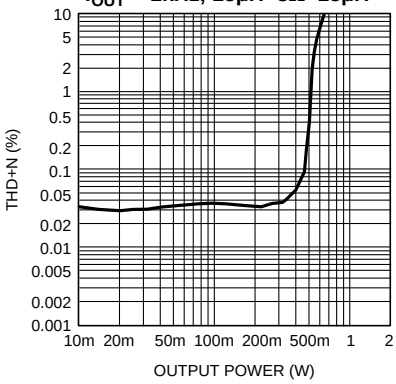


Figure 188.

Loudspeaker THD+N vs Output Power AV_{DD} = 4.2V, 0dB AUX f_{OUT} = 1kHz, 15µH+8Ω+15µH

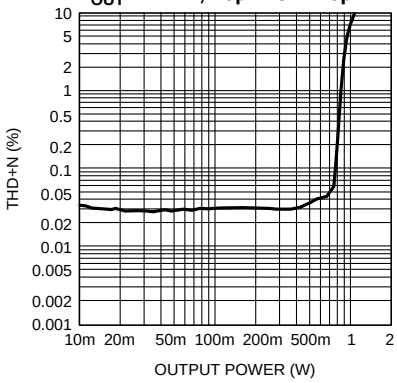


Figure 189.

Loudspeaker THD+N vs Output Power AV_{DD} = 5V, 0dB AUX f_{OUT} = 1kHz, 15µH+8Ω+15µH

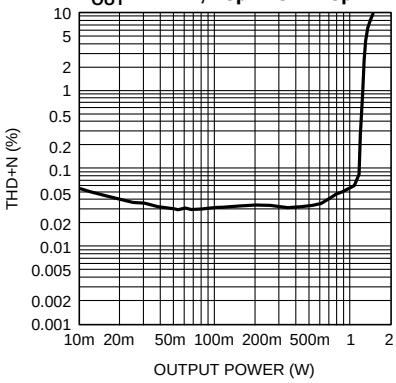


Figure 190.

Loudspeaker THD+N vs Output Power AV_{DD} = 3.3V, 0dB CPI f_{OUT} = 1kHz, 15µH+8Ω+15µH

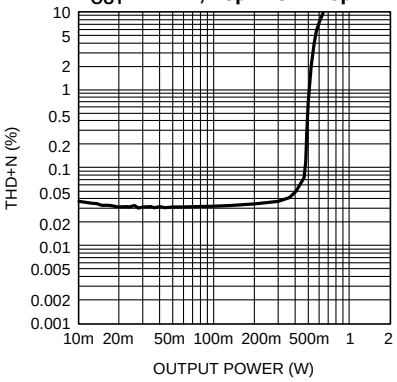


Figure 191.

Loudspeaker THD+N vs Output Power AV_{DD} = 4.2V, 0dB CPI f_{OUT} = 1kHz, 15µH+8Ω+15µH

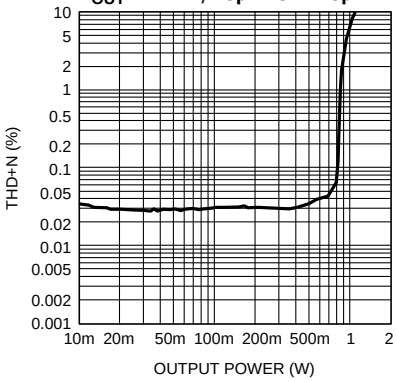


Figure 192.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Loudspeaker THD+N vs Output Power AV_{DD} = 5V, 0dB CPI f_{OUT} = 1kHz, 15µH+8Ω+15µH

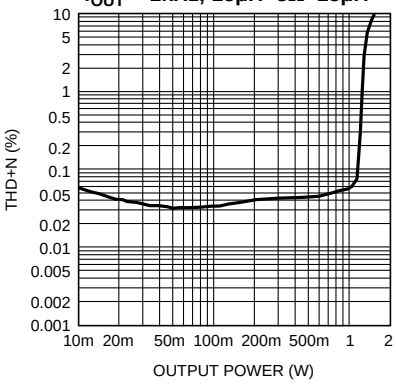


Figure 193.

Loudspeaker THD+N vs Output Power AV_{DD} = 3.3V, 0dB DAC f_{OUT} = 1kHz, 15µH+8Ω+15µH

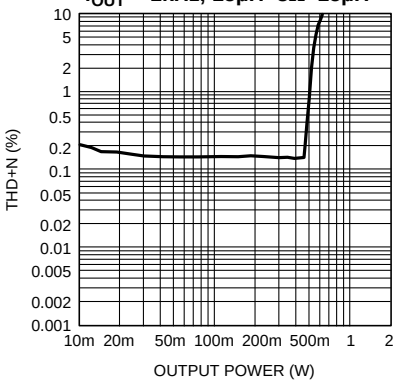


Figure 194.

Loudspeaker THD+N vs Output Power AV_{DD} = 4.2V, 0dB DAC f_{OUT} = 1kHz, 15µH+8Ω+15µH

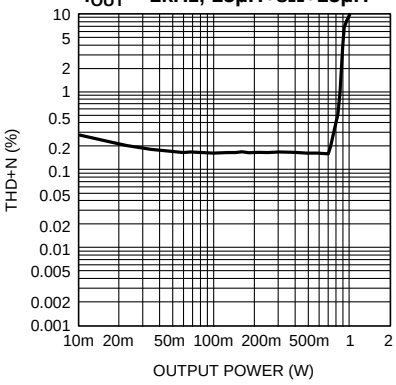


Figure 195.

Loudspeaker THD+N vs Output Power AV_{DD} = 5V, 0dB DAC f_{OUT} = 1kHz, 15µH+8Ω+15µH

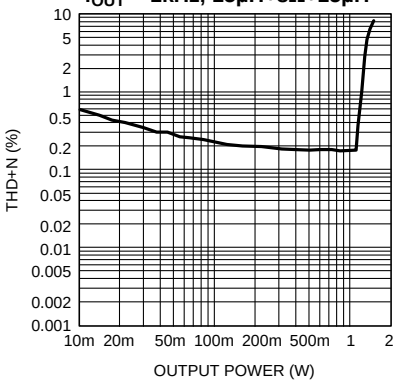


Figure 196.

AUXOUT THD+N vs Output Voltage AV_{DD} = 3.3V, 0dB AUX f_{OUT} = 1kHz, 5kΩ

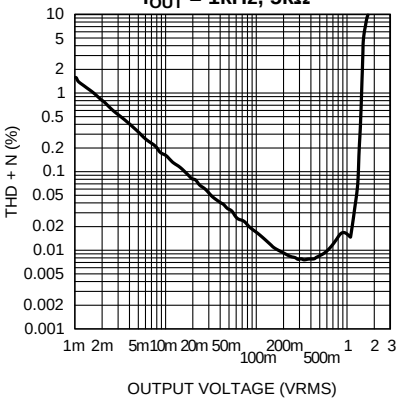


Figure 197.

AUXOUT THD+N vs Output Voltage AV_{DD} = 5V, 0dB AUX f_{OUT} = 1kHz, 5kΩ

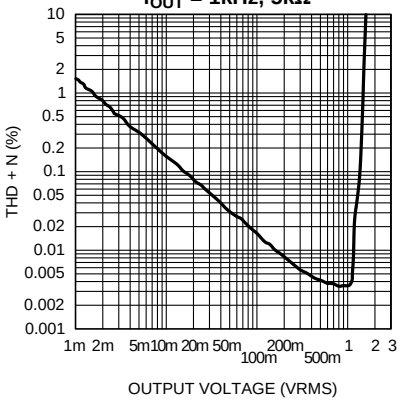


Figure 198.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

AUXOUT THD+N vs Output Voltage AV_{DD} = 3.3V, 0dB CPI f_{OUT} = 1kHz, 5kΩ

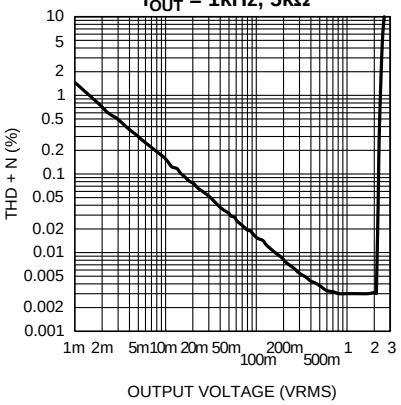


Figure 199.

AUXOUT THD+N vs Output Voltage AV_{DD} = 5V, 0dB CPI f_{OUT} = 1kHz, 5kΩ

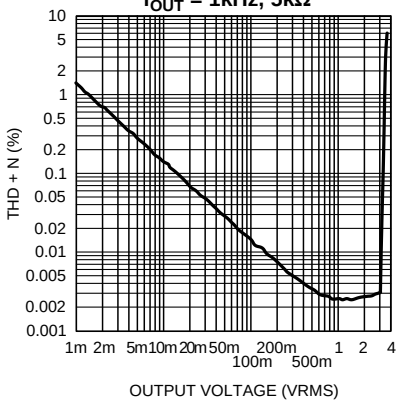


Figure 200.

AUXOUT THD+N vs Output Voltage AV_{DD} = 3.3V, 0dB DAC f_{OUT} = 1kHz, 5kΩ

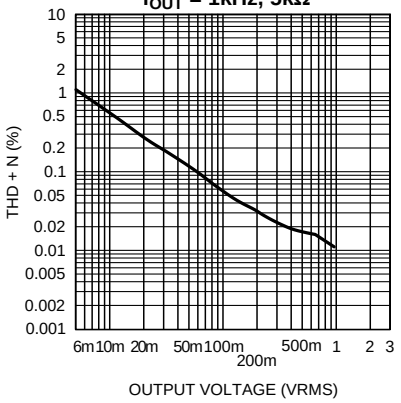


Figure 201.

AUXOUT THD+N vs Output Voltage AV_{DD} = 5V, 0dB DAC f_{OUT} = 1kHz, 5kΩ

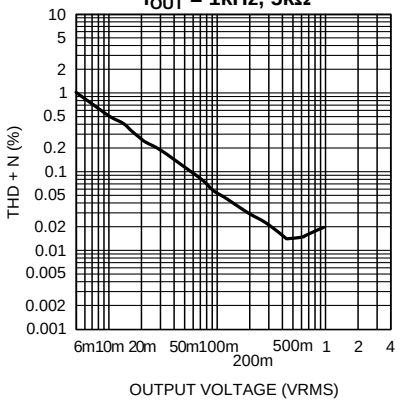


Figure 202.

AUXOUT THD+N vs Output Voltage AV_{DD} = 3.3V, 12dB DAC f_{OUT} = 1kHz, 5kΩ

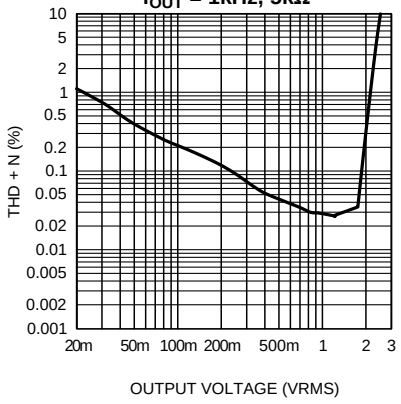


Figure 203.

AUXOUT THD+N vs Output Voltage AV_{DD} = 5V, 12dB DAC f_{OUT} = 1kHz, 5kΩ

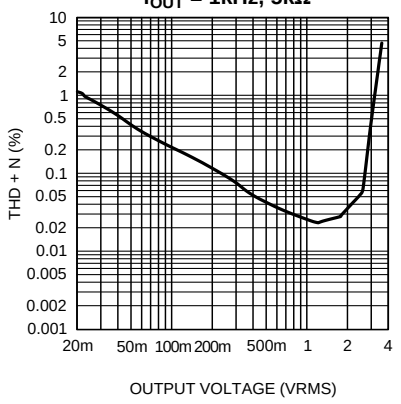


Figure 204.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

CPOUT THD+N vs Output Voltage AV_{DD} = 3.3V, 0dB AUX f_{OUT} = 1kHz, 5kΩ

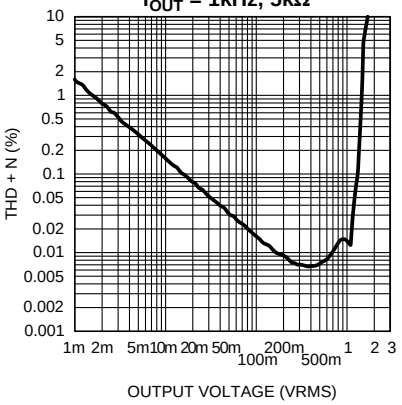


Figure 205.

CPOUT THD+N vs Output Voltage AV_{DD} = 5V, 0dB AUX f_{OUT} = 1kHz, 5kΩ

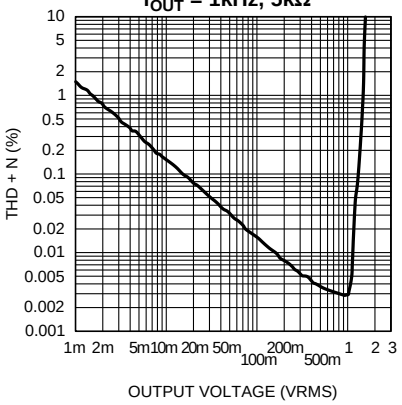


Figure 206.

CPOUT THD+N vs Output Voltage AV_{DD} = 3.3V, 0dB DAC f_{OUT} = 1kHz, 5kΩ

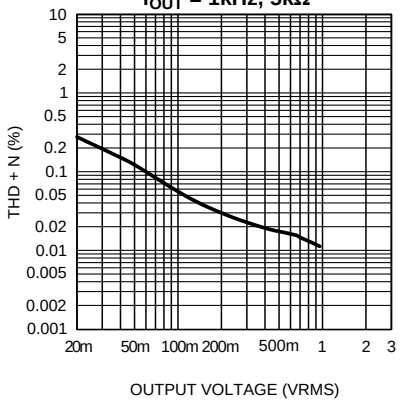


Figure 207.

CPOUT THD+N vs Output Voltage AV_{DD} = 5V, 0dB DAC f_{OUT} = 1kHz, 5kΩ

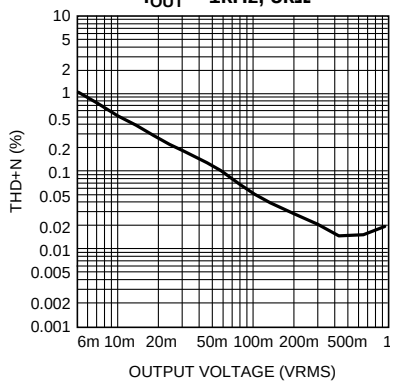


Figure 208.

CPOUT THD+N vs Output Voltage AV_{DD} = 3.3V, 6dB MIC f_{OUT} = 1kHz, 5kΩ

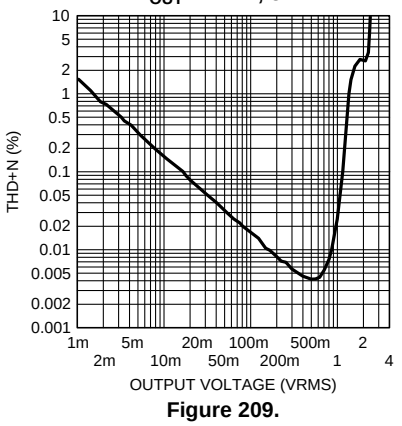


Figure 209.

CPOUT THD+N vs Output Voltage AV_{DD} = 5V, 6dB MIC f_{OUT} = 1kHz, 5kΩ

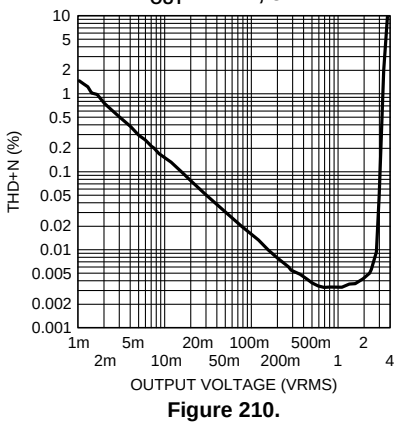


Figure 210.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

CPOUT THD+N vs Output Voltage AV_{DD} = 3.3V, 12dB DAC f_{OUT} = 1kHz, 5kΩ

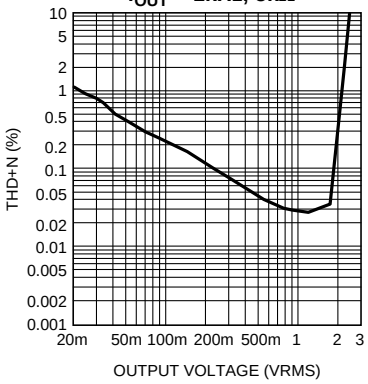


Figure 211.

CPOUT THD+N vs Output Voltage AV_{DD} = 5V, 12dB DAC f_{OUT} = 1kHz, 5kΩ

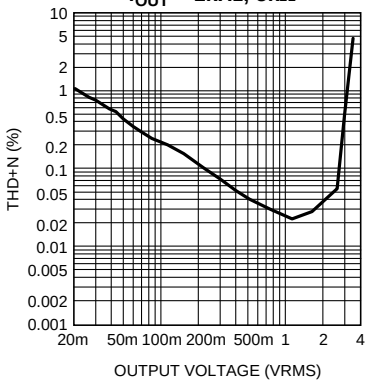


Figure 212.

CPOUT THD+N vs Output Voltage AV_{DD} = 3.3V, 36dB MIC f_{OUT} = 1kHz, 5kΩ

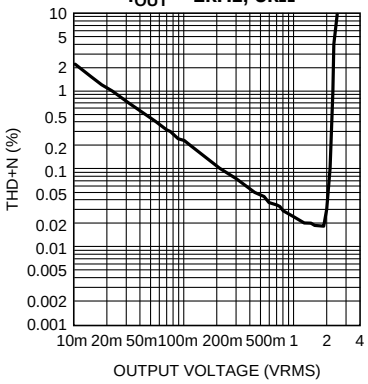


Figure 213.

CPOUT THD+N vs Output Voltage AV_{DD} = 5V, 36dB MIC f_{OUT} = 1kHz, 5kΩ

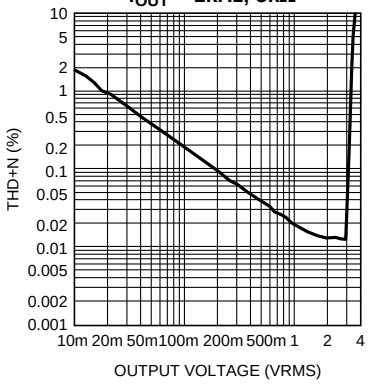


Figure 214.

Headphone Crosstalk vs Frequency OCL 1.2V, 0dB AUX, 32Ω

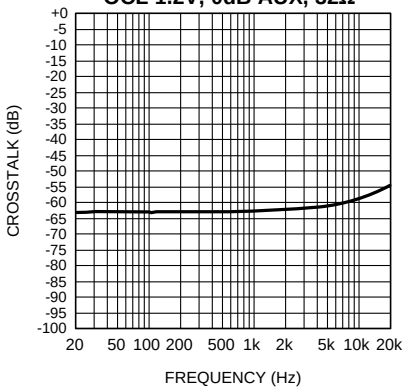


Figure 215.

Headphone Crosstalk vs Frequency OCL 1.5V, 0dB AUX, 32Ω

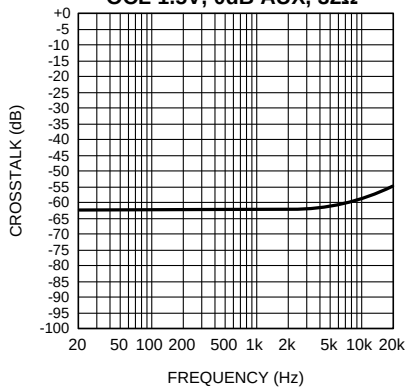


Figure 216.

Typical Performance Characteristics (continued)

(For all performance curves AV_{DD} refers to the voltage applied to the A_V_{DD} and LS_V_{DD} pins. DV_{DD} refers to the voltage applied to the D_V_{DD} and PLL_V_{DD} pins; AV_{DD} = 3.3V and DV_{DD} = 3.3V unless otherwise specified.

Headphone Crosstalk vs Frequency SE, 0dB AUX, 32Ω

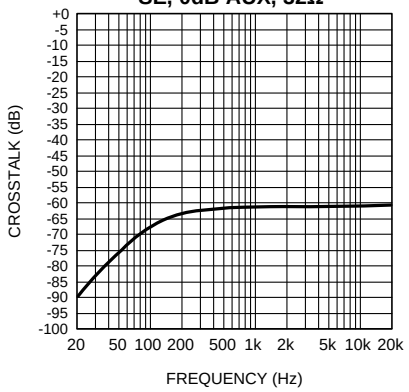


Figure 217.

APPLICATION NOTE

MICROPHONE BIAS CONFIGURATIONS

Schematic Considerations for MEMs Microphones

The internal microphone bias of the LM49370 is provided through a two stage amplifier. Adding a capacitor larger than 100pF directly to this pin can cause instability. In many cases, when using MEMs microphones, a larger bypass capacitor is required on the INT_MIC_BIAS pin. To avoid oscillations and to keep the device stable, it is recommended to add a resistor (R_B) greater than 10Ω in series with the capacitor (C_B). Another option is to bias the MEMs microphone from the 1.8V supply used for D_V_{DD}/IO_V_{DD}.

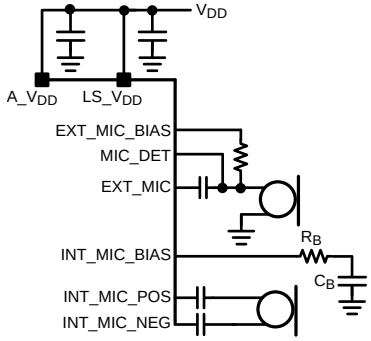


Figure 218. Schematic for MEMs Microphones

Schematic Considerations for ECM Microphones

When using ECM microphones, refer to the configurations shown in Figure 219 to bias the microphones.

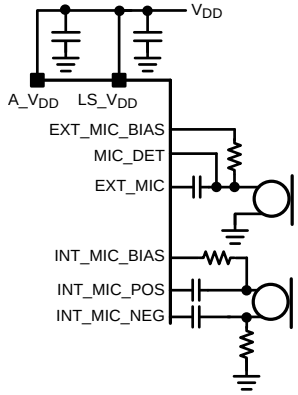


Figure 219. Schematic Option for ECM Microphones

PCB LAYOUT CONSIDERATIONS

A_V_{DD} and LS_V_{DD}

Due to internal ESD diodes structure, for best performance, in the PCB board A_V_{DD} and LS_V_{DD} need to be tied to the same plane, but requires separate bypassing capacitors for each supply rail.

Microphone Inputs

When routing the differential microphone inputs the electrical length of the two traces should be well matched. The differential input pair can be routed in parallel on the same plane or the traces can overlap on two adjacent planes. It is important to surround these traces with a ground plane or trace to isolate the microphone inputs from the noise coupling from the class D amplifier.

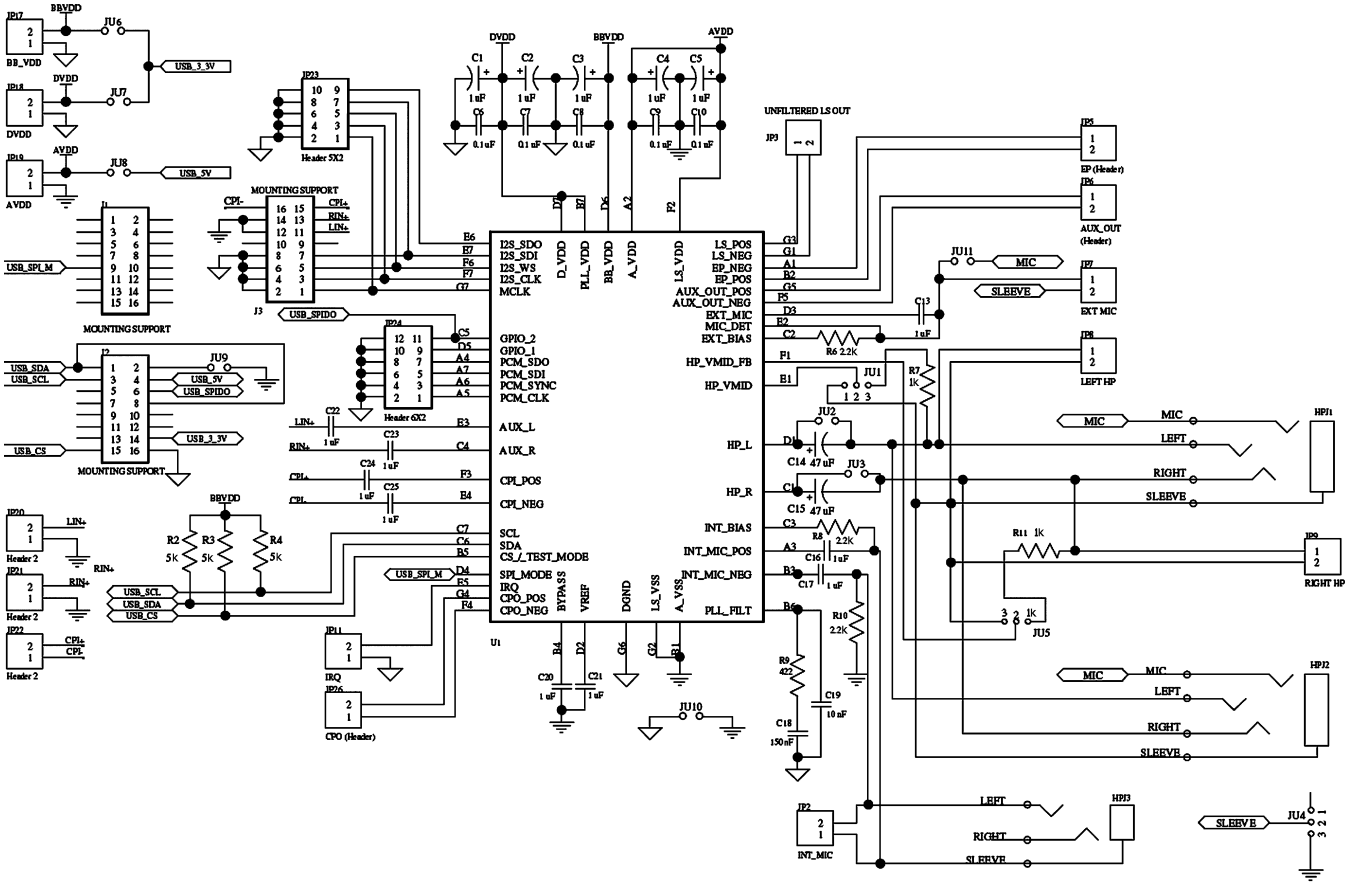
Class D Loudspeaker

To minimize trace resistance and therefore maintain the highest possible output power, the power (LS_V_{DD}) and class D output (LS-, LS+) traces should be as wide as possible. It is also essential to keep these same traces as short and well shielded as possible to decrease the amount of EMI radiation.

Capacitors

All supply bypass capacitors (for A_V_{DD}, D_V_{DD}. I/O V_{DD}, and LS_V_{DD}), and charge pump capacitors should be as close to the device as possible. Careful consideration should be taken with the ground connection of the analog supply (A_V_{DD}) bypass cap, for proper performance it should be referenced to a low noise ground plane. The charge pump capacitors and traces connecting the capacitor to the device should be kept away from the input and output traces to avoid noise coupling issues.

LM49370 Demonstration Board Schematic Diagram



Demoboard PCB Layout

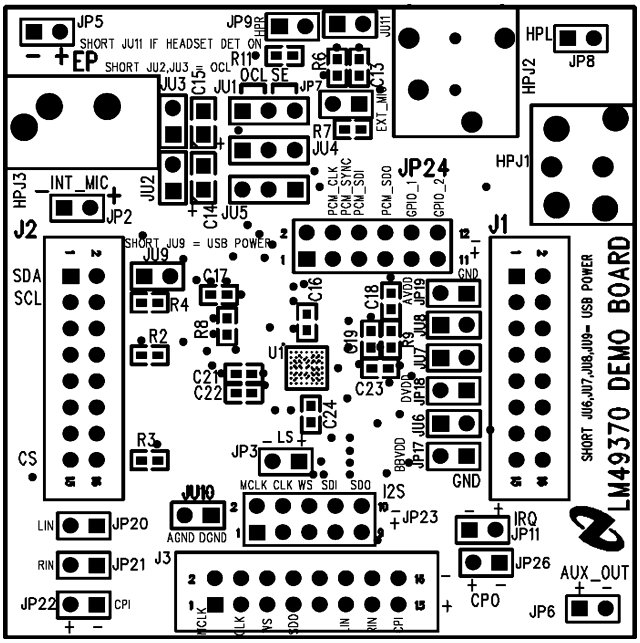


Figure 220. Top Silkscreen

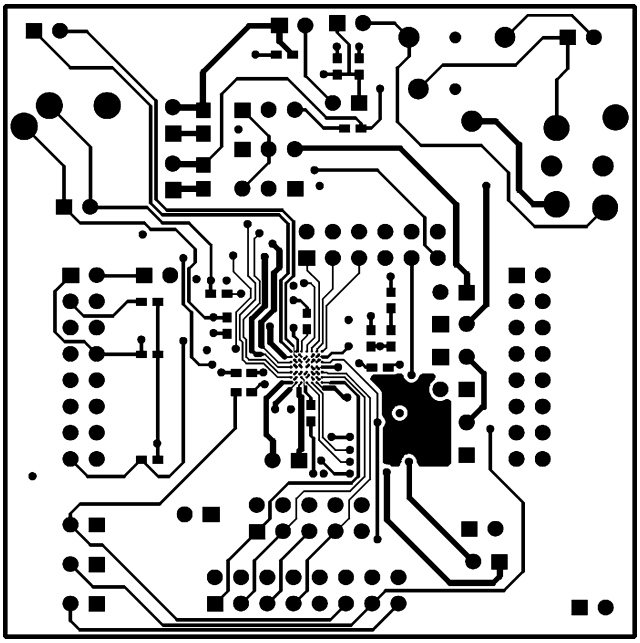


Figure 221. Top Layer

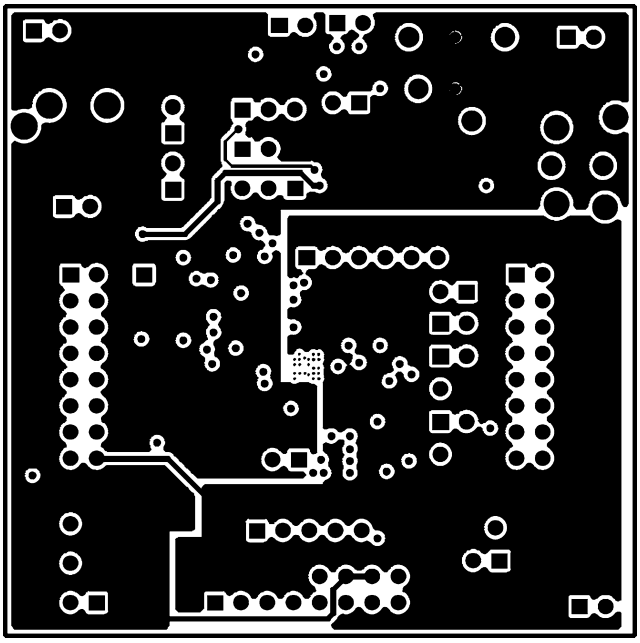


Figure 222. Mid Layer 1

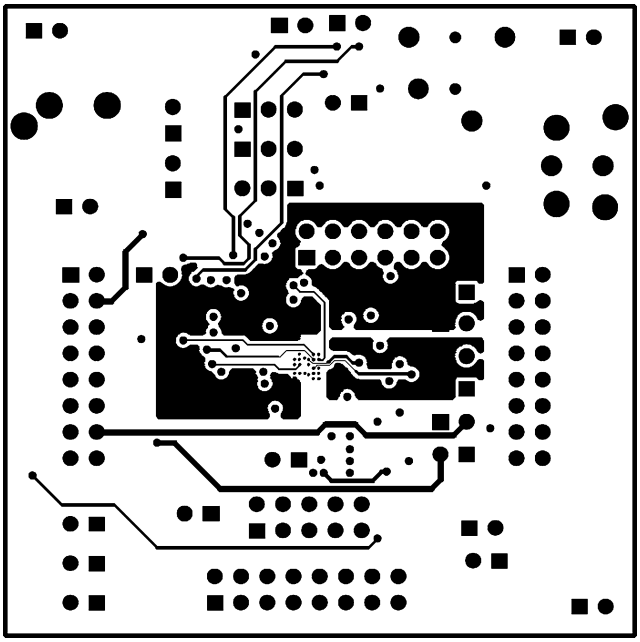


Figure 223. Mid Layer 2

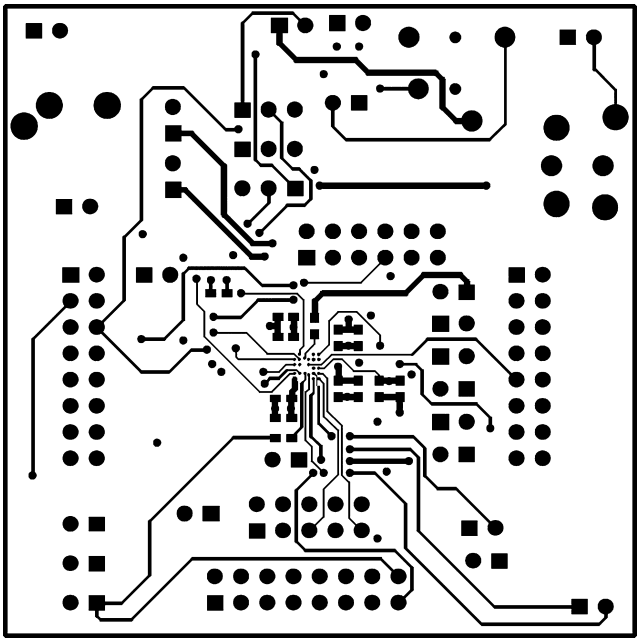


Figure 224. Bottom Layer

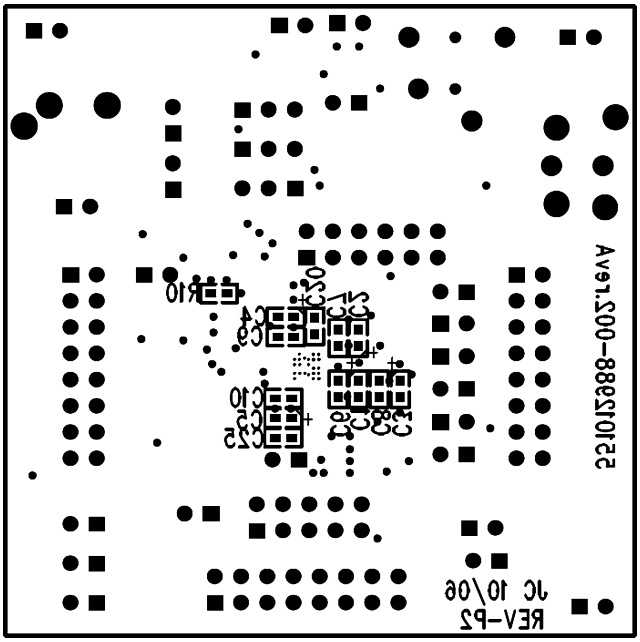


Figure 225. Bottom Silkscreen

REVISION HISTORY

Rev	Date	Description
1.0	02/14/07	Initial release.
1.01	01/08/08	Fixed a typo on X3 value (Physical Dimension section) in the last page.
1.02	02/11/08	Text edits.
1.03	03/31/11	Input edits and added the section ”PLL LOOP FILTER”.
1.04	05/26/11	Added the Application Note section.
1.05	06/02/11	Edited (tweak) Figures 16 and 17 (schematics for MEM and ECM microphones) respectively. Also added the paragraph “In non-OCL mode, two 1kohm resistors are optional..... (under Figure 9, Connection of Headset....)
1.06	03/09/12	Replaced curve 20191721 (stereo DAC crosstalk, 32Ω) with 201917k5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM49370RL/NOPB	OBSOLETE	DSBGA	YPG	49		TBD	Call TI	Call TI	-40 to 85	GI3	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

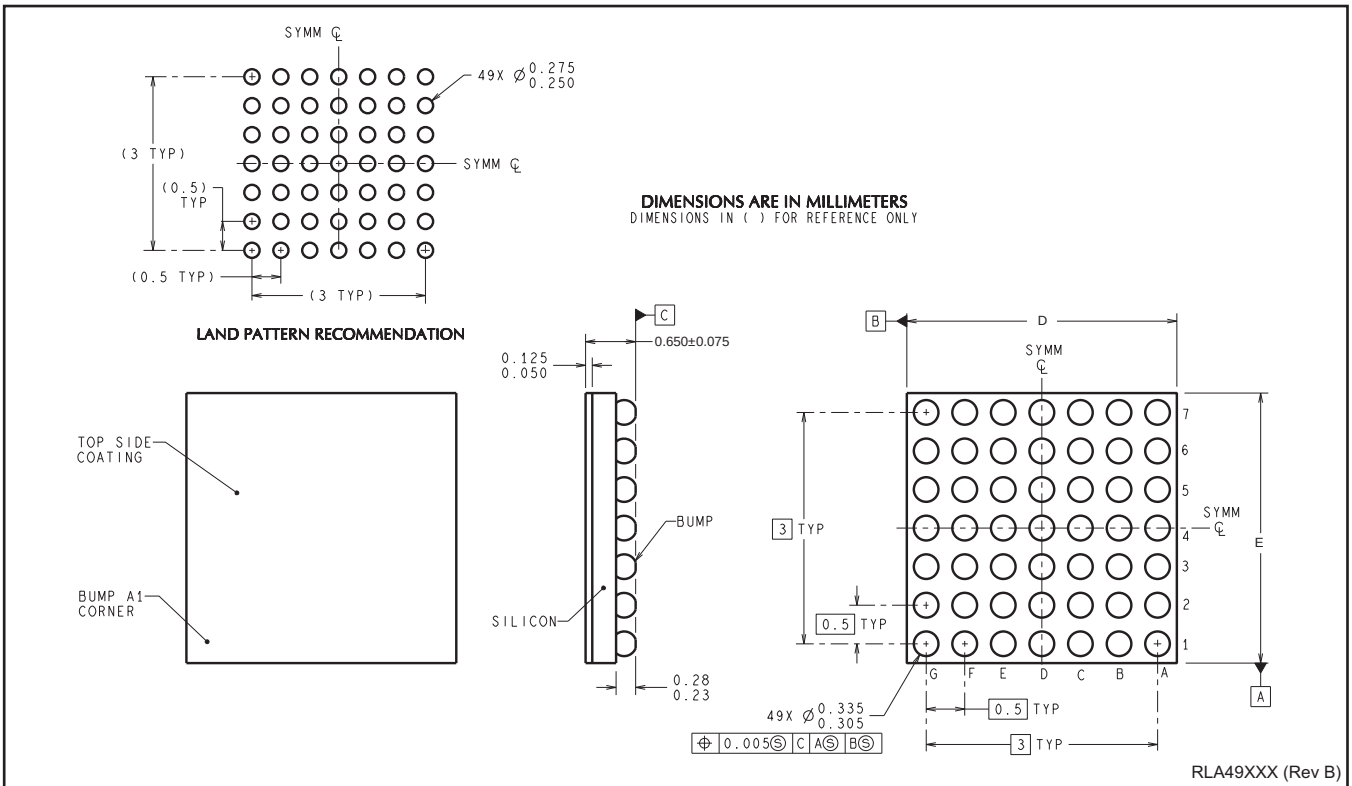
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

YPG0049



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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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