

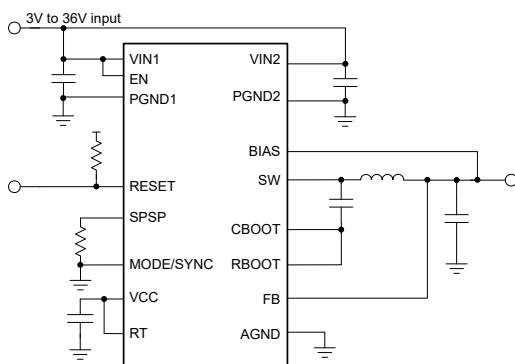
LM614xxT-Q1 Pin-Compatible, 8A/10A, Automotive, Buck Converter Optimized for Power Density and Low EMI in a Thermally Enhanced Package

1 Features

- AEC-Q100 qualified for automotive applications:
 - Temperature grade 1: -40°C to $+125^{\circ}\text{C}$, T_A
- [Functional Safety-Capable](#)
 - [Documentation available to aid functional safety system design](#)
- Input voltage range from 3V to 36V
- $\overline{\text{RESET}}$ output with filter and delayed release
- Designed for low EMI:
 - [CISPR 25 class 5 compliant EVM](#)
 - Pin-configurable spread spectrum
 - Adjustable SW node rise time
 - Above and below AM band operation: pin configurable 400kHz and 2.2MHz fixed or adjustable from 200kHz – 2.2MHz
 - Low EMI symmetrical pinout
 - Light load mode is pin-configurable for constant frequency or pulse frequency modulation (PFM)
- High-efficiency design
 - 95% efficient for an 8A load
 - 5 μA input current while unloaded in auto mode
 - < 1 μA shutdown current (typical)
- Thermally enhanced package enabling top-side cooling
- High power density
 - Built-in compensation, soft start, current limit, thermal shutdown, and UVLO
 - 4.5mm \times 3.5mm wettable flank QFN package

2 Applications

- [Automotive infotainment](#)
- [Instrument cluster](#)
- [Advanced Driver Assistance Systems \(ADAS\)](#)



Simplified Schematic

3 Description

The LM614xxT-Q1 buck converters are automotive-focused regulators providing adjustable output voltage which can be set from 1V to 95% of expected input voltage. These regulators operate under a wide input voltage range of 3V to 36V and have transient tolerance up to 42V.

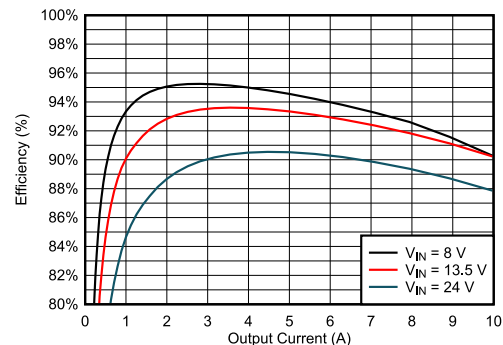
The family is designed for low EMI. The device incorporates pin selectable spread spectrum, and an adjustable SW node rise time. Dual Random Spread Spectrum (DRSS) frequency hopping is set to $\pm 4\%$ (typical), drastically reducing peak emissions through a combination of triangular and pseudorandom modulation, and includes advanced techniques to reduce output voltage ripple caused by spread spectrum modulation.

An open-drain $\overline{\text{RESET}}$ output, with filtering and delayed release, gives a true indication of system status. In auto mode, the device automatically transitions between Fixed frequency Pulse Width Modulation (FPWM) and Pulse Frequency Modulation (PFM) modes of operation, allowing an unloaded current consumption of only 5 μA (typical). Electrical characteristics are specified over a junction temperature range of -40°C to $+150^{\circ}\text{C}$.

Device Information

PART NUMBER ⁽³⁾	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
LM61495T-Q1	VAM (VQFN-HR, 16)	4.50mm \times 3.50mm
LM61480T-Q1		

- (1) For more information, see [Section 11](#).
- (2) The package size (length \times width) is a nominal value and includes pins, where applicable.
- (3) See the [Device Comparison Table](#).



EVM Efficiency: $V_{OUT} = 5\text{V}$, $F_{SW} = 2.2\text{MHz}$



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4 Device Comparison Table

DEVICE	ORDERABLE PART NUMBER	LIGHT LOAD	SPREAD SPECTRUM	OUTPUT VOLTAGE	TYPICAL FREQUENCY	CURRENT
LM61495T-Q1	LM61495TQVAMRQ1	Pin selectable	Pin selectable	Adjustable	Pin selectable	10A
LM61480T-Q1	LM61480TQVAMRQ1	Pin selectable	Pin selectable	Adjustable	Pin selectable	8A

5 Pin Configuration and Functions

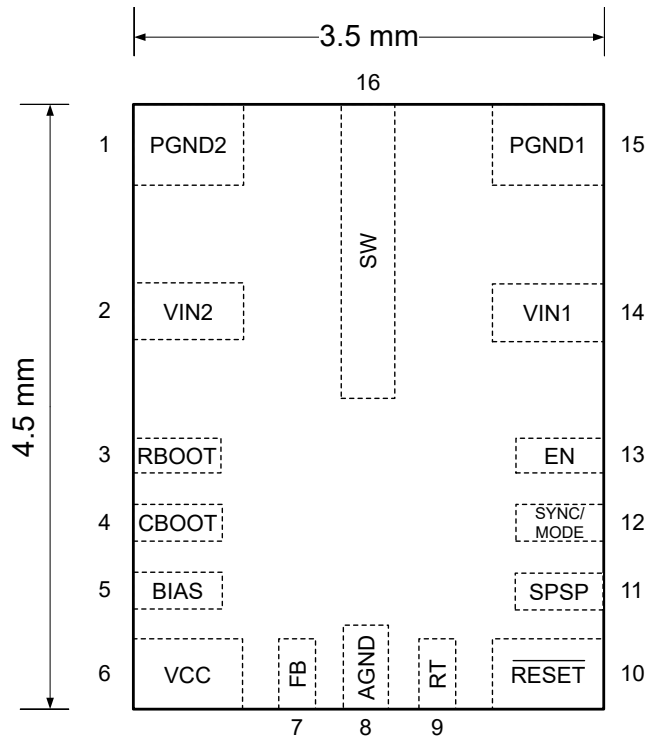


Figure 5-1. 16-Pin VQFN-HR, VAM Package (Top View)

Table 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
PGND2	1	G	Power ground to internal low-side MOSFET. Connect to system ground. Low-impedance connection must be provided to PGND1. Connect a high-quality bypass capacitor or capacitors from this pin to VIN2.
VIN2	2	P	Input supply to the regulator. Connect a high-quality bypass capacitor or capacitors from this pin to PGND2. Provide a low-impedance connection to VIN1.
RBOOT	3	P	Connect to CBOOT through a resistor. A resistance, typically between 0Ω and 100Ω, is used to adjust the slew rate of the SW node rise time. See Figure 7-10 .
CBOOT	4	P	High-side driver upper supply rail. Connect a 100nF capacitor between the SW pin and CBOOT. An internal diode charges the capacitor while SW node is low.
BIAS	5	P	Input to internal voltage regulator. Connect the pin to an output voltage point or an external bias supply from 3.3V to 12V. Connect an optional high-quality 0.1μF capacitor from this pin to GND for the best performance. If output voltage is above 12V and no external supply is used, tie the pin to ground.
VCC	6	O	Internal regulator output. Used as supply to internal control circuits. Do not connect this pin to any external loads. Connect a high-quality 1μF capacitor from this pin to AGND.
FB	7	I	Feedback input to regulator. Connect this pin to a feedback divider tap point. Do not float or ground.
AGND	8	G	Analog ground for regulator and system. All electrical parameters are measured with respect to this pin. Connect this pin to PGND1 and PGND2 on PCB.
RT	9	I/O	Connect this pin to ground through a resistor with a value between 6.8kΩ and 80kΩ to set the switching frequency between 200kHz and 2200kHz. Connect to VCC for 400kHz. Connect to GND for 2.2MHz. Do not float.
RESET	10	O	Open-drain RESET output. Connect to a suitable voltage supply through a current limiting resistor. High = power OK, low = fault. RESET goes low when EN = low.

Table 5-1. Pin Functions (continued)

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
SPSP	11	I	Connect to VCC or through a resistor to ground to enable spread spectrum. Connect to GND to disable spread spectrum. If using spread spectrum, a VCC connection turns off the spread spectrum tone correction while a resistor to ground adjusts the tone correction to lower the output voltage ripple. Do not float this pin. See Section 7.3.10 .
SYNC/MODE	12	I	This pin controls the mode of operation of the LM6x4xx. Modes include Auto mode (automatic PFM/PWM operation), forced pulse width modulation (FPWM), and synchronized to an external clock. The clock triggers on the rising edge of an applied external clock. Pull low to enable PFM operation, pull high to enable FPWM, or connect to a clock to synchronize to an external frequency in FPWM mode. Do not float this pin. When synchronized to an external clock, use the RT pin to set the internal frequency close to the synchronized frequency to avoid disturbances if the external clock is turned on and off.
EN	13	I	Precision enable input to regulator. High = on, low = off. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. Do not float. See Section 7.3.2 .
VIN1	14	P	Input supply to the regulator. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. Low-impedance connection must be provided to VIN2.
PGND1	15	G	Power ground to internal low-side MOSFET. Connect to system ground. Low-impedance connection must be provided to PGND2. Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.
SW	16	P	Switch node of the regulator. Connect to the output inductor.

(1) I = input, O = output, P = power, G = ground

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range⁽¹⁾

PARAMETER		MIN	MAX	UNIT
Voltages	Transient VIN to AGND, PGND ⁽²⁾	-0.3	42	V
Voltages	Continuous VIN to AGND, PGND ⁽²⁾	-0.3	36	V
Voltages	SW to AGND, PGND ⁽³⁾	-0.3	V _{IN} + 0.3	V
Voltages	RBOOT, CBOOT to SW	-0.3	5.5	V
Voltages	Transient EN or SYNC/MODE to AGND, PGND ⁽²⁾	-0.3	42	V
Voltages	Continuous EN or SYNC/MODE to AGND, PGND ⁽²⁾	-0.3	36	V
Voltages	BIAS to AGND, PGND	-0.3	16	V
Voltages	FB to AGND, PGND	-0.3	5.5	V
Voltages	RESET to AGND, PGND	0	20	V
Current	RESET sink current ⁽⁵⁾	0	10	mA
Voltages	RT to AGND, PGND	-0.3	5.5	V
Voltages	VCC to AGND, PGND	-0.3	5.5	V
Voltages	PGND to AGND ⁽⁴⁾	-1	2	V
T _{stg}	Storage temperature	-65	150	°C

- Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- A maximum of 42V can be sustained at this pin for duration of ≤100ms at a duty cycle of ≤0.01%. 36V can be sustained for the life of this device.
- A voltage of 2V below GND and 2V above VIN can appear on this pin for ≤200ns with a duty cycle of ≤ 0.01%.
- This specification applies to voltage durations of 100ns or less. The maximum D.C. voltage must not exceed +/- 0.3V.
- Do not exceed the pin's voltage rating.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000 V
		Charged device model (CDM), per AEC Q100-011	±750 V

- AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of -40°C to 150°C (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	Input voltage range ⁽¹⁾	3	36	V
Output voltage	Output voltage range ⁽²⁾	1	0.95 × VIN	V
Frequency	Frequency adjustment range	200	2200	kHz
Sync Frequency	Synchronization frequency range	200	2200	kHz
Output current	I _{OUT} , LM61480T	0	8	A
Output current	I _{OUT} , LM61495T	0	10	A
Temperature	Operating junction temperature, T _J	-40	150	°C

- 3.7V is required at VIN for start-up, an extended input voltage range down to 3V is possible after start-up; See Minimum operating input voltage for start-up conditions.
- Under no conditions can the output voltage be allowed to fall below zero volts.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LM614XXT-Q1	UNIT
		VAM (VQFN-HR)	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance (LM61495TVAMEVM) ⁽³⁾	TBD	°C/W
R _{θJA}	Junction-to-ambient thermal resistance (JESD 51-7) ⁽²⁾	50.4	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	0.64	°C/W
R _{θJB}	Junction-to-board thermal resistance	11.5	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.7	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	11.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	–	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.
- (2) The value of R_{θJA} given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information please see the [Maximum Ambient Temperature](#) section.
- (3) Refer to the [EVM User's Guide](#) for board layout and additional information. For thermal design information please see the [Maximum Ambient Temperature](#) section.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature range of –40°C to +150°C, unless otherwise noted. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 13.5V. VIN1 shorted to VIN2 = V_{IN}. V_{OUT} is output set point.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V _{IN}	Minimum operating input voltage	Needed to start-up			3.7	V
		Once operating			3	V
V _{IN_OP_H}	Minimum voltage hysteresis			1		V
I _Q	Non-switching input current; measured at VIN pin ⁽³⁾	V _{IN} = 13.5V, V _{FB} = +5%, V _{BIAS} = 5V		0.662	10	μA
I _{SD}	Shutdown quiescent current; measured at VIN pin	V _{EN} = 0V, V _{IN} = 13.5V		0.662	7.5	μA
I _B	Current into BIAS pin (not switching)	V _{IN} = 13.5V, V _{FB} = +5%, V _{BIAS} = 5V, Auto mode enabled		18.5	26	μA
ENABLE (EN PIN)						
V _{EN}	Enable input-threshold voltage - rising	V _{EN} rising	1.161	1.263	1.365	V
V _{EN_HYST}	Enable threshold hysteresis		0.25		0.5	V
V _{EN_WAKE}	Enable Wake-up threshold		0.4			V
I _{EN}	Enable pin input current	V _{IN} = V _{EN} = 13.5V		0.3	50	nA
INTERNAL LDO (VCC PIN)						
V _{CC}	Internal VCC voltage	V _{IN} = 13.5V, V _{BIAS} = 0V		3.4		V
		V _{IN} = 13.5V, V _{BIAS} = 3.3V, 20mA		3.2		
V _{CC_UVLO}	V _{IN} voltage at which Internal VCC undervoltage lockout is released	I _{VCC} = 0A			3.7	V
V _{CC_UVLO_HYST}	Internal VCC under voltage lock-out hysteresis	Hysteresis below V _{CC_UVLO}		1.2		V
VOLTAGE REFERENCE (FB PIN)						
V _{FB}	Internal reference voltage accuracy	V _{IN} = 3.0V to 36V, FPWM Mode	0.99	1	1.01	V
I _{FB}	Input current from FB to AGND	V _{FB} = 1V			50	nA
CURRENT LIMITS						

6.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature range of -40°C to $+150^{\circ}\text{C}$, unless otherwise noted. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at $T_J = 25^{\circ}\text{C}$, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: $V_{IN} = 13.5\text{V}$. VIN1 shorted to VIN2 = V_{IN} . V_{OUT} is output set point.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SC_8}	Short circuit high-side current Limit	8A variant, duty cycle approaches 0%	11.5	13.8	15.6	A
$I_{LS-LIMIT_8}$	Low-side current limit		8	9.2	10.4	A
$I_{PEAK-MIN_8}$	Minimum peak inductor current			1.6		A
I_{L-NEG_8}	Negative current limit		-6.4	-5.3	-3.9	A
I_{SC_10}	Short circuit high-side current Limit	10A variant, duty cycle approaches 0%	14	17.3	20	A
$I_{LS-LIMIT_10}$	Low-side current limit		9.8	11.5	12.9	A
$I_{PEAK-MIN_10}$	Minimum peak inductor current			1.8		A
I_{L-NEG_10}	Negative current limit		-6.6	-5.3	-4	A
I_{L-ZC}	Zero-cross current limit. Positive current direction is out of SW pin.	Auto mode, static measurement	10		200	mA
V_{HICCUP}	Hiccup threshold on FB pin		0.36	0.4	0.44	V
POWER GOOD (/RESET PIN)						
$V_{RESET-OV}$	RESET upper threshold - rising	% of FB voltage	110	112	114	%
$V_{RESET-UV}$	RESET lower threshold - falling	% of FB voltage	92	94	96.5	%
V_{RESET_GUARD}	RESET UV threshold as percentage of steady state output voltage with output voltage and UV threshold, falling, read at the same T_J , and V_{IN} .	Falling			97	%
$V_{RESET-HYS-FALLING}$	RESET falling threshold hysteresis	% of FB voltage	0.5	1.3	2.5	%
$V_{RESET-HYS-RISING}$	RESET rising threshold hysteresis	% of FB voltage	0.5	1.3	2.5	%
V_{RESET_VALID}	Minimum input voltage for proper RESET function	Measured when $V_{RESET} < 0.4\text{V}$ with 10k Ω pullup to external 5V			1.2	V
V_{OL}	RESET Low-level function output voltage	46.0 μA pull up to RESET pin, $V_{IN} = 1.0\text{V}$, $V_{EN} = 0\text{V}$			0.4	V
		1mA pull up to RESET pin, $V_{IN} = 13.5\text{V}$, $V_{EN} = 0\text{V}$			0.4	
		2mA pull up to RESET pin, $V_{IN} = 13.5\text{V}$, $V_{EN} = 3.3\text{V}$			0.4	
R_{RESET}	RESET ON resistance,	$V_{EN} = 5\text{V}$, 1mA pullup current		44	125	Ω
R_{RESET}	RESET ON resistance,	$V_{EN} = 0\text{V}$, 1mA pullup current		18	40	Ω
OSCILLATOR (SYNC/MODE PIN)						
V_{SYNCDL}	SYNC/MODE input voltage low		0.4			V
V_{SYNCDH}	SYNC/MODE input voltage high				1.7	V
V_{SYNCD_HYST}	SYNC/MODE input voltage hysteresis		0.185		1	V
R_{SYNC}	Internal pulldown resistor to make sure SYNC/MODE does not float			100		k Ω
HIGH SIDE DRIVE (CBOOT PIN)						
V_{CBOOT_UVLO}	Voltage on CBOOT pin compared to SW which will turnoff high-side switch			1.9		V
MOSFETS						
$R_{DS-ON-HS}$	High-side MOSFET on-resistance	Load = 1A, $C_{BOOT-SW} = 3.2\text{V}$		21	39	m Ω
$R_{DS-ON-LS}$	Low-side MOSFET on-resistance	Load = 1A, $C_{BOOT-SW} = 3.2\text{V}$		13	25	m Ω

6.6 Timing Requirements

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM LIMITS (SW PIN)						
t_{ON-MIN}	Minimum HS switch on-time	$V_{IN} = 18V, V_{SYNC/MODE} = 5V, I_{OUT} = 2A, R_{BOOT} = 0\Omega$		62	81	ns
$t_{OFF-MIN}$	Minimum HS switch off-time	$V_{IN} = 5V$		70	103	ns
t_{ON-MAX}	Maximum switch on-time	HS timeout in dropout	6.9	8.9	11	μs
START UP						
t_{EN}	Turn-on delay	$V_{IN} = 13.5V, C_{VCC} = 1\mu F$, time from EN high to first SW pulse if output starts at 0V		0.82	1.2	ms
t_{SS}	Time from first SW pulse to V_{REF} at 90%, of set point.		1.7	2.2	2.7	ms
t_W	Short-circuit wait time ("hiccup" time)			40		ms
POWER GOOD (/RESET PIN) and OVERVOLTAGE PROTECTION						
t_{RESET_FILTER}	RESET edge deglitch delay		10	26	45	μs
t_{RESET_ACT}	RESET active time	Time FB must be valid before RESET is released.	1.2	2.1	3.75	ms
OSCILLATOR (SYNC/MODE PIN)						
t_{PULSE_H}	High duration needed to be recognized on SYNC/MODE pin		100			ns
t_{PULSE_L}	Low duration needed to be recognized on SYNC/MODE pin		100			ns
t_{MSYNC}	Time at one level needed to indicate FPWM or Auto mode		7		20	μs
t_{LOCK}	Time needed for clock to lock to a valid synchronization signal	$RT = 39.2k\Omega$		4.3		ms

6.7 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR (RT and SYNC PINS)						
f_{OSC}	Internal oscillator frequency	$RT = GND$	1.90	2.2	2.42	MHz
f_{OSC}	Internal oscillator frequency	$RT = VCC$	350	400	440	kHz
$f_{FIXED_2.2MHz}$	Oscillator frequency measured using maximum value of RT resistor to select 2.2MHz	$RT = 6.81k\Omega$	1.95	2.2	2.42	MHz
$f_{FIXED_0.4MHz}$	Oscillator frequency measured using minimum value of RT resistor to select 400kHz	$RT = 40.2k\Omega$	352	400	448	kHz
f_{ADJ}	Center trim oscillator frequency	$RT = 22.6k\Omega$	630	700	770	kHz
SPREAD SPECTRUM						
ΔF_{C+}	Frequency increase of internal oscillator from spread spectrum		1	4	7.5	%
ΔF_{C-}	Frequency decrease of internal oscillator from spread spectrum		-8	-4	-1	%
SWITCH NODE						
D_{MAX}	Maximum switch duty cycle	While in frequency fold-back	98			%
		$f_{sw} = 1.85MHz$		87		

6.8 Typical Characteristics

Unless otherwise specified, $V_{IN} = 13.5V$.

ADVANCE INFORMATION

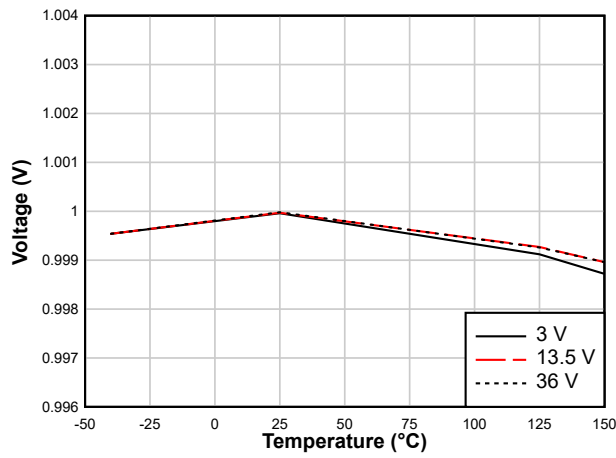
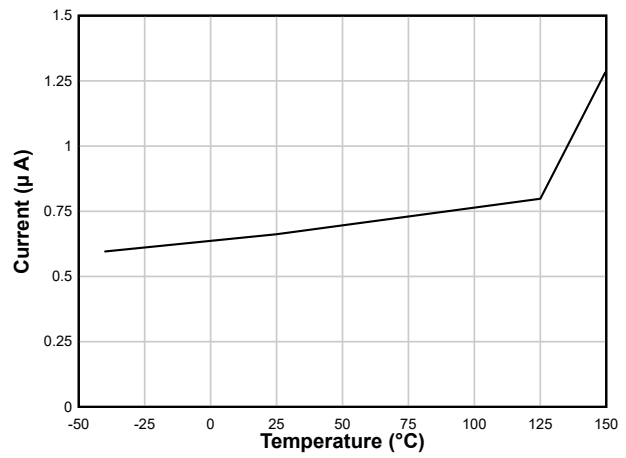


Figure 6-1. Feedback Voltage



EN = 0V

Figure 6-2. Shutdown Supply Current

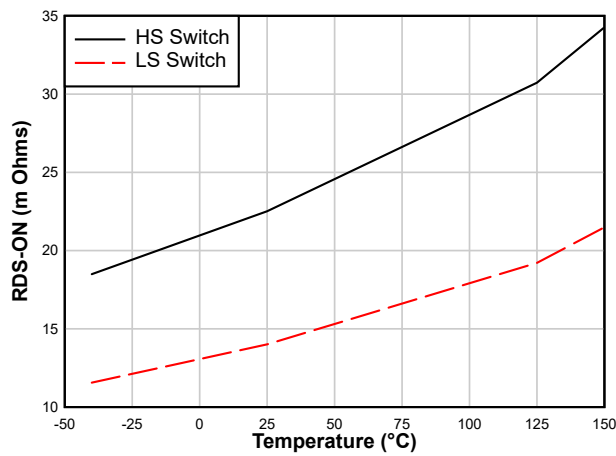


Figure 6-3. High-side and Low-side Switches
 R_{DS_ON}

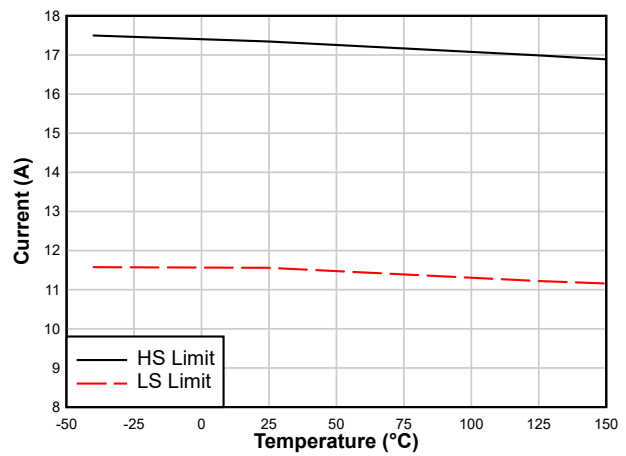


Figure 6-4. High-side and Low-side Current Limits

7 Detailed Description

7.1 Overview

The LM614xxT-Q1 is a wide-input and output-voltage range, low-quiescent current, high-performance regulator that operates over a wide range of frequencies and conversion ratios. If the minimum on-time or minimum off-time does not support the desired conversion ratio, the frequency is reduced. This action automatically allows regulation to be maintained during load dump and with very low dropout during cranking.

This device is designed to minimize end-product cost and size while operating in demanding automotive environments. The LM614xxT-Q1 can be set to operate at fixed 400kHz, fixed 2.2MHz, or is adjustable from 200kHz to 2.2MHz using the RT pin. Internal compensation and an accurate current limit scheme minimizes BOM cost and component count. In addition, the $\overline{\text{RESET}}$ output feature with built-in delayed release and low-current light-load mode lets the user eliminate a backup LDO and reset chip in many applications.

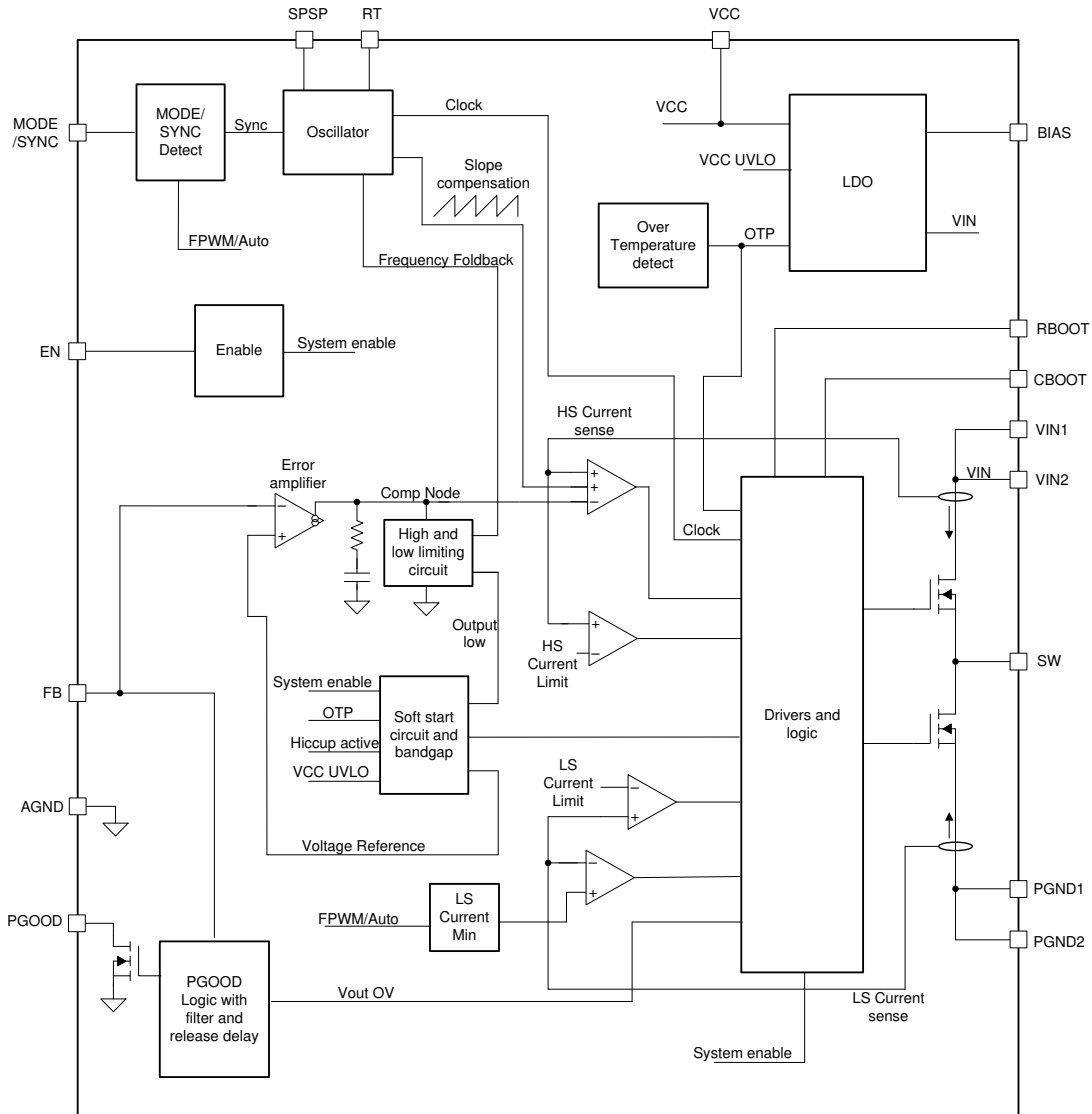
The LM614xxT-Q1 has been designed for low EMI. The device includes the following:

- Adjustable switch node rising slew rate
- Pin-configurable spread spectrum
- Low input inductance package
- Operation over a frequency range above and below AM radio band

Together, these features can eliminate shielding and other expensive EMI mitigation measures.

To use the device in reliability-conscious environments, the LM614xxT-Q1 has a package with enlarged corner terminals for improved BLR and wettable flanks, allowing optical inspection.

7.2 Functional Block Diagram



ADVANCE INFORMATION

7.3 Feature Description

7.3.1 Output Voltage Selection

A voltage divider between output voltage and the FB pin is used to adjust output voltage. See [Figure 7-1](#).

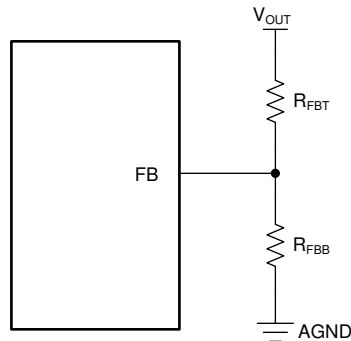


Figure 7-1. Setting Output Voltage of Adjustable Versions

The LM614xxT-Q1 uses a 1V reference for control to derive [Equation 1](#). This equation can be used to determine R_{FBB} for a desired output voltage and a given R_{FBT} . Usually, R_{FBT} is limited to a maximum value of 100k Ω to prevent shifting due to PCB leakage under harsh conditions. A larger resistance of up to 1M Ω can be used to improve light load efficiency in cleaner environments.

$$R_{FBB} = \left(\frac{1}{V_{OUT} - 1} \right) \times R_{FBT} \quad (1)$$

In addition, a feedforward capacitor C_{FF} can be used to optimize the transient response.

7.3.2 Enable EN Pin and Use as V_{IN} UVLO

Apply a voltage less than 0.4V to the EN pin to put the device into shutdown mode. In shutdown mode, the quiescent current drops to 0.66 μ A (typical). Above this voltage but below the LM614xxT-Q1 lower EN threshold, VCC is active but the SW node remains inactive. Once EN is above V_{EN} , the chip operates normally as long as input voltage is above the minimum operating voltage.

The EN terminal cannot be left floating. The simplest way to enable the operation is to connect the EN pin to V_{IN} . This action allows the self-start-up of the device when V_{IN} drives the internal VCC above the UVLO level. However, many applications benefit from employing an enable divider string, which establishes a precision input undervoltage lockout (UVLO). The precision UVLO can be used for the following:

- Sequencing
- Preventing the device from retriggering when used with long input cables
- Reducing the occurrence of deep discharge of a battery power source

Note that EN thresholds are accurate. The rising enable threshold has 8.1% tolerance. Hysteresis is enough to prevent retriggering upon shutdown of the load (approximately 25%). The external logic output of another IC can also be used to drive the EN terminal, allowing system power sequencing.

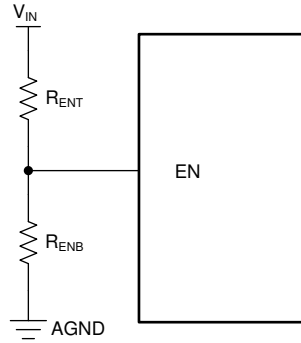


Figure 7-2. VIN UVLO Using the EN Pin

Resistor values can be calculated using Equation 2:

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN}} - 1 \right) \times R_{ENB}$$

$$V_{OFF} = V_{ON} \times \left(1 - \frac{V_{EN_HYST}}{V_{EN}} \right) \tag{2}$$

where

- V_{ON} = V_{IN} turn-on voltage
- V_{OFF} = V_{IN} turn-off voltage
- V_{EN} is the rising threshold voltage on the enable pin and can be found in the [Electrical Characteristics](#) table.

7.3.3 SYNC/MODE Uses for Synchronization

The LM614xxT-Q1 SYNC/MODE pin can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by coupling a positive edge into the SYNC/MODE pin. The coupled edge voltage at the SYNC/MODE pin must exceed the SYNC amplitude threshold of V_{SYNCDH} to trip the internal synchronization pulse detector. The minimum SYNC rising pulse and falling pulse durations must be longer than t_{PULSE_H} and t_{PULSE_L} respectively. The LM614xxT-Q1 switching action can be synchronized to an external clock from 200kHz to 2.2MHz.

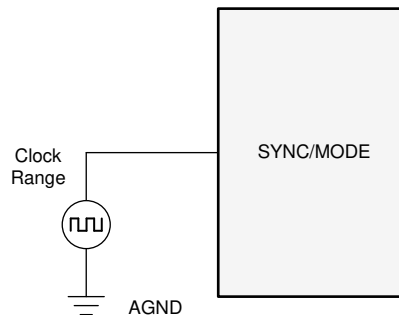
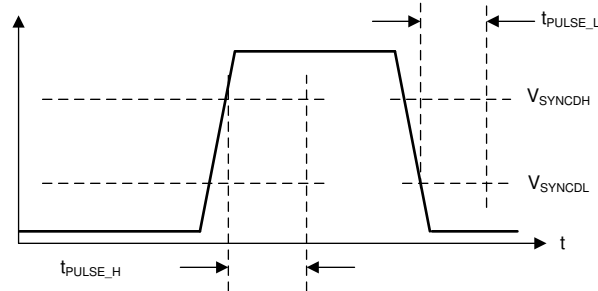


Figure 7-3. Typical Implementation Allowing Synchronization Using the SYNC/MODE Pin

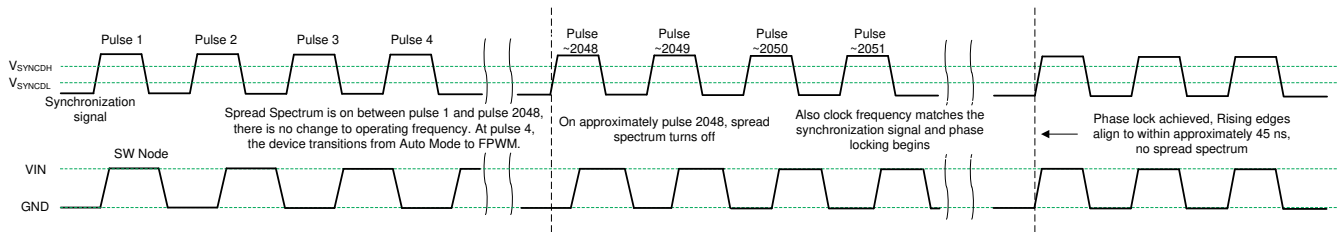


This image shows the conditions needed for detection of a synchronization signal.

Figure 7-4. Typical SYNC/MODE Waveform

7.3.4 Clock Locking

After a valid synchronization signal is detected, a clock locking procedure is initiated. After approximately 2048 pulses, the clock frequency abruptly changes to the frequency of the synchronization signal. While the frequency adjusts suddenly, phase is maintained so the clock cycle lying between operation at the default and synchronization frequencies is of intermediate length. There are no very long or very short pulses. After frequency is adjusted, phase is adjusted over a few tens of cycles so that rising synchronization edges correspond to rising the SW node pulses. See [Figure 7-5](#).



At pulse 4, the synchronization signal is detected. After approximately pulse 2048, the synchronization signal is ready to synchronize and the frequency is adjusted using a glitch-free technique. Later, phase is locked.

Figure 7-5. Synchronization Process

7.3.5 Adjustable Switching Frequency

The RT pin is configurable. This pin can be tied to VCC for 400kHz operation, grounded for 2.2MHz operation, or a resistor to AGND can be used to set an adjustable operating frequency. See [Figure 7-6](#) for resistor values. Note that if a resistor value falls outside of the recommended range, the fall can cause the LM614xxT-Q1 to revert to 400kHz or 2.2MHz. Do not apply a pulsed signal to this pin to force synchronization. If synchronization is needed, see the SYNC/MODE pin in [Section 7.3.3](#).

$$R_T(\text{k}\Omega) = \frac{16.4}{f_{\text{sw}}(\text{MHz})} - 0.633 \quad (3)$$

For example, for $f_{\text{sw}} = 400\text{kHz}$, $R_T = (16.4 / 0.4) - 0.633 = 40.37\text{k}\Omega$, so a 40.2k Ω resistor is selected as the closest choice.

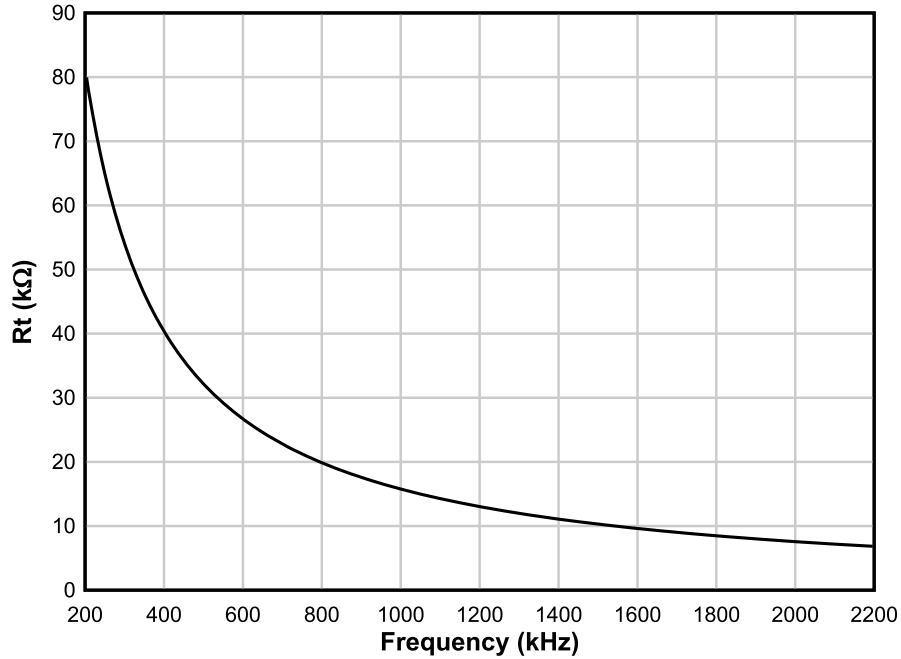


Figure 7-6. Setting Clock Frequency

7.3.6 $\overline{\text{RESET}}$ Output Operation

While the $\overline{\text{RESET}}$ function of the LM614xxT-Q1 resembles a standard power-good function, the functionality is designed to replace a discrete reset IC, reducing BOM cost. There are three major differences between the reset function and the normal power-good function seen in most regulators:

- A delay has been added for release of reset. See [Table 7-1](#).
- $\overline{\text{RESET}}$ output signals a fault (pulls the output to ground) while the part is disabled.
- $\overline{\text{RESET}}$ continues to operate with input voltage as low as 1.2V. Below this input voltage, $\overline{\text{RESET}}$ output can be high impedance.

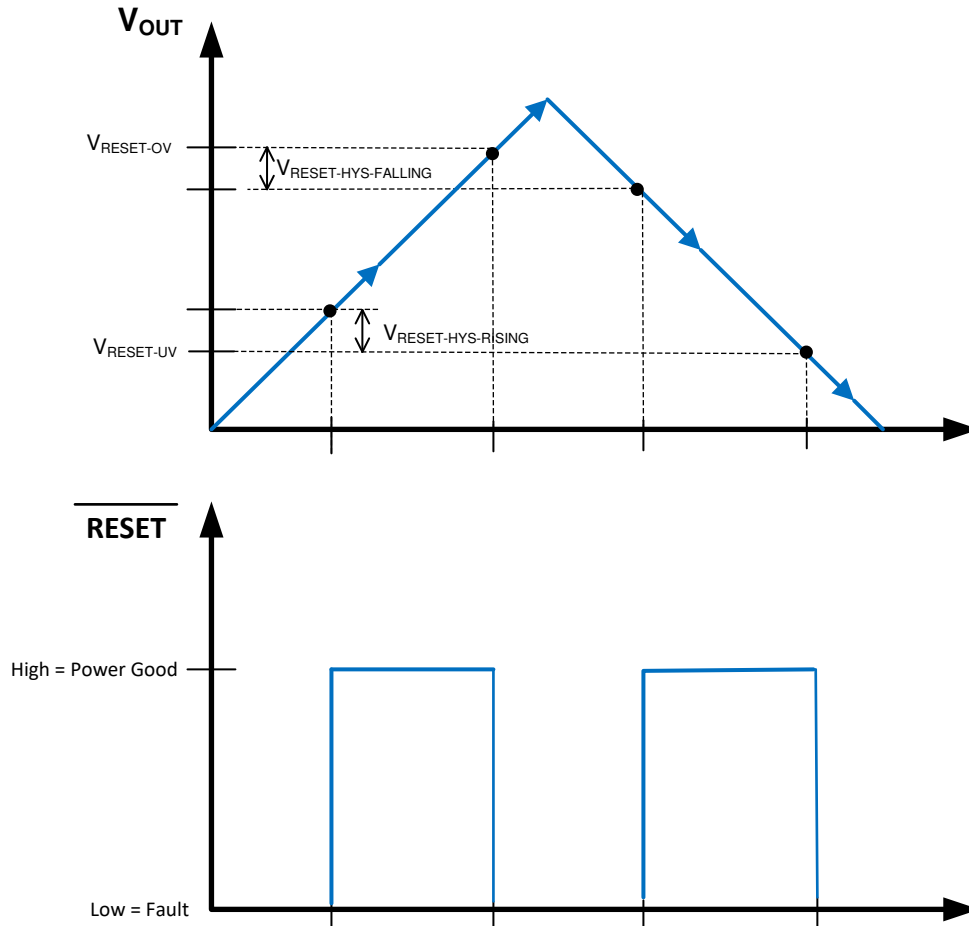


Figure 7-7. \overline{RESET} Static Voltage Thresholds

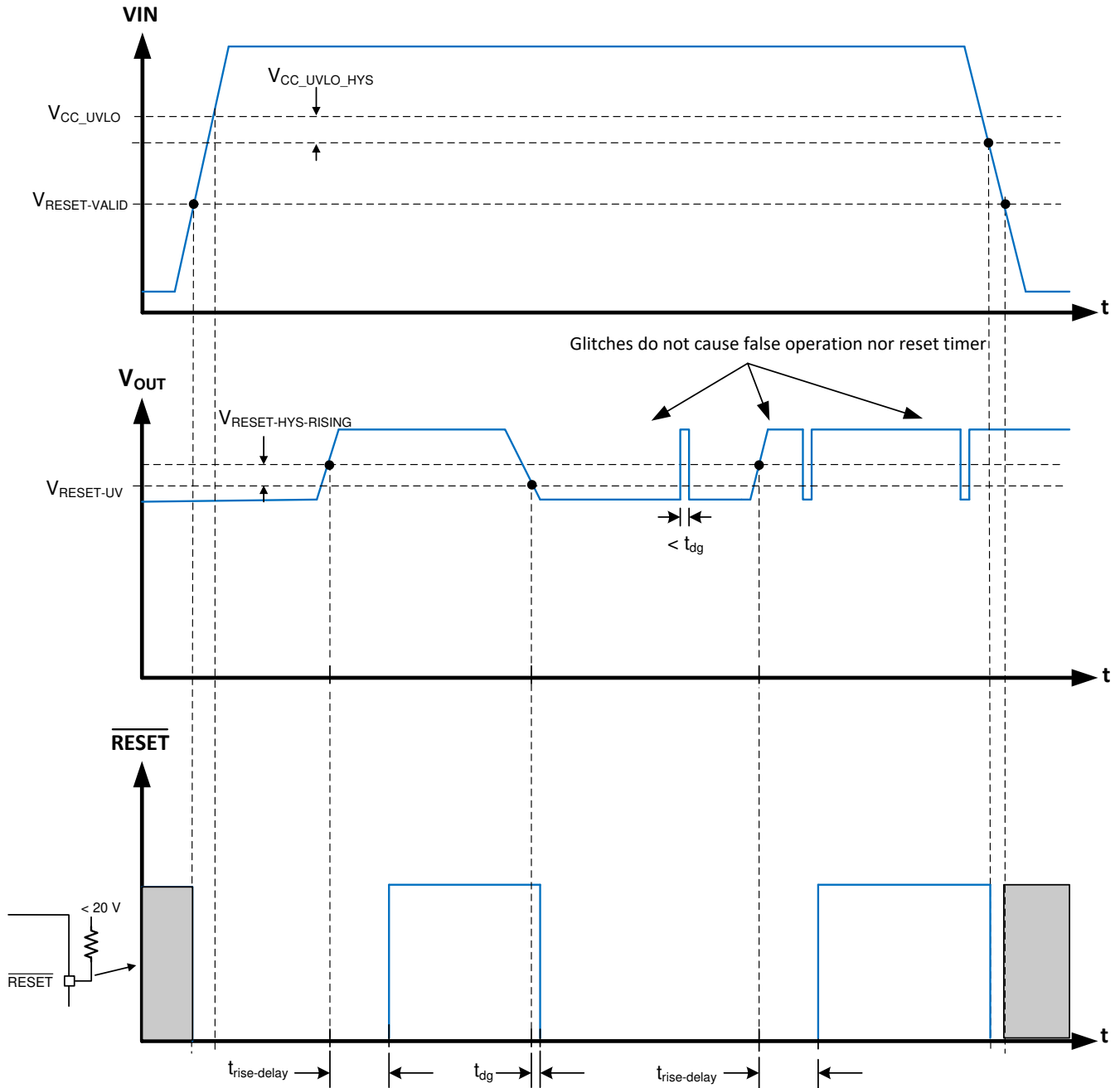


Figure 7-8. $\overline{\text{RESET}}$ Timing Diagram (Excludes OV Events)

Table 7-1. Conditions that Cause $\overline{\text{RESET}}$ to Signal a Fault (Pull Low)

FAULT CONDITION INITIATED	FAULT CONDITION ENDS (AFTER WHICH $t_{\text{RESET_ACT}}$ MUST PASS BEFORE RESET OUTPUT IS RELEASED)
FB below $V_{\text{RESET_UV}}$ for longer than $t_{\text{RESET_FILTER}}$	FB above $V_{\text{RESET_UV}} + V_{\text{RESET_HYST}}$ for longer than $t_{\text{RESET_FILTER}}$
FB above $V_{\text{RESET_OV}}$ for longer than $t_{\text{RESET_FILTER}}$	FB below $V_{\text{RESET_OV}} - V_{\text{RESET_HYST}}$ for longer than $t_{\text{RESET_FILTER}}$
Junction temperature exceeds $T_{\text{SD_R}}$	Junction temperature falls below $T_{\text{SD_F}}$ ⁽¹⁾
EN low	t_{EN} passes after EN becomes high ⁽¹⁾
VIN falls low enough so that VCC falls below $V_{\text{CC_UVLO}} - V_{\text{CC_UVLO_HYST}}$. This value is called $V_{\text{IN_OPERATE}}$.	Voltage on VIN is high enough so that VCC pin exceed $V_{\text{CC_UVLO}}$ ⁽¹⁾

(1) As an additional operational check, $\overline{\text{RESET}}$ remains low during soft start. It is defined as until the lesser of either full output voltage is reached or t_{SS2} has passed since initiation. This statement is true even if all other conditions in this table are met and $t_{\text{RESET_ACT}}$ has passed. Lockout during soft start does not require $t_{\text{RESET_ACT}}$ to pass before $\overline{\text{RESET}}$ is released.

The threshold voltage for the $\overline{\text{RESET}}$ function is specified to take advantage of the availability of the LM614xxT-Q1 internal feedback threshold to the $\overline{\text{RESET}}$ circuit. This action allows a maximum threshold of 96.5% of selected output voltage to be specified at the same time as 96% of actual operating point. The net result is a more accurate reset function while expanding the system allowance for transient response. See the output voltage error stack-up comparison in Figure 7-9.

In addition to signaling a fault upon overvoltage detection (FB above $V_{\text{RESET_OV}}$), the switch node is shut down and a small, approximately 1mA pulldown is applied to the SW node.

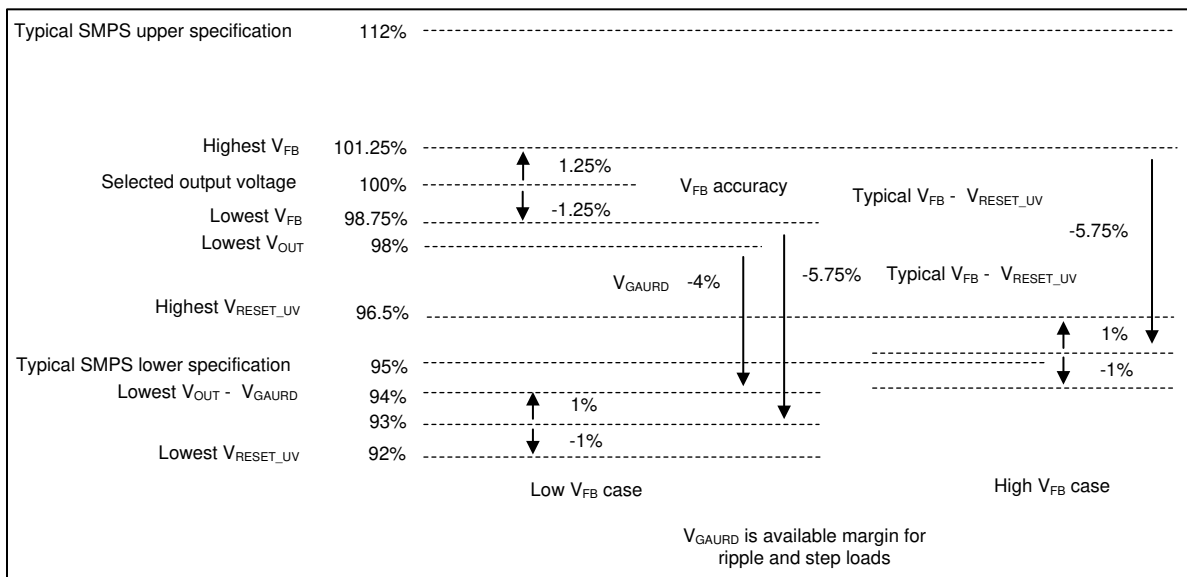


Figure 7-9. Reset Threshold Voltage Stack-Up

7.3.7 Internal LDO, VCC UVLO, and BIAS Input

The LM614xxT-Q1 uses VCC as the internal power supply. VCC is, in turn, powered from VIN or BIAS. Once the LM614xxT-Q1 is active, power comes from VIN if BIAS is less than approximately 3.1V. Power comes from BIAS if BIAS is more than 3.1V. VCC is typically 3V to 3.3V under most conditions, but can be lower if VIN is very low. To prevent unsafe operation, VCC has a UVLO that prevents switching if the internal voltage is too low. See $V_{\text{CC_UVLO}}$ and $V_{\text{CC_UVLO_HYST}}$ in *Electrical Characteristics*. During start-up, VCC momentarily exceeds the normal operating voltage until $V_{\text{CC_UVLO}}$ is exceeded, then drops to the normal operating voltage. These UVLO values, when combined with the dropout of the LDO when only powering the LM614xxT-Q1, are used to derive minimum $V_{\text{IN_OPERATE}}$ and $V_{\text{IN_OP_H}}$.

7.3.8 Bootstrap Voltage and V_{CBOOT_UVLO} (CBOOT Pin)

The driver of the high-side power switch (HS switch) requires bias higher than V_{IN} when the HS switch is ON. The capacitor connected between CBOOT and SW works as a charge pump to boost voltage on the CBOOT terminal to $(SW + VCC)$. The boot diode is integrated on the LM614xxT-Q1 die to minimize the physical design size. TI recommends a 100nF capacitor rated for 10V with X7R or better dielectric for the CBOOT capacitor. The boot (CBOOT) rail has a UVLO to protect the chip from operation with too little bias. This UVLO has a threshold of V_{BOOT_UVLO} and is typically 2.1V. If the CBOOT capacitor voltage drops below V_{BOOT_UVLO} , then the device initiates a charging sequence using the low-side FET before attempting to turn on the high-side device.

7.3.9 Adjustable SW Node Slew Rate

To allow optimization of EMI with respect to efficiency, the LM614xxT-Q1 is designed to allow a resistor to select the strength of the high-side FET driver during turn-on. See [Figure 7-10](#). The current drawn through the RBOOT pin (the dotted loop) is magnified and drawn through from CBOOT (the dashed line). This current is used to turn on the high-side power MOSEFT.

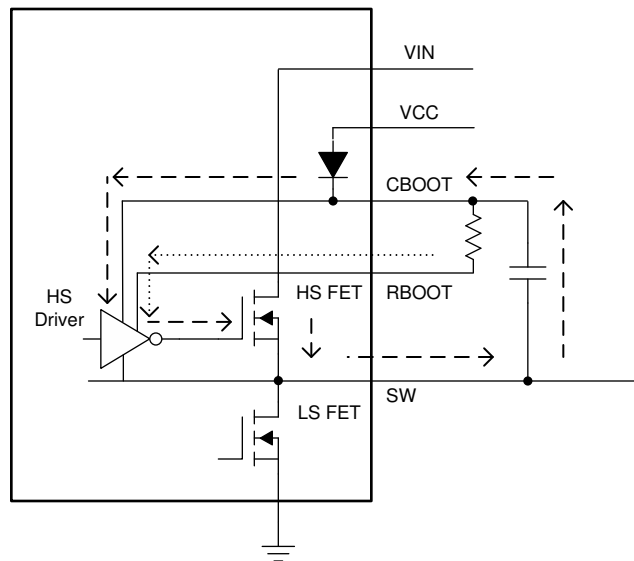


Figure 7-10. Simplified Circuit Showing How RBOOT Functions

Rise time is rapid with RBOOT short circuited to CBOOT. In this condition, the SW node harmonics roll off at $-20\text{dB}\mu\text{V}$ per decade until around 150MHz where the harmonics begin rolling off at $-40\text{dB}\mu\text{V}$ per decade. Slowing the rise time decreases the frequency where this transition occurs which provides more rolloff in the higher frequencies which provides more margin on EMI scans. If CBOOT and RBOOT are connected through 700Ω , slew time due to high-side turnon is limited to no more than 13ns. 10ns is typical when converting 13.5V to 5V. This slow rise time allows energy in SW node harmonics to roll off near 50MHz under most conditions. Rolling off harmonics eliminates the need for shielding and common mode chokes in many applications. Note that rise time increases with increasing input voltage. Noise due to stored charge is also greatly reduced with higher RBOOT resistance. Switching with a slower slew rate decreases efficiency. Take care to optimize the resistance to provide the best EMI while not generating too much heat. If RBOOT is left open, rise time is set to the maximum value.

7.3.10 Spread Spectrum

Spread spectrum is configurable using the SPSP pin. Spread spectrum eliminates peak emissions at specific frequencies by spreading these peaks across a wider range of frequencies than a part with fixed-frequency operation. The LM614xxT-Q1 implements a modulation pattern designed to reduce low frequency-conducted emissions from the first few harmonics of the switching frequency. The pattern can also help reduce the higher harmonics that are more difficult to filter, which can fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node and inductor. The LM614xxT-Q1 uses a $\pm 4\%$ (typical)

spread of frequencies which can spread energy smoothly across the FM and TV bands. The device implements Dual Random Spread Spectrum (DRSS). DRSS is a combination of a triangular frequency spreading pattern and pseudorandom frequency hopping. The combination allows the spread spectrum to be very effective at spreading the energy at the following:

- Fundamental switching harmonic with slow triangular pattern
- High frequency harmonics with additional pseudorandom jumps at the switching frequency

The advantage of DRSS is the equivalent harmonic attenuation in the upper frequencies with a smaller fundamental frequency deviation. This reduces the amount of input current and output voltage ripple that is introduced at the modulating frequency. Additionally, the LM614xxT-Q1 also allows you to further reduce the output voltage ripple caused by the spread spectrum modulating pattern. With the SPSP pin grounded, the spread spectrum is disabled. With the SPSP pin tied to VCC, the spread spectrum is on. With the SPSP pin tied through a resistor to ground, the spread spectrum is on. Also, a modulating tone correction is applied to the switcher to reduce the output voltage ripple caused by the frequency modulation. The resistor is usually around 20kΩ, and can be more precisely calculated using Equation 4.

$$R_{SPSP}(k\Omega) = \frac{14.17 \times \frac{V_{IN}}{V_{OUT}}}{\frac{V_{IN} - V_{OUT}}{I_{RATED} \times L \times f_{SW}} + 1.22} \quad (4)$$

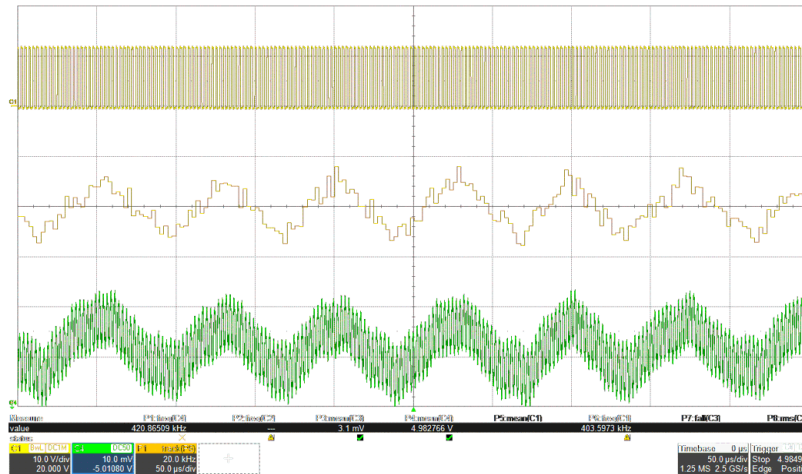


Figure 7-11. Output Ripple Without Ripple Cancellation Showing V_{SW} (Top), F_{SW} (Middle), V_{OUT} (Bottom)

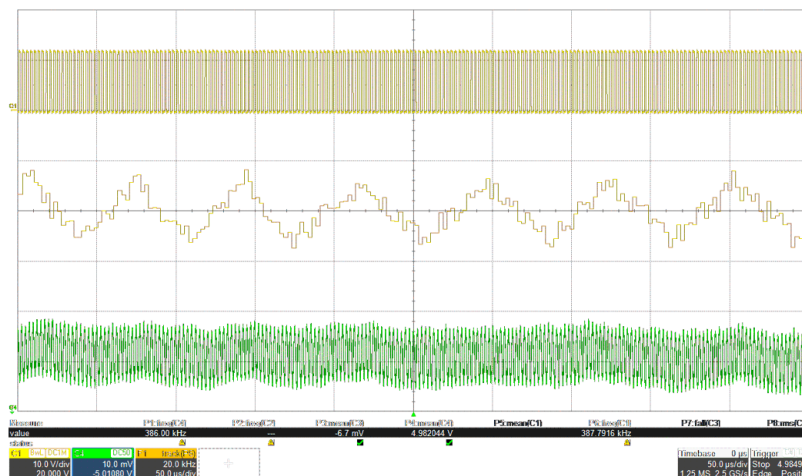


Figure 7-12. Output Ripple With Ripple Cancellation Showing V_{SW} (Top), F_{SW} (Middle), V_{OUT} (Bottom)

The spread spectrum is only available while the clock of the LM614xxT-Q1 are free running at the natural frequency. Any of the following conditions overrides spread spectrum, turning spread spectrum off:

- The clock is slowed due to operation at low input voltage. This action is operation in dropout.
- The clock is slowed under light load in auto mode. This is normally not seen above 750mA load. Note that if the device is operating in FPWM mode, spread spectrum is active, even if there is no load.
- The clock is slowed due to high input-to-output voltage ratio. This mode of operation is expected if on-time reaches minimum on-time. See the [Timing Requirements](#).
- The clock is synchronized with an external clock.

7.3.11 Soft Start and Recovery From Dropout

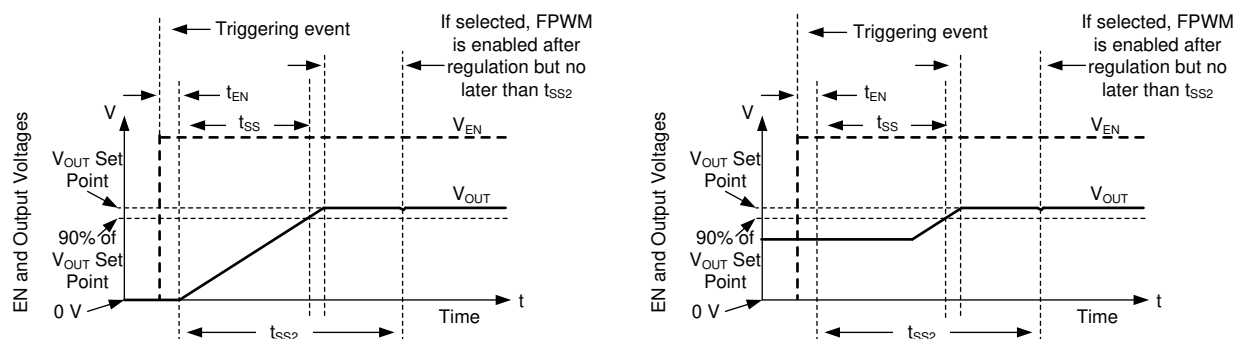
When designing with the LM614xxT-Q1, slowed rise in output voltage due to recovery from dropout and soft start must be considered separate phenomena. Soft start is triggered by any of the following conditions:

- EN is used to turn on the device.
- Recovery from a hiccup waiting period; see [Section 7.3.13](#).
- Recovery from shutdown due to overtemperature protection.
- Power is applied to the VIN of the IC or the VCC UVLO is released.

After soft start is triggered, the IC takes the following actions:

- The reference used by the IC to regulate output voltage is slowly ramped from zero. The net result is that output voltage, if previously 0V, takes t_{SS} to reach 90% of the desired value.
- Operating mode is set to auto, activating diode emulation. This action allows start-up without pulling output low if there is a voltage already present on the output.
- Hiccup is disabled for the duration of soft start; see [Section 7.3.13](#).

All of these actions together provide start-up with limited inrush currents. These actions also allow the use of output capacitors and loading conditions that cause current to border on current limit during start-up without triggering hiccup. In addition, if output voltage is already present, output is not pulled down. See [Figure 7-13](#).



The left curves show soft start from 0V. The right curves show soft starting behavior from a prebiased or non-zero voltage. In either case, the output voltage reaches within 10% of the desired setpoint t_{SS} time after soft start is initiated. During soft start, FPWM and hiccup are disabled. Both hiccup and FPWM are enabled once output reaches regulation or t_{SS2} , whichever happens first.

Figure 7-13. Soft-Start Operation

Any time output voltage is more than a few percent low for any reason, output voltage ramps up slowly. This condition, called recovery from dropout, differs from soft start in three important ways:

- Hiccup is allowed only if output voltage is less than 0.4 times the set point. Note that during dropout regulation, hiccup is inhibited. See [Section 7.3.13](#).
- FPWM mode is allowed during recovery from dropout. If output voltage were to suddenly be pulled up by an external supply, the LM614xxT-Q1 can pull down on the output. Note that all the protections that are present during normal operation are in place, protecting the device if output is shorted to a high voltage or ground.

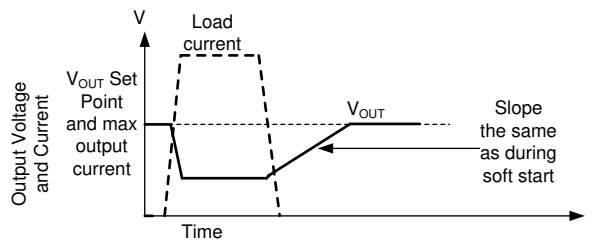
- The reference voltage is set to approximately 1% above that needed to achieve the current output voltage. The reference voltage is not started from zero.

Despite the name, recovery from dropout is active whenever output voltage is more than a few percent lower than the setpoint for long enough that:

- Duty factor is controlled by minimum on-time or
- When the part is operating in current limit.

This primarily occurs under the following conditions:

- Dropout: when there is insufficient input voltage for the desired output voltage to be generated. See [Section 7.4.3.5](#).
- Overcurrent that is not severe enough to trigger hiccup or if the duration is too short to trigger hiccup. See [Section 7.3.13](#).



Whether output voltage falls due to high load or low input voltage, after the condition that causes output to fall below the setpoint is removed, output climbs at the same speed as during start-up. Even though hiccup does not trigger due to dropout, hiccup can, in principal, be triggered during recovery if output voltage is below 0.4 times output the setpoint for more than 128 clock cycles during recovery.

Figure 7-14. Recovery From Dropout

7.3.12 Overcurrent and Short-Circuit Protection

The LM614xxT-Q1 is protected from overcurrent conditions by cycle-by-cycle current limiting on both the high-side and the low-side MOSFETs.

High-side MOSFET overcurrent protection is implemented by the nature of the peak current mode control. The HS switch current is sensed when the HS is turned on after a short blanking time. The HS switch current is compared to the minimum of a fixed current setpoint, or the output of the voltage regulation loop minus slope compensation, every switching cycle. Since the voltage loop has a maximum value and slope compensation increases with duty cycle, the HS current limit decreases with increased duty cycle if duty cycle is above 35%. See [Figure 7-15](#).

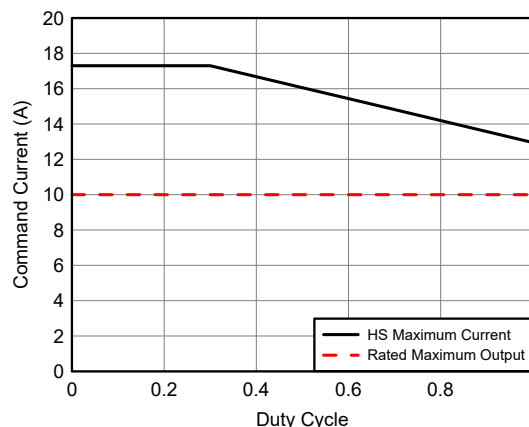


Figure 7-15. Maximum Current Allowed Through the HS FET - Function of Duty Cycle for LM61495T-Q1

When the LS switch is turned on, the current going through is also sensed and monitored. Like the high-side device, the low-side device turn-off is commanded by the voltage control loop. For a low-side device, turn-off is prevented if current exceeds this value, even if the oscillator normally starts a new switching cycle. See [Section 7.4.3.4](#). Also like the high-side device, there is a limit on how high the turn-off current is allowed to be. This limit is called the low-side current limit; see the [Electrical Characteristics](#) for values. If the LS current limit is exceeded, the LS MOSFET stays on and the HS switch is not turned on. The LS switch is turned off after the LS current falls below the limit. The HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

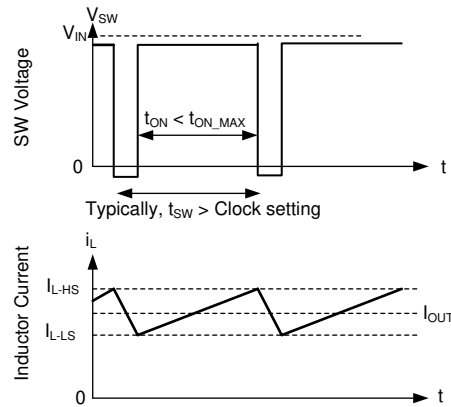
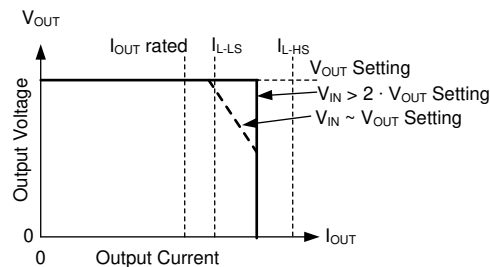


Figure 7-16. Current Limit Waveforms

The net effect of the operation of high-side and low-side current limit is that the IC operates in hysteretic control. Since the current waveform assumes values between I_{L-HS} and I_{L-LS} , output current is close to the average of these two values unless duty cycle is very high. Once operating in current limit, hysteretic control is used and current does not increase as output voltage approaches zero.

If duty cycle is very high, current ripple must be very low to prevent instability; see [Section 8.2.2.3](#). Because current ripple is low, the part is able to deliver full current. The current delivered is very close to I_{L-LS} .



Under most conditions, current is limited to the average of I_{L-HS} and I_{L-LS} , approximately 1.4 times the rated current. If input voltage is low, current can be limited to approximately I_{L-LS} . Current does not exceed the average of I_{L-HS} and I_{L-LS} as output drops to 0.4 times the output voltage setting. Below 0.4 times the output voltage setting, the peak current does not exceed the average of I_{L-HS} and I_{L-LS} and the hiccup mode activates, preventing excessive heating.

Figure 7-17. Output Voltage vs Output Current

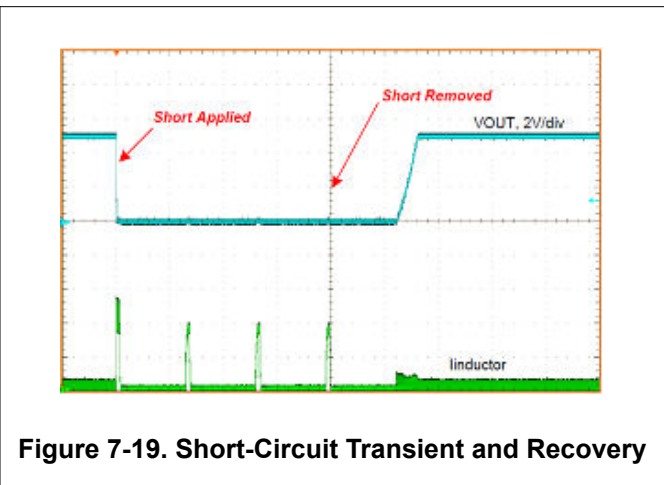
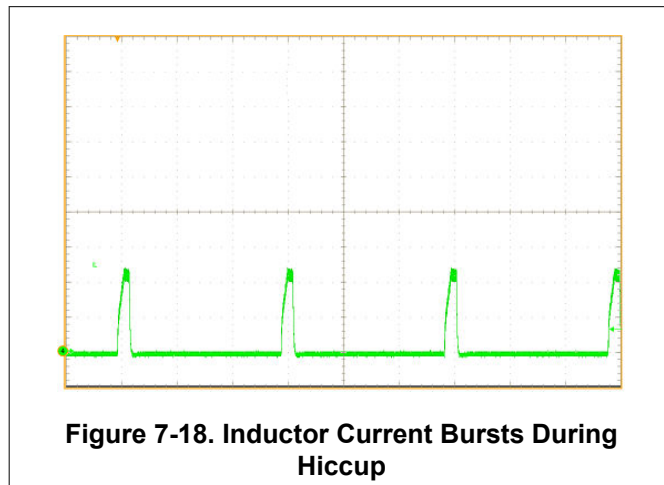
After the overload is removed, the device recovers as though in soft start; see [Section 7.3.11](#). Note that hiccup can be triggered if output voltage drops below approximately 0.4 times the intended output voltage.

7.3.13 Hiccup

The LM614xxT-Q1 employs hiccup overcurrent protection when all of the following conditions are met for 128 consecutive switching cycles:

- A time greater than t_{SS2} has passed since soft start has started; see [Section 7.3.11](#).
- Output voltage is below approximately 0.4 times output setpoint.
- The part is not operating in dropout defined as having minimum off-time controlled by duty factor.

In hiccup mode, the device shuts down and attempts to soft start after t_{W} . Hiccup mode helps reduce the device power dissipation under severe overcurrent conditions and short circuits.



7.3.14 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the IC junction temperature exceeds 168°C (typical). Thermal shutdown does not trigger below 158°C. After thermal shutdown occurs, hysteresis prevents the device from switching until the junction temperature drops to approximately 159°C. When the junction temperature falls below 159°C (typical), the LM614xxT-Q1 attempts to soft start.

While the LM614xxT-Q1 is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating from a short circuit applied to VCC, the LDO providing power to VCC has reduced current limit while the part is disabled due to high junction temperature. The LDO only provides a few milliamperes during thermal shutdown.

7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical on and off control of the device. When the EN pin voltage is below 0.4V, both the regulator and the internal LDO have no output voltage and the part is in shutdown mode. In shutdown mode, the quiescent current drops to typically 0.66µA.

7.4.2 Standby Mode

The internal LDO has a lower EN threshold than the output of the regulator. The internal LDO regulates the VCC voltage at 3.3V, typically when:

- The EN pin voltage is above 1.1V (maximum).
- The EN pin voltage is below the precision enable threshold for the output voltage.

The precision enable circuitry is ON after VCC is above the UVLO. The internal power MOSFETs of the SW node remain off unless the voltage on the EN terminal goes above the precision enable threshold. The LM614xxT-Q1 also employs UVLO protection. If the VCC voltage is below the UVLO level, the output of the regulator is turned off.

7.4.3 Active Mode

The LM614xxT-Q1 is in active mode when the following occurs:

- The EN pin is above V_{EN} .
- V_{IN} is above V_{EN} .
- V_{IN} is high enough to satisfy the V_{IN} minimum operating input voltage.
- No other fault conditions are present.

See [Section 7.3](#) for protection features. The simplest way to enable the operation is to connect EN to VIN, allowing self-start-up when the applied input voltage exceeds the minimum $V_{IN_OPERATE}$.

In active mode, depending on the load current, input voltage, and output voltage, the LM614xxT-Q1 is in one of six sub-modes:

- Continuous conduction mode (CCM) with fixed switching frequency and peak current mode operation
- Discontinuous conduction mode (DCM) while in auto mode when the load current is lower than half of the inductor current ripple. If current continues to reduce, the device enters Pulse Frequency Modulation (PFM) which reduces the switch frequency to maintain regulation while reducing switching losses to achieve higher efficiency at light load.
- Minimum on-time operation while the on-time of the device needed for full-frequency operation at the requested low-duty cycle is not supported by T_{ON_MIN} .
- Forced pulse width modulation (FPWM) similar to CCM with fixed-switching frequency, but extends the fixed frequency range of operation from full to no load.
- Dropout mode when switching frequency is reduced to minimize dropout.
- Recovery from dropout similar to other modes of operation except the output voltage setpoint is gradually moved up until the programmed setpoint is reached.

7.4.3.1 Peak Current Mode Operation

The following operating description of the LM614xxT-Q1 refers to [Section 7.2](#) and the waveforms in [Figure 7-20](#). Both supply a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) NMOS switches with varying duty cycle (D). During the HS switch on-time, the SW terminal voltage, V_{SW} , swings up to approximately V_{IN} , and the inductor current, i_L , increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off-time, t_{OFF} , the LS switch is turned on. Inductor current discharges through the LS switch, forcing V_{SW} to swing below ground by the voltage drop across the LS switch. The regulator loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on-time of the HS switch over the switching period: $D = T_{ON} / (T_{ON} + T_{OFF})$.

In an ideal buck converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: $D = V_{OUT} / V_{IN}$.

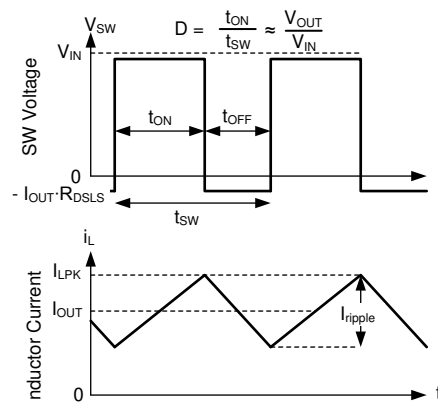


Figure 7-20. SW Voltage and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

To get accurate DC load regulation, a voltage feedback loop is used. Peak and valley inductor currents are sensed for peak current mode control and current protection. The regulator operates with continuous conduction mode with constant switching frequency when load level is above one half of the minimum peak inductor current. The internally-compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

7.4.3.2 Auto Mode Operation

The LM614xxT-Q1 can have two behaviors while lightly loaded. One behavior, called auto mode operation, allows a seamless transition between normal current mode operation while heavily loaded and in highly-efficient light-load operation. The other behavior, called FPWM mode, maintains full frequency even when unloaded. Which mode the LM614xxT-Q1 operates in depends on the SYNC/MODE pin. When SYNC/MODE is high, the part is in FPWM. When SYNC/MODE is low, the part is in PFM.

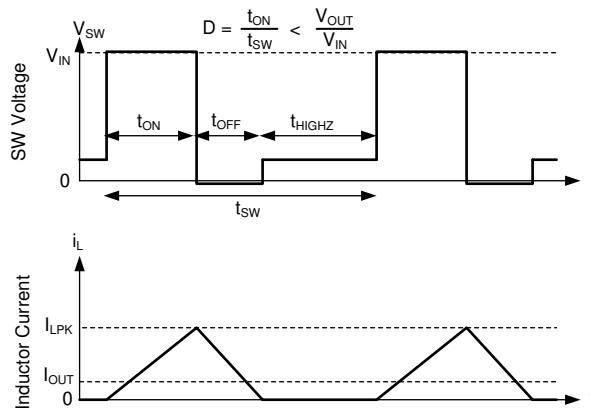
In auto mode, light-load operation is employed in the LM614xxT-Q1 at load lower than approximately 1/10th of the rated maximum output current. Light-load operation employs two techniques to improve efficiency:

- Diode emulation, which allows DCM operation
- Frequency reduction

Note that while these two features operate together to create excellent light load behavior, these features operate independently of each other.

7.4.3.2.1 Diode Emulation

Diode emulation prevents reverse current through the inductor, which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. Frequency is reduced when peak inductor current goes below $I_{PEAK-MIN}$. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.



In auto mode, the low-side device is turned off once inductor current is near zero. As a result, after output current is less than half of inductor ripple in CCM, the part operates in DCM. This statement is equivalent to saying that diode emulation is active.

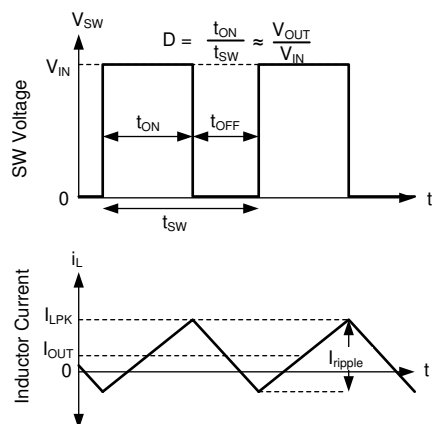
Figure 7-21. PFM Operation

The LM614xxT-Q1 has a minimum peak inductor current setting in auto mode. That being said, when current is reduced to a low value with fixed input voltage, on-time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called PFM mode regulation.

7.4.3.3 FPWM Mode Operation

Like auto mode operation, FPWM mode operation during light-load operation is selected using the SYNC/MODE pin.

In FPWM Mode, frequency is maintained while lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry. See the [Electrical Characteristics](#) for reverse current limit values.



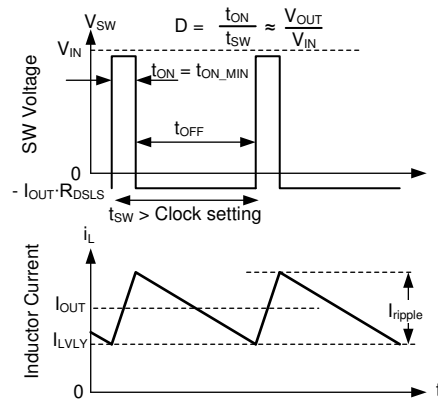
FPWM mode Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of I_{ripple} .

Figure 7-22. FPWM Mode Operation

In FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on-time, even while lightly loaded. This allows good behavior during faults which involves the output being pulled up.

7.4.3.4 Minimum On-time (High Input Voltage) Operation

The LM614xT-Q1 continues to regulate output voltage. This statement is true even if the input-to-output voltage ratio requires an on-time less than the minimum on-time of the chip with a given clock setting. This action is accomplished using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If, for any reason, valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If not operating in current limit, the maximum valley current is set above the peak inductor current. This action prevents valley control from being used unless there is a failure to regulate using peak current only. If the input-voltage to output-voltage ratio is too high, even though current exceeds the peak value dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. See t_{ON_MIN} in the [Electrical Characteristics](#). As a result, the compensation circuit reduces both peak and valley current. After a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Since on-time is fixed at the minimum value, this type of operation resembles that of a device using a COT control scheme. See [Figure 7-23](#).

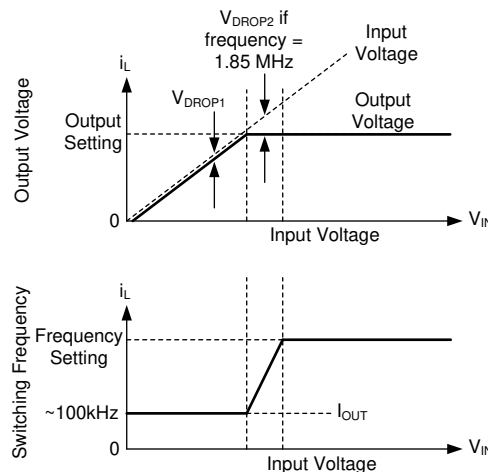


In valley control mode, the minimum inductor current is regulated, not peak inductor current.

Figure 7-23. Valley Current Mode Operation

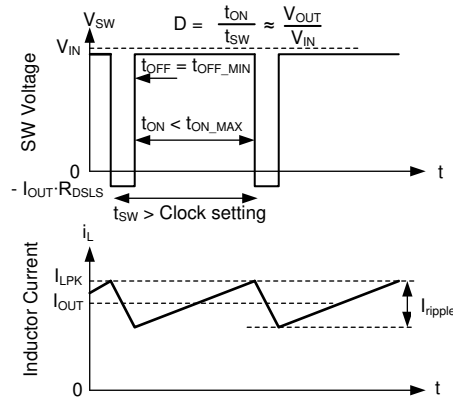
7.4.3.5 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the needed duty factor. At a given clock frequency, duty factor is limited by minimum off-time. After this limit is reached, if clock frequency is maintained, output voltage falls. Instead of allowing the output voltage to drop, the LM614xxT-Q1 extends on-time past the end of the clock cycle until the required peak inductor current is achieved. The clock can start a new cycle once peak inductor current is achieved or once a pre-determined maximum on-time, t_{ON_MAX} , of approximately $9\mu s$ passes. As a result, after the needed duty factor cannot be achieved at the selected clock frequency due to the existence of a minimum off-time, frequency drops to maintain regulation. If input voltage is low enough that the output voltage cannot be regulated even with an on-time of t_{ON_MAX} , output voltage drops to slightly below input voltage, V_{DROPO1} . See Section 6.



Output voltage and frequency versus input voltage: if there is little difference between input voltage and output voltage setting, the IC reduces frequency to maintain regulation. If input voltage is too low to provide the desired output voltage at approximately 110kHz, output voltage tracks input voltage.

Figure 7-24. Frequency and Output Voltage in Dropout



This image shows the switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by t_{ON_MAX} .

Figure 7-25. Dropout Waveforms

7.4.3.6 Recovery from Dropout

In some applications, input voltage can drop below the desired output voltage then recover to a higher value suddenly. With most regulators, the sudden increase in input voltage results in output voltage rising at a rate limited only by current limit until regulation is achieved. As input voltage reaches the desired output voltage, there is overshoot due to wind up in the control loop. This overshoot can be large in applications that have small output capacitors and light loads. Also, large inrush currents can cause large fluctuations on the input line once the regulator starts regulating the output voltage. This typically requires less current than during this initial inrush.

The LM614xxT-Q1 greatly reduces inrush current and overshoot. This reduction is done by engaging the soft-start circuit whenever the input voltage suddenly rises, after dipping low enough to cause the output voltage to droop. To prevent this feature from accidentally engaging, output voltage must fall more than 1% to engage this feature. Also, this feature engages only if operating in dropout or current limit, preventing interference with normal transient response but allowing several percent overshoot while engaging. If output voltage is very close to the desired level, overshoot is reduced by inductor current not having time to rise to a high level before regulation starts.

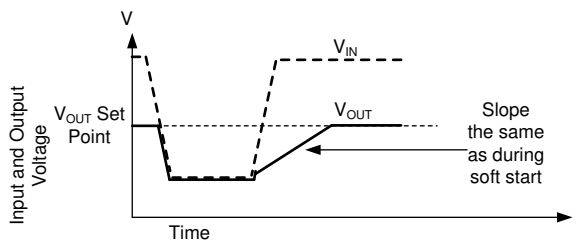


Figure 7-26. When Output Voltage Falls, Output Voltage Recovers Slowly Preventing Overshoot and Large Inrush Currents

7.4.3.7 Other Fault Modes

Fault modes and descriptions can be found in [Section 7.3](#) of this data sheet.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LM614xxT-Q1 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 10A. The following design procedure can be used to select components for the LM614xxT-Q1.

8.2 Typical Application

Figure 8-1 shows a typical application circuit for the LM614xxT-Q1. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, Table 8-2 provides typical component values for some of the most common configurations. The values given in the table are typical. Other values can be used to enhance certain performance criterion as required by the application. Note that for this QFN package, the input capacitors are split and placed on either side of the package. See Section 8.2.2.5 for more details.

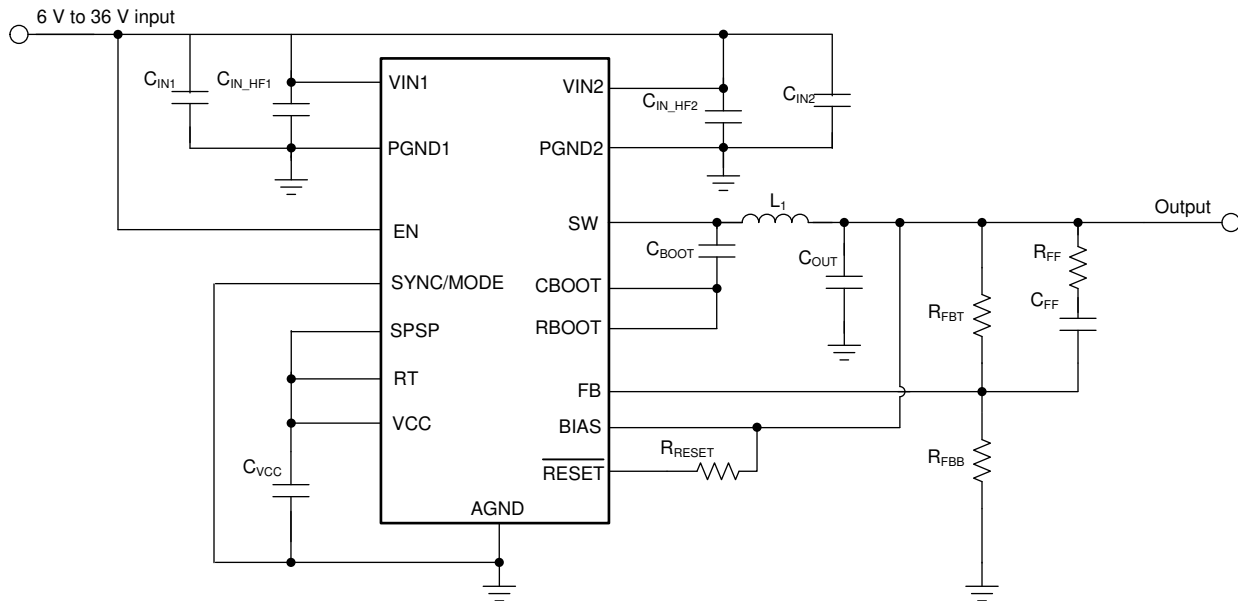


Figure 8-1. Example Application Circuit - 400kHz Adjustable Output

8.2.1 Design Requirements

The following table provides the parameters for our detailed design procedure example:

Table 8-1. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	13.5V (6V to 36V)
Output voltage	5V
Maximum output current	10A continuous
Switching frequency	400kHz

Table 8-2. Typical External Component Values

f _{sw} (kHz)	V _{OUT} (V)	I _{OUT} (A)	L1 (μH)	C _{OUT} (RATED)	R _{FBT} (kΩ)	R _{FBB} (kΩ)	C _{IN} + C _{HF} (μF)	C _{BOOT} (μF)	R _{BOOT} (Ω)	C _{VCC} (μF)	C _{FF} (pF)	R _{FF} (kΩ)
400	5	10	2.7	5 × 22μF ceramic or 2 × 22μF + 15mΩ 150μF	100	24.9	2 × 10 + 2 × 0.47	0.1	0	1	10	4.99
400	3.3	10	2.2	3 × 47μF ceramic or 3 × 22μF + 15mΩ 150μF	100	43.2	2 × 10 + 2 × 0.47	0.1	0	1	10	4.99

8.2.2 Detailed Design Procedure

The following design procedure refers to [Figure 8-1](#) and [Table 8-1](#).

8.2.2.1 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall design size. Lower switching frequency implies reduced switching losses, usually resulting in less power dissipated in the IC. Lower power dissipated in the IC results in higher system efficiency and a lower IC temperature. However, higher switching frequency allows the use of smaller inductors and output capacitors, hence, a more compact design. Many applications require that the AM band be avoided. These applications tend to operate at either 400kHz below the AM band, or 2.2MHz above the AM band. In this example, 400kHz is chosen.

8.2.2.2 Setting the Output Voltage

The output voltage of the LM614xxT-Q1 is externally adjustable using a resistor divider network. Two divider networks for two recommended output voltages are found in [Table 8-2](#). The divider network is comprised of the top and bottom feedback resistors, R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{FB} = 1V. The total resistance of the divider is a compromise between excessive noise pickup and excessive loading of the output. Lower resistance values reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for R_{FBT} is 100kΩ with a maximum value of 1MΩ. If 1MΩ is selected for R_{FBT}, then a feedforward capacitor C_{FF} must be used across this resistor to provide adequate loop phase margin (see [Section 8.2.2.9](#)). Once R_{FBT} is selected, [Equation 1](#) is used to select R_{FBB}. For this 5V example, R_{FBT} = 100kΩ and R_{FBB} = 24.9kΩ.

8.2.2.3 Inductor Selection

The main parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current. The inductance is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current for systems with a fixed input voltage. For systems with a variable input voltage such as the 12V battery in a car, 25% is commonly used. This example uses V_{IN} = 13.5V, which is closer to the nominal voltage of a 12V car battery. When selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, the maximum device current must still be used for this calculation. [Equation 5](#) can be used to determine the value of the inductance. The constant K is the percentage of peak-to-peak inductor current ripple to rated output current. For this 10A, 400kHz, 5V example, K = 0.25 is chosen and an inductance of approximately 3.15μH is found. The closest standard value of 3μH is selected.

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times K \times I_{OUTmax}} \times \frac{V_{OUT}}{V_{IN}} \quad (5)$$

Ideally, the saturation current rating of the inductor must be at least as large as the high-side switch current limit, I_{SC}. This size makes sure that the inductor does not saturate, even during a soft-short condition on the output. A hard short causes the LM614xxT-Q1 to enter hiccup mode (see [Section 7.3.13](#)). A soft short can hold the output current at current limit without triggering hiccup. When the inductor core material saturates, the inductance can fall to a very low value, causing the inductor current to rise very rapidly. Although the valley

current limit, $I_{LS-LIMIT}$, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly. This action can lead to component damage, so the inductor not saturating is crucial. Inductors with a ferrite core material have very hard saturation characteristics, but usually have lower core losses than powdered iron cores. Powdered iron cores exhibit a soft saturation, allowing some relaxation in the saturation current rating of the inductor. However, powdered iron cores have more core losses at frequencies typically above 1MHz. To avoid subharmonic oscillation, the inductance value must not be less than that given in Equation 6. The maximum inductance is limited by the minimum current ripple required for the current mode control to perform correctly. As a rule-of-thumb, the minimum inductor ripple current must be no less than about 10% of the device maximum rated current under nominal conditions.

$$L > \frac{V_{OUT}}{f_{SW} \times 0.6 \times I_{RATED}} \quad (6)$$

8.2.2.4 Output Capacitor Selection

The output capacitor value and ESR determine the output voltage ripple and load transient performance. The output capacitor is usually limited by the load transient requirements rather than the output voltage ripple. Table 8-3 can be used to find capacitor values for C_{OUT} and C_{FF} for a few common applications. Note that 4.99kΩ R_{FF} must be used in series with C_{FF} . In this example, good transient performance is desired, giving 4 × 47μF ceramic + 220μF electrolytic as the output capacitor and 15pF as C_{FF} .

Table 8-3. Selected Output Capacitor and C_{FF} Values

FREQUENCY	I_{OUT}	TRANSIENT PERFORMANCE	3.3V OUTPUT		5V OUTPUT	
			C_{OUT}	C_{FF}	C_{OUT}	C_{FF}
2.2MHz	10A	Minimum	4 × 22μF ceramic	15pF	2 × 22μF ceramic + 220μF electrolytics	15pF
2.2MHz	10A	Better Transient	4 × 22μF ceramic + 220μF electrolytics	15pF	2 × 22μF ceramic + 220μF electrolytics	15pF
2.2MHz	8A	Minimum	5 × 22μF ceramic	15pF	3 × 22μF ceramic	15pF
2.2MHz	8A	Better Transient	5 × 22μF ceramic + 220μF electrolytic	15pF	3 × 22μF ceramic + 220μF electrolytic	15pF

8.2.2.5 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum of 10μF ceramic capacitance is required on the input of the LM614xxT-Q1. Use 2 × 10μF ceramic capacitance or more for better EMI performance. This must be rated for at least the maximum input voltage that the application requires. Having twice the maximum input voltage to reduce DC bias derating is preferable. This capacitance can be increased to help reduce input voltage ripple and maintain the input voltage during load transients. In addition, a small case size (0603 or 0402) ceramic capacitor must be used at each input, ground pin pair, VIN1/PGND1 and VIN2/PGND2, immediately adjacent to the regulator. The capacitor must have a voltage rating of at least double the maximum input voltage to minimize derating. The capacitor must also have an X7R or better dielectric. Choose the highest capacitor value with these parameters. This capacitor value provides a high frequency bypass to reduce switch-node ring and electromagnetic interference emissions. The QFN (VAM) package provides two input voltage pins and two power ground pins on opposite sides of the package. These pins allow the input capacitors to be split and placed optimally with respect to the internal power MOSFETs, thus improving the effectiveness of the input bypassing. This example places two 10μF, 50V, 1206, X7R ceramic capacitors and two 0.47μF, 50V, 0603, X7R ceramic capacitors at each VIN/PGND pin pair.

Often, using an electrolytic capacitor on the input in parallel with the ceramics is desirable. This statement is especially true if long leads, traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help dampen ringing on the input supply caused by the inductance of the long power leads. The use of this additional capacitor also helps with momentary voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitors. The approximate worst case RMS value of this current can be calculated with [Equation 7](#). This value must be checked against the manufacturer maximum ratings.

$$I_{\text{RMS}} \approx \frac{I_{\text{OUT}}}{2} \quad (7)$$

8.2.2.6 BOOT Capacitor

The LM614xxT-Q1 requires a bootstrap capacitor connected between the CBOOT pin and the SW pin. This capacitor stores energy, which is used to supply the gate drivers for the power MOSFETs. A high-quality 100nF ceramic capacitor with a rating of at least 10V is required. The package provides space between the VIN2 and RBOOT pins to route SW to the boot capacitor without needing long traces or multi-layer routing.

8.2.2.7 BOOT Resistor

A BOOT resistor can be connected between the CBOOT and RBOOT pins to slow the rise-time of the SW node. If EMI performance is not critical, these two pins can be shorted. If EMI is critical, use a 0Ω placeholder. The value can be increased if additional EMI margin is required. Increase to 200Ω as a first step. This increase slows the rise-time of the SW node, reducing EMI at hundreds of MHz by a few dBμV. This action is at the expense of about 0.3% efficiency at 400kHz at 10A. Use 50Ω for a similar efficiency drop at 2.2MHz at 8A. In this example, 0Ω is chosen to maximize efficiency. Continue to increase the value of RBOOT to further improve high-frequency EMI emissions at the expense of lower efficiency. RBOOT connected to pins RBOOT and CBOOT can be any value between a short and an open without triggering BOOT UVLO.

8.2.2.8 VCC

The VCC pin is the output of the internal LDO used as a supply to the internal control circuits of the regulator. This output requires a 1μF, 16V, X7R or similar, 0603 or similar ceramic capacitor connected from VCC to AGND for proper operation. Generally avoid loading this output with any external circuitry. However, this output can be used to supply the pullup for the RESET (power-good) function (see [Section 7.3.6](#)). A pullup resistor with value of 100kΩ is a good choice in this case. The nominal output voltage on VCC is 3.3V. Do not short this output to ground or any other external voltage.

8.2.2.9 C_{FF} and R_{FF} Selection

A feedforward capacitor, C_{FF} on the order of tens of picofarads, is used to improve phase margin and transient response of circuits which have output capacitors with low ESR. Because this C_{FF} capacitor can conduct noise from the output of the circuit directly to the FB node of the IC, a 4.99kΩ resistor, R_{FF}, must be placed in series with C_{FF}. If the ESR zero of the output capacitor is below 200kHz, no C_{FF} must be used.

If output voltage is less than 2.5V, C_{FF} has little effect, so C_{FF} can be omitted. If output voltage is greater than 14V, C_{FF} must be used cautiously because C_{FF} can easily introduce too much gain at higher frequencies.

If 1MΩ is selected for R_{F_{BT}}, then a feedforward capacitor C_{FF} must be used.

8.2.2.10 R_{SPSP} Selection

The SPSP pin can be connected to GND to disable spread spectrum. The pin can be connected to VCC to enable spread spectrum. The pin can also be connected to GND through a resistor to enable spread spectrum with ripple cancellation. This action actively reduces the output ripple associated with spread spectrum which arises from the inductor current ripple amplitude modulation caused by the spread spectrum frequency modulation. The value is typically approximately 20kΩ and can be more precisely calculated using [Equation 4](#).

8.2.2.11 R_T Selection

The R_T resistor sets the switching frequency of the converter. See [Section 7.3.5](#) for more details. A resistor value of 40.2kΩ corresponds to 400kHz. The pin is also configured to set the switching frequency at 400kHz when the RT pin is connected to VCC. Connecting the RT pin to VCC allows the user to save cost and space, but placing a 40.2kΩ resistor allows for more flexibility if a different frequency is desired at a later time.

8.2.2.12 R_{MODE} Selection

The SYNC/MODE pin allows you to synchronize the converter to an external clock voltage (SYNC). The pin also allows the selection between two modes (MODE). The following are the selectable modes:

- Forced pulse width modulation (FPWM) operation, which operates at a fixed frequency at all loads in typical operation
- Auto mode, which automatically switches to pulse-frequency modulation (PFM) at light loads to improve light-load efficiency

Connect the SYNC/MODE pin to VCC for FPWM. Connect to GND for auto mode. The user can also apply a clock signal to synchronize the switching frequency to an external clock. See [Section 7.3.3](#) for more information.

8.2.2.13 External UVLO

In some cases, the user can need an input undervoltage lockout (UVLO) level different than that provided internal to the device. This level can be accomplished by using the circuit shown in [Figure 7-2](#). The input voltage at which the device turns on is designated V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10kΩ to 100kΩ, then [Equation 2](#) is used to calculate R_{ENT} and V_{OFF}.

8.2.2.14 Maximum Ambient Temperature

As with any power conversion device, the LM614xxT-Q1 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient temperature. The internal die temperature (T_J) is a function of the following:

- Ambient temperature
- Power loss
- Effective thermal resistance, R_{θJA} of the device
- PCB layout

The maximum internal die temperature for the LM614xxT-Q1 must be limited to 150°C. This limit establishes a limit on the maximum device power dissipation and, therefore, the load current. [Equation 8](#) shows the relationships between the important parameters. Larger ambient temperatures (T_A) and larger values of R_{θJA} reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in the [Application Curves](#) section. If the desired operating conditions cannot be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of R_{θJA} is more difficult to estimate. As stated in the [Semiconductor and IC Package Thermal Metrics application note](#), the value of R_{θJA} given in the [Section 6.4](#) is not valid for design purposes and must not be used to estimate the thermal performance of the device in a real application. The values reported in the [Section 6.4](#) table are measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{\text{out}} |_{\text{MAX}} = \frac{(T_J - T_A)}{R_{\theta JA}} \times \frac{\eta}{1 - \eta} \times \frac{1}{V_{\text{OUT}}} \quad (8)$$

where

- η = efficiency
- T_A = ambient temperature in °C
- T_J = junction temperature in °C
- R_{θJA} = the effective thermal resistance of the IC junction to the air, mainly through the PCB in °C/W

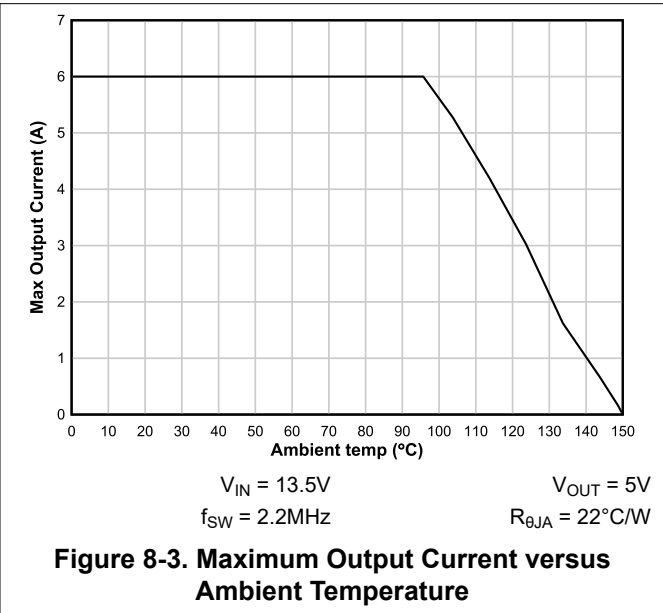
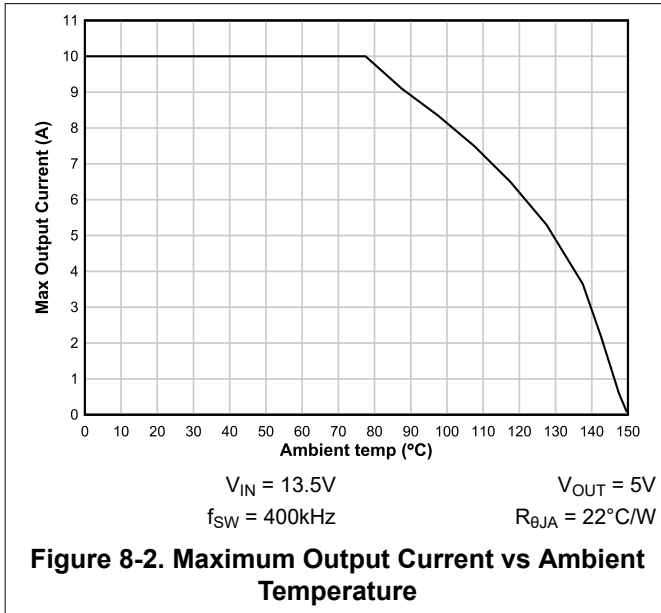
The effective R_{θJA} is a critical parameter and depends on many factors (just to mention a few of the most critical parameters:

- Power dissipation
- Air temperature
- Airflow
- PCB area
- Copper area

- Heatsink size
- Number of thermal vias under or near the package
- Adjacent component placement

Due to the ultra-miniature size of the VQFN (VAM) package, a die-attach pad is not available, requiring most of the heat to flow from the pins to the board. This action means that this package exhibits a somewhat large $R_{\theta JA}$ value when the layout does not allow for heat to flow from the pins. A typical curve of maximum output current versus ambient temperature is shown in [Figure 8-2](#) and [Figure 8-3](#) for a good thermal layout. This data was taken on the LM61495RPHEVM evaluation board with a device and PCB combination, giving an $R_{\theta JA}$ of about 21.6°C/W. Remember that the data given in these graphs are for illustration purposes only, and the actual performance in any given application depends on all of the previously mentioned factors.

ADVANCE INFORMATION

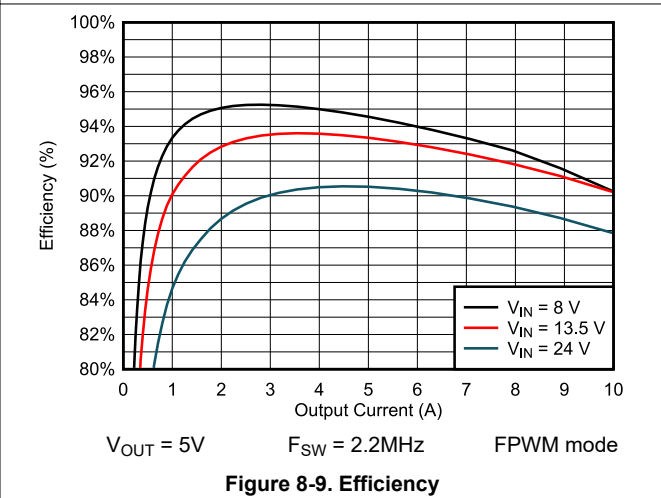
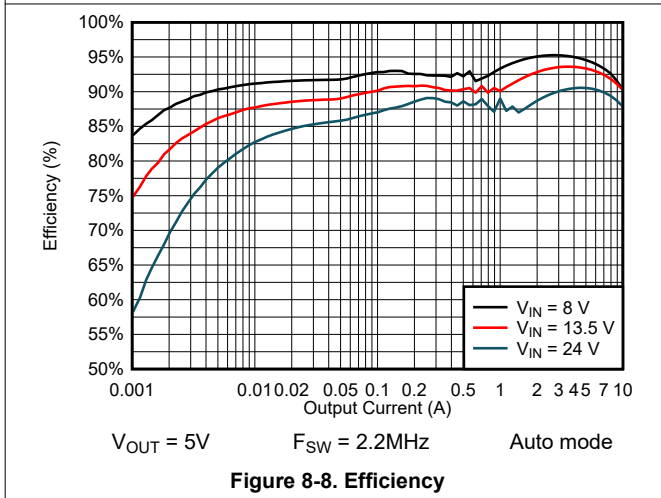
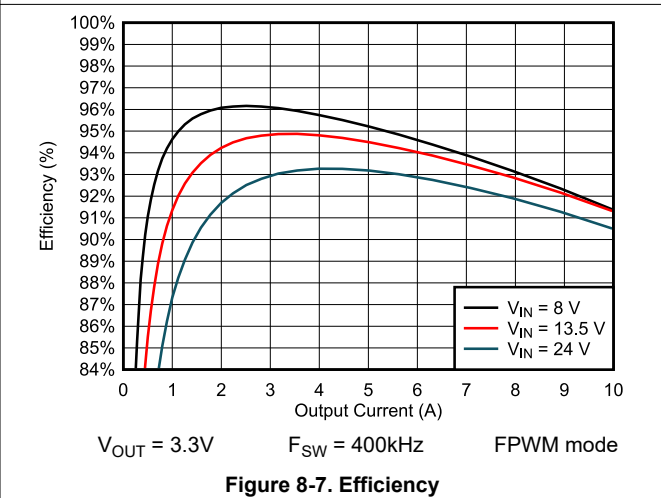
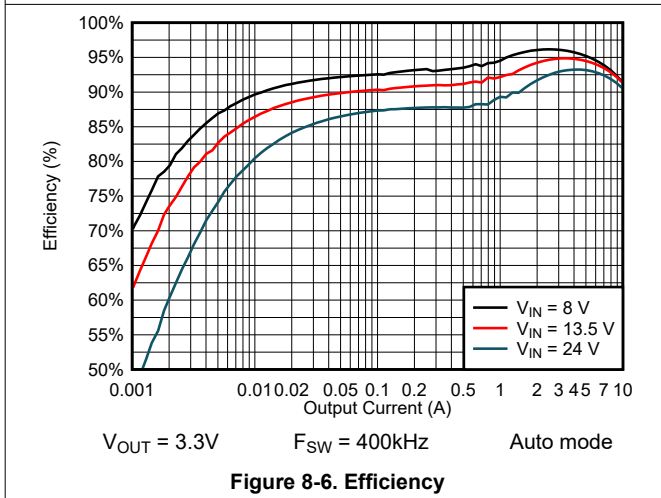
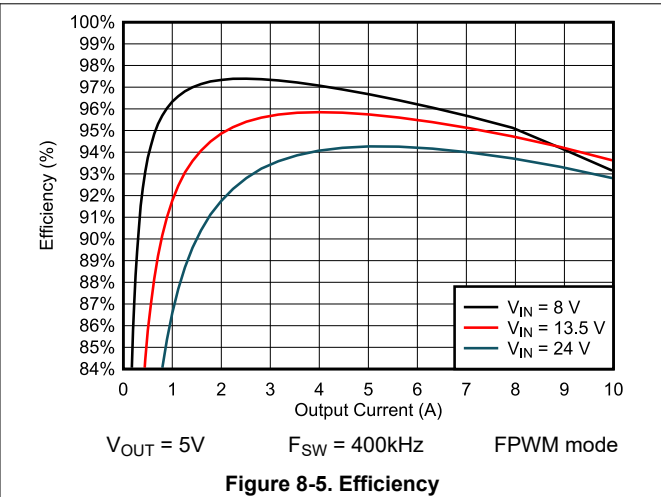
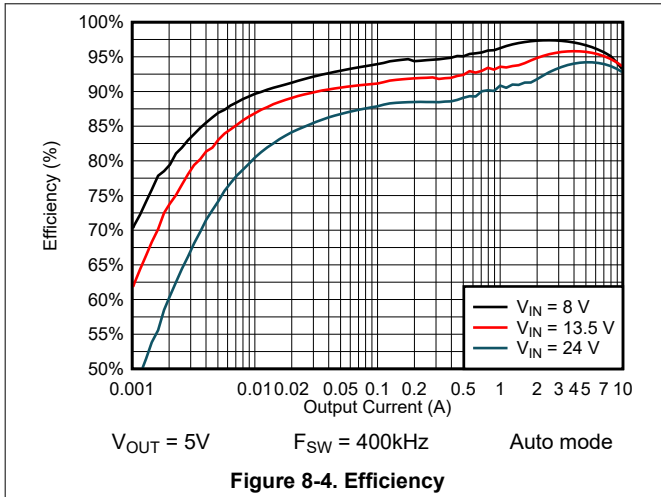


Use the following resources as a guide to excellent thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- [Thermal Design by Insight not Hindsight application note](#)
- [A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages application note](#)
- [Semiconductor and IC Package Thermal Metrics application note](#)
- [Thermal Design Made Simple with LM43603 and LM43602 application note](#)
- [PowerPAD™ Thermally Enhanced Package application note](#)
- [PowerPAD™ Made Easy application brief](#)
- [Using New Thermal Metrics application note](#)

8.2.3 Application Curves

Unless otherwise specified, the following conditions apply: device: LM61495-Q1, $V_{IN} = 13.5V$, $T_A = 25^\circ C$. The circuit is shown in Figure 8-1, with the appropriate BOM from Table 8-4.

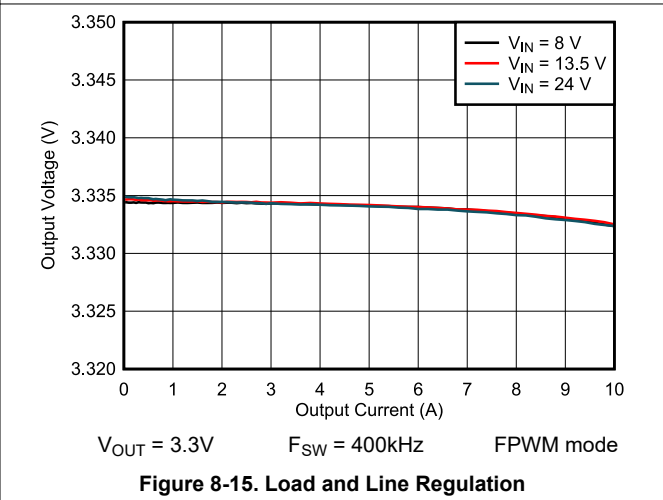
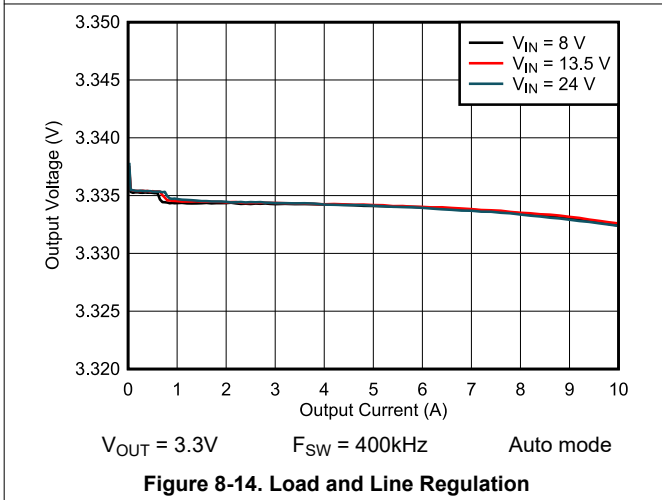
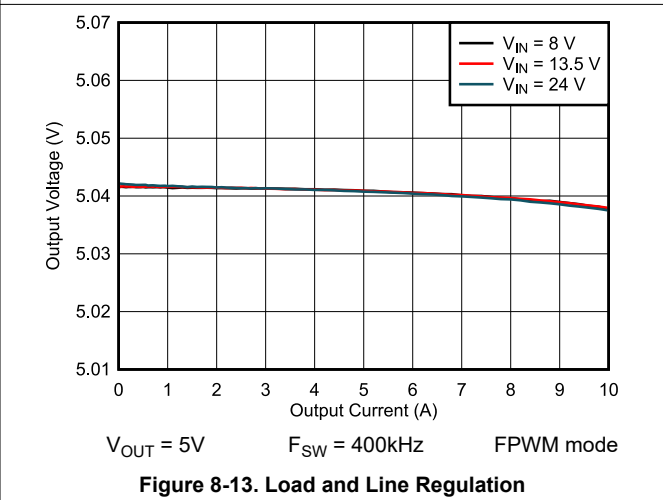
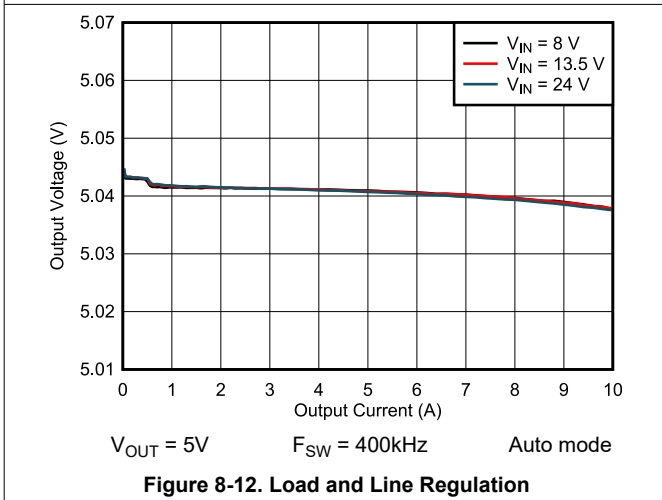
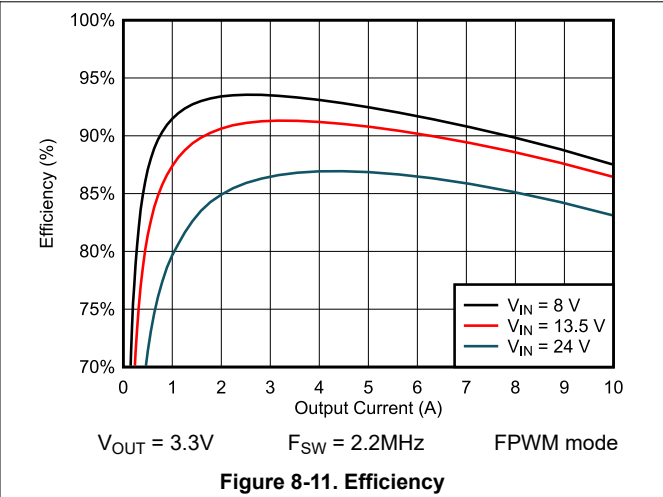
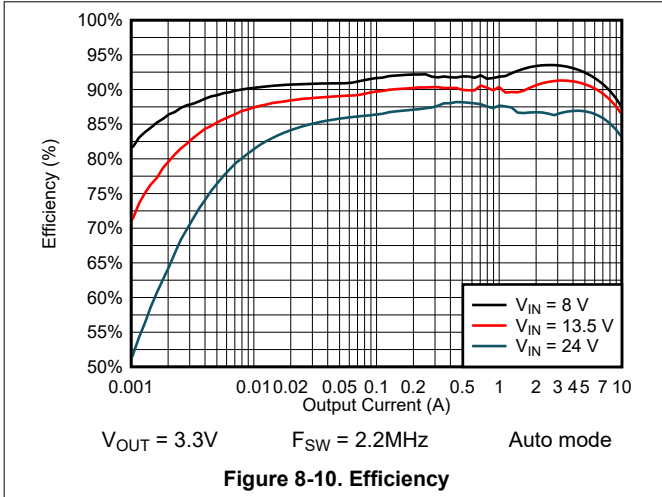


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8.2.3 Application Curves (continued)

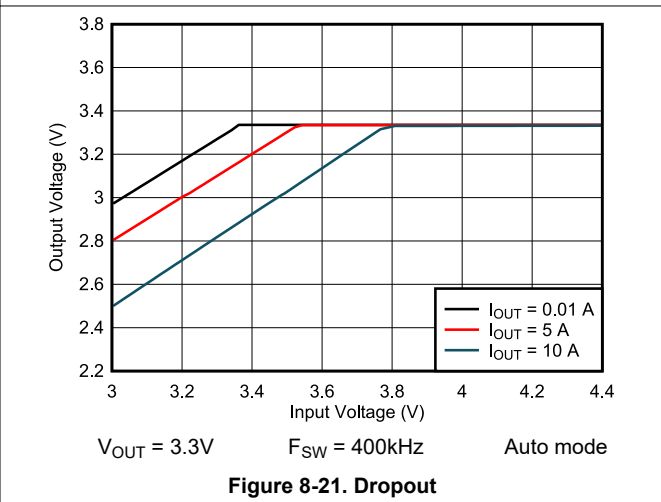
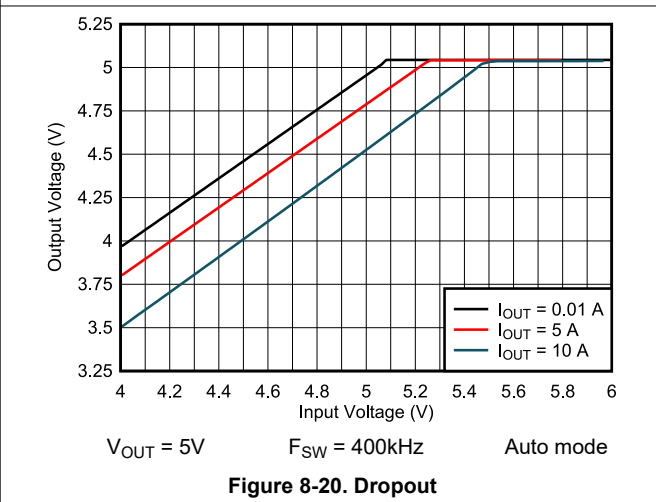
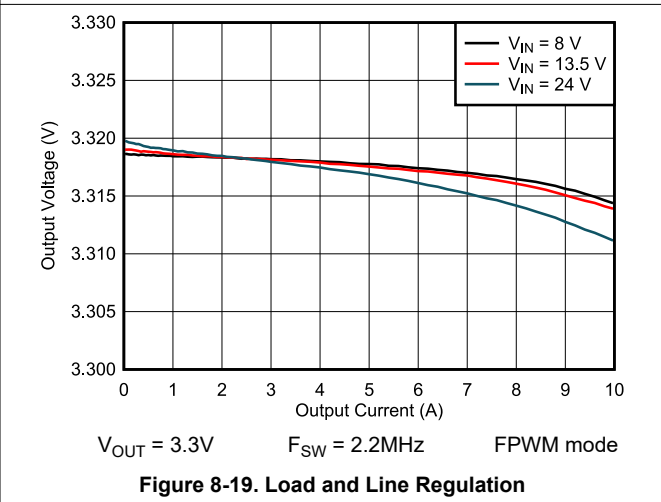
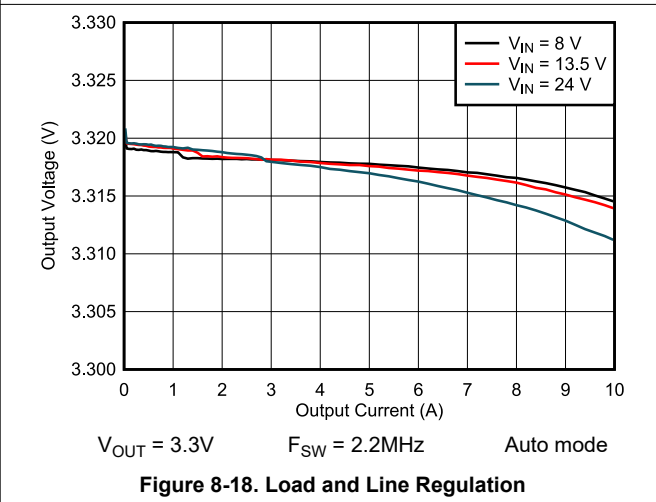
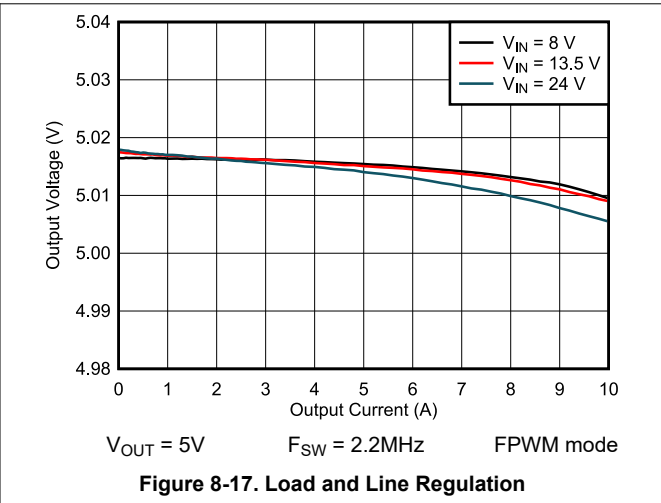
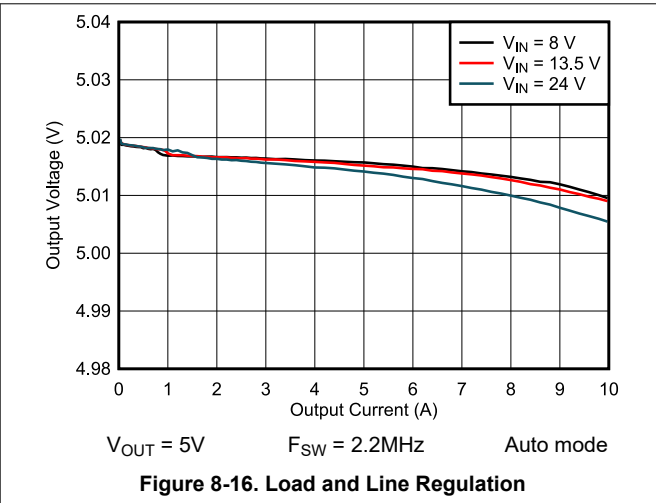
Unless otherwise specified, the following conditions apply: device: LM61495-Q1, $V_{IN} = 13.5V$, $T_A = 25^\circ C$. The circuit is shown in Figure 8-1, with the appropriate BOM from Table 8-4.

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8.2.3 Application Curves (continued)

Unless otherwise specified, the following conditions apply: device: LM61495-Q1, $V_{IN} = 13.5V$, $T_A = 25^\circ C$. The circuit is shown in Figure 8-1, with the appropriate BOM from Table 8-4.



8.2.3 Application Curves (continued)

Unless otherwise specified, the following conditions apply: device: LM61495-Q1, $V_{IN} = 13.5V$, $T_A = 25^\circ C$. The circuit is shown in Figure 8-1, with the appropriate BOM from Table 8-4.

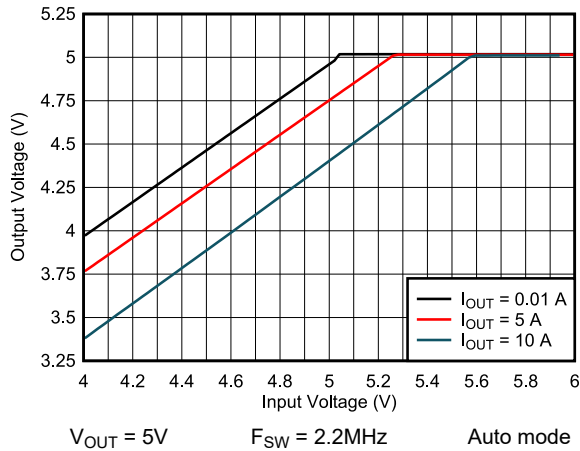


Figure 8-22. Dropout

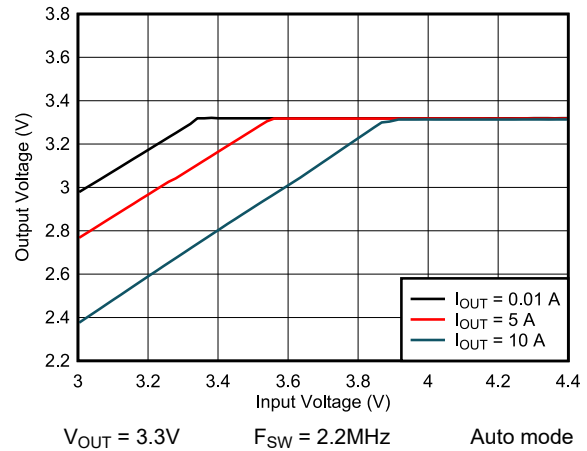


Figure 8-23. Dropout

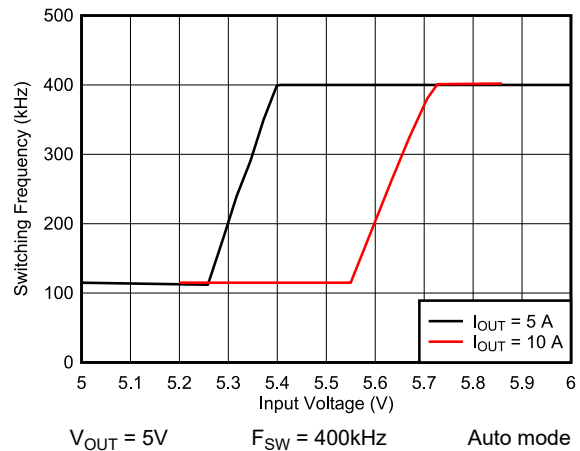


Figure 8-24. Frequency Dropout

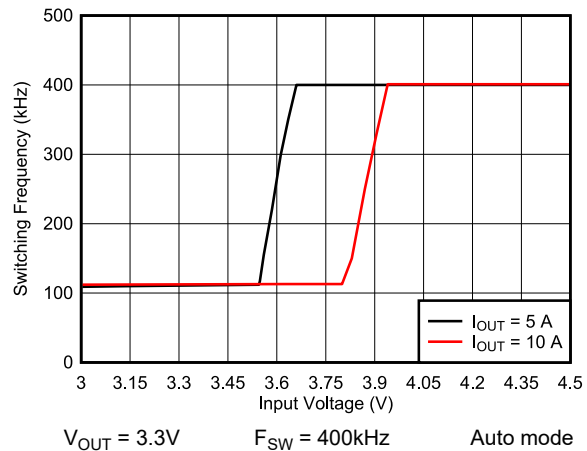


Figure 8-25. Frequency Dropout

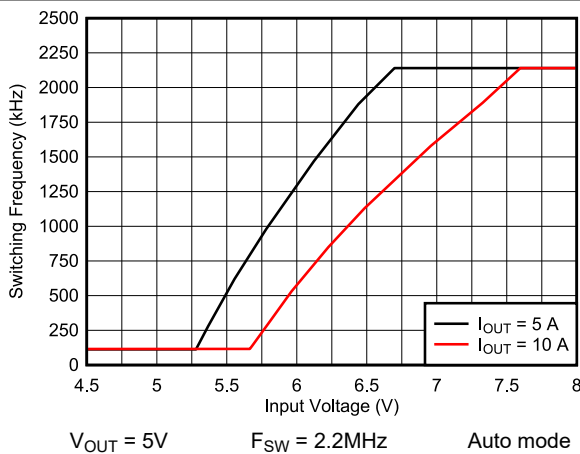


Figure 8-26. Frequency Dropout

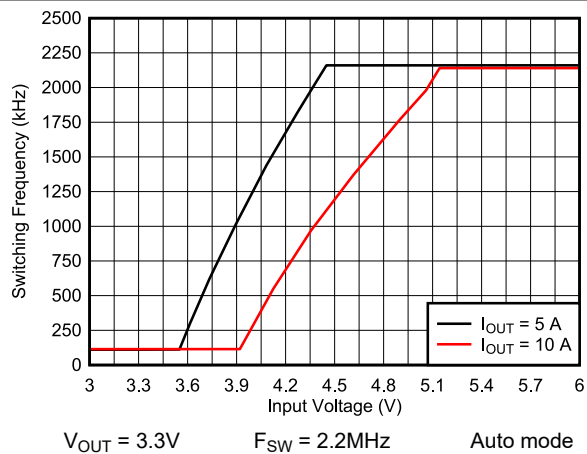
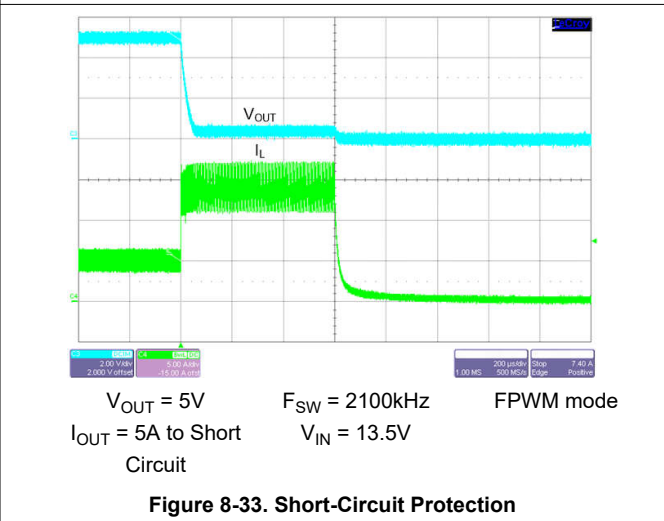
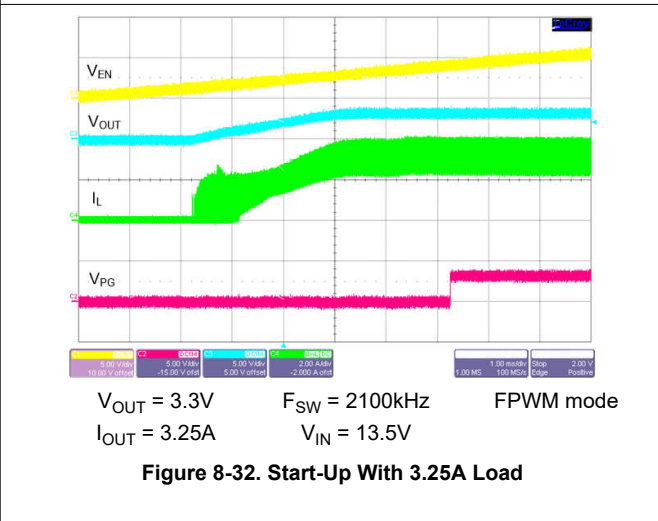
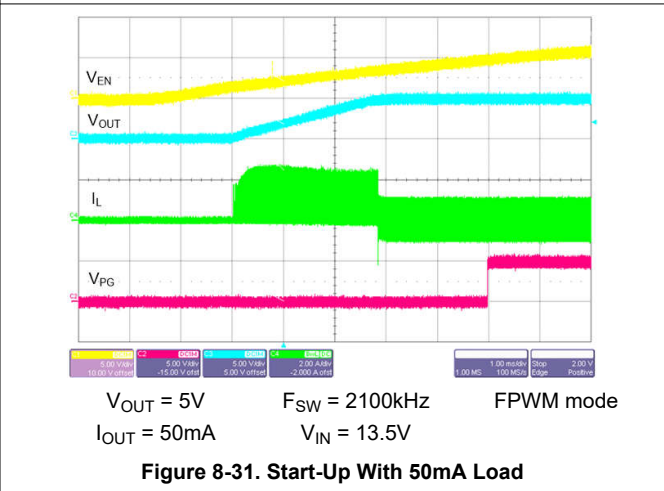
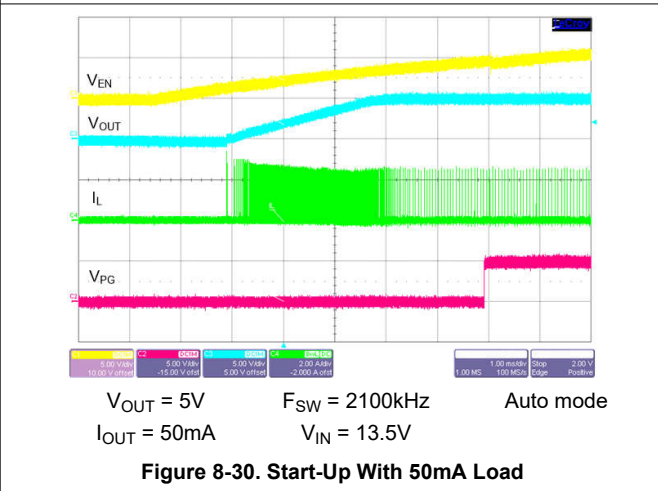
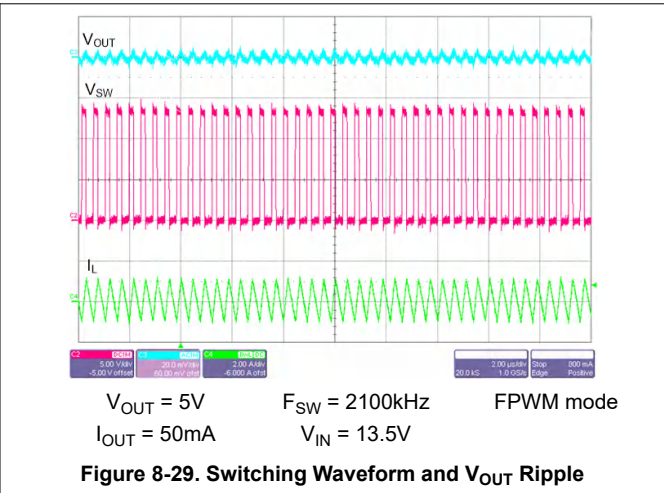
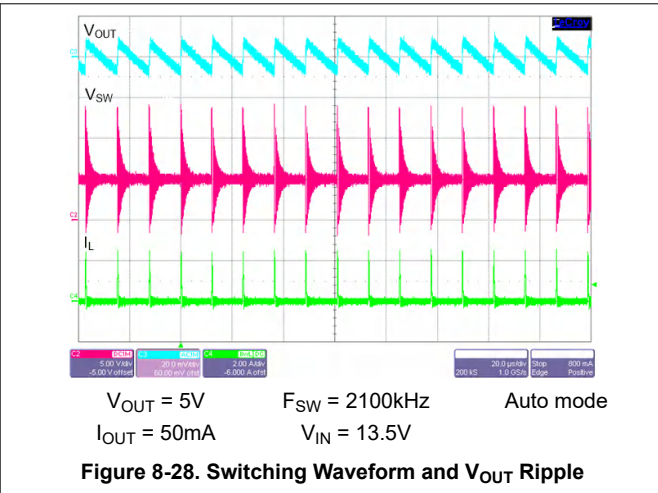


Figure 8-27. Frequency Dropout

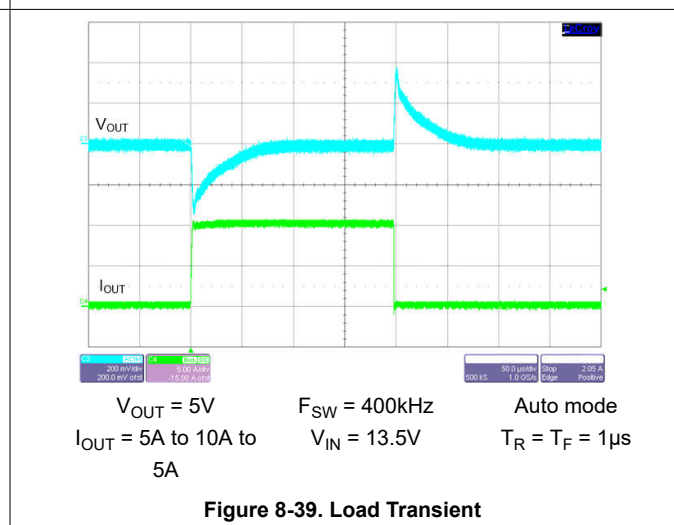
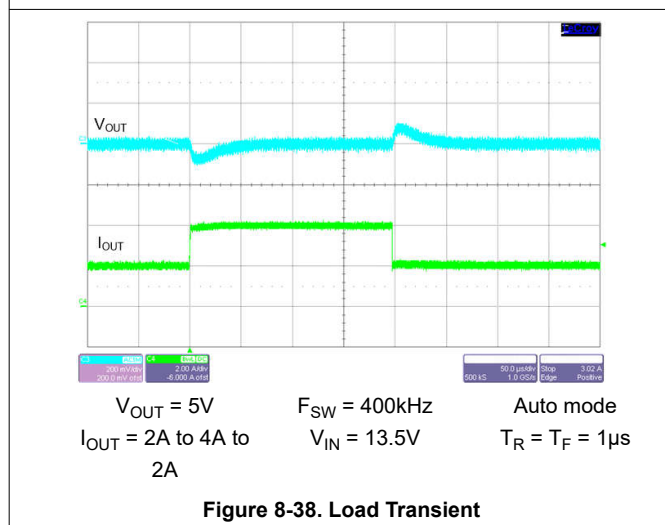
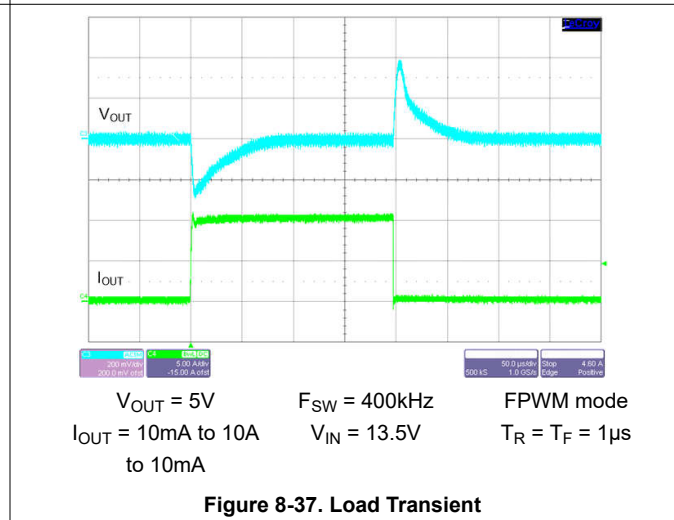
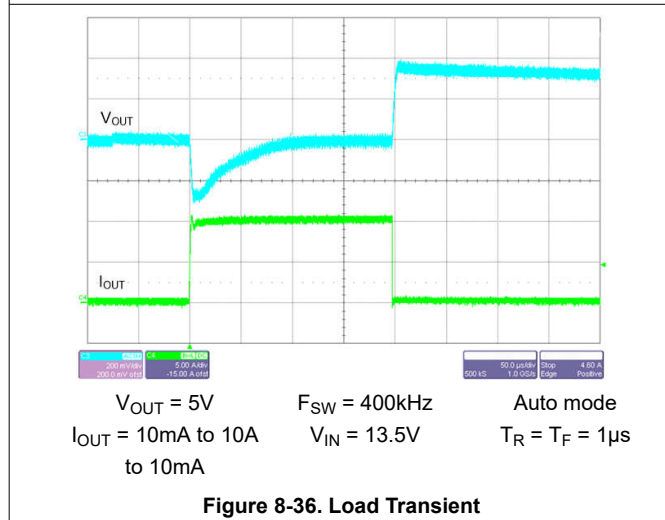
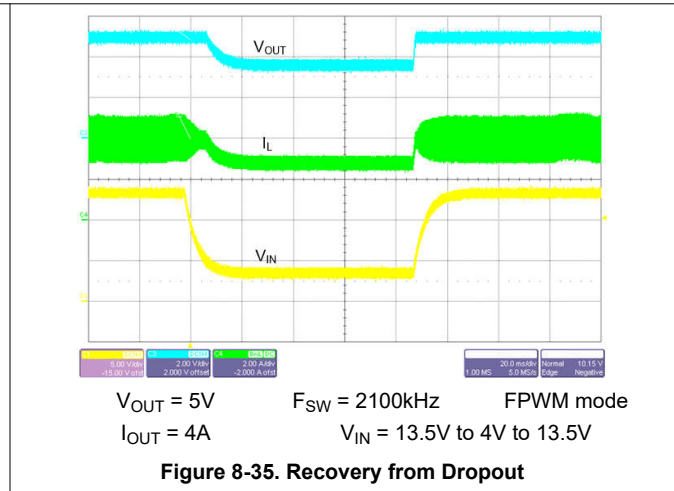
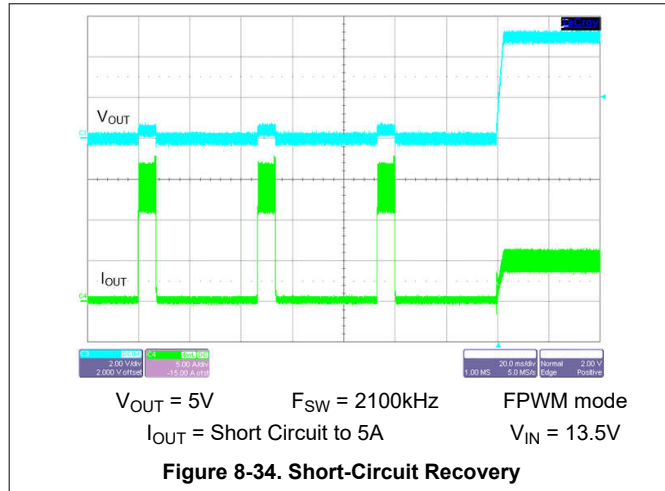
8.2.3 Application Curves (continued)

Unless otherwise specified, the following conditions apply: device: LM61495-Q1, $V_{IN} = 13.5V$, $T_A = 25^\circ C$. The circuit is shown in Figure 8-1, with the appropriate BOM from Table 8-4.



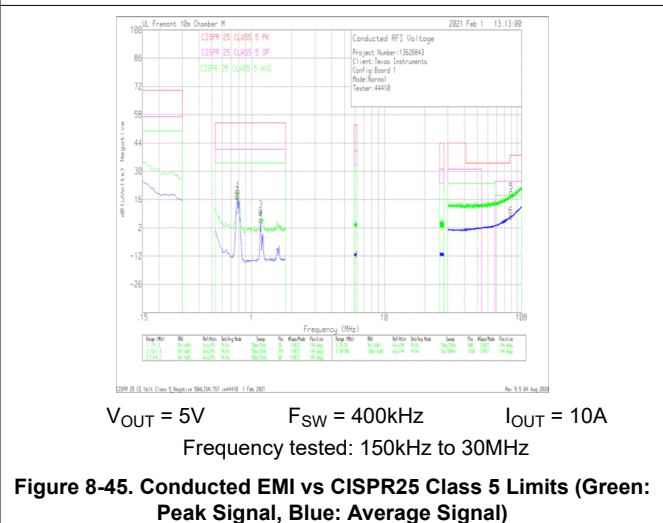
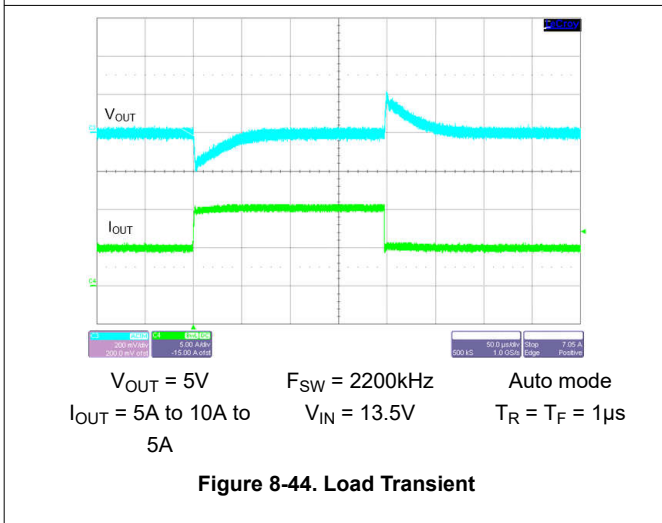
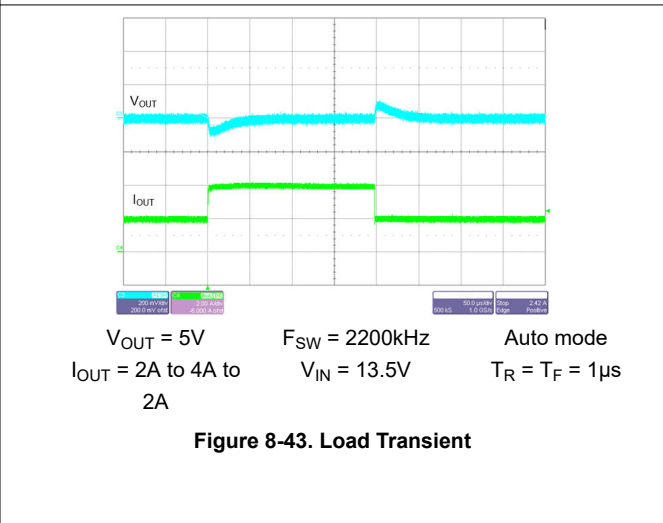
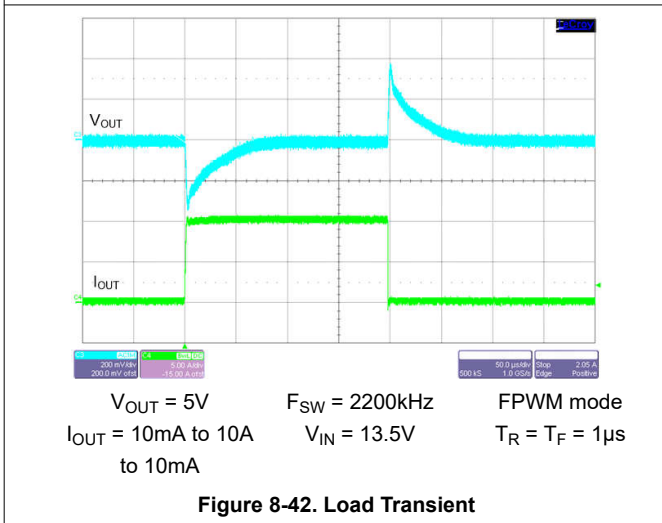
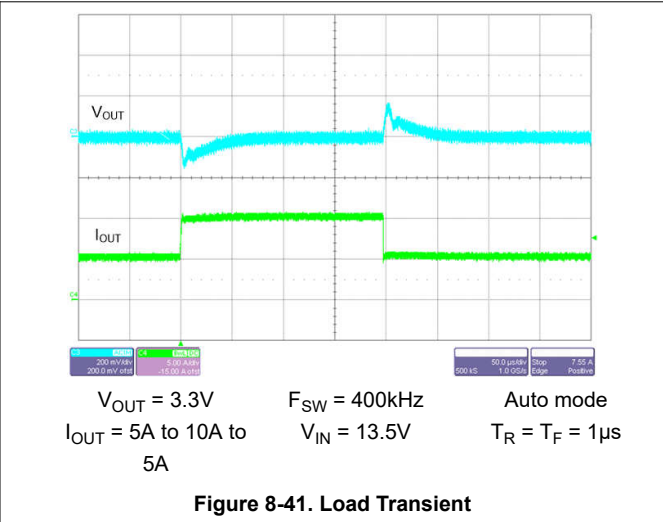
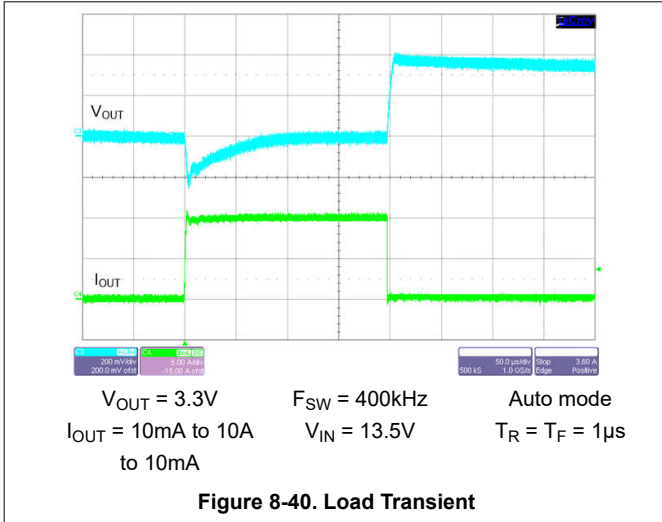
8.2.3 Application Curves (continued)

Unless otherwise specified, the following conditions apply: device: LM61495-Q1, $V_{IN} = 13.5V$, $T_A = 25^\circ C$. The circuit is shown in Figure 8-1, with the appropriate BOM from Table 8-4.



8.2.3 Application Curves (continued)

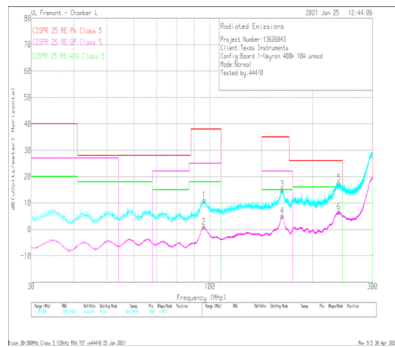
Unless otherwise specified, the following conditions apply: device: LM61495-Q1, $V_{IN} = 13.5V$, $T_A = 25^\circ C$. The circuit is shown in Figure 8-1, with the appropriate BOM from Table 8-4.



8.2.3 Application Curves (continued)

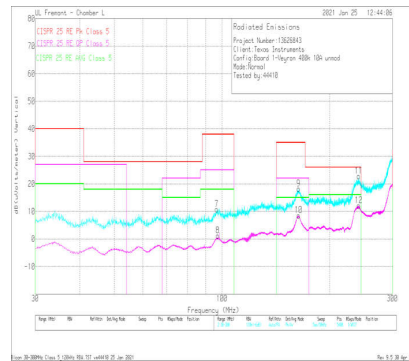
Unless otherwise specified, the following conditions apply: device: LM61495-Q1, $V_{IN} = 13.5V$, $T_A = 25^{\circ}C$. The circuit is shown in Figure 8-1, with the appropriate BOM from Table 8-4.

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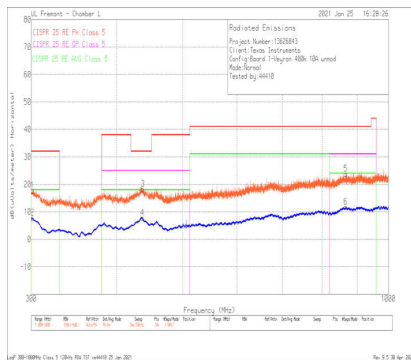
$V_{OUT} = 5V$ $F_{SW} = 400kHz$ $I_{OUT} = 10A$
Frequency tested: 30MHz to 300MHz

Figure 8-46. Radiated EMI Bicon Horizontal vs CISPR25 Class 5 Limits



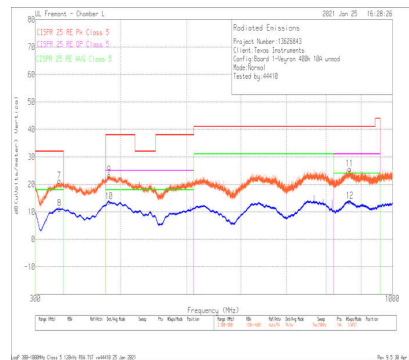
$V_{OUT} = 5V$ $F_{SW} = 400kHz$ $I_{OUT} = 10A$
Frequency tested: 30MHz to 300MHz

Figure 8-47. Radiated EMI Bicon Vertical vs CISPR25 Class 5 Limits



$V_{OUT} = 5V$ $F_{SW} = 400kHz$ $I_{OUT} = 10A$
Frequency tested: 300MHz to 1GHz

Figure 8-48. Radiated EMI Log Horizontal vs CISPR25 Class 5 Limits



$V_{OUT} = 5V$ $F_{SW} = 400kHz$ $I_{OUT} = 10A$
Frequency tested: 300MHz to 1GHz

Figure 8-49. Radiated EMI Log Vertical vs CISPR25 Class 5 Limits

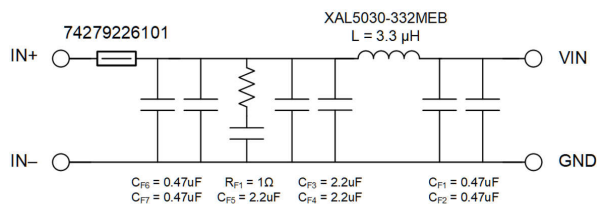
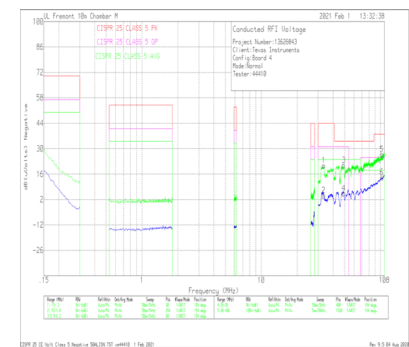


Figure 8-50. Recommended Input EMI Filter

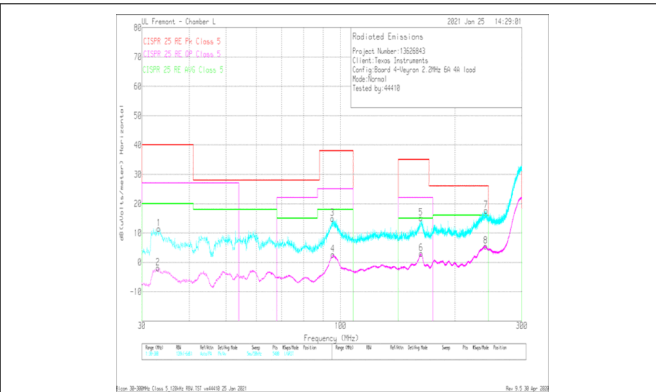


$V_{OUT} = 5V$ $F_{SW} = 2.2MHz$ $I_{OUT} = 4A$
Frequency tested: 150kHz to 30MHz

Figure 8-51. Conducted EMI vs CISPR25 Class 5 Limits (Green: Peak Signal, Blue: Average Signal)

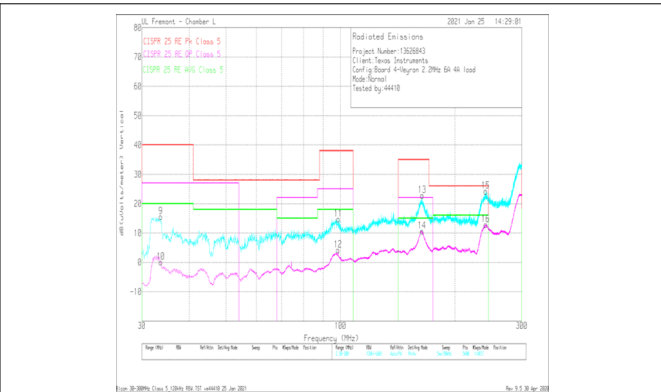
8.2.3 Application Curves (continued)

Unless otherwise specified, the following conditions apply: device: LM61495-Q1, $V_{IN} = 13.5V$, $T_A = 25^{\circ}C$. The circuit is shown in Figure 8-1, with the appropriate BOM from Table 8-4.



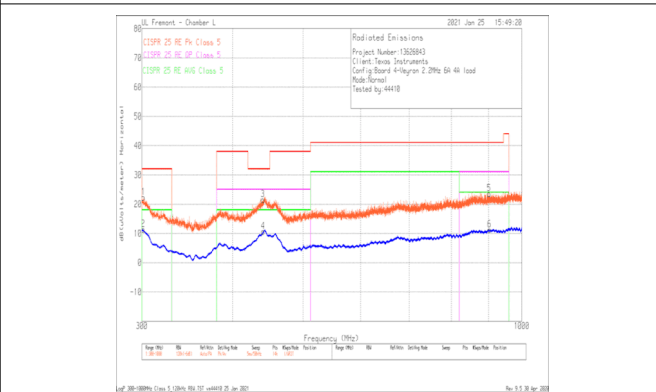
$V_{OUT} = 5V$ $F_{SW} = 2.2MHz$ $I_{OUT} = 4A$
Frequency tested: 30MHz to 300MHz

Figure 8-52. Radiated EMI Bicon Horizontal vs CISPR25 Class 5 Limits



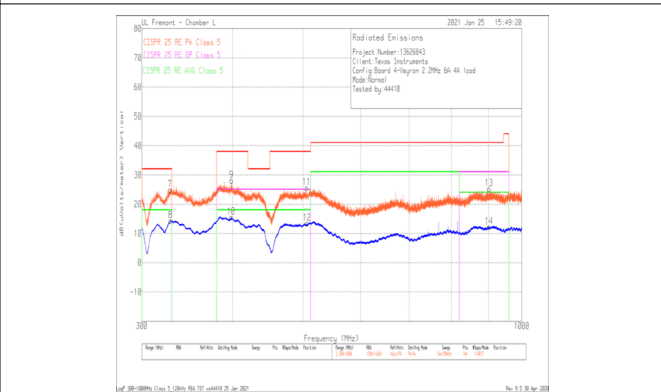
$V_{OUT} = 5V$ $F_{SW} = 2.2MHz$ $I_{OUT} = 4A$
Frequency tested: 30MHz to 300MHz

Figure 8-53. Radiated EMI Bicon Vertical vs CISPR25 Class 5 Limits



$V_{OUT} = 5V$ $F_{SW} = 2.2MHz$ $I_{OUT} = 4A$
Frequency tested: 300MHz to 1GHz

Figure 8-54. Radiated EMI Log Horizontal vs CISPR25 Class 5 Limits



$V_{OUT} = 5V$ $F_{SW} = 2.2MHz$ $I_{OUT} = 4A$
Frequency tested: 300MHz to 1GHz

Figure 8-55. Radiated EMI Log Vertical vs CISPR25 Class 5 Limits

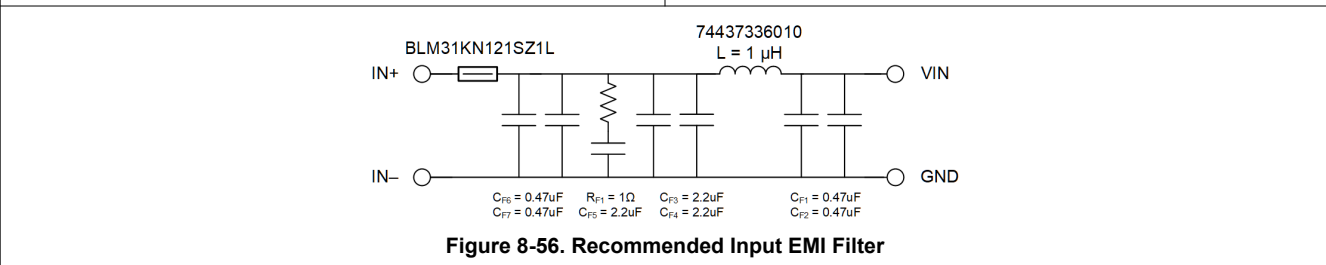


Figure 8-56. Recommended Input EMI Filter

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8.2.3 Application Curves (continued)

Unless otherwise specified, the following conditions apply: device: LM61495-Q1, $V_{IN} = 13.5V$, $T_A = 25^\circ C$. The circuit is shown in [Figure 8-1](#), with the appropriate BOM from [Table 8-4](#).

Table 8-4. BOM for Typical Application Curves

V_{OUT}	FREQUENCY	R_{FBB}	C_{OUT}	$C_{IN} + C_{HF}$	L	C_{FF}
3.3V	400kHz	43.2k Ω	4 × 47 μ F + 100 μ F electrolytic + 2 × 2.2 μ F	4 × 10 μ F + 2 × 470nF + 100 μ F electrolytic	2.4 μ H (744325240)	22pF
3.3V	2.2MHz	43.2k Ω	2 × 47 μ F + 100 μ F electrolytic + 2 × 2.2 μ F	2 × 10 μ F + 2 × 470nF + 100 μ F electrolytic	0.68 μ H (744373460068)	10pF
5V	400kHz	24.9k Ω	4 × 47 μ F + 100 μ F electrolytic + 2 × 2.2 μ F	4 × 10 μ F + 2 × 470nF + 100 μ F electrolytic	2.4 μ H (744325240)	22pF
5V	2.2MHz	24.9k Ω	2 × 47 μ F + 100 μ F electrolytic + 2 × 2.2 μ F	2 × 10 μ F + 2 × 470nF + 100 μ F electrolytic	0.68 μ H (744373460068)	10pF

8.3 Power Supply Recommendations

The characteristics of the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with [Equation 9](#).

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (9)$$

where

- η is the efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR ceramic input capacitors, can form an underdamped resonant circuit. This can result in overvoltage transients at the input to the regulator or tripping UVLO. Consider that the supply voltage can dip when a load transient is applied to the output depending on the parasitic resistance and inductance of the harness and characteristics of the supply. If the application is operating close to the minimum input voltage, this dip can cause the regulator to momentarily shut down and reset. The best way to solve these kinds of issues is to reduce the distance from the input supply to the regulator. Additionally, use an aluminum input capacitor in parallel with the ceramics. The moderate ESR of this type of capacitor helps damp the input resonant circuit and reduce any overshoots or undershoots. A value in the range of 20 μ F to 100 μ F is usually sufficient to provide input damping and help hold the input voltage steady during large load transients.

In some cases, a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a snap-back characteristic (thyristor type). TI does not recommend to use a device with this type of characteristic. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow can damage the device.

The input voltage must not be allowed to fall below the output voltage. In this scenario, such as a shorted input test, the output capacitors discharge through the internal parasitic diode found between the VIN and SW pins of the device. During this condition, the current can become uncontrolled, possibly causing damage to the device. If this scenario is considered likely, then use a Schottky diode between the input supply and the output.

8.4 Layout

8.4.1 Layout Guidelines

The PCB layout of any DC-DC converter is critical to the optimal performance of the design. Bad PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore,

the EMI performance of the regulator is dependent on the PCB layout to a great extent. In a buck converter, the most EMI-critical PCB feature is the loop formed by the input capacitor or capacitors and power ground. This loop is shown in Figure 8-57. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. Excessive transient voltages can disrupt the proper operation of the converter. Because of this disrupt, the traces in this loop must be wide and short while keeping the loop area as small as possible to reduce the parasitic inductance. Figure 8-58 shows a recommended layout for the critical components of the LM614xxT-Q1 circuit.

- *Place the input capacitor or capacitors as close as possible to the input pin pairs:* VIN1 to PGND1 and VIN2 to PGND2. Place the small capacitors closest. Each pair of pins are adjacent, simplifying the input capacitor placement. With the QFN package, there are two VIN/PGND pairs on either side of the package. These pins provide a symmetrical layout and helps minimize switching noise and EMI generation. Use a wide VIN plane on a mid-layer to connect both of the VIN pairs together to the input supply. Routing symmetrically from the supply to each VIN pin to best use the benefits of the symmetric pinout is best.
- *Place the bypass capacitor for VCC close to the VCC pin and AGND pin:* this capacitor must be routed with short, wide traces to the VCC and AGND pins.
- *Place the CBOOT capacitor as close as possible to the device with short, wide traces to the CBOOT and SW pins:* route the SW connection under the device through the gap between VIN2 and RBOOT pins, reducing exposed SW node area. If an RBOOT resistor is used, place as close as possible to the CBOOT and RBOOT pins. If high efficiency is desired, RBOOT and CBOOT pins can be shorted. This short must be placed as close as possible to the RBOOT and CBOOT pins.
- *Place the feedback divider as close as possible to the FB pin of the device:* place R_{FBB} , R_{FBT} , C_{FF} if used, and R_{FF} if used, physically close to the device. The connections to FB and AGND through R_{FBB} must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
- *MAke layer 2 of the PCB a ground plane:* this plane acts as a noise shield and as a heat dissipation path. Using layer 2 reduces the inclosed area in the input circulating current in the input loop, reducing inductance.
- *Provide wide paths for V_{IN} , V_{OUT} , and GND:* these paths must be as wide and direct as possible to reduce any voltage drops on the input or output paths of the converter to maximize efficiency.
- *Provide enough PCB area for proper heat sinking:* enough copper area must be used to make sure of a low $R_{\theta JA}$, considering maximum load current and ambient temperature. Make the top and bottom PCB layers with two-ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), thermal vias can also be connected to the inner layer heat-spreading ground planes. Note that the package of this device dissipates heat through all pins. Wide traces can be used for all pins except where noise considerations dictate minimization of area.
- *Keep the switch area small:* keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time, the total area of this node must be minimized to help reduce radiated EMI.

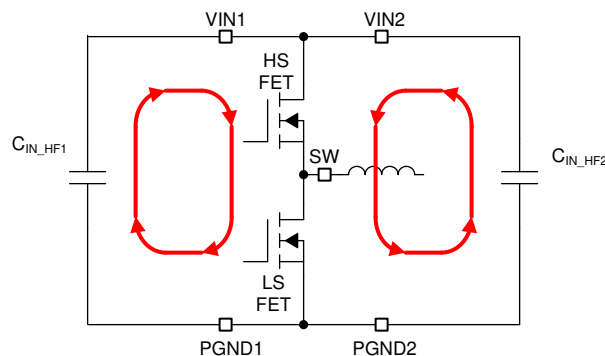


Figure 8-57. Input Current Loop

8.4.1.1 Ground and Thermal Considerations

As mentioned above, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces. A ground plane also provides a quiet reference potential for the control circuitry. The AGND and PGND pins must be connected to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low-side MOSFET, and connect directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and must be used for sensitive traces.

TI recommends providing adequate device heat sinking by using vias near PGND and VIN pins to connect to the system ground plane or V_{IN} strap, both of which dissipate heat. Use as much copper as possible for the system ground plane on the top and bottom layers and avoid plane cuts and bottlenecks for the heat flow for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2oz / 1oz / 1oz / 2oz. A four-layer board with enough copper thickness and proper layout provides low current conduction impedance, proper shielding, and low thermal resistance.

8.4.2 Layout Example

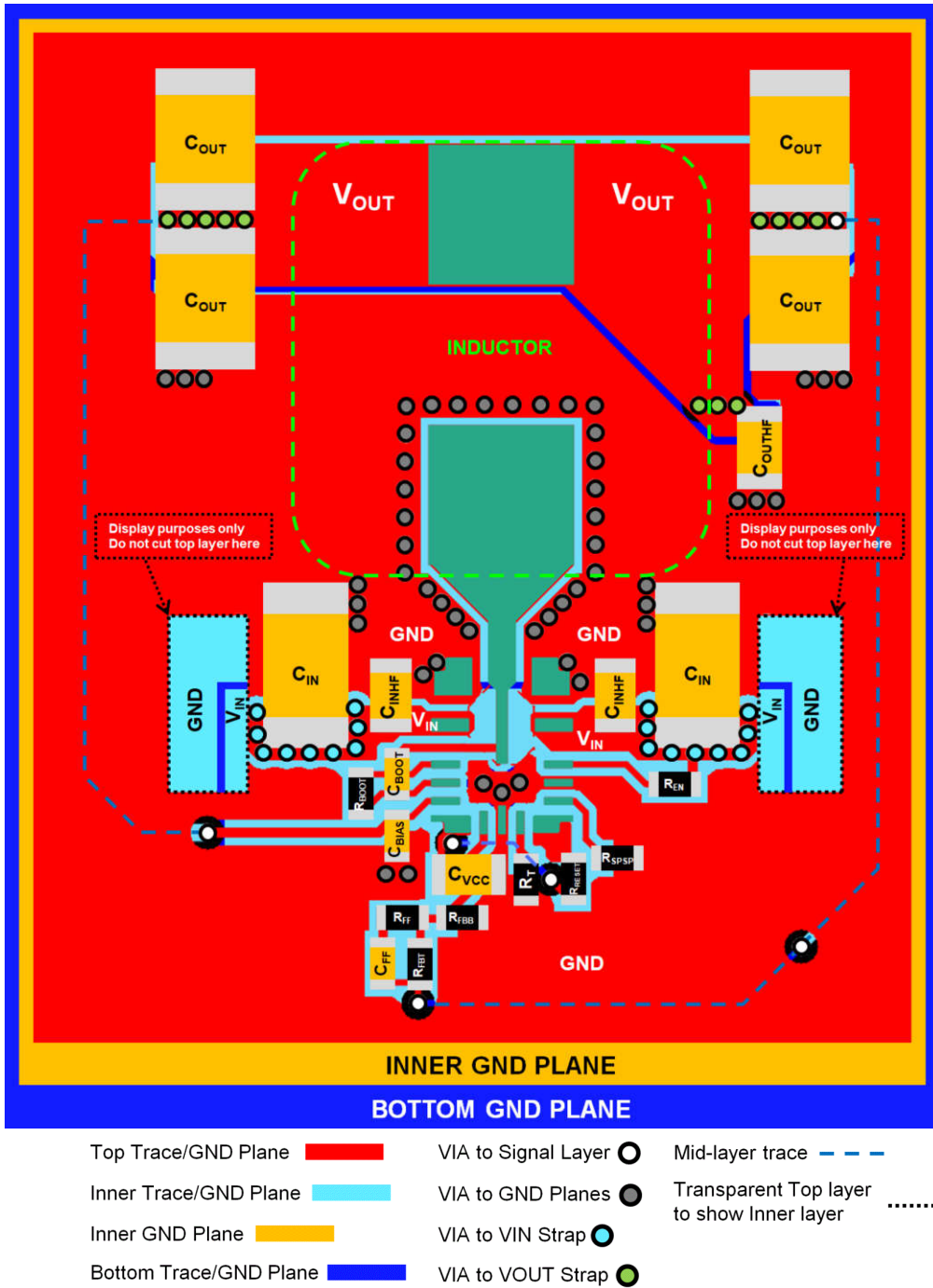


Figure 8-58. Layout Example

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9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Thermal Design by Insight not Hindsight application note](#)
- Texas Instruments, [A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages application note](#)
- Texas Instruments, [Semiconductor and IC Package Thermal Metrics application note](#)
- Texas Instruments, [Thermal Design Made Simple with LM43603 and LM43602 application note](#)
- Texas Instruments, [PowerPAD™ Thermally Enhanced Package application note](#)
- Texas Instruments, [PowerPAD™ Made Easy application brief](#)
- Texas Instruments, [Using New Thermal Metrics application note](#)

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Trademarks

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9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

9.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10 Revision History

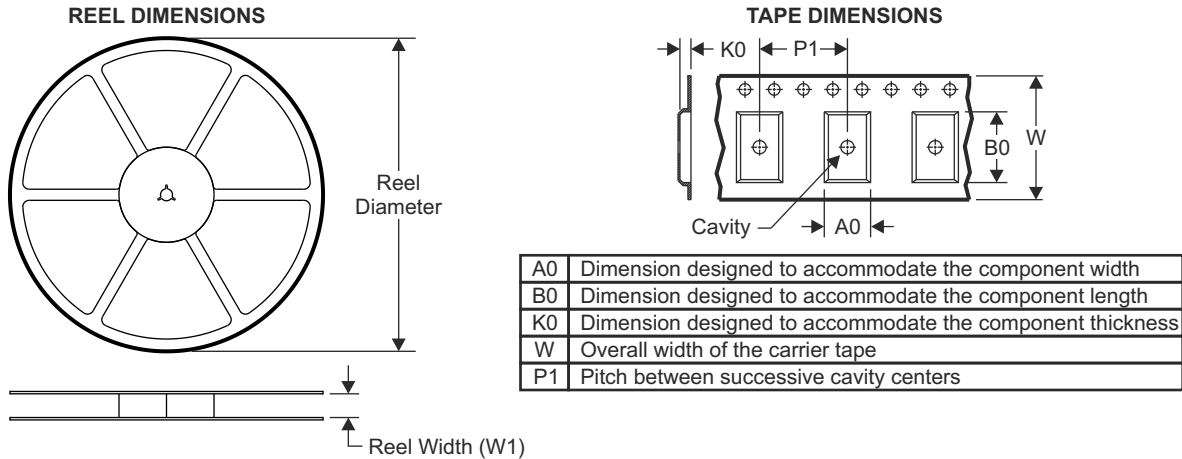
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
October 2024	*	Initial Release

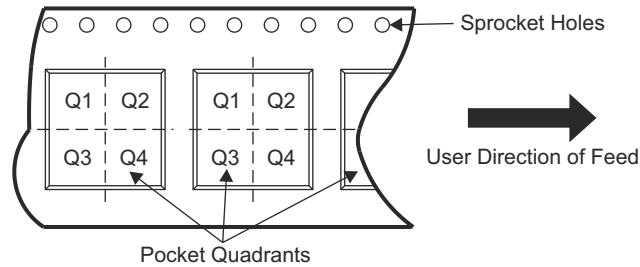
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

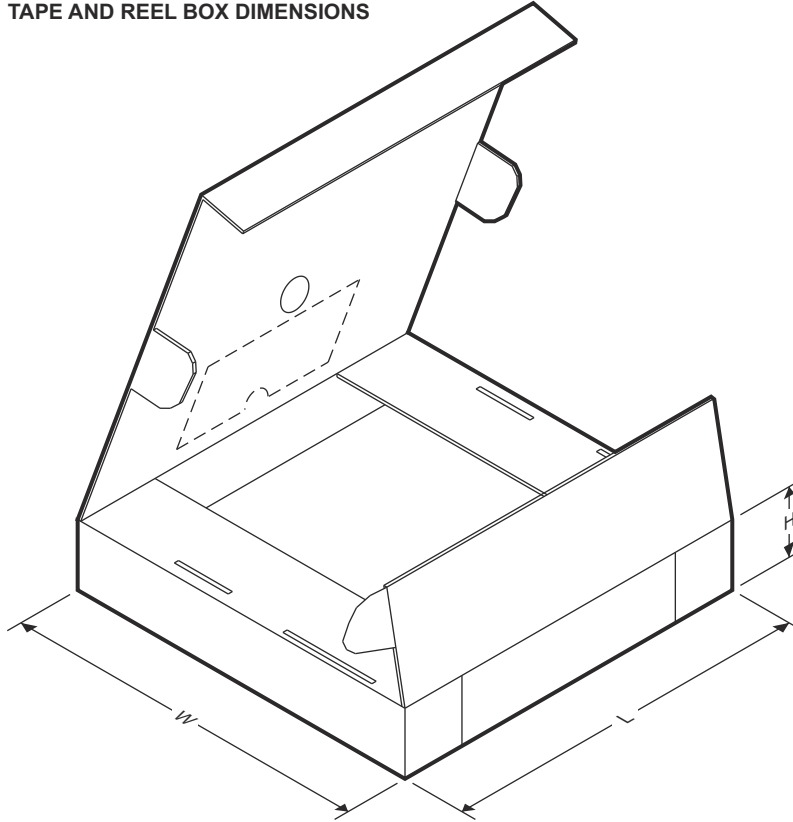


QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM61480TQVAMRQ1	VQFN-HR	VAM	16	3000	330	12.4	3.8	4.8	1.18	8.0	12.0	Q1
LM61495TQVAMRQ1	VQFN-HR	VAM	16	3000	330	12.4	3.8	4.8	1.18	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



ADVANCE INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM61480TQVAMRQ1	VQFN-HR	VAM	16	3000	367.0	367.0	38.0
LM61495TQVAMRQ1	VQFN-HR	VAM	16	3000	367.0	367.0	38.0

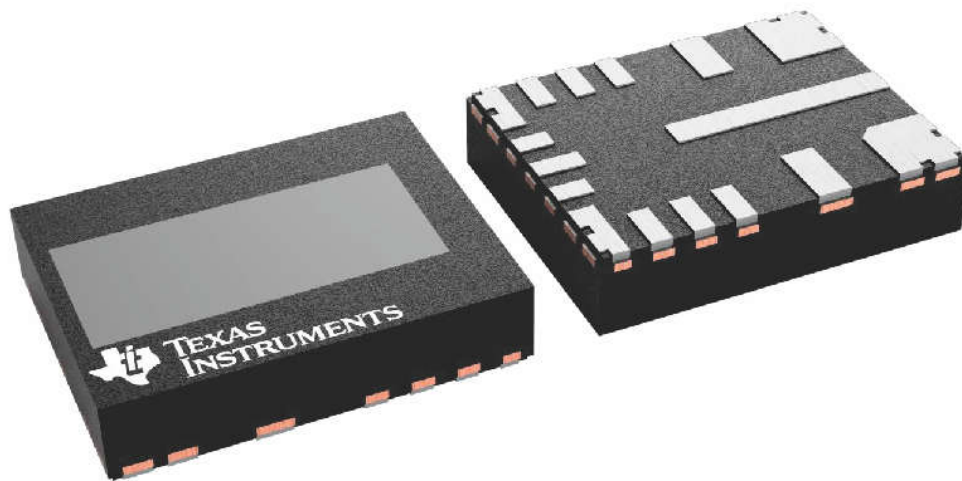
VAM 16

3.5 x 4.5 mm, 0.5mm pitch

GENERIC PACKAGE VIEW

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



ADVANCE INFORMATION

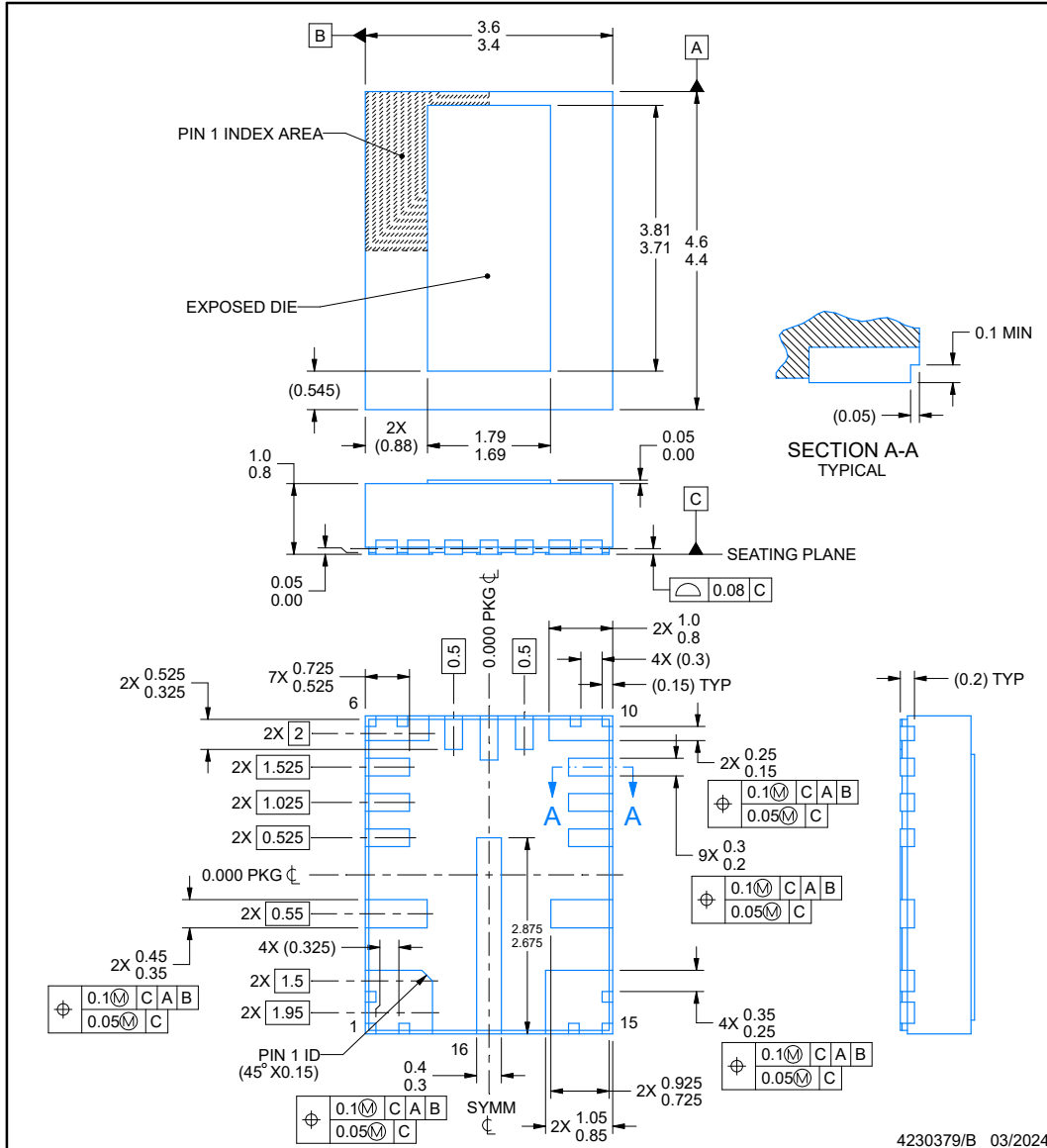
This page is an engineering mock-up. Images above are just a representation of the package family, actual package may vary. Refer to the product datasheet for package details.

VAM0016A



PACKAGE OUTLINE
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

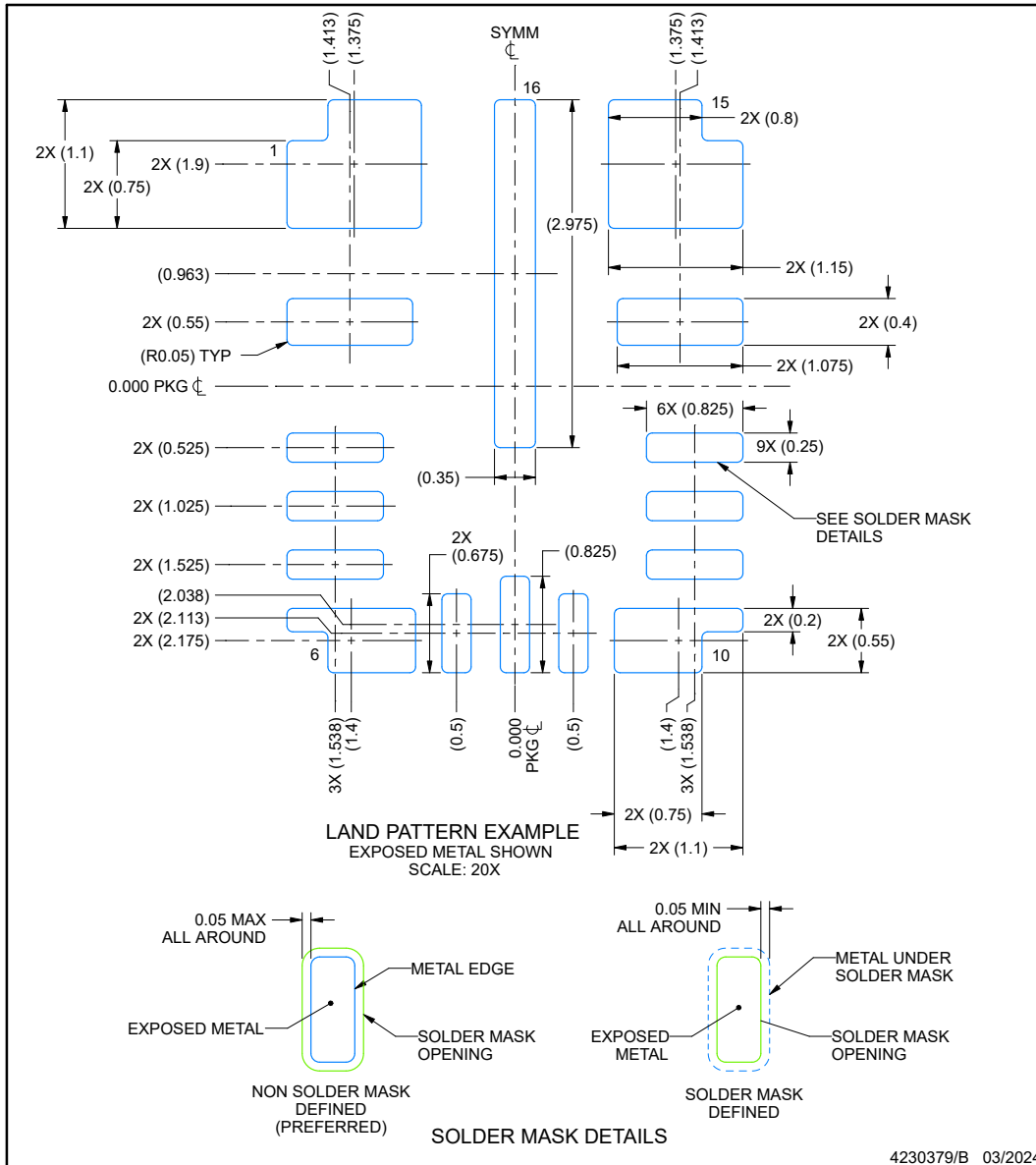
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

VAM0016A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sl原因271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

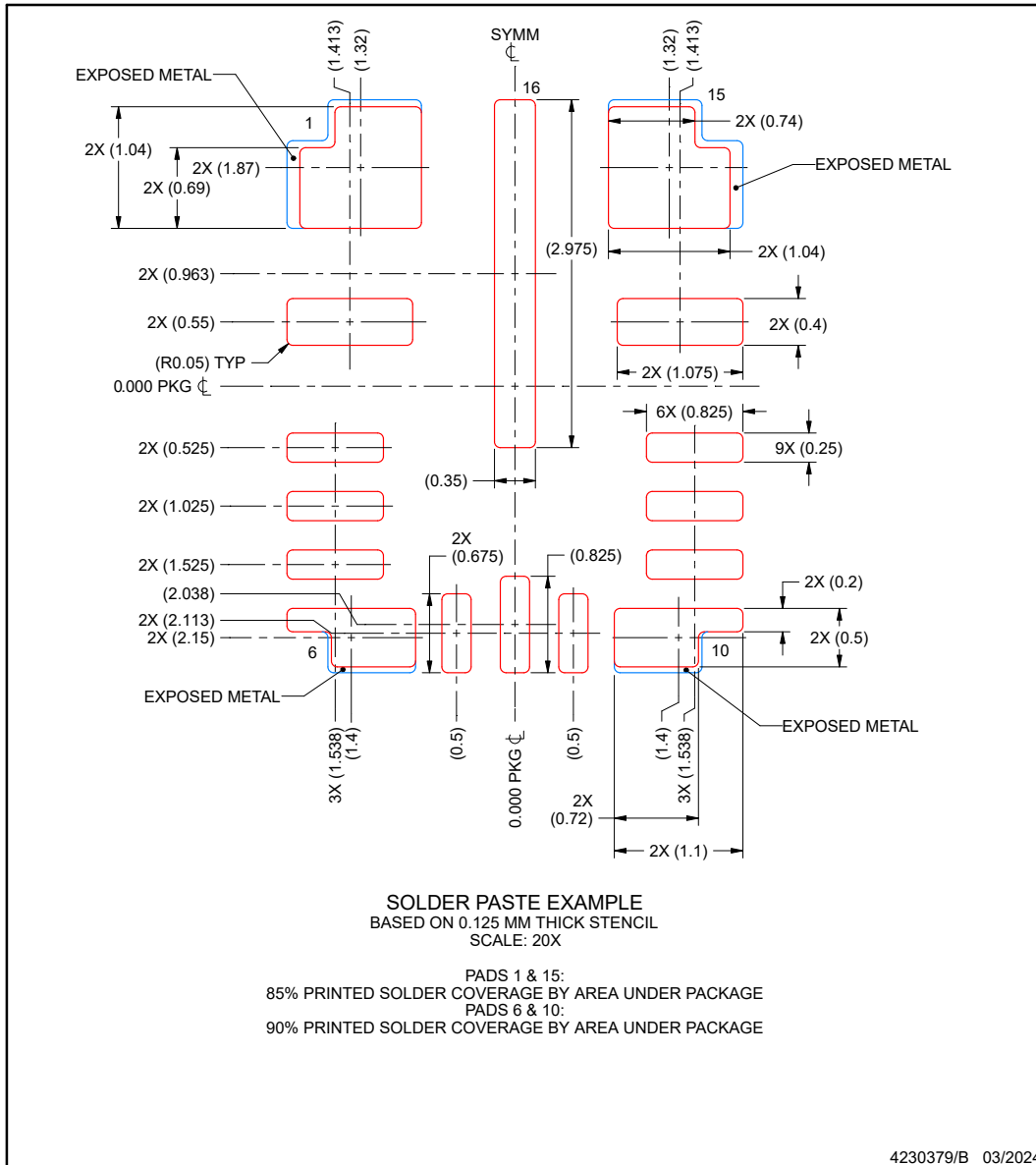
EXAMPLE STENCIL DESIGN

VAM0016A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

ADVANCE INFORMATION



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLM61495TQVAMRQ1	ACTIVE	VQFN-HR	VAM	16	3000	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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