# LMC7101 Tiny, Low-Power Operational Amplifier With Rail-to-Rail Input and Output

## 1 Features

- Tiny 5-Pin SOT-23 package saves space; typical circuit layouts take half the space of 8-pin SOIC designs
- Specified for 2.7V, 3V, 5V, and 15V supplies
- Typical supply current 0.5mA at 5V
- Typical total harmonic distortion of 0.01% at 5V
- 1MHz gain bandwidth
- Specified to industrial temperature: –40°C to +85°C
- Similar to popular LMC6482 and LMC6484
- Rail-to-rail input and output

## 2 Applications

- Mobile communications
- Notebooks and PDAs
- Battery-powered products
- Sensor interface
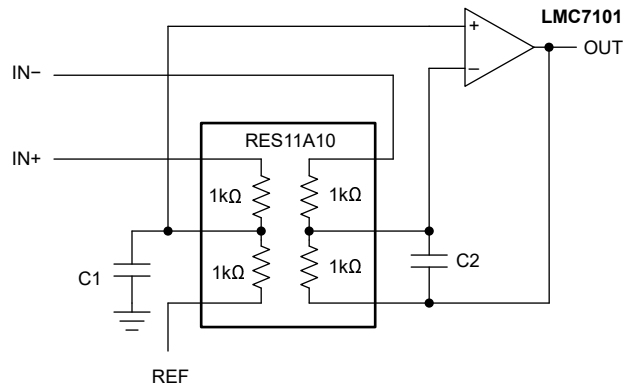- Automotive applications

## 3 Description

The LMC7101 device is a high-performance, automotive, CMOS operational amplifier available in a space-saving, 5-pin, SOT-23 tiny package. This design makes the LMC7101 an excellent choice for space- and weight-critical designs. The performance is similar to the single amplifier of the LMC6482 and LMC6484, with rail-to-rail input and output, high open-loop gain, low distortion, and low-supply currents.

The main benefits of the tiny package are most apparent in small, portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The tiny amplifiers can be placed on a board where needed, thus simplifying board layout.

### Package Information

| PART NUMBER | PACKAGE[1] | PACKAGE SIZE[2] |
|---|---|---|
| LMC7101 | DBV (SOT-23, 5) | 2.9mm × 2.8mm |

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



**Difference Amplifier Application With RES11A**

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# 4 Pin Configuration and Functions
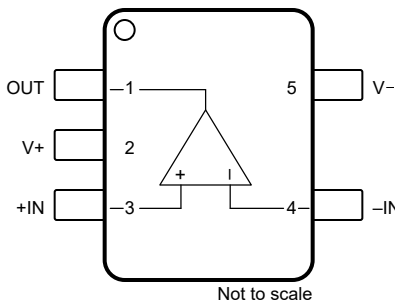


Figure 4-1. DBV Package, 5-Pin SOT-23 (Top View)

**Table 4-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | OUT | Output | Output |
| 2 | V+ | Power | Positive supply |
| 3 | +IN | Input | Noninverting input |
| 4 | −IN | Input | Inverting input |
| 5 | V− | Power | Negative supply |

Product Folder Links: *LMC7101*

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1] [2]

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
|  | Difference Input voltage |  | ±Supply voltage | V |
|  | Voltage at input and output pins | (V−) − 0.3 | (V+) + 0.3 | V |
| $V_S$ | Supply voltage, $V_S$ = (V+) − (V−) |  | 16 | V |
|  | Current at input pin | −5 | 5 | mA |
|  | Current at output pin[3] | −35 | 35 | mA |
|  | Current at power supply pin |  | 35 | mA |
|  | Lead temperature (soldering, 10s) |  | 260 | °C |
| $T_J$ | Junction temperature[4] |  | 150 | °C |
| $T_{stg}$ | Storage temperature | −65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) If Military/Aerospace specified devices are required, contact the TI Sales Office or Distributors for availability and specifications.
(3) Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C
(4) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$ and $T_A$. The maximum allowable power dissipation at any ambient temperature is $P_D$ = ($T_{J(MAX)}$ − $T_A$) / $R_{\theta JA}$. All numbers apply for packages soldered directly into a PC board.

## 5.2 ESD Ratings

|  |  |  | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±1000 | V |
|  |  | Charged-device model (CDM), per JEDEC specification JESD22-C101[2] | ±1000 |  |

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|  |  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_S$ | Supply voltage, $V_S$ = (V+) − (V−) | 2.7 |  | 15.5 | V |
| $T_J$ | Junction temperature | −40 |  | 85 | °C |

## 5.4 Thermal Information

|  | THERMAL METRIC[1] | LMC7101 DBV (SOT) 5 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 193.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case(top) thermal resistance | 128.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 88.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 66.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 88.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case(bottom) thermal resistance | N/A | °C/W |

(1) For information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 5.5 Electrical Characteristics for V$_S$ = ±1.35V or 2.7V

at T$_J$ = 25°C, V+ = 2.7V, V– = 0V, V$_{CM}$ = V$_{OUT}$ = V+ / 2, and R$_L$ > 1MΩ connected to V+ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| V$_{OS}$ | Input offset voltage | LMC7101A | | | ±0.11 | ±6 | mV |
| | | LMC7101B | | | ±0.11 | ±9 | |
| dV$_{OS}$/dT | Input offset voltage drift | T$_J$ = –40°C to +85°C | | | 1 | | μV/°C |
| PSRR | Power-supply rejection ratio | V+ = 1.35V to 1.65V, V– = –1.35V to –1.65V, V$_{CM}$ = 0V | | 45 | 60 | | dB |
| **INPUT BIAS CURRENT** | | | | | | | |
| I$_B$ | Input bias current | T$_J$ = –40°C to +85°C | | | ±1 | ±64 | pA |
| I$_{OS}$ | Input offset current | T$_J$ = –40°C to +85°C | | | ±0.5 | ±32 | pA |
| **INPUT VOLTAGE** | | | | | | | |
| V$_{CM}$ | Input common-mode voltage | For CMRR ≥ 47dB | Positive | 2.7 | 3 | | V |
| | | | Negative | | 0 | 0 | |
| CMRR | Common-mode rejection | 0V ≤ V$_{CM}$ ≤ 2.7V | | 47 | 70 | | dB |
| **INPUT IMPEDANCE** | | | | | | | |
| R$_{IN}$ | Input resistance | | | | > 1 | | TΩ |
| C$_{IN}$ | Common-mode input capacitance | | | | 3 | | pF |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain bandwidth product | | | | 0.6 | | MHz |
| SR | Slew rate[1] | (V+) = 15V, 10V step, R$_L$ = 100kΩ to 7.5V, V$_{OUT}$ = 10V$_{PP}$, f = 1kHz | | | 0.7 | | V/μs |
| **OUTPUT** | | | | | | | |
| V$_O$ | Voltage output swing | Positive rail | R$_L$ = 2kΩ | 2.15 | 2.45 | | V |
| | | | R$_L$ = 10kΩ | 2.64 | 2.68 | | |
| | | Negative rail | R$_L$ = 2kΩ | | 0.25 | 0.5 | |
| | | | R$_L$ = 10kΩ | | 0.025 | 0.06 | |
| **POWER SUPPLY** | | | | | | | |
| I$_Q$ | Quiescent current per amplifier | | | | 500 | 810 | μA |
| | | T$_J$ = –40°C to +85°C | | | 500 | 950 | |

(1)     Number specified is the slower of the positive and negative slew rates.

## 5.6 Electrical Characteristics for $V_S$ = ±1.5V or 3V

at $T_J$ = 25°C, V+ = 3V, V− = 0V, $V_{CM}$ = $V_{OUT}$ = V+ / 2, and $R_L$ = 1MΩ connected to V+ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | LMC7101A | | | ±0.11 | ±3 | mV |
| | | LMC7101B | | | ±0.11 | ±7 | |
| $dV_{OS}/dT$ | Input offset voltage drift | $T_J$ = −40°C to +85°C | | | 1 | | µV/°C |
| PSRR | Power-supply rejection ratio | V+ = 1.5V to 7.5V V− = −1.5V to −7.5V $V_{OUT}$ = $V_{CM}$ = 0V | LMC7101A | 68 | 80 | | dB |
| | | | LMC7101B | 60 | 80 | | |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | $T_J$ = −40°C to +85°C | | | ±1 | ±64 | pA |
| $I_{OS}$ | Input offset current | $T_J$ = −40°C to +85°C | | | ±0.5 | ±32 | pA |
| **INPUT VOLTAGE** | | | | | | | |
| $V_{CM}$ | Input common-mode voltage | For CMRR ≥ 47dB | Positive | 3 | 3.3 | | V |
| | | | Negative | | 0 | 0 | |
| CMRR | Common-mode rejection | 0V ≤ $V_{CM}$ ≤ 3V | | 47 | 70 | | dB |
| **INPUT IMPEDANCE** | | | | | | | |
| $R_{IN}$ | Input resistance | | | | > 1 | | TΩ |
| $C_{IN}$ | Common-mode input capacitance | | | | 3 | | pF |
| **OUTPUT** | | | | | | | |
| $V_O$ | Voltage output swing | Positive rail | $R_L$ = 2kΩ | 2.6 | 2.8 | | V |
| | | | $R_L$ = 600Ω | 2.5 | 2.7 | | |
| | | Negative rail | $R_L$ = 2kΩ | | 0.2 | 0.4 | |
| | | | $R_L$ = 600Ω | | 0.37 | 0.6 | |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current per amplifier | | | | 500 | 810 | µA |
| | | $T_J$ = −40°C to +85°C | | | 500 | 950 | |

## 5.7 Electrical Characteristics for $V_S$ = ±2.5V or 5V

at $T_J$ = 25°C, V+ = 5V, V− = 0V, $V_{CM}$ = $V_{OUT}$ = V+ / 2, and $R_L$ = 1MΩ connected to V+ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | LMC7101A | | | ±0.11 | ±3 | mV |
| | | | $T_J$ = −40°C to +85°C | | ±0.11 | ±5 | |
| | | LMC7101B | | | ±0.11 | ±7 | |
| | | | $T_J$ = −40°C to +85°C | | ±0.11 | ±9 | |
| $dV_{OS}/dT$ | Input offset voltage drift | $T_J$ = −40°C to +85°C | | | 1 | | µV/°C |
| PSRR | Power-supply rejection ratio | Positive<br>V+ = 5V to 15V<br>V− = 0V, $V_{OUT}$ = 1.5V | LMC7101A | 70 | 82 | | dB |
| | | | LMC7101B | 65 | 82 | | |
| | | | LMC7101A<br>$T_J$ = −40°C to +85°C | 65 | 82 | | |
| | | | LMC7101B<br>$T_J$ = −40°C to +85°C | 62 | 82 | | |
| | | Negative<br>V+ = −5V to −15V<br>V− = 0V, $V_{OUT}$ = −1.5V | LMC7101A | 70 | 82 | | |
| | | | LMC7101B | 65 | 82 | | |
| | | | LMC7101A<br>$T_J$ = −40°C to +85°C | 65 | 82 | | |
| | | | LMC7101B<br>$T_J$ = −40°C to +85°C | 62 | 82 | | |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | | | | ±1 | | pA |
| | | $T_J$ = −40°C to +85°C | | | | ±64 | |
| $I_{OS}$ | Input offset current | | | | ±0.5 | | pA |
| | | $T_J$ = −40°C to +85°C | | | | ±32 | |
| **NOISE** | | | | | | | |
| THD | Total harmonic distortion | f = 10kHz, G = − 2V/V, $R_L$ = 10kΩ, $V_{OUT}$ = 4$V_{pp}$ | | | 0.01 | | % |
| **INPUT VOLTAGE** | | | | | | | |
| $V_{CM}$ | Input common-mode voltage | To positive rail<br>CMRR > 50dB | | 5.2 | 5.3 | | V |
| | | | $T_J$ = −40°C to +85°C | 5 | 5.3 | | |
| | | To negative rail<br>CMRR > 50dB | | | −0.3 | −0.2 | |
| | | | $T_J$ = −40°C to +85°C | | −0.3 | 0 | |
| CMRR | Common-mode rejection ratio | 0V ≤ $V_{CM}$ ≤ 5V | | 52 | 75 | | dB |
| | | | $T_J$ = −40°C to +85°C | 51 | 74 | | |
| **INPUT IMPEDANCE** | | | | | | | |
| $R_{IN}$ | Input resistance | | | | > 1 | | TΩ |
| $C_{IN}$ | Input capacitance | | | | 3 | | pF |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain bandwidth product | | | | 1 | | MHz |
| SR | Slew rate | | | | 1 | | V/µs |

## 5.7 Electrical Characteristics for V$_S$ = ±2.5V or 5V (continued)

at T$_J$ = 25°C, V+ = 5V, V– = 0V, V$_{CM}$ = V$_{OUT}$ = V+ / 2, and R$_L$ = 1MΩ connected to V+ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | | |
| V$_O$ | Voltage output swing | Positive rail R$_L$ = 2kΩ | | 4.7 | 4.9 | | V |
| | | | T$_J$ = –40°C to +85°C | 4.6 | 4.9 | | |
| | | Negative rail R$_L$ = 2kΩ | | | 0.1 | 0.18 | |
| | | | T$_J$ = –40°C to +85°C | | 0.1 | 0.24 | |
| | | Positive rail R$_L$ = 600Ω | | 4.5 | 4.7 | | |
| | | | T$_J$ = –40°C to +85°C | 4.24 | 4.7 | | |
| | | Negative rail R$_L$ = 600Ω | | | 0.3 | 0.5 | |
| | | | T$_J$ = –40°C to +85°C | | 0.3 | 0.65 | |
| I$_{SC}$ | Short-circuit current | Sourcing V$_{OUT}$ = 0V | | 16 | 24 | | mA |
| | | | T$_J$ = –40°C to +85°C | 11 | 24 | | |
| | | Sinking V$_{OUT}$ = 5V | | 11 | 19 | | |
| | | | T$_J$ = –40°C to +85°C | 7.5 | 19 | | |
| **POWER SUPPLY** | | | | | | | |
| I$_Q$ | Quiescent current per amplifier | | | | 0.5 | 0.85 | mA |
| | | | T$_J$ = –40°C to +85°C | | 0.5 | 1 | |

## 5.8 Electrical Characteristics for $V_S$ = ±7.5V or 15V

at $T_J$ = 25°C, V+ = 15V, V– = 0V, $V_{CM}$ = $V_{OUT}$ = V+ / 2, and $R_L$ = 1MΩ connected to V+ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | | | | ±0.26 | | mV |
| $dV_{OS}/dT$ | Input offset voltage drift | $T_J$ = –40°C to +85°C | | | 1 | | µV/°C |
| PSRR | Power-supply rejection ratio | Positive V+ = 5V to 15V V– = 0V, $V_{OUT}$ = 1.5V | LMC7101A | 70 | 82 | | dB |
| | | | LMC7101B | 65 | 82 | | |
| | | | LMC7101A $T_J$ = –40°C to +85°C | 65 | 82 | | |
| | | | LMC7101B $T_J$ = –40°C to +85°C | 60 | 82 | | |
| | | Negative V+ = –5V to –15V V– = 0V, $V_{OUT}$ = –1.5V | LMC7101A | 70 | 82 | | |
| | | | LMC7101B | 65 | 82 | | |
| | | | LMC7101A $T_J$ = –40°C to +85°C | 65 | 82 | | |
| | | | LMC7101B $T_J$ = –40°C to +85°C | 62 | 82 | | |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | | | | ±1 | | pA |
| | | $T_J$ = –40°C to +85°C | | | | ±64 | |
| $I_{OS}$ | Input offset current | | | | ±0.5 | | pA |
| | | $T_J$ = –40°C to +85°C | | | | ±32 | |
| **NOISE** | | | | | | | |
| $e_n$ | Input voltage noise density | f = 1kHz, $V_{CM}$ = 1V | | | 37 | | nV/√Hz |
| $i_n$ | Input current noise density | f = 1kHz | | | 6.8 | | fA/√Hz |
| THD | Total harmonic distortion | f = 10kHz, G = – 2V/V, $R_L$ = 10kΩ, $V_{OUT}$ = 8.5$V_{pp}$ | | | 0.01 | | % |
| **INPUT VOLTAGE** | | | | | | | |
| $V_{CM}$ | Input common-mode voltage | To positive rail CMRR > 50dB | | 15.2 | 15.3 | | V |
| | | | $T_J$ = –40°C to +85°C | 15 | 15.3 | | |
| | | To negative rail CMRR > 50dB | | | –0.3 | –0.2 | |
| | | | $T_J$ = –40°C to +85°C | | –0.3 | 0 | |
| CMRR | Common-mode rejection ratio | 0V ≤ $V_{CM}$ ≤15V | | 62 | 82 | | dB |
| | | | $T_J$ = –40°C to +85°C | 60 | 82 | | |
| **INPUT IMPEDANCE** | | | | | | | |
| $R_{IN}$ | Input resistance | | | | > 1 | | TΩ |
| $C_{IN}$ | Input capacitance | | | | 3 | | pF |
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | Sourcing 7.5V < $V_O$ < 12.5V, $V_{CM}$ = 1.5V $R_L$ = 2kΩ to 7.5V | | 80 | 340 | | V/mV |
| | | | $T_J$ = –40°C to +85°C | 40 | 340 | | |
| | | Sinking 2.5V < $V_O$ < 7.5V, $V_{CM}$ = 1.5V $R_L$ = 2kΩ to 7.5V | | 15 | 24 | | |
| | | | $T_J$ = –40°C to +85°C | 10 | 24 | | |
| | | Sourcing, $V_{CM}$ = 1.5V, 7.5V < $V_O$ < 12.5V, $R_L$ = 600Ω | | 34 | 300 | | |
| | | Sinking, $V_{CM}$ = 1.5V, 2.5V < $V_O$ < 7.5V, $R_L$ = 600Ω | | 6 | 15 | | |

Product Folder Links: *LMC7101*

## 5.8 Electrical Characteristics for $V_S$ = ±7.5V or 15V (continued)

at $T_J$ = 25°C, V+ = 15V, V– = 0V, $V_{CM}$ = $V_{OUT}$ = V+ / 2, and $R_L$ = 1MΩ connected to V+ / 2 (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain bandwidth product | | | | 1.1 | | MHz |
| SR | Slew rate[1] | $V_S$ = 15V, 10V step, $R_L$ = 100kΩ to 7.5V $V_{OUT}$ = 10V$_{PP}$, f = 1kHz | | 0.5 | 1.1 | | V/µs |
| | | | $T_J$ = –40°C to +85°C | 0.4 | 1.1 | | |
| $θ_m$ | Phase margin | | | | 45 | | ° |
| $G_m$ | Gain margin | | | | 10 | | dB |
| **OUTPUT** | | | | | | | |
| $V_O$ | Voltage output swing | Positive rail $R_L$ = 2kΩ | | 14.4 | 14.7 | | V |
| | | | $T_J$ = –40°C to +85°C | 14.2 | 14.7 | | |
| | | Negative rail $R_L$ = 2kΩ | | | 0.16 | 0.32 | |
| | | | $T_J$ = –40°C to +85°C | | 0.16 | 0.45 | |
| | | Positive rail $R_L$ = 600Ω | | 13.4 | 14.1 | | |
| | | | $T_J$ = –40°C to +85°C | 13 | 14.1 | | |
| | | Negative rail $R_L$ = 600Ω | | | 0.5 | 1 | |
| | | | $T_J$ = –40°C to +85°C | | 0.5 | 1.3 | |
| $I_{SC}$ | Short-circuit current[2] | Sourcing $V_{OUT}$ = 0V | | 30 | 50 | | mA |
| | | | $T_J$ = –40°C to +85°C | 20 | 50 | | |
| | | Sinking $V_{OUT}$ = 12V | | 30 | 50 | | |
| | | | $T_J$ = –40°C to +85°C | 20 | 50 | | |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current per amplifier | | | | 0.8 | 1.5 | mA |
| | | $T_J$ = –40°C to +85°C | | | 0.8 | 1.71 | |

(1) Number specified is the slower of the positive and negative slew rates.
(2) Do not short circuit output to V+ when V+ is greater than 12V or reliability can be adversely affected.

Product Folder Links: *LMC7101*

## 5.9 Typical Characteristics for V$_S$ = 2.7V

at V+ = 2.7V, V– = 0V, and T$_A$ = 25°C (unless otherwise specified)
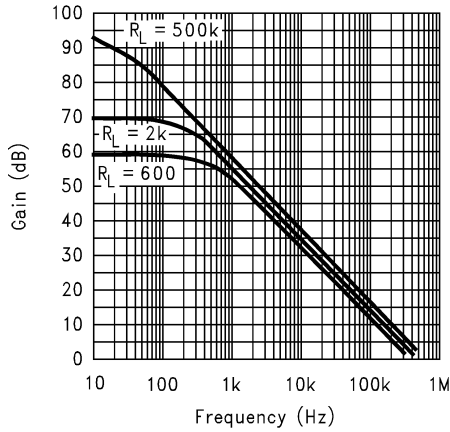


**Figure 5-1. Open-Loop Frequency Response**
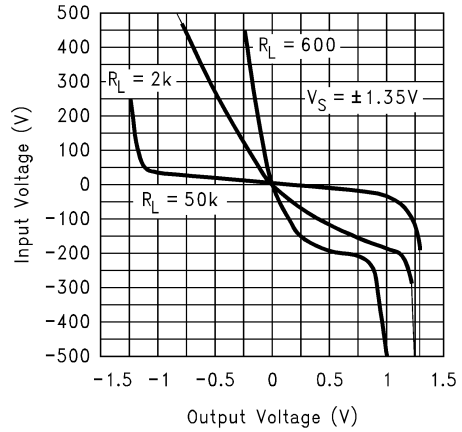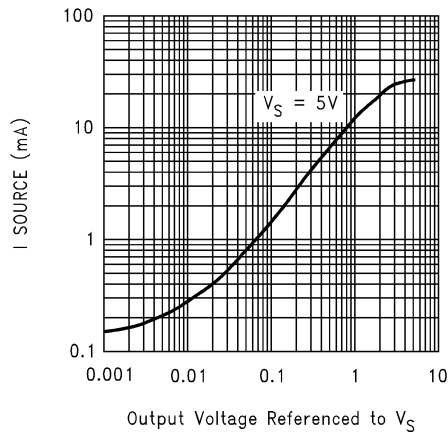


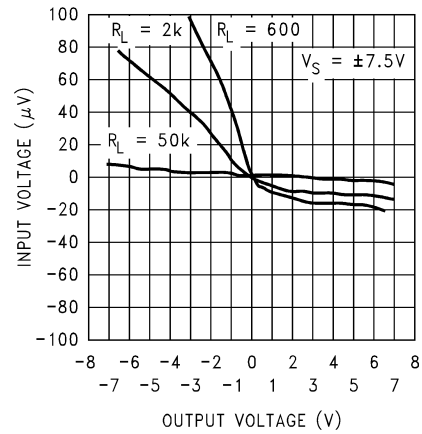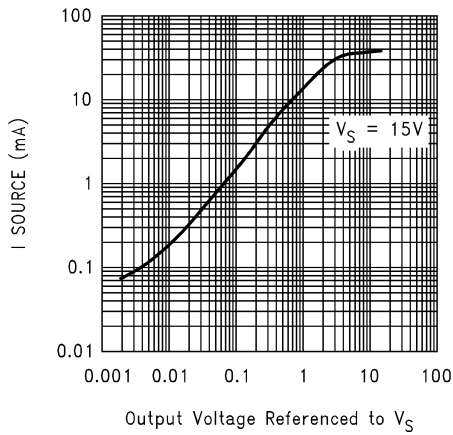**Figure 5-2. Input Voltage vs Output Voltage**
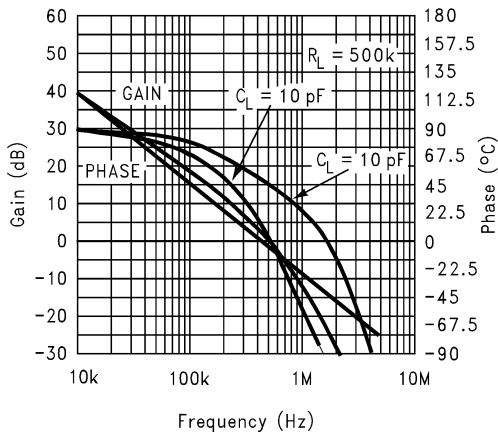


**Figure 5-3. Gain and Phase vs Capacitance Load**
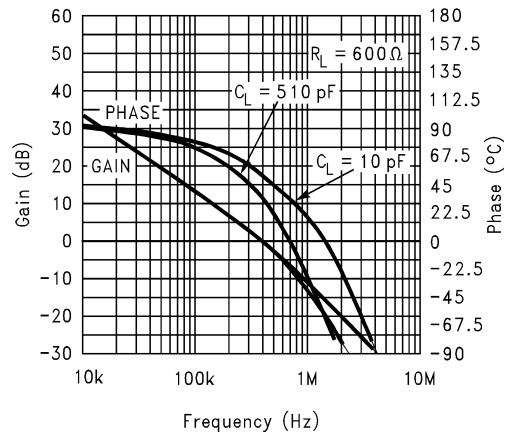


**Figure 5-4. Gain and Phase vs Capacitance Load**
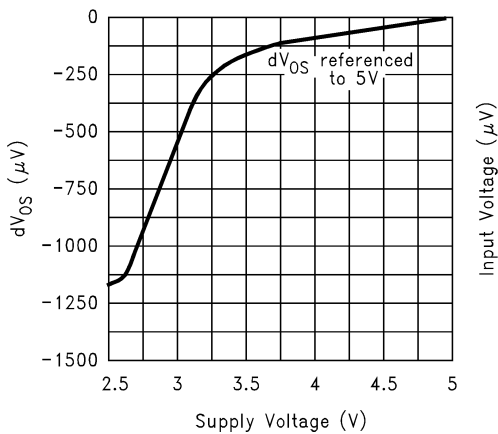


**Figure 5-5. dV$_{OS}$ vs Supply Voltage**



5 typical units
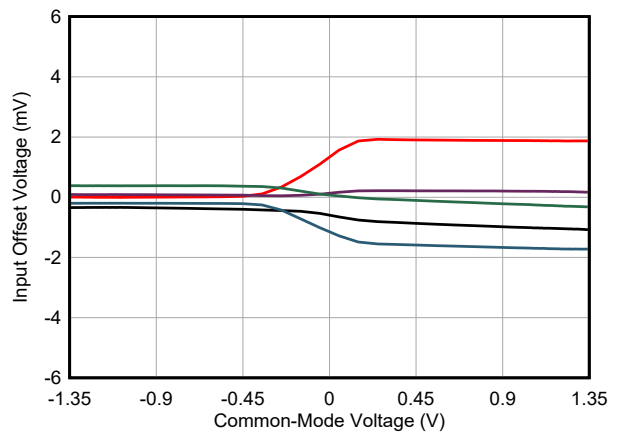
**Figure 5-6. Input Offset Voltage vs Common-Mode Voltage**

Product Folder Links: *LMC7101*

## 5.9 Typical Characteristics for V$_S$ = 2.7V (continued)

at V+ = 2.7V, V– = 0V, and T$_A$ = 25°C (unless otherwise specified)
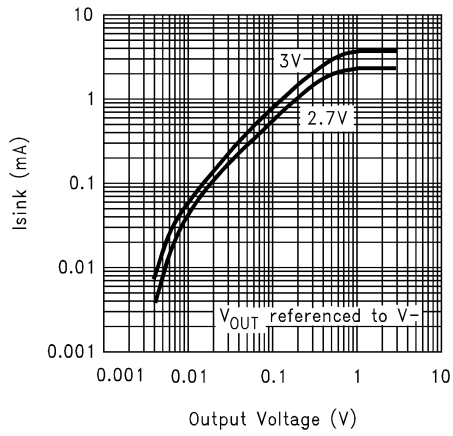


**Figure 5-7. Sinking Current vs Output Voltage**
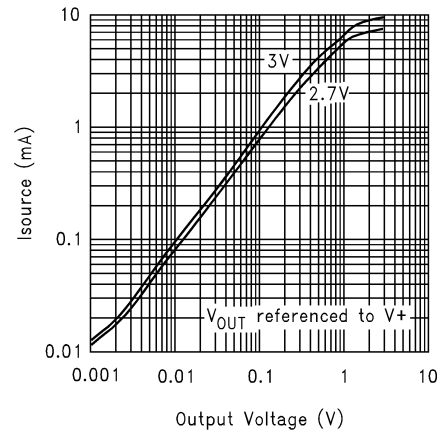


**Figure 5-8. Sourcing Current vs Output Voltage**

Product Folder Links: *LMC7101*

## 5.10 Typical Characteristics for $V_S$ = 3V

at V+ = 3V, V– = 0V, and $T_A$ = 25°C (unless otherwise specified)
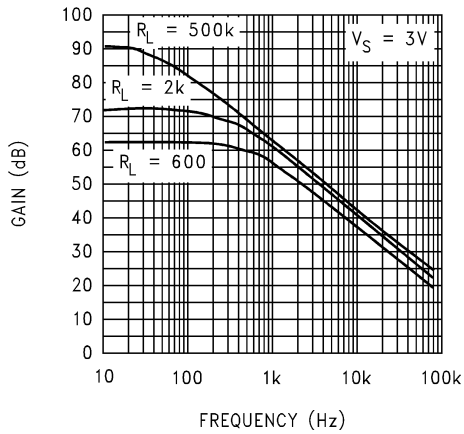
**Figure 5-9. Open-Loop Frequency Response**
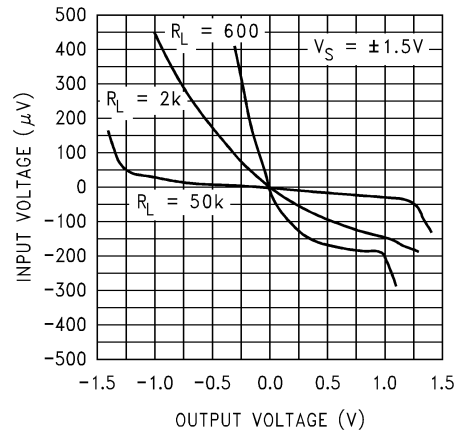
**Figure 5-10. Input Voltage vs Output Voltage**
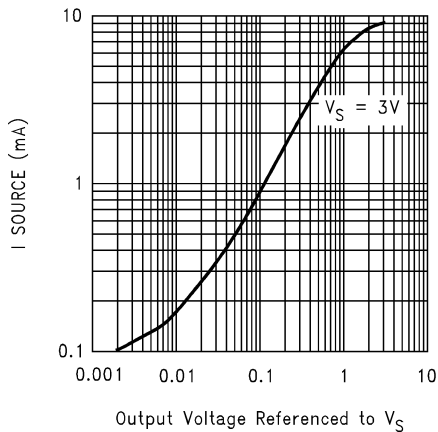
**Figure 5-11. Sourcing Current vs Output Voltage**
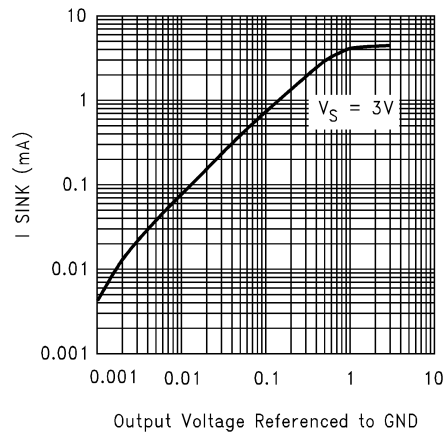
**Figure 5-12. Sinking Current vs Output Voltage**

Product Folder Links: *LMC7101*

## 5.11 Typical Characteristics for $V_S$ = 5V

at V+ = 5V, V– = 0V, and $T_A$ = 25°C (unless otherwise specified)
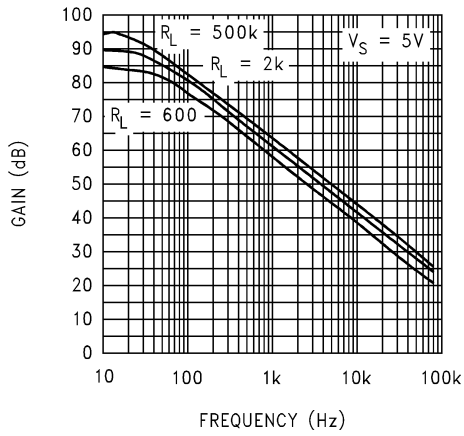
**Figure 5-13. Open-Loop Frequency Response**
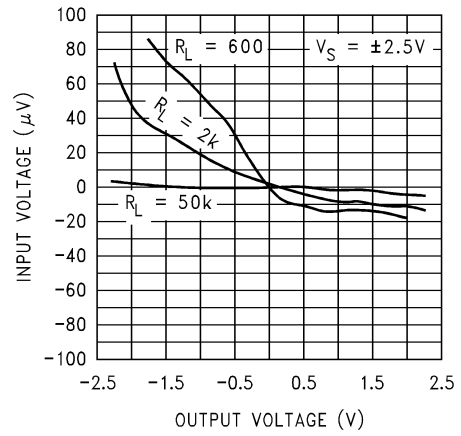
**Figure 5-14. Input Voltage vs Output Voltage**

**Figure 5-15. Sourcing Current vs Output Voltage**
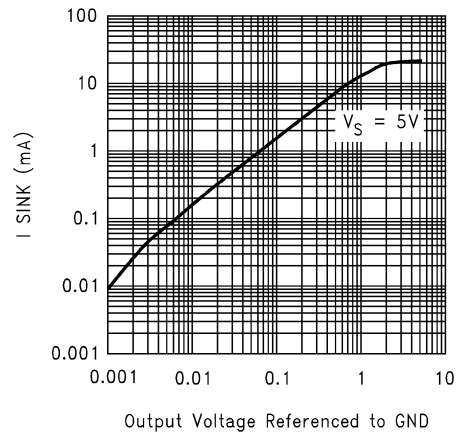
**Figure 5-16. Sinking Current vs Output Voltage**

Product Folder Links: *LMC7101*

## 5.12 Typical Characteristics for V$_S$ = 15V

at V+ = 15V, V– = 0V, and T$_A$ = 25°C (unless otherwise specified)
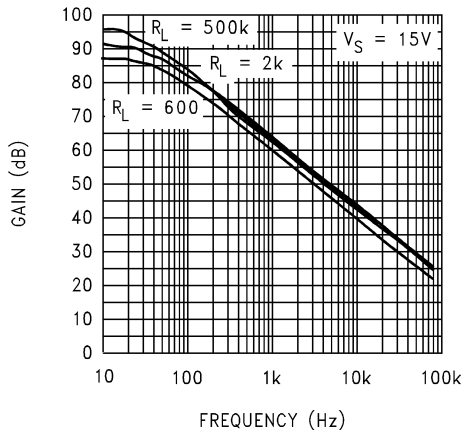
Figure 5-17. Open-Loop Frequency Response

Figure 5-18. Input Voltage vs Output Voltage

Figure 5-19. Sourcing Current vs Output Voltage
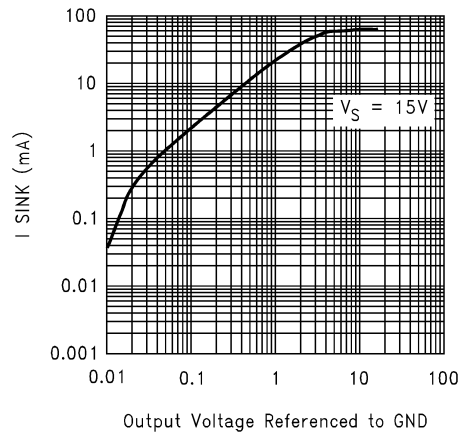
Figure 5-20. Sinking Current vs Output Voltage
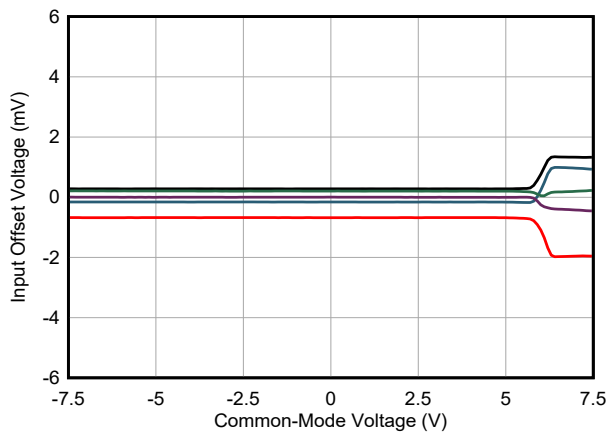
Figure 5-21. Input Offset Voltage vs Common-Mode Voltage
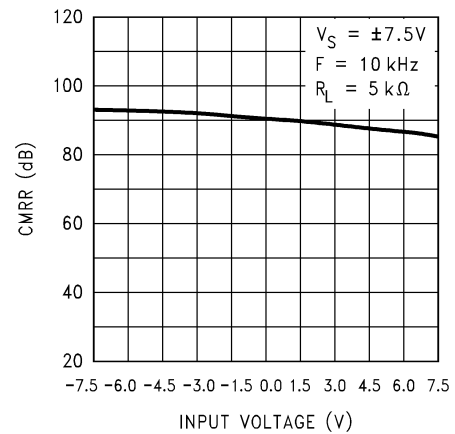
Figure 5-22. CMRR vs Input Voltage

Product Folder Links: *LMC7101*

## 5.12 Typical Characteristics for V$_S$ = 15V (continued)

at V+ = 15V, V– = 0V, and T$_A$ = 25°C (unless otherwise specified)
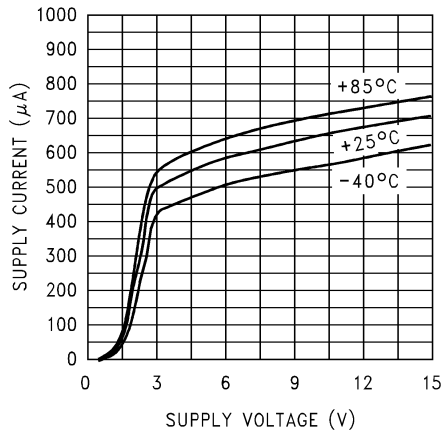
**Figure 5-23. Supply Current vs Supply Voltage**
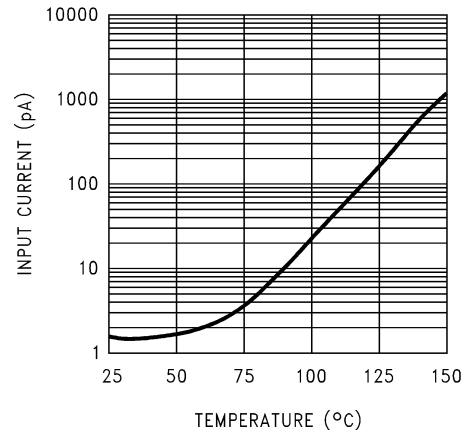
**Figure 5-24. Input Current vs Temperature**
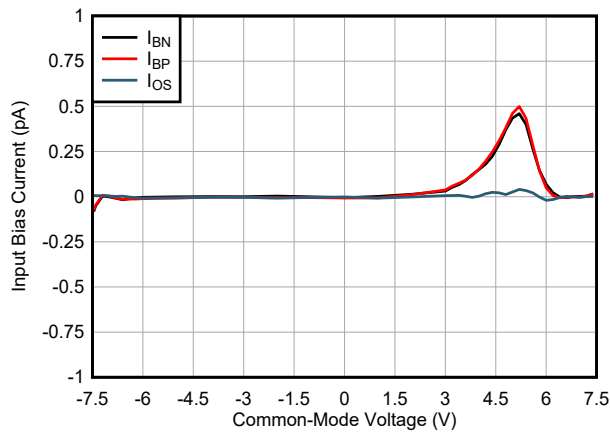
**Figure 5-25. Input Bias Current vs Common-Mode Voltage**
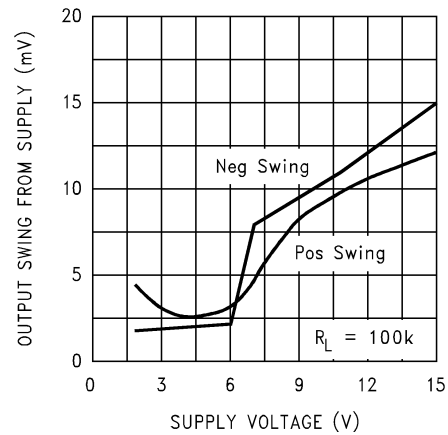
**Figure 5-26. Output Voltage Swing vs Supply Voltage**
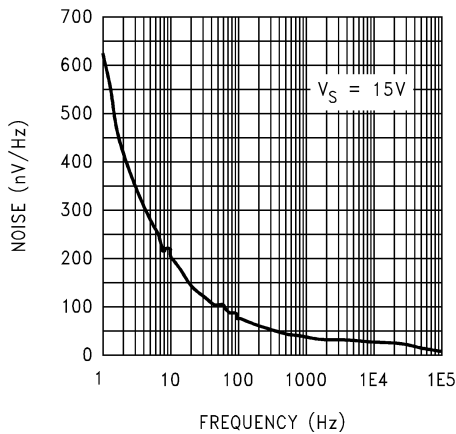
**Figure 5-27. Input Voltage Noise vs Frequency**
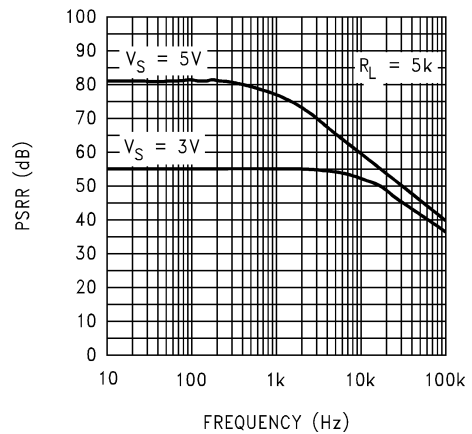
**Figure 5-28. Positive PSRR vs Frequency**

## 5.12 Typical Characteristics for V$_S$ = 15V (continued)

at V+ = 15V, V– = 0V, and T$_A$ = 25°C (unless otherwise specified)
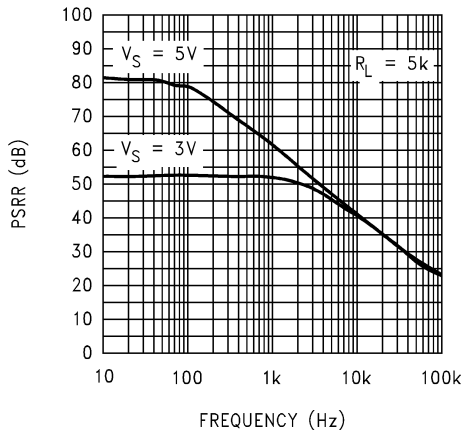


**Figure 5-29. Negative PSRR vs Frequency**
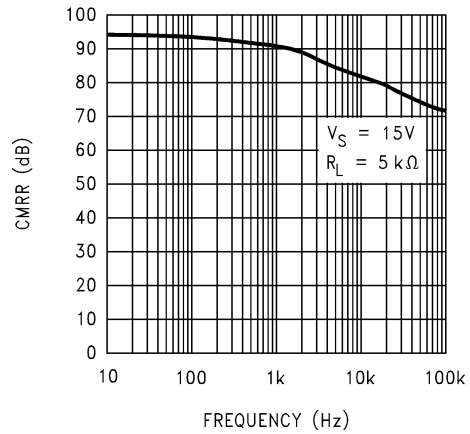


**Figure 5-30. CMRR vs Frequency**
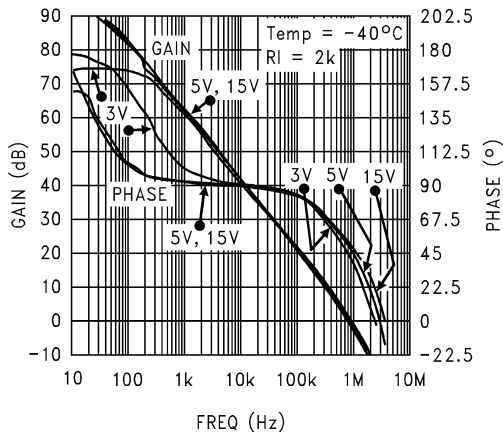


**Figure 5-31. Open-Loop Frequency Response at –40°C**
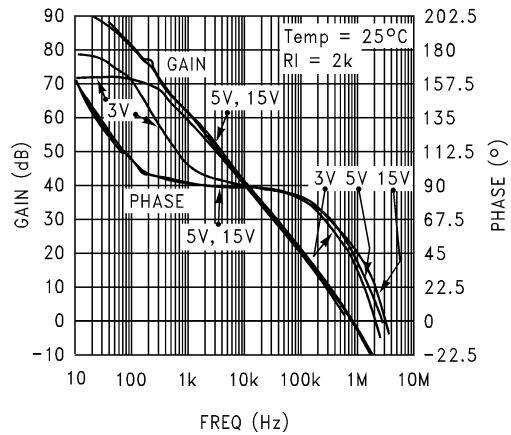


**Figure 5-32. Open-Loop Frequency Response at 25°C**
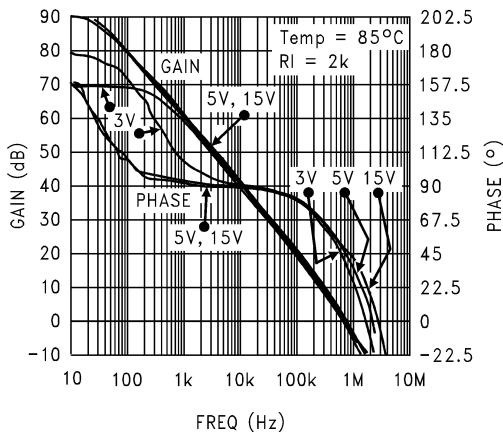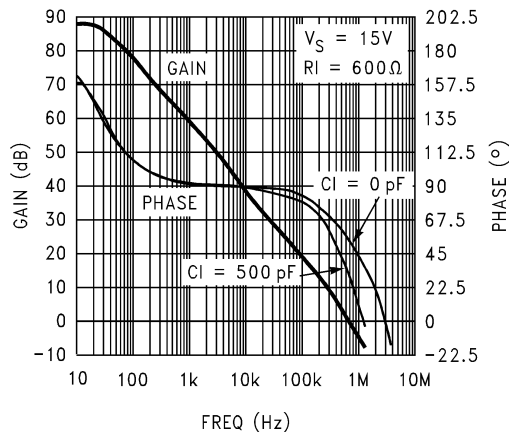


**Figure 5-33. Open-Loop Frequency Response at 85°C**



**Figure 5-34. Gain and Phase vs Capacitive Load**

Product Folder Links: *LMC7101*

## 5.12 Typical Characteristics for $V_S$ = 15V (continued)

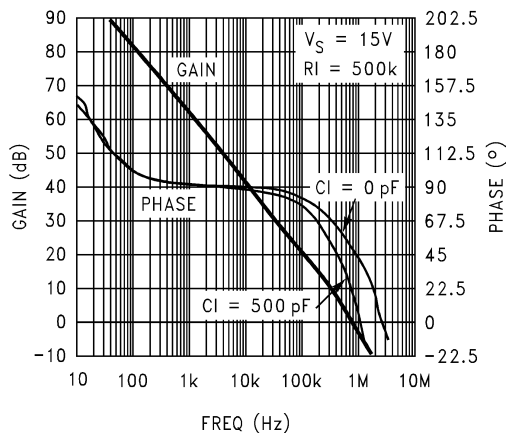at V+ = 15V, V– = 0V, and $T_A$ = 25°C (unless otherwise specified)

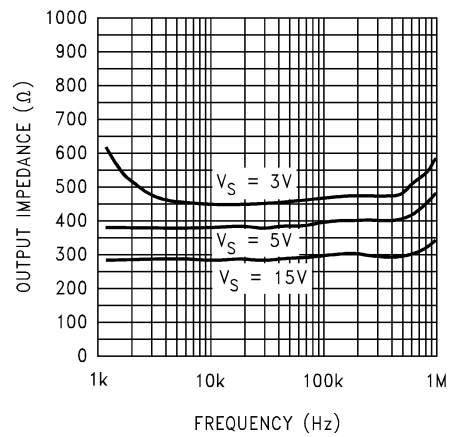**Figure 5-35. Gain and Phase vs Capacitive Load**
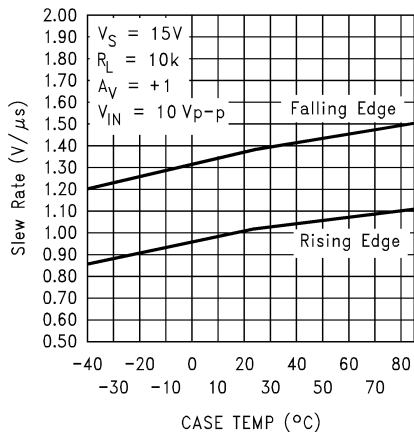
**Figure 5-36. Output Impedance vs Frequency**

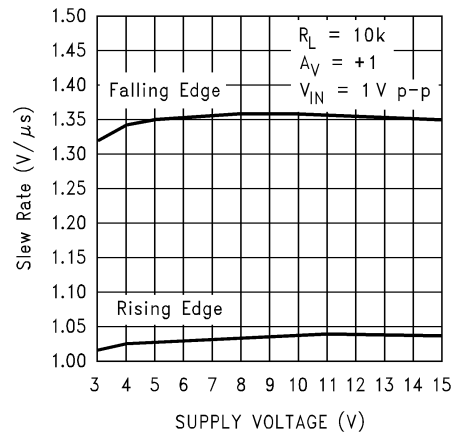**Figure 5-37. Slew Rate vs Temperature**
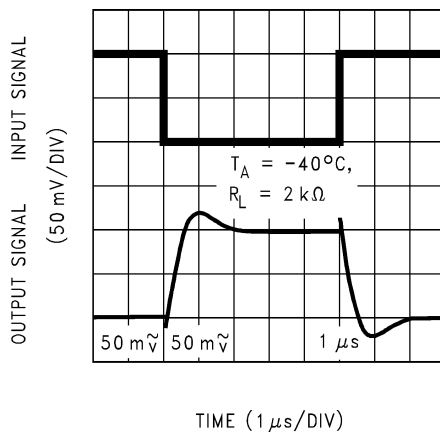
**Figure 5-38. Slew Rate vs Supply Voltage**

**Figure 5-39. Inverting Small-Signal Pulse Response**

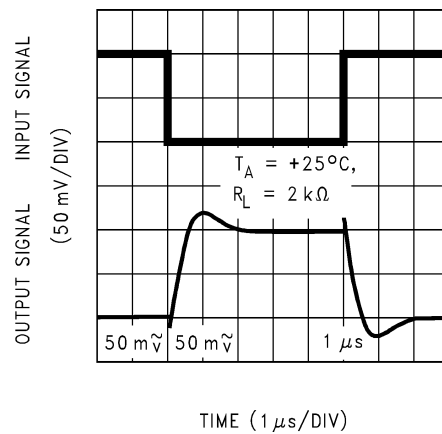**Figure 5-40. Inverting Small-Signal Pulse Response**

Product Folder Links: LMC7101

## 5.12 Typical Characteristics for $V_S$ = 15V (continued)

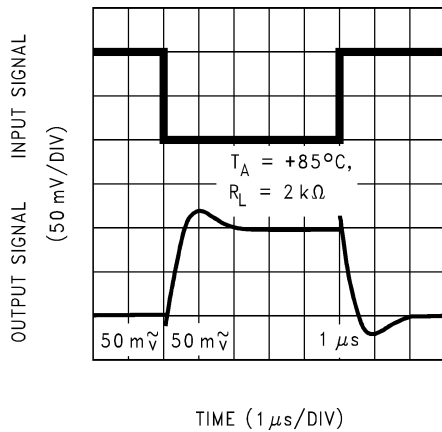at V+ = 15V, V– = 0V, and $T_A$ = 25°C (unless otherwise specified)

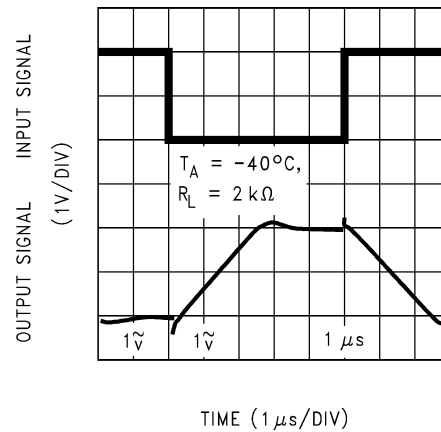**Figure 5-41. Inverting Small-Signal Pulse Response**

**Figure 5-42. Inverting Large-Signal Pulse Response**

**Figure 5-43. Inverting Large-Signal Pulse Response**

**Figure 5-44. Inverting Large-Signal Pulse Response**

**Figure 5-45. Noninverting Small-Signal Pulse Response**

**Figure 5-46. Noninverting Small-Signal Pulse Response**

Product Folder Links: *LMC7101*

## 5.12 Typical Characteristics for $V_S$ = 15V (continued)

at V+ = 15V, V– = 0V, and $T_A$ = 25°C (unless otherwise specified)



Figure 5-47. Noninverting Small-Signal Pulse Response
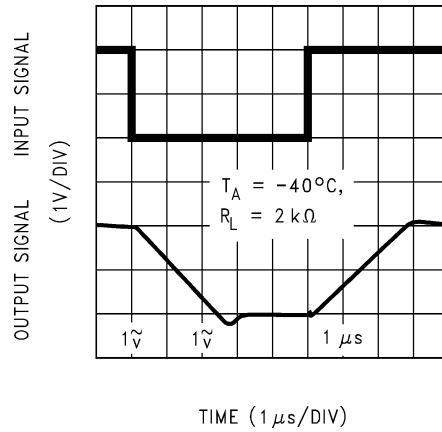


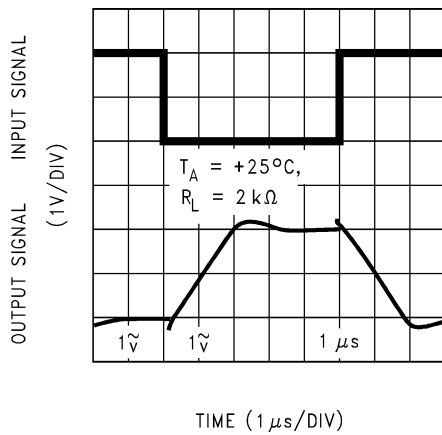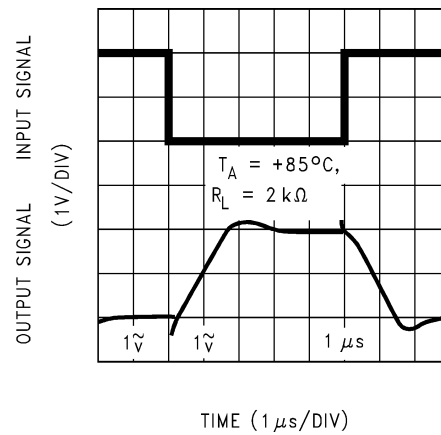Figure 5-48. Noninverting Large-Signal Pulse Response
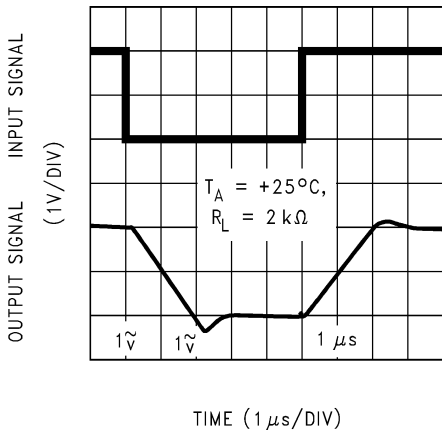


Figure 5-49. Noninverting Large-Signal Pulse Response
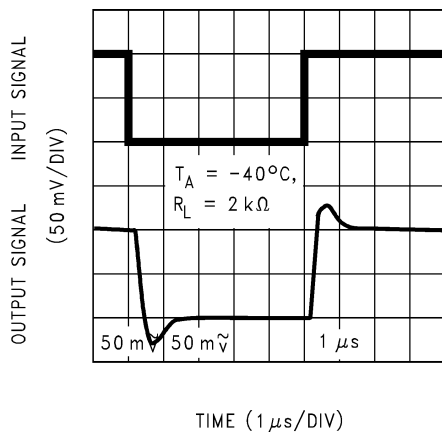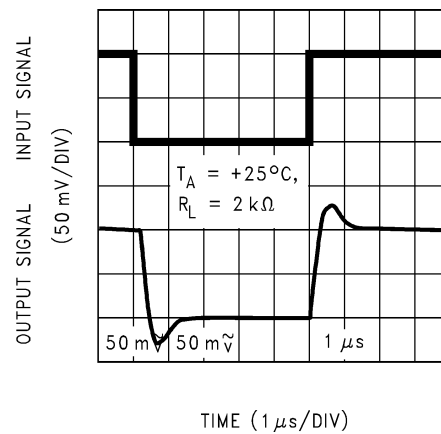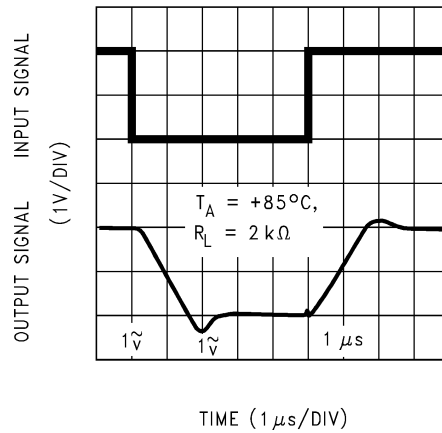


Figure 5-50. Noninverting Large-Signal Pulse Response
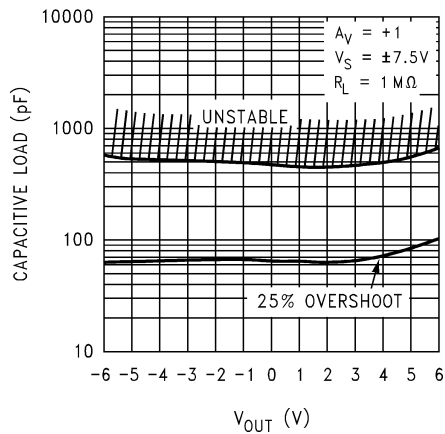


Figure 5-51. Stability vs Capacitive Load
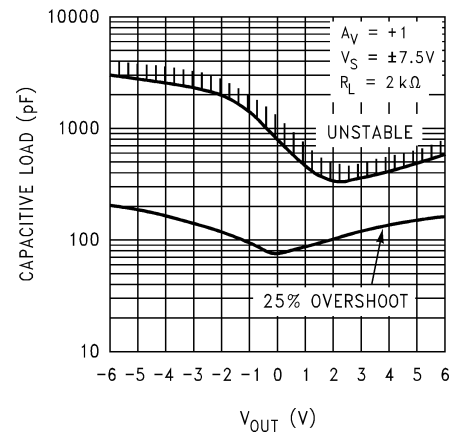


Figure 5-52. Stability vs Capacitive Load

Product Folder Links: *LMC7101*

## 5.12 Typical Characteristics for V$_S$ = 15V (continued)

at V+ = 15V, V– = 0V, and T$_A$ = 25°C (unless otherwise specified)



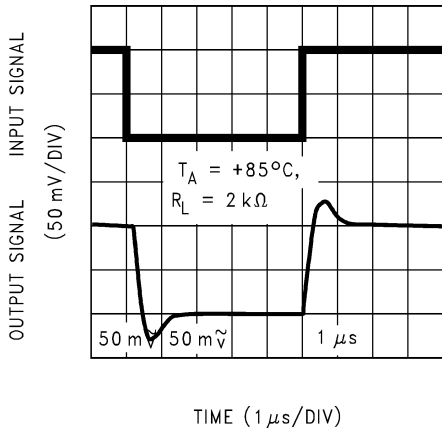Figure 5-53. Stability vs Capacitive Load



Figure 5-54. Stability vs Capacitive Load



Figure 5-55. Stability vs Capacitive Load



Figure 5-56. Stability vs Capacitive Load

Product Folder Links: *LMC7101*

# 6 Detailed Description

## 6.1 Overview

The LMC7101 is a single-channel, low-power operational amplifier available in a space-saving SOT-23 package, offering rail-to-rail input and output operation across a wide range of power-supply configurations.

The LMC7101 is also available in an automotive-grade variant, see LMC7101Q-Q1.

## 6.2 Functional Block Diagram



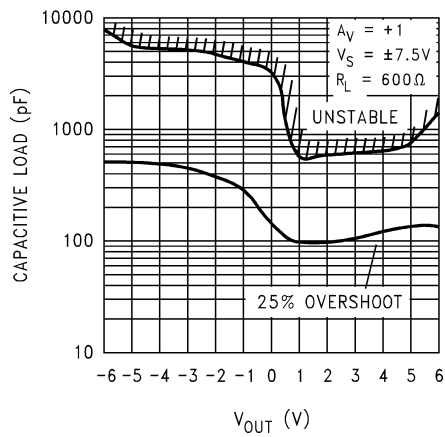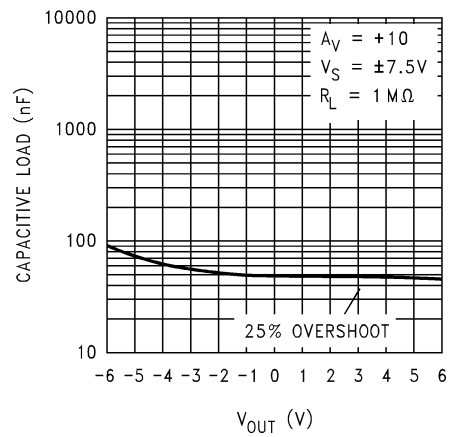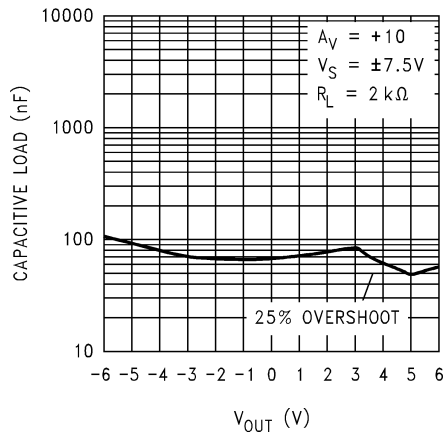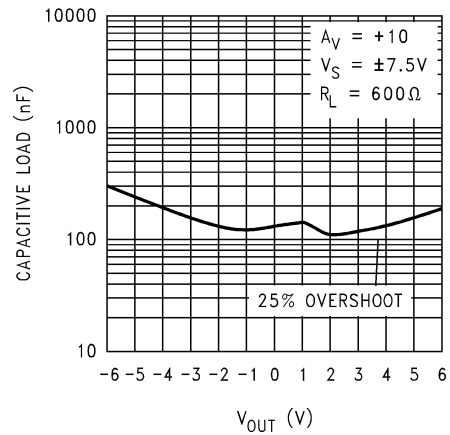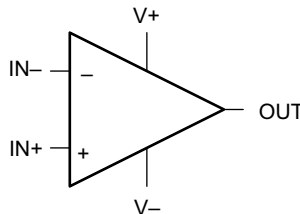## 6.3 Feature Description

### 6.3.1 Benefits of the LMC7101 Tiny Amplifier

#### 6.3.1.1 Size

The small footprint of the SOT-23-5 packaged tiny amplifier, (0.12in × 0.118in, 3.05mm × 3mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Many customers prefer smaller and lighter products because the designs can contribute to overall weight reduction in portable electronics.

#### 6.3.1.2 Height

The 0.056 inches (1.43mm) height of the tiny LMC7101 amplifier makes the device an excellent choice for use in a wide range of circuit boards in which a thin profile is required.

#### 6.3.1.3 Signal Integrity

Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the tiny amplifier can be placed closer to the signal source, thus reducing noise pickup and increasing signal integrity. The tiny amplifier can also be placed next to the signal destination, such as a buffer, for the reference of an analog-to-digital converter.

#### 6.3.1.4 Simplified Board Layout

The tiny LMC7101 amplifier can simplify board layout in several ways. Avoid long PCB traces by correctly placing amplifiers instead of routing signals to a dual or quad device. By using multiple tiny amplifiers instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

#### 6.3.1.5 Low THD

The high open-loop gain of the LMC7101 amplifier helps to achieve very low audio distortion—typically 0.01% at 10kHz with a 10kΩ load at 5V supplies. This makes the tiny amplifier an excellent choice for audio and low-frequency signal-processing applications.

#### 6.3.1.6 Low Supply Current

The typical 0.5mA supply current of the LMC7101 can help improve thermal performance on high density circuit boards, and can allow the reduction of the overall board size in some applications.

#### 6.3.1.7 Wide Voltage Range

The LMC7101 is characterized at 15V, 5V and 3V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7101 a good choice for devices where the supply voltage can vary.

## 6.4 Device Functional Modes

### 6.4.1 Input Common Mode

#### 6.4.1.1 Input Common-Mode Voltage Range

The LMC7101 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 6-1 shows an input voltage exceeding both supplies with no resulting phase inversion of the output.

The absolute maximum input voltage is 300mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating, as in Figure 6-2, can cause excessive current to flow in or out of the input pins, thus adversely affecting reliability.



The input voltage signal exceeds the amplifier power supply voltage with no output phase inversion.

**Figure 6-1. Input Voltage**



The ±7.5V input signal greatly exceeds the 3V supply in Figure 6-3 causing no phase inversion due to $R_I$.

**Figure 6-2. Input Signal**
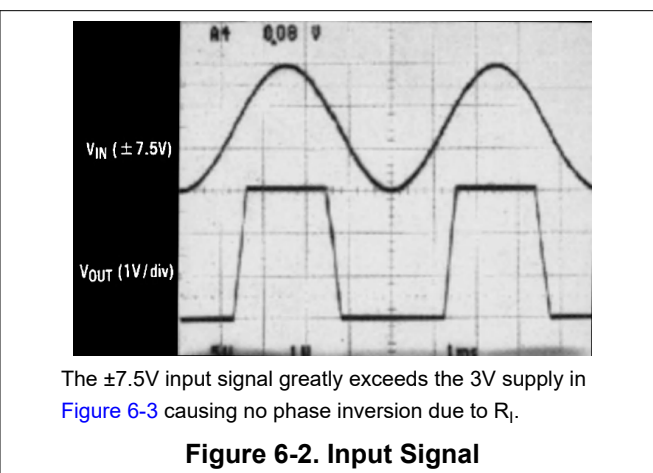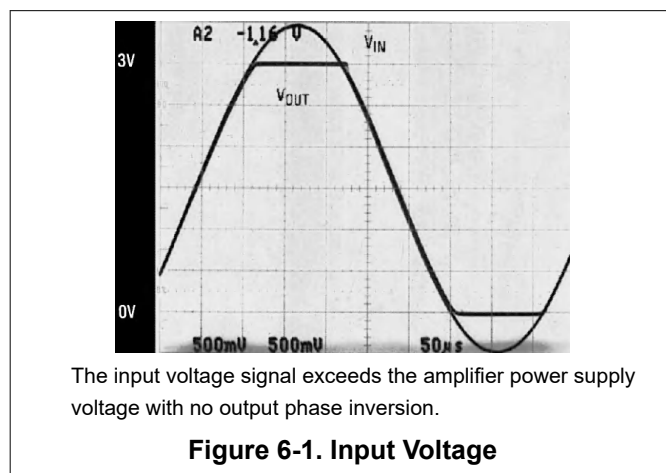
Applications that exceed this rating must externally limit the maximum input current to ±5mA with an input resistor as shown in Figure 6-3.



**Figure 6-3. $R_I$ Input Current Protection for Voltages Exceeding the Supply Voltage**

Product Folder Links: *LMC7101*

# 7 Application and Implementation

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.
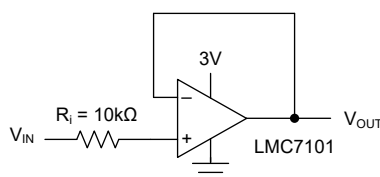
## 7.1 Application Information

### 7.1.1 Rail-to-Rail Output

The approximate output resistance of the LMC7101 is 180Ω sourcing and 130Ω sinking at $V_S$ = 3V and 110Ω sourcing and 80Ω sinking at $V_S$ = 5V. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

### 7.1.2 Capacitive Load Tolerance

The LMC7101 can typically directly drive a 100pF load with $V_S$ = 15V at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of operational amplifiers. The combination of the output impedance and the capacitive load of the operational amplifier induces phase lag, which results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 7-1. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.
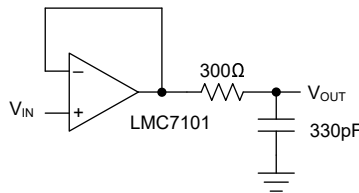


**Figure 7-1. Resistive Isolation of a 330pF Capacitive Load**

### 7.1.3 Compensating for Input Capacitance When Using Large Value Feedback Resistors

When using very large value feedback resistors, (usually >500 kΩ) the large feed back resistance can react with the input capacitance due to transducers, photo diodes, and circuit board parasitics to reduce phase margins.

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 7-2), $C_f$ is first estimated by Equation 1 and Equation 2, which typically provides significant overcompensation.

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \tag{1}$$

$$2\pi R_1 C_{IN} \leq 2\pi R_2 C_f \tag{2}$$

Printed circuit board stray capacitance can be larger or smaller than that of a breadboard, so the actual optimum value for $C_F$ can be different. The values of $C_F$ must be checked on the actual circuit.
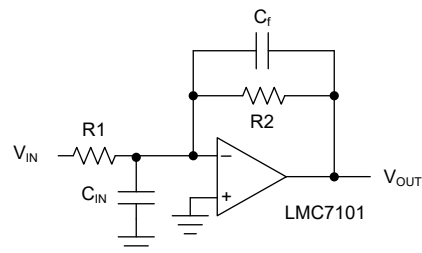


**Figure 7-2. Canceling the Effect of Input Capacitance**

## 7.2 Typical Application

Figure 7-3 shows a high input impedance noninverting circuit. This circuit gives a closed-loop gain equal to the ratio of the sum of R1 and R2 to R1 and a closed-loop 3dB bandwidth equal to the amplifier unity-gain frequency divided by the closed-loop gain. This design has the benefit of a very high input impedance, which is equal to the differential input impedance multiplied by loop gain (open loop gain / closed loop gain). In dc-coupled applications, input impedance is not as important as input current and the voltage drop across the source resistance. The amplifier output can go into saturation if the input is allowed to float, which can be important if the amplifier must be switched from source to source.
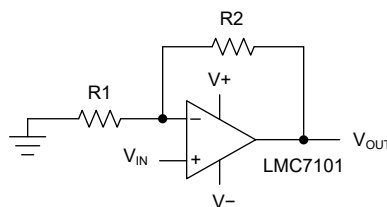


**Figure 7-3. Example Application**

### 7.2.1 Design Requirements

For this example application, the supply voltage is 5V, and 100 × ±5% of noninverting gain is necessary. The signal input impedance is approximately 10kΩ.

### 7.2.2 Detailed Design Procedure

Use the equation for a noninverting amplifier configuration; G = 1 + R2 / R1, set R1 to 10kΩ, and R2 to 99 × R1, which is 990kΩ. Replacing the 990kΩ resistor with a more readily available 1MΩ resistor results in a gain of 101, which is within the desired gain tolerance. The gain-frequency characteristic of the amplifier and the feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never exceed 180° for any frequency where the gain of the amplifier and the feedback network is greater than unity. In practical applications, the phase shift must not approach 180° because this is the situation of conditional stability. The most critical case occurs when the attenuation of the feedback network is zero.
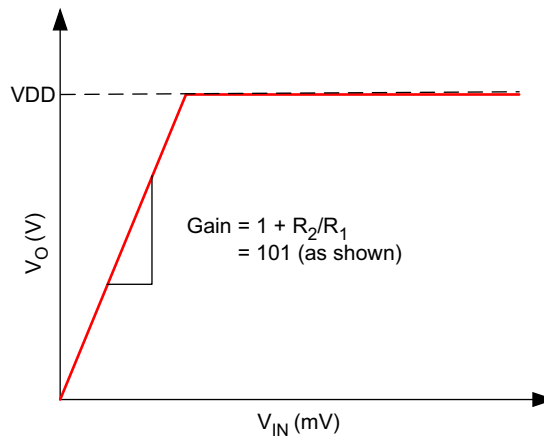
### 7.2.3 Application Curve



**Figure 7-4. Output Response**

## 7.3 Power Supply Recommendations

For proper operation, the power supplies must be decoupled. For supply decoupling, TI recommends placing 10nF to 1µF capacitors as close as possible to the operational-amplifier power supply pins. For single supply configurations, place a capacitor between the V+ and V− supply pins. For dual supply configurations, place one capacitor between V+ and ground, and place a second capacitor between V− and ground. Bypass capacitors must have a low ESR of less than 0.1Ω.

## 7.4 Layout

### 7.4.1 Layout Guidelines

Care must be taken to minimize the loop area formed by the bypass capacitor connection between supply pins and ground. A ground plane underneath the device is recommended; any bypass components to ground must have a nearby via to the ground plane. The optimum bypass capacitor placement is closest to the corresponding supply pin. Use of thicker traces from the bypass capacitors to the corresponding supply pins can lower the power-supply inductance and provide a more stable power supply.

The feedback components must be placed as close as possible to the device to minimize stray parasitics.
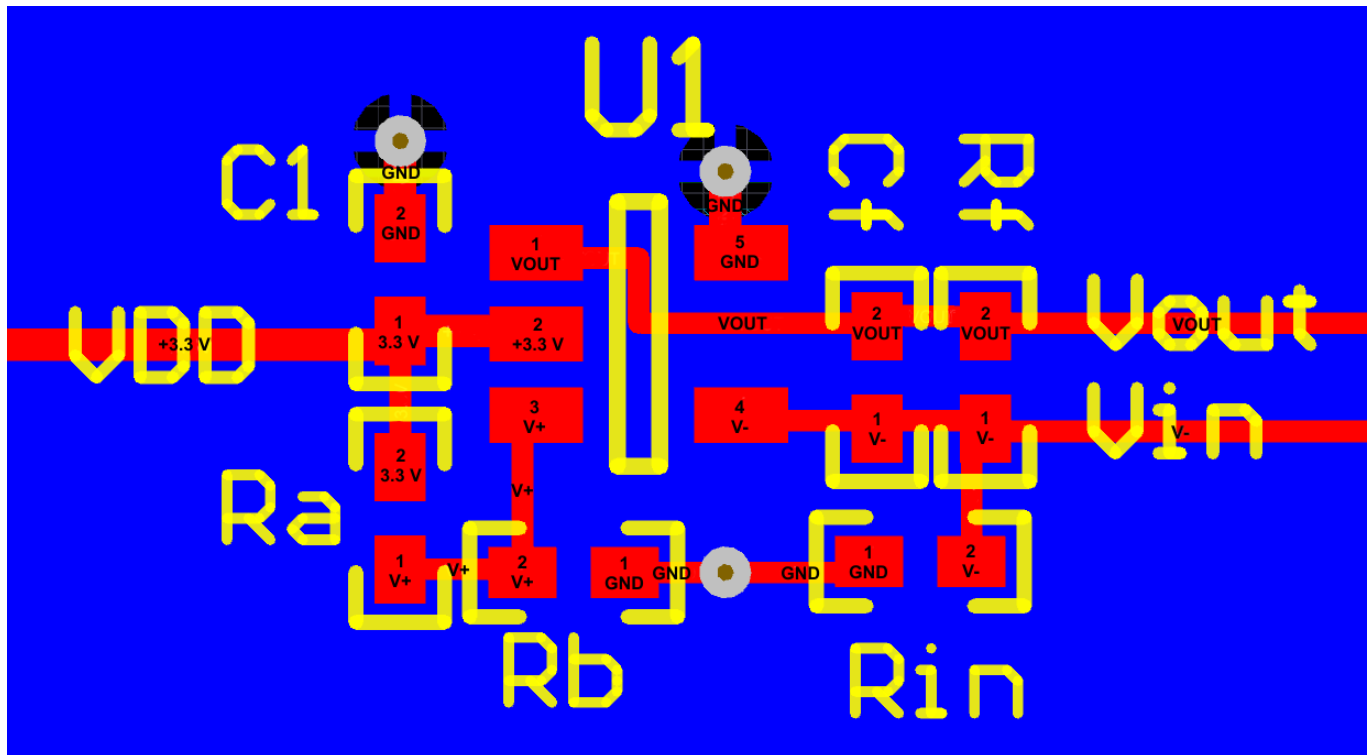
### 7.4.2 Layout Example



**Figure 7-5. LMC7101 Example Layout**

Product Folder Links: *LMC7101*

# 8 Device and Documentation Support

## 8.1 Documentation Support

### 8.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *LMC66x CMOS Dual Operational Amplifiers* data sheet
- Texas Instruments, *RES11A Matched, Thin-Film Resistor Dividers With 1kΩ Inputs* data sheet

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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## 8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

TI Glossary          This glossary lists and explains terms, acronyms, and definitions.

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMC7101AIM5/NOPB | OBSOLETE | SOT-23 | DBV | 5 | | TBD | Call TI | Call TI | -40 to 85 | A00A | |
| LMC7101AIM5X/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | A00A | Samples |
| LMC7101BIM5/NOPB | OBSOLETE | SOT-23 | DBV | 5 | | TBD | Call TI | Call TI | -40 to 85 | A00B | |
| LMC7101BIM5X/NOPB | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | A00B | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMC7101AIM5X/NOPB | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LMC7101AIM5X/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LMC7101BIM5X/NOPB | SOT-23 | DBV | 5 | 3000 | 178.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| LMC7101BIM5X/NOPB | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMC7101AIM5X/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| LMC7101AIM5X/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LMC7101BIM5X/NOPB | SOT-23 | DBV | 5 | 3000 | 208.0 | 191.0 | 35.0 |
| LMC7101BIM5X/NOPB | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

PKG ℄

5X (1.1)

1

5X (0.6)

5

2

SYMM ℄

(1.9)

2X (0.95)

3

4

(R0.05) TYP

(2.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK OPENING

METAL

EXPOSED METAL

0.07 MAX ARROUND

NON SOLDER MASK DEFINED
(PREFERRED)

METAL UNDER SOLDER MASK

SOLDER MASK OPENING

EXPOSED METAL

0.07 MIN ARROUND

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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