LP2960 Adjustable Micropower 0.5A Low-Dropout Regulators

Check for Samples: LP2960

FEATURES

- **Output Voltage Adjusts from 1.23V–29V**
- **Ensured 500 mA Output Current**
- **5V and 3.3V Versions Available**
- **16-Pin SO Package**
- **Low Dropout Voltage**
- **Low Quiescent Current**
- **Tight Line and Load Regulation**
- **Low Temperature Coefficient**
- **Current Limiting and Thermal Protection**
- **Logic-Level Shutdown**
- **Can be Wired for Snap-ON and Snap-OFF**
- **Reverse Battery Protection**

APPLICATIONS

- **High-Efficiency Linear Regulator**
- **Regulator with Under-Voltage Shutdown**
- **Low Dropout Battery-Powered Regulator**
- **Cellular Telephones**

DESCRIPTION

The LP2960 is a micropower voltage regulator with very low dropout voltage (12 mV typical at 1 mA load and 470 mV typical at 500 mA load) and very low quiescent current (450 µA typical at 1 mA load).

The LP2960 is ideally suited for battery-powered systems: the quiescent current increases only slightly at dropout, which prolongs battery life.

The LP2960 retains all the desirable characteristics of the LP2953, and offers increased output current.

The error flag goes low any time the output drops more than 5% out of regulation.

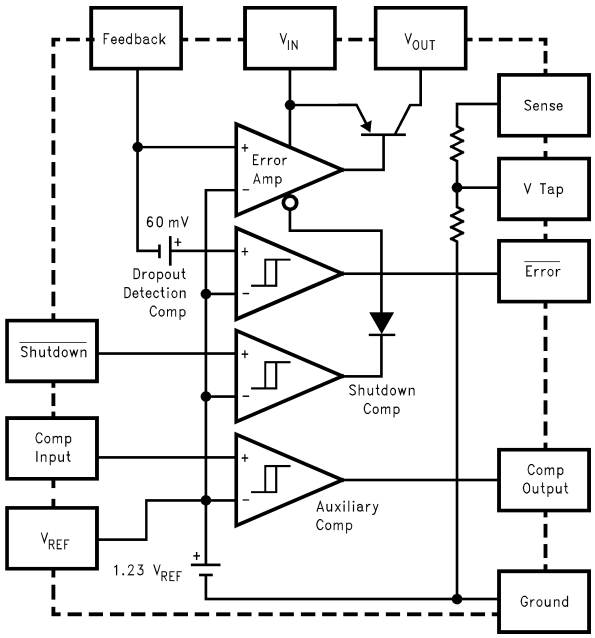
Reverse battery protection is provided.

The LP2960 requires only 10 µF of output capacitance for stability (5V version).

The internal voltage reference is made available for external use, providing a low-T.C. reference with very good regulation characteristics.

The part is available in a 16-pin surface mount (SOIC) package.

Block Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)

Storage Temperature Range		−65°C to +150°C
Operating Junction Temperature Range	LP2960AI/LP2960I	−40°C to +125°C
Lead Temperature (Soldering, 5 sec.)		260°C
Power Dissipation(2)		Internally Limited
Input Supply Voltage		−20V to +30V
Feedback Input Voltage(3)		−0.3V to +5V
Comparator Input Voltage(4)		−0.3V to +30V
Comparator Output Voltage(4)		−0.3V to +30V
ESD Rating(5)		1.5 kV

(1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
(2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (max), the junction-to-ambient thermal resistance, θ_{J-A}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{(max)} = \frac{T_{J(max)} - T_A}{\theta_{J-A}}$ Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. See Application Hints for additional information on heatsinking and thermal resistance.
(3) When used in dual-supply systems where the regulator load is returned to a negative supply, the output voltage must be diode-clamped to ground.
(4) May exceed the input supply voltage.
(5) Human Body Model, 200 pF discharged through 1.5 kΩ.

Electrical Characteristics

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: C_{IN} = 4.7 µF, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA, C_{OUT} = 10 µF for 5V parts or C_{OUT} = 22 µF for 3.3V parts, Feedback pin is tied to V_{TAP} pin, Output pin is tied to Sense pin, $V_{S/D}$ = 2V.

Symbol	Parameter	Conditions	Typ	LP2960AI(1)		LP2960I(1)		Units
				Min	Max	Min	Max	
V_O	Output Voltage (5V Versions)	1 mA ≤ I_L ≤ 500 mA	5.0	4.962 **4.930**	5.038 **5.070**	4.925 **4.880**	5.075 **5.120**	V
	Output Voltage (3.3 Versions)	1 mA ≤ I_L ≤ 500 mA	3.3	3.275 **3.254**	3.325 **3.346**	3.250 **3.221**	3.350 **3.379**	
$\frac{\Delta V_O}{\Delta T}$	Output Voltage Temperature Coefficient	See(2)	**20**		**130**		**160**	ppm/°C
$\frac{\Delta V_O}{V_O}$	Output Voltage Line Regulation	V_{IN} = [V_O(NOM) + 1V] to 30V	0.06		0.2 **0.5**		0.4 **0.8**	%
$\frac{\Delta V_O}{V_O}$	Output Voltage Load Regulation	See(3)	0.08		0.16 **0.30**		0.20 **0.40**	%

(1) All room temperature limits are 100% production tested. All limits at **temperature extremes** are ensured via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level.
(2) Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.
(3) Output voltage load regulation is measured at constant junction temperature using low duty cycle pulse testing. Two separate tests are performed, one for the load current range of 100 µA to 1 mA and one for the 1 mA to 500 mA range. Changes in output voltage due to heating effects are covered by the thermal regulation specification.

Electrical Characteristics (continued)

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: C_{IN} = 4.7 µF, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA, C_{OUT} = 10 µF for 5V parts or C_{OUT} = 22 µF for 3.3V parts, Feedback pin is tied to V_{TAP} pin, Output pin is tied to Sense pin, $V_{S/D}$ = 2V.

Symbol	Parameter	Conditions	Typ	LP2960AI(1)		LP2960I(1)		Units
				Min	Max	Min	Max	
$V_{IN} - V_O$	Dropout Voltage(4)	I_L = 1 mA	12		30 **50**		30 **50**	mV
		I_L = 100 mA	180		250 **350**		250 **350**	
		I_L = 200 mA	260		350 **450**		350 **450**	
		I_L = 500 mA	470		600 **800**		600 **800**	
I_{GND}	Ground Pin Current(5)	I_L = 1 mA	450		600 **750**		600 **750**	µA
		I_L = 100 mA	2.6		4.0 **5.0**		4.0 **5.0**	mA
		I_L = 200 mA	2.5		8 **10**		8 **10**	
		I_L = 500 mA	21		35 **40**		35 **40**	
I_{GND}	Ground Pin Current at Dropout(5)	V_{IN} = V_O(NOM) − 0.5V I_L = 100 µA	1.8		3 **5**		3 **5**	mA
	Ground Pin Current at Shutdown(5)	V_{SD} ≤ 1.1V	300		400		400	µA
I_{LIMIT}	Current Limit	R_L = 0.5Ω	1000		1500 **1600**		1500 **1600**	mA
$\frac{\Delta V_O}{P_D}$	Thermal Regulation	See(6)	0.05		0.2		0.2	%/W
e_n	Output Noise Voltage @ I_L = 100 mA (10 Hz–100kHz)	C_{OUT} = 10 µF	300					µV RMS
		C_{OUT} = 47 µF	210					
		C_{OUT} = 47 µF(7)	130					
V_{REF}	Reference Voltage		1.235	1.220 **1.210**	1.250 **1.265**	1.210 **1.195**	1.260 **1.275**	V
$\frac{\Delta V_{REF}}{V_{REF}}$	Reference Voltage Line Regulation	See(8)	0.05		0.1 **0.30**		0.2 **0.4**	%
$\frac{\Delta V_{REF}}{V_{REF}}$	Reference Voltage Load Regulation	I_{REF} = 0–200 µA	0.45		0.6 **0.9**		1.2 **1.5**	%
$\frac{\Delta V_{REF}}{\Delta T}$	Reference Voltage Temperature Coefficient	See(9)	**20**					ppm/°C
I_B(FB)	Feedback Pin Bias Current		−20		−50 **−70**		−50 **−70**	nA

(4) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1V differential. At very low values of programmed output voltage, the input voltage minimum of 2V **(2.3V over temperature)** must be observed.
(5) Ground pin current is the regulator quiescent current. The total current drawn from the source is the sum of the ground pin current, output load current, and current through the external resistive divider (if used).
(6) Thermal regulation is the change in output voltage at a time T after a change in power dissipation, excluding load or line regulation effects. Specifications are for a 400 mA load pulse at V_{IN} = V_O(NOM) + 15V (6W pulse) for T = 10 ms.
(7) Connect a 0.1 µF capacitor from the output to the feedback pin.
(8) Two separate tests are performed for reference voltage line regulation, one covering 2.5V ≤ V_{IN} ≤ V_O(NOM) + 1V and the other test for V_O(NOM) + 1V ≤ V_{IN} ≤ 30V.
(9) Output or reference voltage temperature coefficient is defined as the worst case voltage change divided by the total temperature range.

Electrical Characteristics (continued)

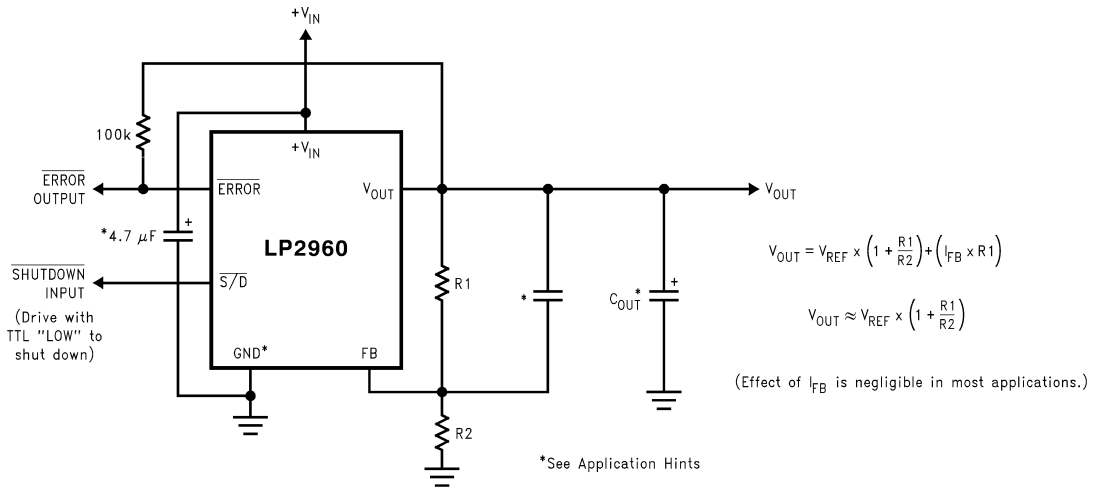
Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: C_{IN} = 4.7 µF, V_{IN} = V_O(NOM) + 1V, I_L = 1 mA, C_{OUT} = 10 µF for 5V parts or C_{OUT} = 22 µF for 3.3V parts, Feedback pin is tied to V_{TAP} pin, Output pin is tied to Sense pin, $V_{S/D}$ = 2V.

Symbol	Parameter	Conditions	Typ	LP2960AI(1)		LP2960I(1)		Units
				Min	Max	Min	Max	
DROPOUT DETECTION COMPARATOR								
I_{OH}	Output HIGH Leakage	V_{OH} = 30V	0.01		1 **2**		1 **2**	µA
V_{OL}	Output LOW Voltage	V_{IN} = V_O(NOM) − 1V I_O(COMP) = 400 µA	125		250 **400**		250 **400**	mV
V_{THR}(max)	Upper Threshold Voltage	See(10)	−60	−80 **−100**	−35 **−25**	−80 **−100**	−35 **−25**	mV
V_{THR}(min)	Lower Threshold Voltage	See(10)	−85	−130 **−200**	−70 **−35**	−130 **−200**	−70 **−35**	mV
HYST	Hysteresis	See(10)	25					mV
SHUTDOWN INPUT								
V_{OS}	Input Offset Voltage	(Referred to V_{REF})	±5	−18 **−24**	18 **24**	−18 **−24**	18 **24**	mV
HYST	Hysteresis	(Referred to V_{REF})	10					mV
I_B	Input Bias Current	$V_{S/D}$ = 0–5V	−20	−60 **−100**	60 **100**	−60 **−100**	60 **100**	nA
I_{OUT}(S/D)	Regulator Output Current in Shutdown	See(11)	3		12 **20**		12 **20**	µA
AUXILIARY COMPARATOR								
V_{OS}	Input Offset Voltage	(Referred to V_{REF})	±5	−15 **−20**	15 **20**	−15 **−20**	15 **20**	mV
HYST	Hysteresis	(Referred to V_{REF})	10					mV
I_B	Input Bias Current	V_{COMP} = 0–5V	−20	−60 **−100**	60 **100**	−60 **−100**	60 **100**	nA
I_{OH}	Output HIGH Leakage	V_{OH} = 30V, V_{COMP} = 1.3V	0.01		1 **2**		1 **2**	µA
V_{OL}	Output LOW Voltage	V_{COMP} = 1.1V, I_O = 400 µA	125		250 **400**		250 **400**	mV

(10) Dropout detection comparator threshold voltages are expressed in terms of a voltage differential measured at the Feedback terminal below the *nominal* reference voltage, which is the reference voltage measured with V_{IN} = V_O(NOM) + 1V. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain which is V_O/V_{REF} = (R1 + R2)/R2 (see Basic Application Circuit).

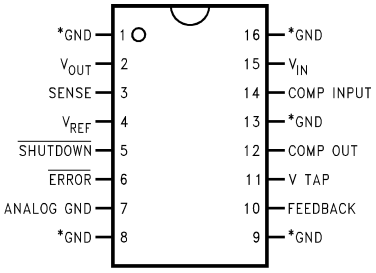
(11) Vshutdown ≤ 1.1V, V_{IN} < 30V, V_{OUT} = 0V.

Basic Application Circuit



Connection Diagram

Top View



*Internally Connected to Power Ground

Figure 1. 16-Pin Surface Mount SOIC Package
See Package Number D0016A

Typical Performance Characteristics

Unless otherwise specified: C_{IN} = 4.7 µF, V_{IN} = 6V, I_L = 1 mA, C_{OUT} = 10 µF, Feedback pin is tied to V_{TAP} pin, Output pin is tied to Sense pin, $V_{S/D}$ = 2V, V_{OUT} = 5V.

Ground Pin Current

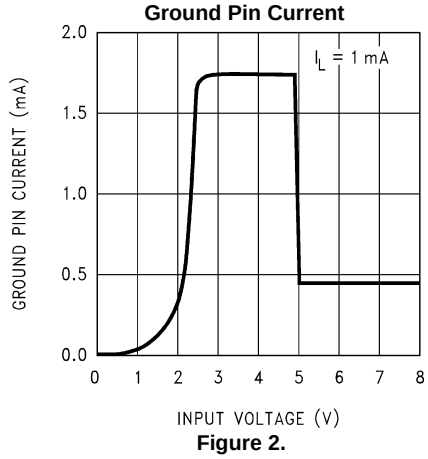


Figure 2.

Ground Pin Current

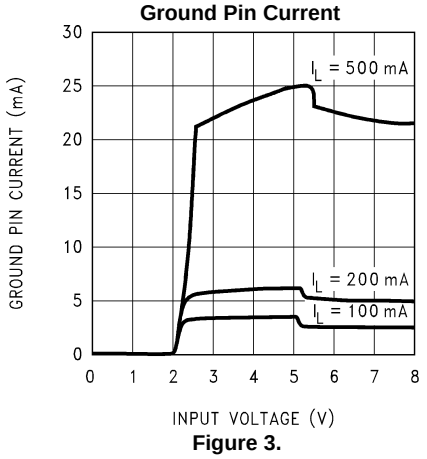


Figure 3.

Ground Pin Current

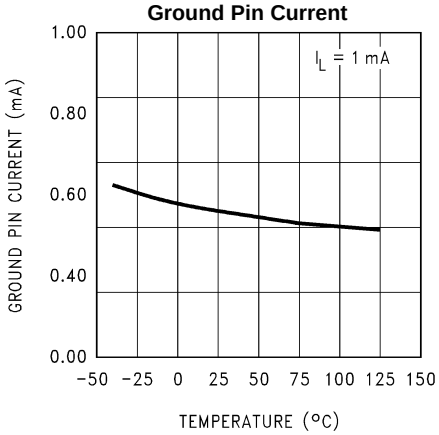


Figure 4.

Ground Pin Current

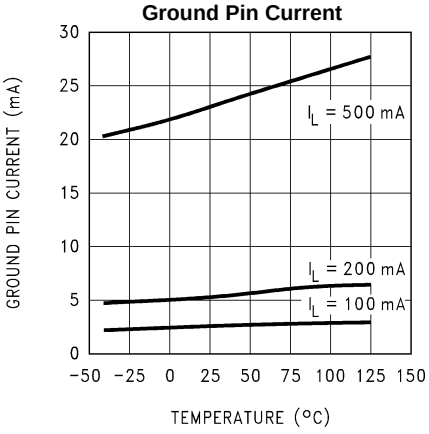


Figure 5.

Ground Pin Current

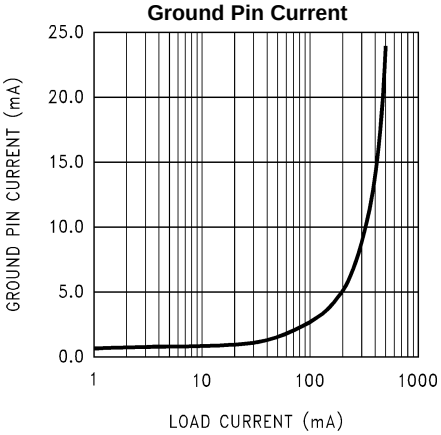


Figure 6.

Dropout Characteristics

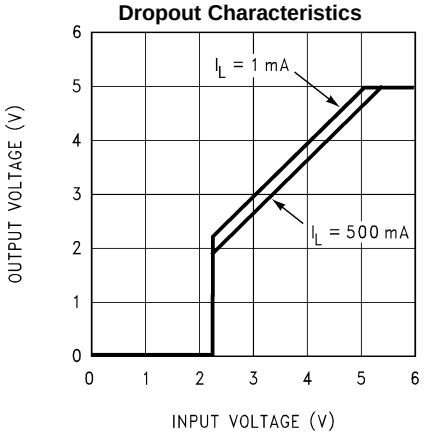


Figure 7.

Typical Performance Characteristics (continued)

Unless otherwise specified: C_{IN} = 4.7 µF, V_{IN} = 6V, I_L = 1 mA, C_{OUT} = 10 µF, Feedback pin is tied to V_{TAP} pin, Output pin is tied to Sense pin, $V_{S/D}$ = 2V, V_{OUT} = 5V.

Dropout Voltage vs Temperature

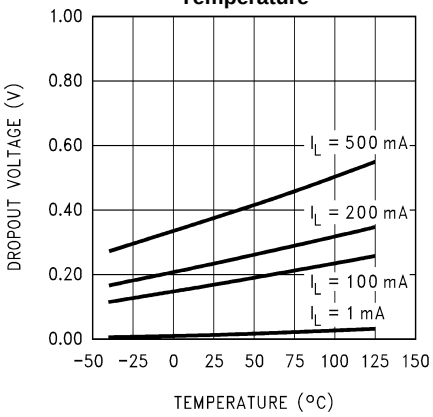


Figure 8.

Dropout Voltage vs Load Current

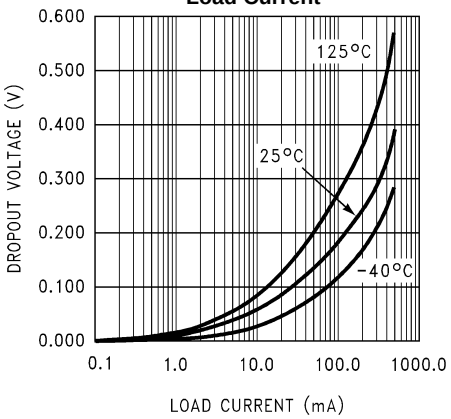


Figure 9.

Enable Transient

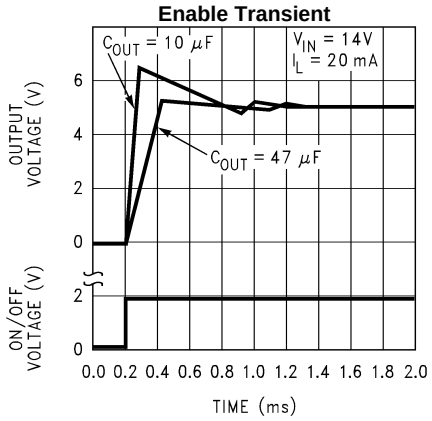


Figure 10.

Enable Transient

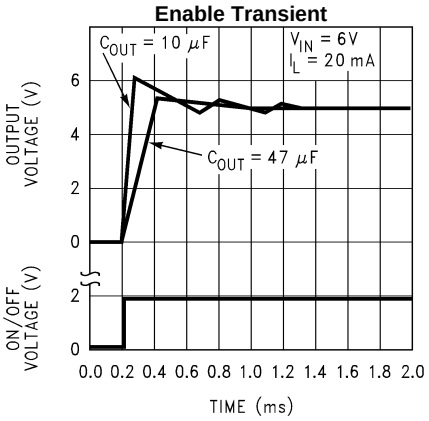


Figure 11.

Load Transient

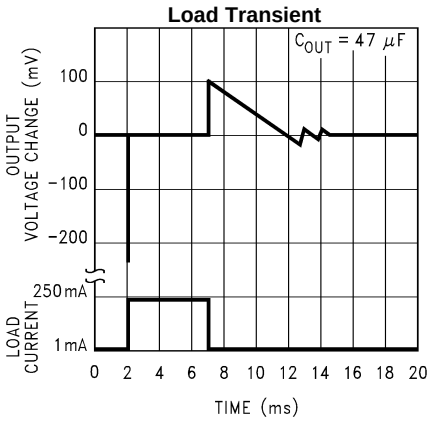


Figure 12.

Load Transient

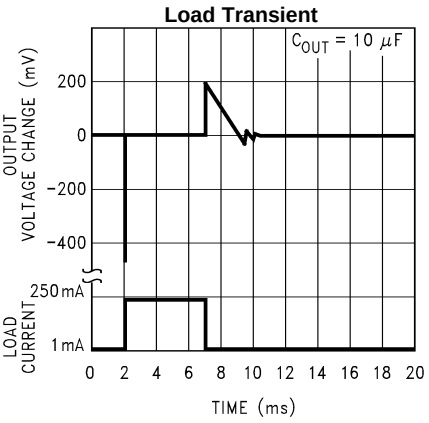


Figure 13.

Typical Performance Characteristics (continued)

Unless otherwise specified: C_{IN} = 4.7 µF, V_{IN} = 6V, I_L = 1 mA, C_{OUT} = 10 µF, Feedback pin is tied to V_{TAP} pin, Output pin is tied to Sense pin, $V_{S/D}$ = 2V, V_{OUT} = 5V.

Current Limit vs Temperature

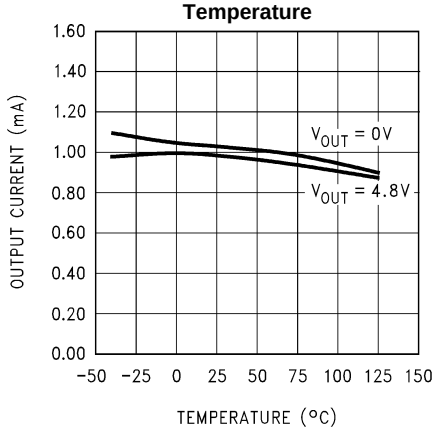


Figure 14.

Line Transient Response

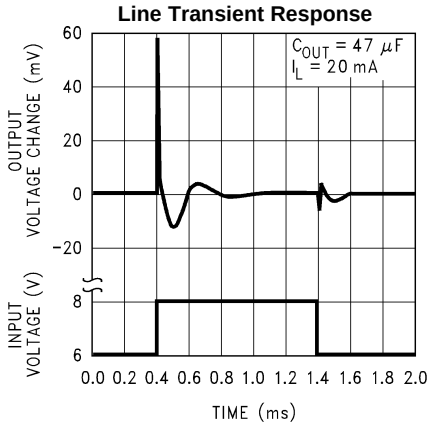


Figure 15.

Line Transient Response

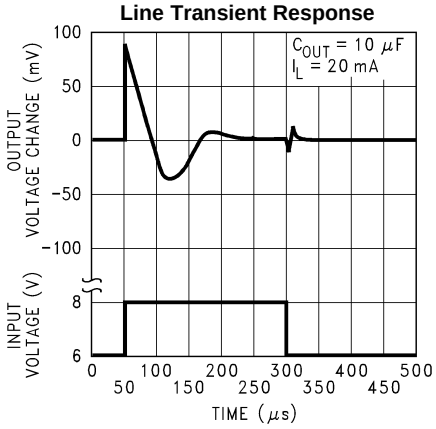


Figure 16.

Ripple Rejection

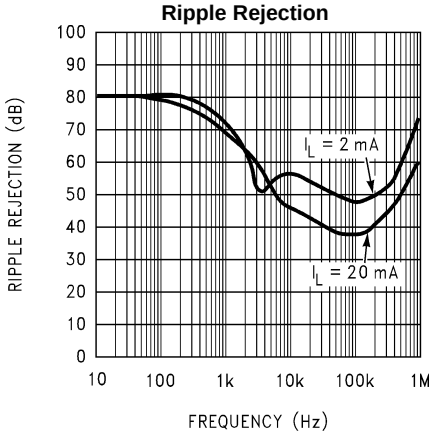


Figure 17.

Ripple Rejection

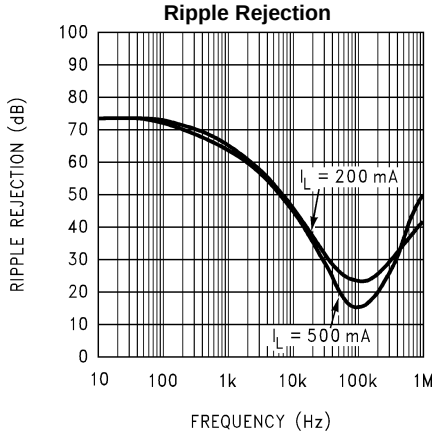


Figure 18.

Thermal Regulation

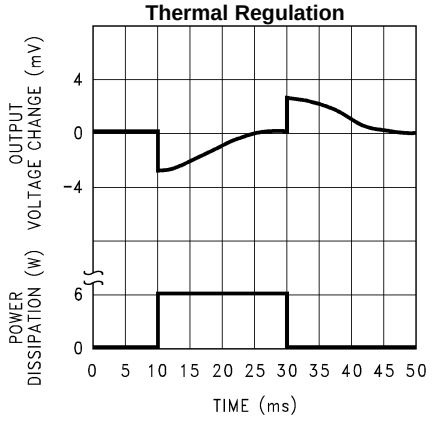


Figure 19.

Typical Performance Characteristics (continued)

Unless otherwise specified: C_{IN} = 4.7 µF, V_{IN} = 6V, I_L = 1 mA, C_{OUT} = 10 µF, Feedback pin is tied to V_{TAP} pin, Output pin is tied to Sense pin, $V_{S/D}$ = 2V, V_{OUT} = 5V.

Output Impedance

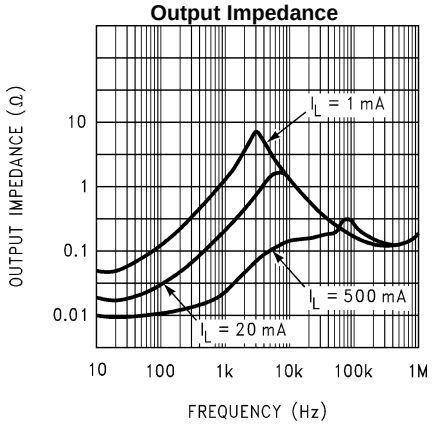


Figure 20.

Output Noise Voltage

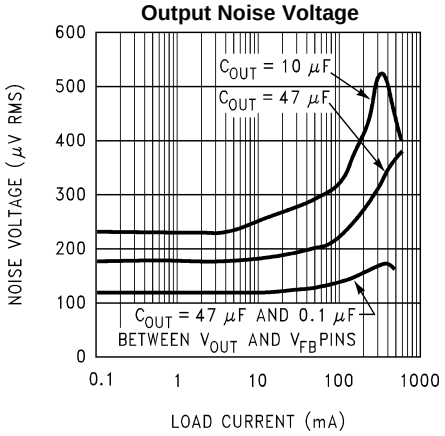


Figure 21.

Feedback Bias Current

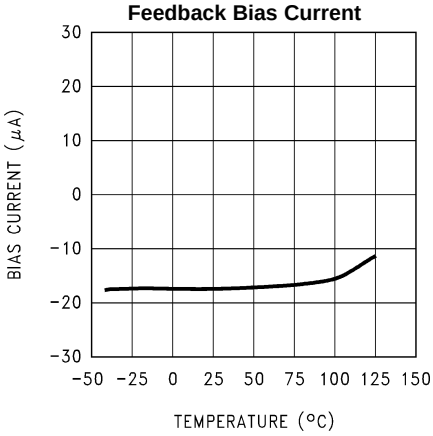


Figure 22.

Divider Resistance

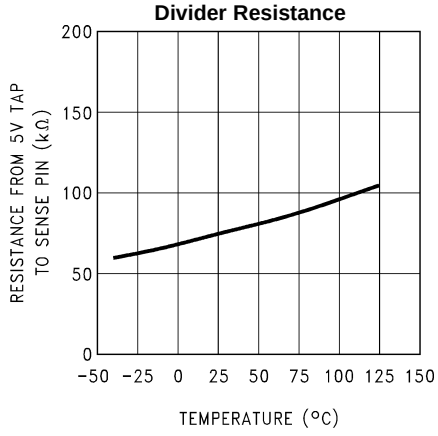


Figure 23.

Error Output Voltage vs Input Voltage

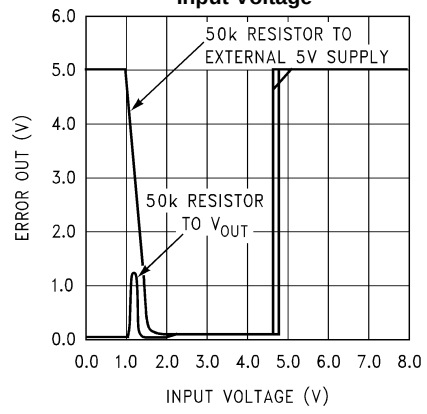


Figure 24.

Dropout Detection Comparator Threshold Voltage

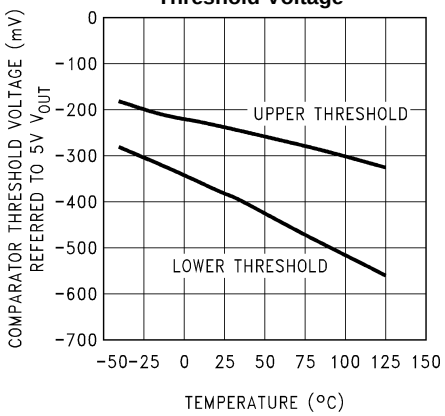
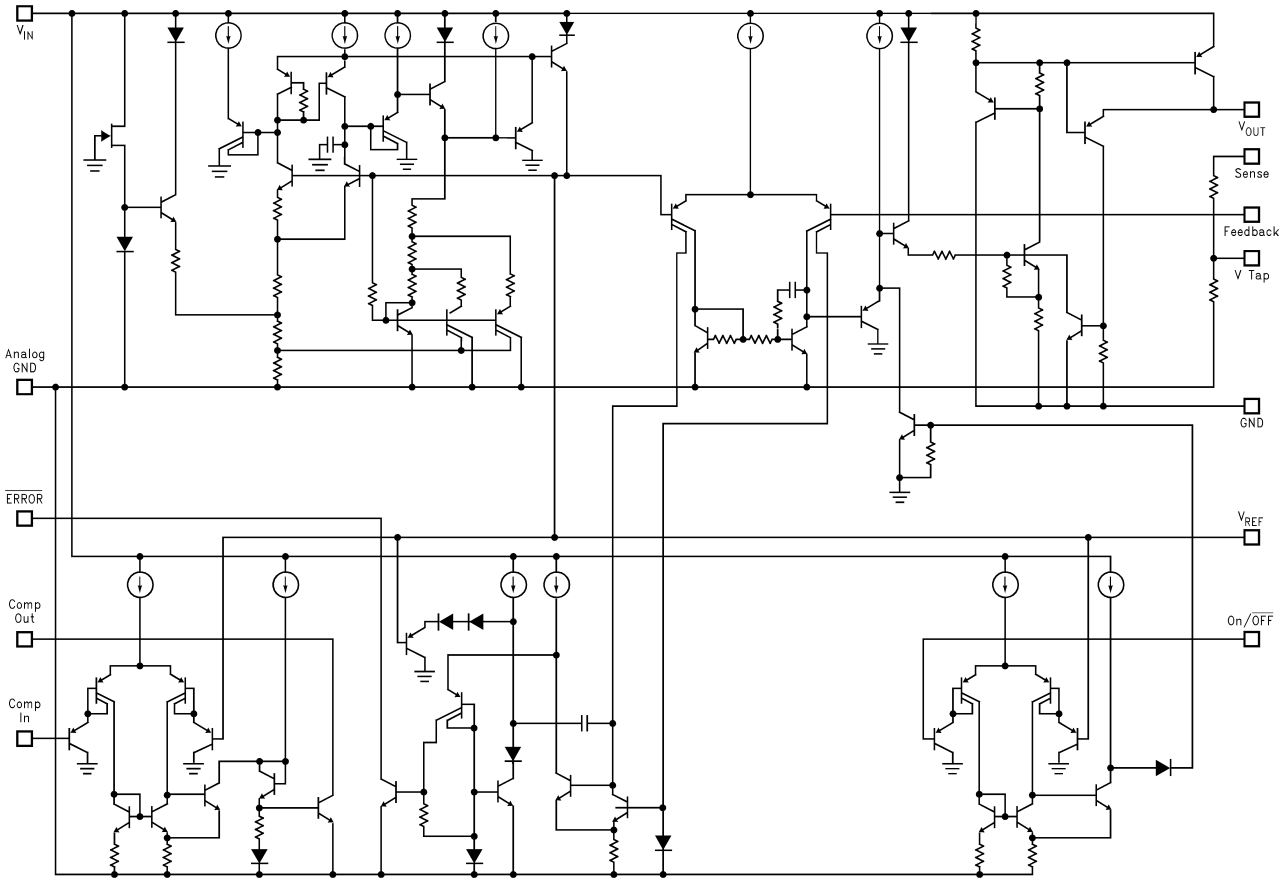


Figure 25.

Schematic Diagram



APPLICATION HINTS

EXTERNAL CAPACITORS

Bypass capacitors on the input and output of the LP2960 are required: without these capacitors, *the part will oscillate*.

A capacitor (whose value is *at least* 4.7 µF) must be connected from the V_{IN} pin to ground. If the input capacitor is located more than one inch away from the LP2960, the capacitor may have to be increased to 22 µF to assure stability. A capacitor is also required between V_{OUT} and Ground, and the minimum amount of capacitance required here depends on output voltage.

If the output voltage of the LP2960 is set to 5V, a minimum of 10 µF is needed in output capacitance. At 3.3V output, at least 22 µF is required to assure stability.

ESR LIMIT: The ESR of the capacitor used on the LP2960 must be less than 0.7Ω *throughout the entire operating temperature range* to assure stability.

The ESR of an aluminum electrolytic capacitor is typically only specified at 25°C, and does not reflect the maximum ESR that can be expected to occur over the entire temperature range of the capacitor.

Aluminum electrolytics show a marked increase in ESR at low temperatures (ESR can increase by a factor of 30 or more when going from 25°C to −30°C) which could lead to oscillation problems in applications with very low ambient temperatures. Solid tantalum capacitors are recommended for use in such cases.

Regulator instability can be caused by stray (board layout) capacitance appearing at the Feedback terminal. Oscillations from this effect are most likely to occur when very high value resistors are used to set the output voltage.

Adding a 100 pF capacitor between the Output and Feedback pins and increasing the output capacitor to at least 22 µF will stop the oscillations.

MINIMUM LOAD

The internal resistive divider in the LP2960 provides sufficient output loading for proper regulation. If external resistors are used to set the LP2960 output voltage, a minimum current of 5 µA through the external resistive divider is recommended.

It should be noted that a minimum load current is specified in several of the test conditions listed under Electrical Characteristics, and this value of load current must be used to get correlation on these test limits.

PROGRAMMING THE OUTPUT VOLTAGE

The LP2960 regulator may be pin-strapped for operation at the nominal output voltage using its internal resistive divider by tying the Output and Sense pins together and also tying the Feedback and V_{TAP} pins together.

Alternatively, it may be programmed for any voltage between the 1.23V reference and the 30V maximum rating using an external pair of resistors (see Basic Application Circuit).

The complete equation for the output voltage is:

$$V_{OUT} = V_{REF} \times (1 + R1/R2) + (I_{FB} \times R1) \quad (1)$$

The term V_{REF} is the 1 .23V reference and I_{FB} is the Feedback pin bias current (−20 nA typical). The minimum recommended load current of 5 µA sets an upper limit of 240 kΩ on the value of R2 in cases where the regulator must work with no load (see Minimum Load).

For best output accuracy, choosing R2 = 100 kΩ will reduce the error resulting from I_{FB} to 0.17% while increasing the resistive divider current to 12 µA. Since the typical quiescent current of the LP2960 is 450 µA, this added current through R2 is negligible.

DROPOUT VOLTAGE

The dropout voltage of the regulator is defined as the minimum input-to-output voltage differential required for the output voltage to stay within 100 mV of the output voltage measured with a 1V differential. The dropout voltage is independent of the programmed output voltage.

OUTPUT ISOLATION

If the LP2960 output is connected to an active voltage source (such as a battery) the regulator input should not be shorted to ground, as this will cause a large current to flow from the battery into the LP2960 output lead.

If the LP2960 input is *left floating* with the output connected to a battery, a small current (a few mA) will flow into the output lead.

The “reverse” current flowing from the battery into the LP2960 output can be prevented by using a blocking diode between the output and the battery.

REDUCING OUTPUT NOISE

In reference applications it may be desirable to reduce the AC noise present on the output. One method is to reduce regulator bandwidth by increasing output capacitance. This is relatively inefficient, since large increases in capacitance are required to get significant improvement.

Noise can be reduced more effectively by a bypass capacitor placed across R1 (refer to Basic Application Circuit).

A 0.1 µF capacitor connected across R1 will reduce the high frequency gain of the circuit to unity, lowering the RMS output noise voltage from 210 µV to 130 µV (typical) using a 10 Hz–100 kHz bandwidth test measurement.

Also, output noise is no longer proportional to the output voltage, so improvements are more pronounced at higher output voltages.

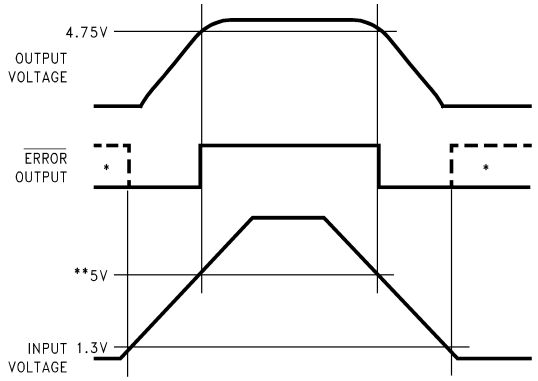
IMPORTANT: Since the 0.1 µF capacitor reduces the AC gain of the LP2960 to unity, the output capacitance must be increased to at least 33 µF to assure regulator stability.

DROPOUT DETECTION COMPARATOR

The dropout detection comparator produces a logic “LOW” on the Error output whenever the LP2960 output drops out of regulation by more than about 5%. This figure results from the comparator’s built-in offset of 60 mV divided by the 1.23V reference (refer to Block Diagram).

The “5% below nominal” trip level remains constant regardless of the programmed output voltage. An out-of-regulation condition can result from low input voltage, current limiting, or thermal limiting.

The figure below gives a timing diagram showing the relationship between the output voltage, the Error output, and input voltage as the input voltage is ramped up and down to a regulator programmed for 5V output.



*In shutdown mode, $\overline{\text{ERROR}}$ will go high if it has been pulled up to an external supply. To avoid this invalid response, pull-up to regulator output.
**Exact value depends on dropout voltage. (See Application Hints)

Figure 26. Error Output Timing Diagram

The Error signal becomes low as V_{IN} exceeds about 1.3V. It goes high at about 5V input, where the output equals 4.75V. Since the dropout voltage is load dependent, the *input voltage* trip points will vary with load current, but the *output voltage* trip point does not.

The comparator has an open-collector output which requires an external pull-up resistor. This resistor may be connected to the LP2960 output or another supply voltage.

Best operation is obtained by connecting the pull-up to the LP2960 output. If the pull-up resistor is connected to an external 5V supply, the error flag will incorrectly signal "HIGH" whenever V_{IN} < 1.3V (see Figure 26).

In selecting a value for the pull-up resistor, note that while the output can sink 400 µA, this current adds to battery drain. Suggested values range from 100 kΩ–1 MΩ. The resistor is not required if the output is unused.

If a large output capacitance is used, a false logic "HIGH" can be generated when V_{IN} ≈1.3V. In this case, the error output becomes a high impedance, causing the voltage at the error output to rise to its pull-up value. If the pull-up resistor is connected to V_{OUT}, the error output can rise to 1.2V (which is a logic "HIGH" signal *incorrectly* signifying the output is in regulation).

The user may wish to divide down the error flag voltage using equal-value resistors (10 kΩ suggested) to ensure a low-level logic signal during any fault condition, while still allowing a valid high logic level during normal operation.

AUXILIARY COMPARATOR

The LP2960 contains an auxiliary comparator whose inverting input is connected to the 1.23V reference. The auxiliary comparator has an open-collector output whose electrical characteristics are similar to the dropout detection comparator. The non-inverting input and output are brought out for external connections.

SHUTDOWN INPUT

A logic-level signal will shut off the regulator output when a "LOW" (< 1.2V) is applied to the Shutdown input.

To prevent possible mis-operation, the Shutdown input must be actively terminated. If the input is driven from open-collector logic, a pull-up resistor (20 kΩ–100 kΩ recommended) should be connected from the Shutdown input to the regulator input.

If the Shutdown input is driven from a source which actively pulls low and high (like an op-amp), the pull-up resistor is not required, but may be used.

If the Shutdown input is to be unused, the cost of the pull-up resistor can be saved by tying the Shutdown input directly to the regulator input.

IMPORTANT: Since the Absolute Maximum Ratings state that the Shutdown input can not go more than 0.3V below ground, the reverse-battery protection feature which protects the regulator input is sacrificed if the Shutdown input is tied directly to the regulator input.

If reverse-battery protection is required in an application, *the pull-up resistor between the Shutdown input and the regulator input must be used*.

GROUND CONNECTIONS

The pins designated GND (see Connection Diagram) must be connected to the high-current ground point in the circuit.

The GND pins are electrically connected (through the lead frame) to the die substrate, making them ideal for conducting ground current or heat (see HEATSINKING).

The surface-mount (D) package also has an Analog Ground pin, which is the ground point on the die for the regulator reference circuitry.

Along with the Sense pin, the availability of the Analog Ground pin allows the designer the ability to use "remote" sensing and eliminate output voltage errors due to IR drops occurring along PC board traces.

IMPORTANT: The Analog Ground pin must be connected to circuit ground at some point for the regulator to operate.

If remote sensing is not needed, the Analog Ground pin can simply be pin-strapped to the adjacent GND pin.

HEATSINKING

A heatsink may be required with the LP2960 depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under Absolute Maximum Ratings.

To determine if a heatsink is required, the power dissipated by the regulator, P_D, must be calculated.

The figure below shows the voltages and currents which are present in the circuit, as well as the formula for calculating the power dissipated in the regulator:

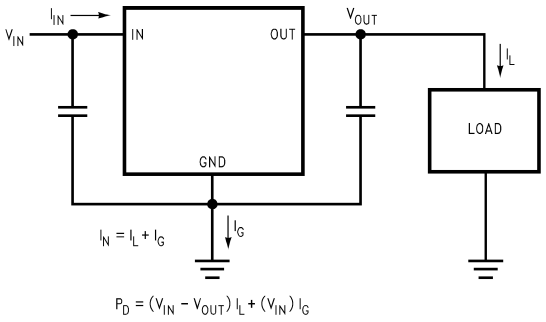


Figure 27. Power Dissipation Diagram

The next parameter which must be calculated is the maximum allowable temperature rise, T_R (max). This is calculated by using the formula:

$$T_R \text{ (max)} = T_J \text{ (max)} - T_A \text{ (max}$$

where

- T_J (max) is the maximum allowable junction temperature, which is 125°C for commercial grade parts
- T_A (max) is the maximum ambient temperature which will be encountered in the application) (2)

Using the calculated values for T_R (max) and P_D, the maximum allowable value for the junction-to-ambient thermal resistance, $\theta_{(J-A)}$, can now be found:

$$\theta_{(J-A)} = T_R \text{ (max)}/P_D \quad (3)$$

The heatsink for the LP2960 is made using the PC board copper, with the heat generated on the die being conducted through the lead frame and out to the pins which are soldered to the PC board.

The GND pins are the only ones capable of conducting any significant amount of heat, as they are internally attached to the lead frame on which the die is mounted.

The figure below shows recommended copper foil patterns to be used for heatsinking the DIP and Surface Mount (SOIC) packages:

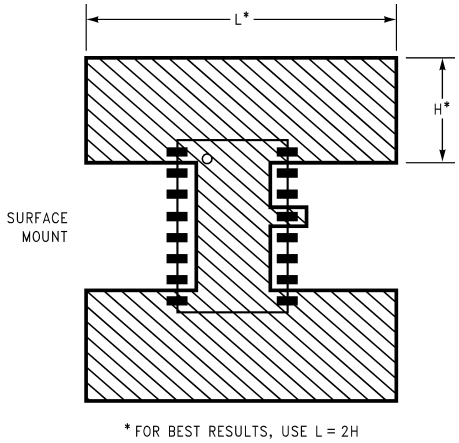


Figure 28. Heat Sink Foil Patterns

The table below shows measured values of $\theta_{(J-A)}$ for a PC board with 1 ounce copper weight:

Package	L (in.)	H (in.)	θ_{J-A}(°C/W)
DIP	1	0.5	50
	2	0.2	52
Surface Mount SOIC	1	0.5	72
	2	0.2	74

As the heat must transfer from the copper to the surrounding air, best results (lowest θ_{J-A}) will be obtained by using a *surface* copper layer with the solder resist opened up over the heatsink area.

If an *internal* copper layer of a multi-layer board is used for heatsinking, the board material acts as an insulator, inhibiting heat transfer and increasing θ_{J-A}.

As with any heatsink, increasing the airflow across the board will significantly improve the heat transfer.

Typical Applications

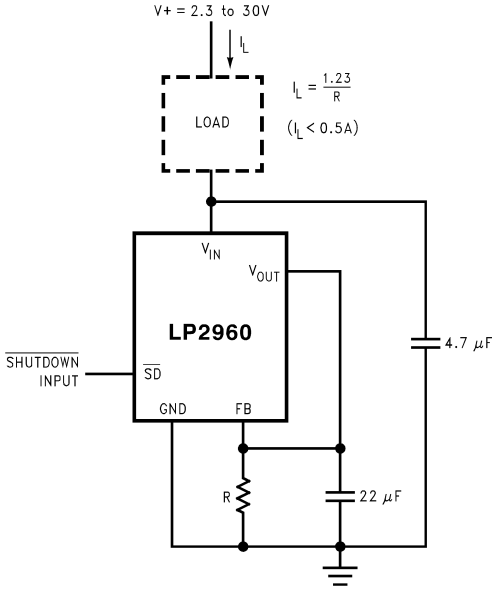
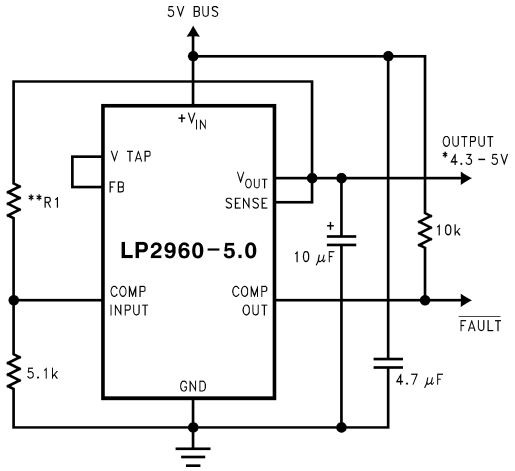
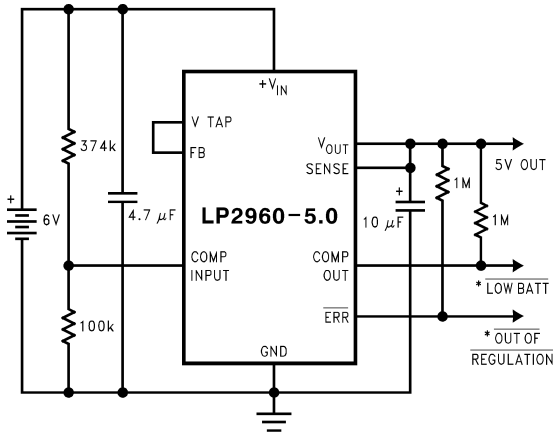


Figure 29. Low T.C. Current Sink



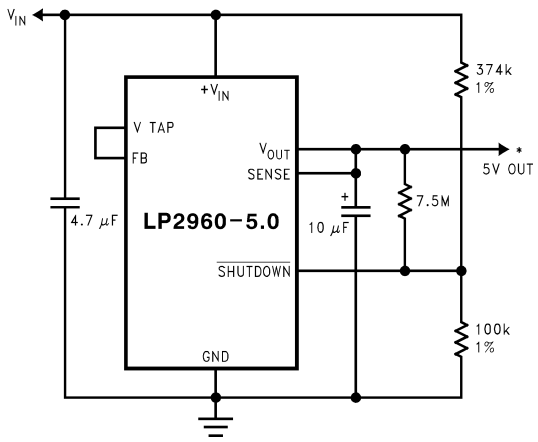
*Output voltage equals $+V_{IN}$ minus dropout voltage, which varies with output current. Current limits at a maximum of 1000 mA (typical).
**Select R1 so that the comparator input voltage is 1.23V at the output voltage which corresponds to the desired fault current value.

Figure 30. 5V Bus Current Limiter with Load Fault Indicator



*Connect to Logic or µP control inputs.
LOW BATT flag warns the user that the battery has discharged down to about 5.8V, giving the user time to recharge the battery or power-down some hardware with high power requirements. The output is still in regulation at this time. OUT OF REGULATION flag indicates when the battery is almost completely discharged, and can be used to initiate a power-down sequence.

Figure 31. 5V Regulator with Error Flags for LOW BATTERY and OUT OF REGULATION



*Turns ON at V_{IN} = 5.87V
Turns OFF at V_{IN} = 5.64V
(for component values shown)

Figure 32. 5V Regulator with Snap-ON/Snap-OFF Feature and Hysteresis

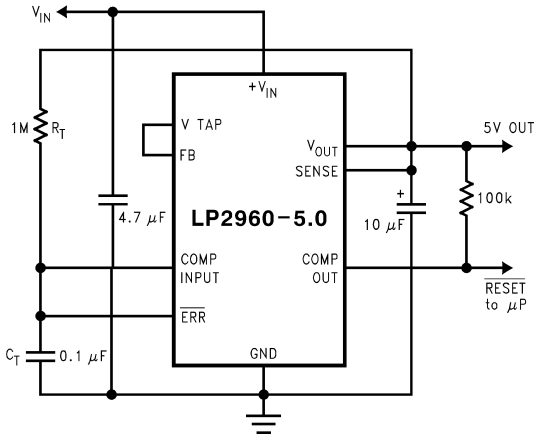
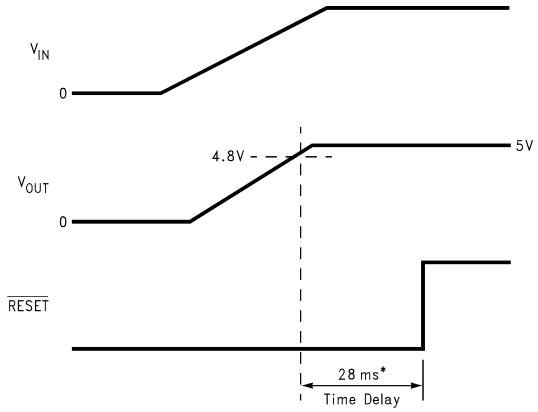


Figure 33. 5V Regulator with Timed Power-On Reset



*R_T = 1 Meg, C_T = 0.1 μF

Figure 34. Timing Diagram for Timed Power-On Reset

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2960AIMX-5.0/NOPB	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LP2960AIM -5.0	Samples
LP2960IM-5.0/NOPB	ACTIVE	SOIC	D	16	48	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LP2960IM -5.0	Samples
LP2960IMX-3.3/NOPB	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LP2960IM -3.3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

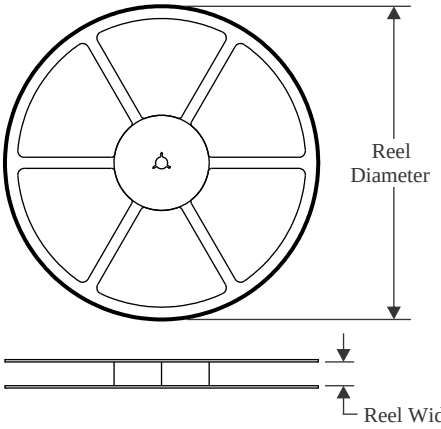
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

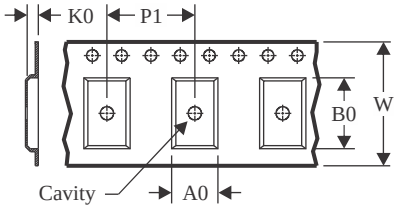
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

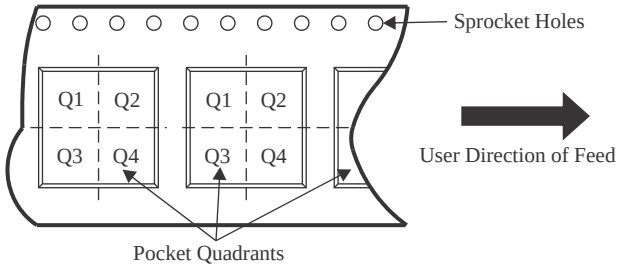


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

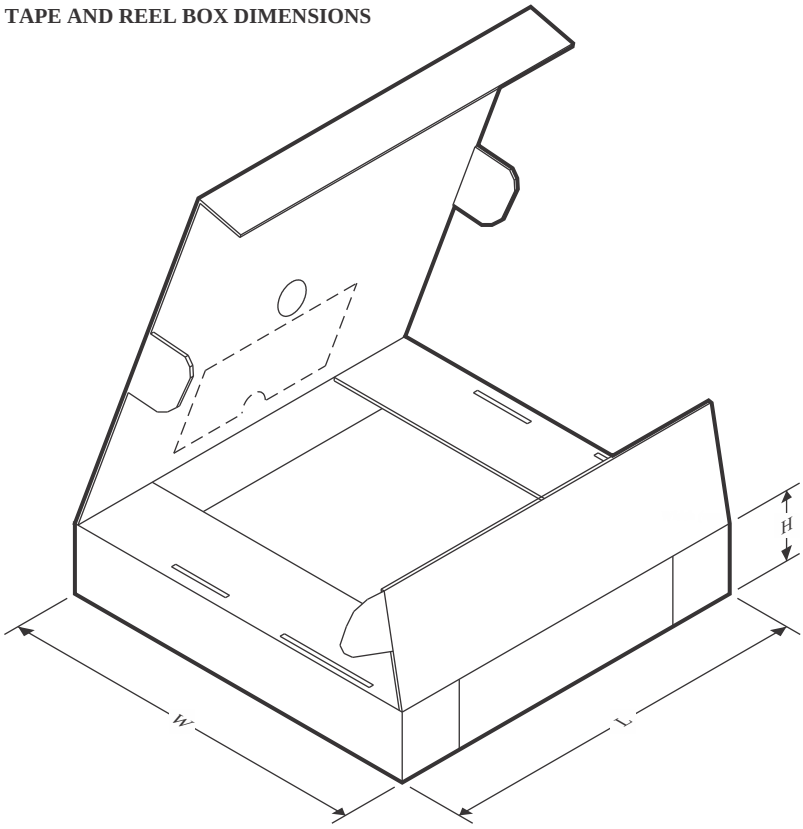
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2960AIMX-5.0/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1
LP2960IMX-3.3/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

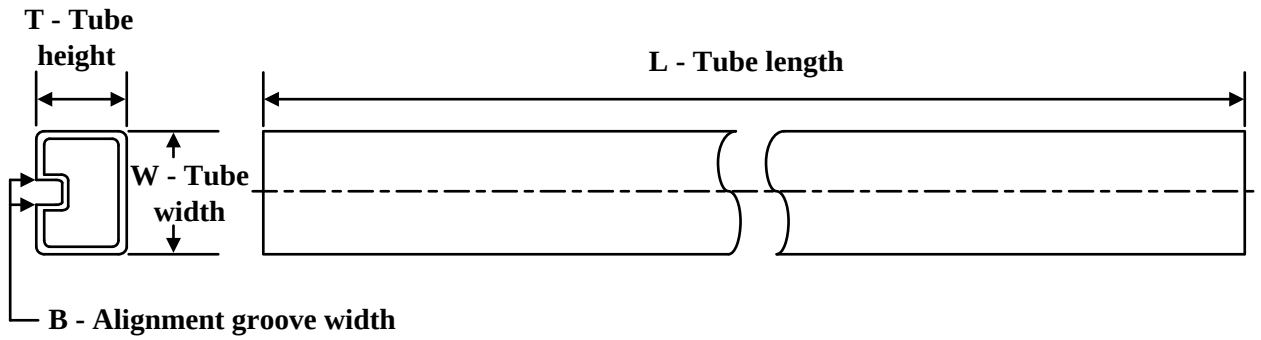
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2960AIMX-5.0/NOPB	SOIC	D	16	2500	356.0	356.0	36.0
LP2960IMX-3.3/NOPB	SOIC	D	16	2500	356.0	356.0	36.0

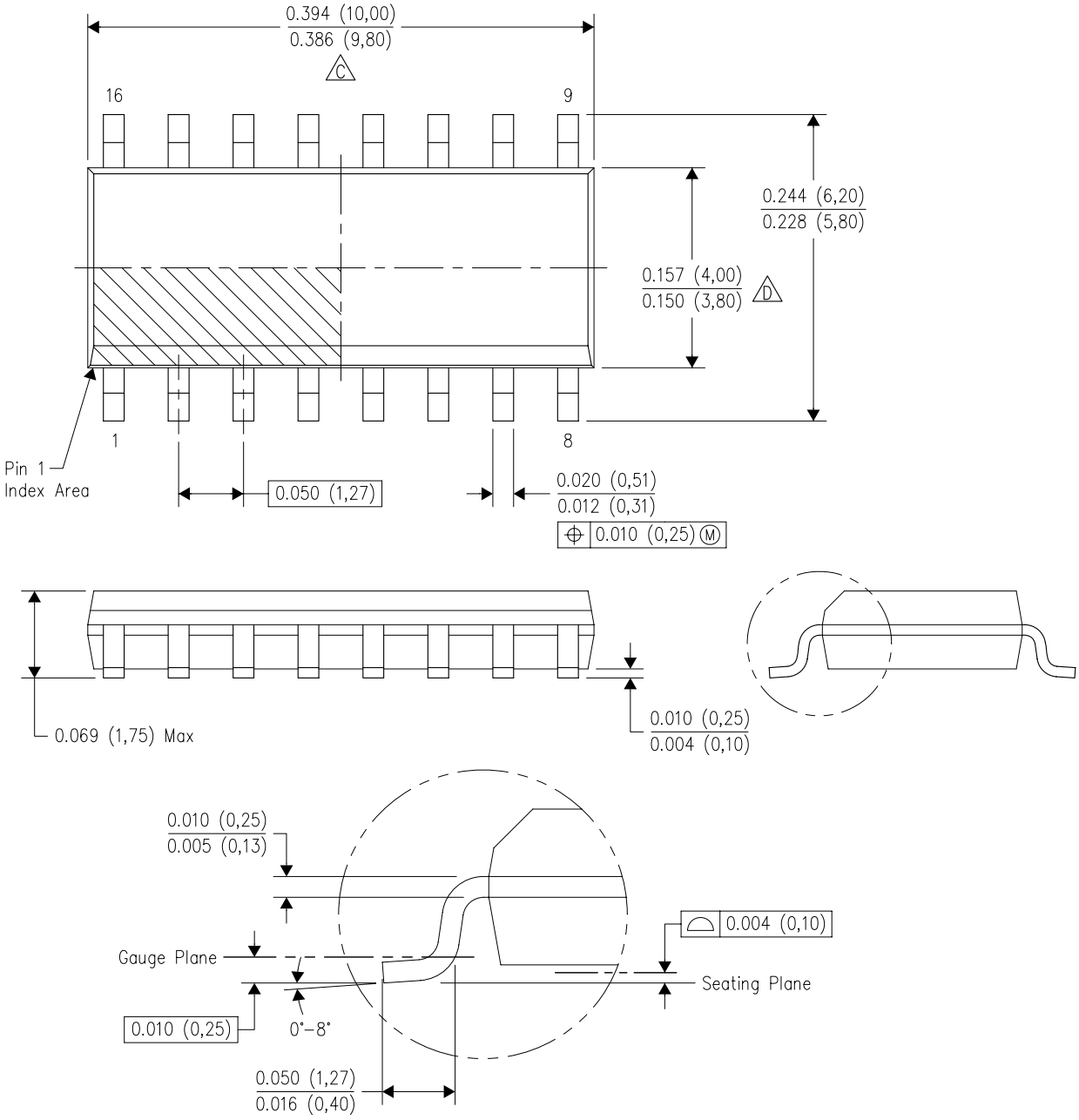
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP2960IM-5.0/NOPB	D	SOIC	16	48	495	8	4064	3.05

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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