LP5899-Q1 Automotive SPI-Compatible Connectivity for LP589x-Q1 Device Family

1 Features

- AEC-Q100 qualified for automotive applications
  - Grade 1: –40°C to 125°C ambient temperature
  - Device HBM classification level H3A
  - Device CDM classification level C5
- Operating voltage V_{CC} range: 2.5V to 5.5V
- SPI peripheral
  - Data transfer rate up to 20MHz
  - Support multiple peripherals with one controller
- Continuous Clock Serial Interface (CCSI) Controller and Peripheral
  - Data transfer rate up to 20MHz
  - Programmable clock jitter for EMI enhancement
- Diagnostics
  - Open-drain FAULT pin
  - SPI communication loss detection
  - CRC for SPI communication
  - CCSI data integrity
- Data ready interrupt for availability of data

2 Applications

- SPI compatible connectivity for LP5891-Q1 and LP5892-Q1

3 Description

The LP5899-Q1 SPI-compatible connectivity enables LP589x-Q1 device family to be controlled using a standard SPI controller. The device features an internal oscillator to generate the continuous clock required by the LP589x-Q1 device family. Jitter can be added to the continuous clock for EMI enhancement. The transmitted data is aligned to the continuous clock to maintain the timing requirements of the CCSI interface.

LP5899-Q1 incorporates reporting of faults in both the LP589x-Q1 daisy chain and LP5899-Q1 internal. Data transmission of register and VSYNC commands to the LP589x-Q1 daisy chain is CRC protected by LP5899-Q1. In addition, the data line is guarded by LP5899-Q1 for stuck-at faults.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LP5899-Q1	SOT-23-THN (14)	4.20mm x 2.00mm
	WSON (12) Wettable flank	3.00mm x 3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value.

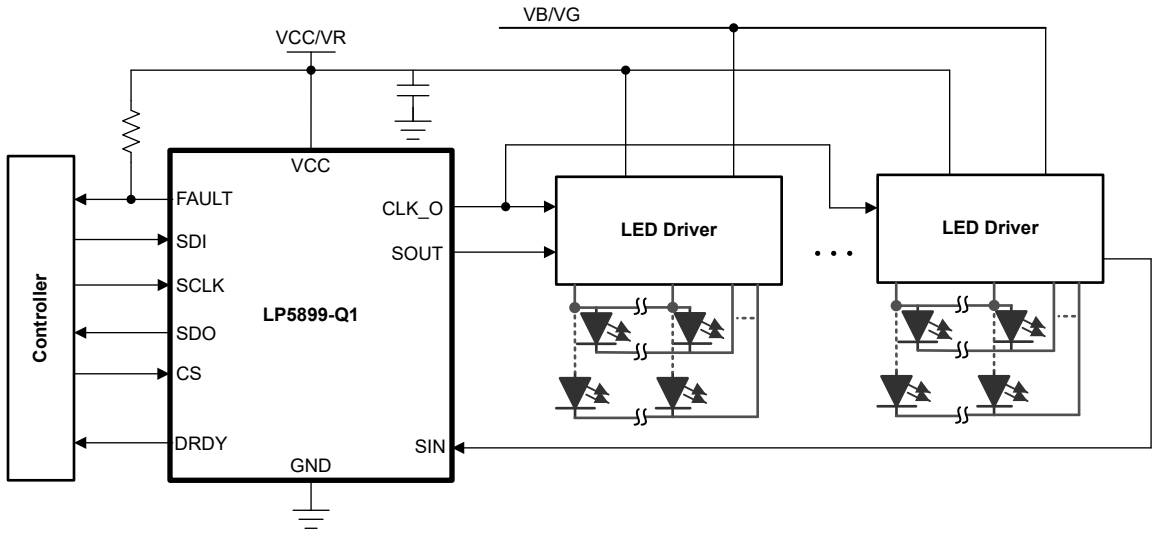

Figure 3-1. Typical Application Diagram

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4 Device Comparison

PART NUMBER	MATERIAL	PACKAGE
LP5899-Q1	LP5899QDYYRQ1	SOT-23-THN (14)
	LP5899QDRRRQ1	WSON (12)

5 Pin Configuration and Functions

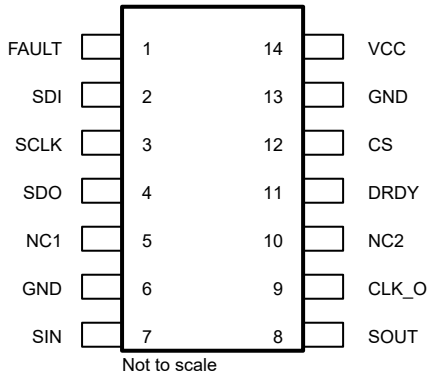


Figure 5-1. LP5899-Q1 DYY Package 14-pin SOT-23-THN Top View

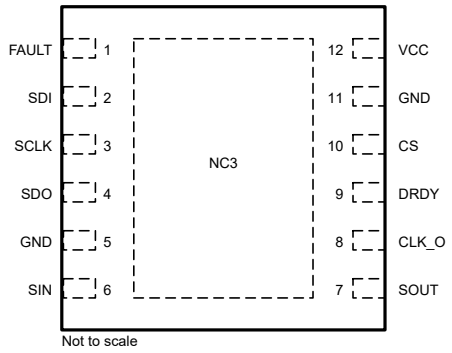


Figure 5-2. LP5899-Q1 DRR Package 12-pin WSON with Exposed Thermal Pad Top View

Table 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	DYY NO.	DRR NO.		
FAULT	1	1	O	Fault indicator pin
SDI	2	2	I	SPI Serial Data Input
SCLK	3	3	I	SPI Serial Clock Input
SDO	4	4	O	SPI Serial Data Output
NC1	5	-	NC	No connection. Can be used for signal routing.
GND	6	5	G	Ground pin (must connect to Ground)
SIN	7	6	I	CCSI Serial Data Input
SOUT	8	7	O	CCSI Serial Data Output
CLK_O	9	8	O	CCSI Serial Clock Output
NC2	10	-	NC	No connection. Can be used for signal routing.
DRDY	11	9	O	Data ready interrupt.
CS	12	10	I	SPI Chip Select
GND	13	11	G	Ground pin (must connect to Ground)
VCC	14	12	P	VCC Power Supply Input
NC3	-	Exposed Pad	NC	No connection. Need to be electrically isolated from any signal except Ground.

(1) I = Input, O = Output, G = Ground, P = Power, NC = Not Connected.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage on pins	VCC	–0.3	6	V
	SDI, SCLK, CS, SIN	–0.3	VCC + 0.3	V
	SDO, DRDY, SOUT, CLK_O	–0.3	VCC + 0.3	V
	FAULT	–0.3	6	V
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Thermal Information

THERMAL METRIC(1)		DRR (SON)	DYY (SOT)	UNIT
		12 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.6	127.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.1	58.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.1	54.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.3	3.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	36.9	54.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	12.7		°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.5		5.5	V
Voltage on pins	SDI, SCLK, CS, SIN	0		V_{CC}	V
	SDO, DRDY, SOUT, CLK_O	0		V_{CC}	V
	FAULT	0		V_{CC}	V
f_{SCLK}	SPI clock frequency			20	MHz
C_{VCC}	V_{CC} decoupling capacitor	100			nF
T_A	Ambient temperature	–40		125	°C

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted), 2.5V < V_{CC} < 5.5V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply					

over operating free-air temperature range (unless otherwise noted), 2.5V < V_{CC} < 5.5V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Device supply voltage				5.5	V
V_{UVR}	Undervoltage restart	V_{CC} rising			2.3	V
V_{UVF}	Undervoltage shutdown	V_{CC} falling	2			V
$V_{UV,HYS}$	Undervoltage shutdown hysteresis			0.12		V
I_{CC}	Device supply current	V_{CC} = 3.3V, CCSI_DATA_RATE[3:0] = 4b'1110		3.6		mA
Oscillator						
f_{OSC}	Internal Oscillator frequency		–3%	40	3%	MHz
$t_{WD,OSC}$	Internal Oscillator Watchdog		0.66	1.45	2.48	µs
Digital IO						
V_{IH}	High level input voltage (SCLK, SDI, CS, SIN)		1.05			V
V_{IL}	Low level input voltage (SCLK, SDI, CS, SIN)				0.45	V
V_{OH}	High level output voltage (SOUT, CLK_O, SDO, DRDY)	I_{OH} = –3mA	VCC – 0.4		VCC	V
V_{OL}	Low level output voltage (SOUT, CLK_O, SDO, DRDY)	I_{OL} = 3mA			0.4	V
I_{LOGIC}	Logic pin current (SCLK, SDI, CS, SIN)	SCLK/SDI/CS/SIN = V_{CC} or GND	–1		1	µA
FAULT						
$I_{PD,FAULT}$	FAULT pull-down current capability	V_{FAULT} = 0.4V	22	59		mA
$I_{LKG,FAULT}$	FAULT leakage current				1	µA
$V_{OH,FAULT}$	High level output voltage (FAULT)	Voltage applied to FAULT pin through external pullup resistor			VCC	V
$V_{OL,FAULT}$	Low level output voltage (FAULT)	I_{OL} = 3mA, must be limited by external pullup resistor			0.4	V
Diagnostics						
$t_{WD,SIN}$	SIN Watchdog			5		ms

6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$f_{SCLK,NORMAL}$	SCLK clock frequency in NORMAL state				20	MHz
$f_{SCLK,INIT}$	SCLK clock frequency in INIT state				5	MHz
$t_{LEAD,CS}$	Delay time, first SCLK rising edge after CS falling edge		15			ns
$t_{LAG,CS}$	Delay time, CS rising edge after final SCLK falling edge		5			ns
$t_{SU,SDI}$	SDI input data setup time before SCLK rising egde		10			ns
$t_{HD,SDI}$	SDI input data hold time after SCLK rising edge		5			ns
$t_{wh,CS}$	Pulse duration, CS high		40			ns
$t_{SU,SIN}$	SIN input data setup time before CLK_O rising edge		10			ns
$t_{HD,SIN}$	SIN input data hold time after CLK_O rising edge		2			ns

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{ACC,CS}$	Propagation delay time, CS falling edge to SDO driven				50	ns
$t_{DIS,CS}$	Propagation delay time, CS rising edge to SDO high impedance				75	ns
$t_{VALID,SDO}$	Propagation delay time, SCLK falling edge to valid new SDO				22	ns
DC_{CLK_O}	Duty cycle CLK_O	CCSI_DATA_RATE[3:0] = 4b'1110		33.33%		
		CCSI_DATA_RATE[3:0] = 4b'1100		40%		
		CCSI_DATA_RATE[3:0] = Others		50%		
$t_{r,SOUT}$	Rise time (SOUT) - from 10% of V_{CC} to 90% of V_{CC}	V_{CC} = 3.3V, C_{SOUT} = 30pF		2	10	ns
$t_{f,SOUT}$	Fall time (SOUT) - from 90% of V_{CC} to 10% of V_{CC}	V_{CC} = 3.3V, C_{SOUT} = 30pF		2	10	ns
f_{CLK_O}	CLK_O output frequency. The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.	V_{CC} = 3.3V, C_{CLK_O} = 30pF			20.6	MHz

6.8 Timing Diagrams

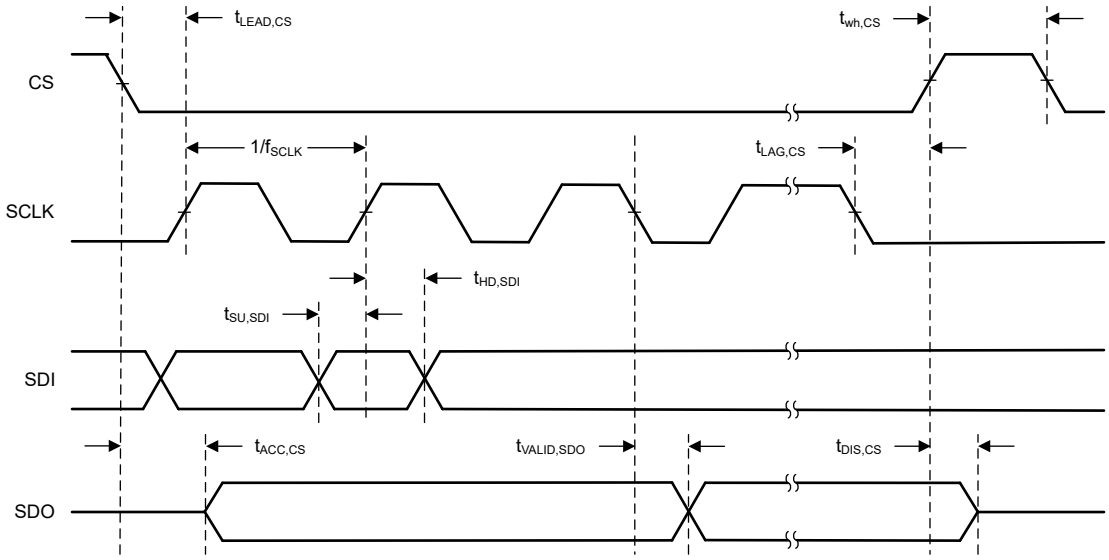


Figure 6-1. SPI Peripheral Timing Diagram

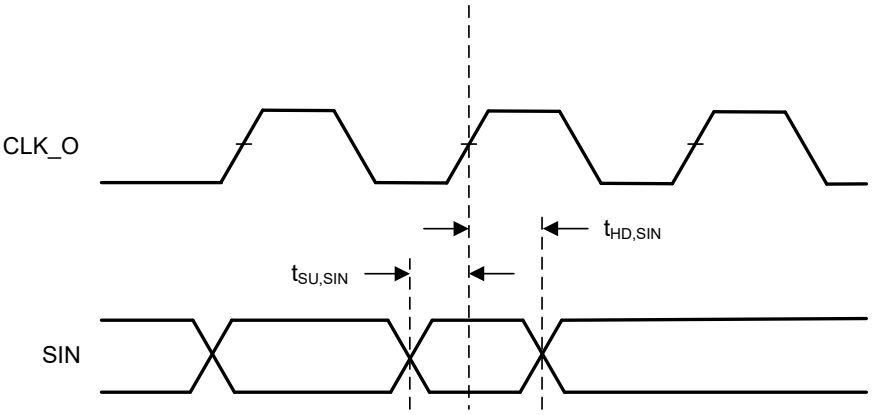


Figure 6-2. CCSI Peripheral Timing Diagram

6.9 Typical Characteristics

At T_A = 25°C and V_{CC} = 3.3V, unless otherwise noted.

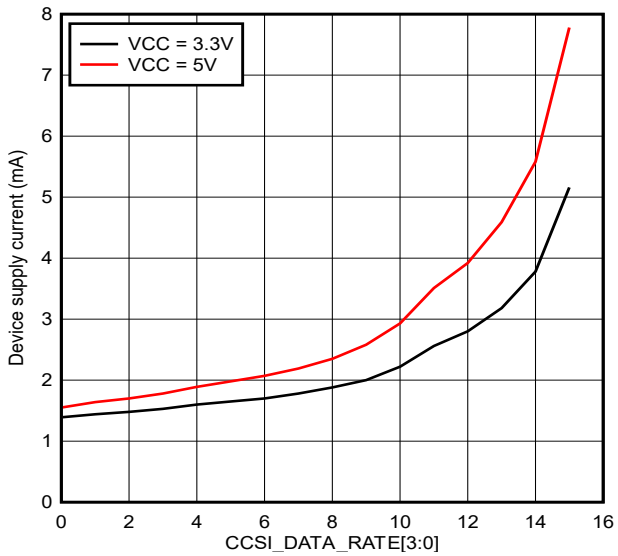


Figure 6-3. Device supply current vs CCSI_DATA_RATE

7 Detailed Description

7.1 Overview

The LP5899-Q1 is an SPI-compatible connectivity between an SPI and a Continuous Clock Serial Interface (CCSI). The device can drive any number of cascaded LED drivers of the LP589x-Q1 family. The maximum number of cascaded devices is limited by the LED driver.

The LP5899-Q1 uses an internal oscillator and clock divider to provide a programmable continuous clock frequency for the CCSI. Data words received by the SPI peripheral are forwarded by the CCSI controller where the data is aligned to the continuous clock. Data words received by the CCSI peripheral can be stored by the LP5899-Q1 and read by the Controller using SPI. The continuous clock incorporates a programmable pseudo-random jitter (spread spectrum) feature to reduce EMI emissions.

The LP5899-Q1 automatically inserts the required start bit and check bits when forwarding the data words received by SPI peripheral. For data words received by the CCSI peripheral, the LP5899-Q1 automatically analyses the check bits and reports when an error is detected. When the data words are stored for reading by SPI, the start bit and check bits are removed from the data string.

The LP5899-Q1 automatically inserts the required end byte when forwarding the data words received by SPI peripheral to make sure that different SPI commands are recognized as different CCSI commands. When the data words are stored for reading by SPI, the end byte is removed from the data string.

7.2 Functional Block Diagram

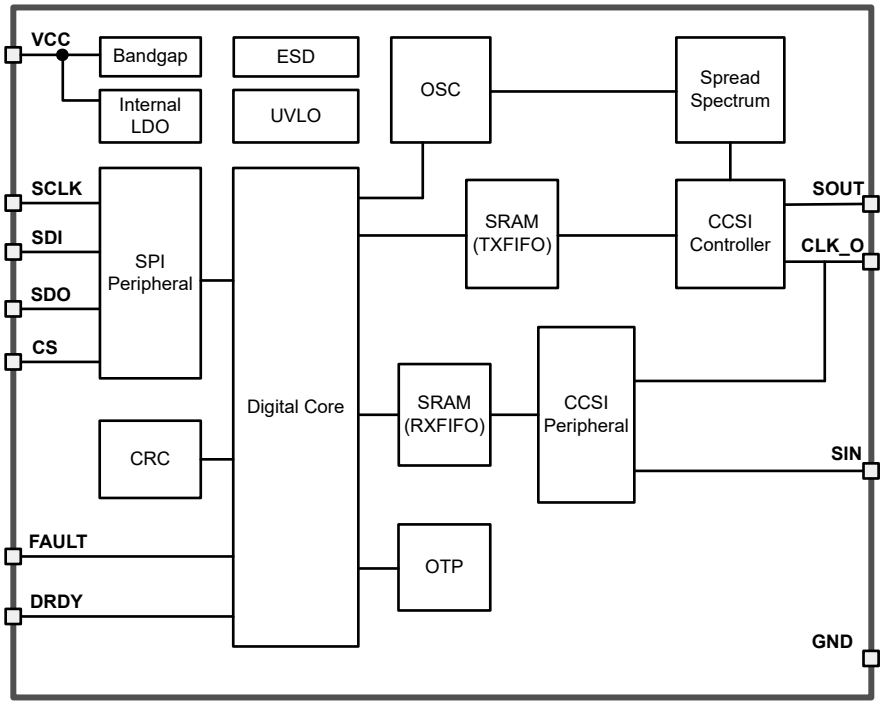


Figure 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Internal Oscillator and Clocks

7.3.1.1 System Clock

The LP5899-Q1 has an internal oscillator which provides a 40MHz system clock for the device. The system clock is used to operate the digital logic.

Internal Oscillator Watchdog

The internal oscillator watchdog timer ($t_{WD,OSC}$) is automatically enabled upon exit from POR. If the internal oscillator stops toggling for more than $t_{WD,OSC}$, the watchdog expires and holds the logic in reset (POR) until the oscillator begins toggling again. The internal oscillator is used as the system clock.

7.3.1.2 Continuous Clock Serial Interface (CCSI) Clock

The clock for transmitting data by the CCSI controller is derived from the system clock. There are 16 divider options available (CCSI_DATA_RATE in register CCSICTRL) to achieve the desired clock frequency for the daisy chain of LED drivers.

The CCSI clock can be modulated by a programmable digital spread spectrum to improve the system level EMI performance. Field CCSI_SS_CLKO in register CCSICTRL determines if the spread spectrum is enabled. When CCSI_DATA_RATE * CCSI_SS_CLKO * 2 is smaller than 120kBit/s, a modulation frequency of 30kHz is used. Otherwise the modulation frequency is 120kHz. When CCSI_DATA_RATE in register CCSICTRL is set to 4b'1111 or 4b'1110, spread spectrum is not recommended to be enabled.

7.3.2 Continuous Clock Serial Interface (CCSI)

The continuous clock series interface (CCSI) provides access to the programmable functions and registers of the LED drivers that are connected in a daisy chain between the CCSI controller and CCSI peripheral. The serial data output (SOUT) and serial clock output (CLK_O) are used for the CCSI controller. When the CCSI controller is not transmitting, the SOUT is set to logic HIGH, while the CLK_O remains active and continuous. The continuous clock starts after the device powers up. To start transmission by the CCSI controller, the device needs to be in NORMAL state and the flag FLAG_POR has to be cleared.

The CCSI peripheral consists of one wire, which is the serial data input (SIN). The data is shifted in using the same clock source as CLK_O.

7.3.2.1 Command Format

The command format is viewed from the CCSI peripheral side. Figure 7-2 defines the format of the command transmission. There are three states in one command:

- **IDLE:** CLK_O is always active and continuous. SIN is always HIGH.
- **START:** SIN changes from HIGH to LOW after the IDLE state.
- **DATA:**
  - **Head_byte:** The command identifier, contains one 16-bit data and one check bit.
  - **Data_bytes_N-1:** Each data-byte contains 3 × 17-bit data, each 17-bit data contains one 16-bit data word and one check bit.
- **END:** The device recognizes continuous 18-bit HIGH on SIN, and then returns to IDLE state.
- **CHECK BIT:** The check bit (17^{th} bit) value is the *NOT* of 16^{th} bit value to avoid continuous 18-bit HIGH (to distinguish with END).

The IDLE state is not necessary, which means the START state of the next command can connect to the END state of the current command.

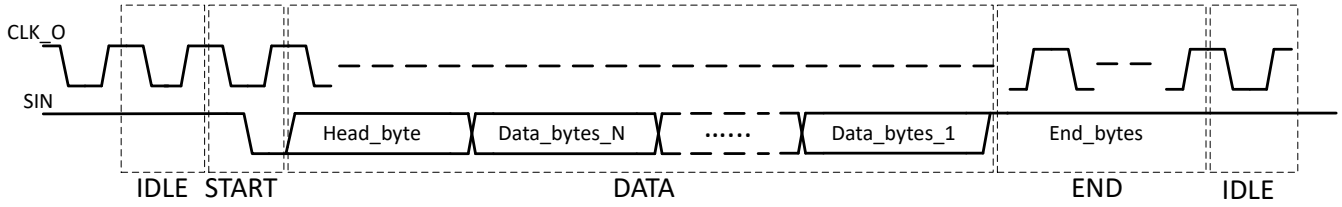


Figure 7-2. Command Format

7.3.2.2 Command Recognition and Synchronization

Two different CCSI commands require at least one END byte in between the commands to be able to be recognized as separate commands. The LP5899-Q1 automatically inserts one END byte after all the data from one SPI command has been transmitted. However, for certain CCSI commands, the LED drivers add data to the data stream. In this case, one END byte during transmission is not sufficient to distinguish the two CCSI commands by the CCSI peripheral. Without sufficient END bytes, the CCSI controller and CCSI peripheral get out of synchronization. The synchronization is required for several actions. For example, to determine if the received data needs to be stored on the RXFIFO or if a CRC needs to be calculated over the received data and compared to the CRC over the transmitted data. In case the synchronization is lost, the SPI command SOFTRESET_CRC can be used to bring the CCSI controller and peripheral back in sync. The SPI controller is responsible there are sufficient END bytes between CCSI commands to keep the synchronization by using a dedicated SPI command that inserts extra END bytes.

7.3.2.3 CCSI Command Queue

The CCSI controller has the ability to queue multiple SPI commands. This means that when the CCSI controller is still transmitting, a new SPI forward command can be received by the SPI peripheral. This new command is automatically transmitted after the old command is finished transmitting. An example is depicted in Figure 7-3. Note that in this figure every data word is 16 bits. That means that when the width of the block is larger, the clock frequency is lower. In this example the CCSI frequency is lower than the SPI frequency.

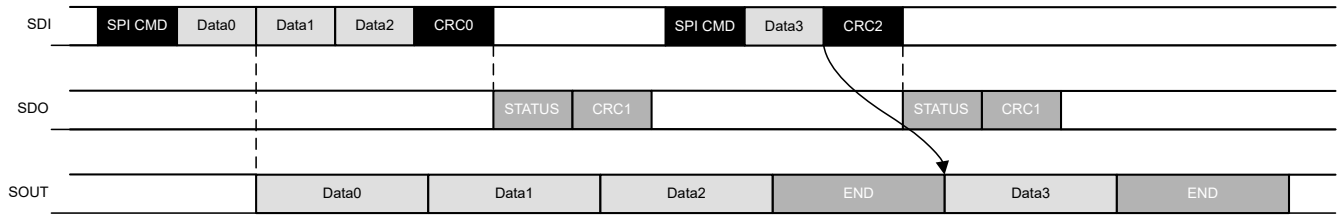


Figure 7-3. Example of queuing CCSI commands

7.3.2.4 CCSI Start Bit and Check Bits Insertion and Removal

The LP5899-Q1 automatically inserts and removes the start bit and check bits that are required for the CCSI. This means that those bits do not have to be inserted in the SPI data words when transmitted by the controller. In addition, when reading back data using SPI, the start bit and check bits are removed. This results in standard 16 bits SPI data words. An example of this feature is depicted in Figure 7-4. In the remaining part of this document, the start bit and check bits are not explicitly shown anymore.

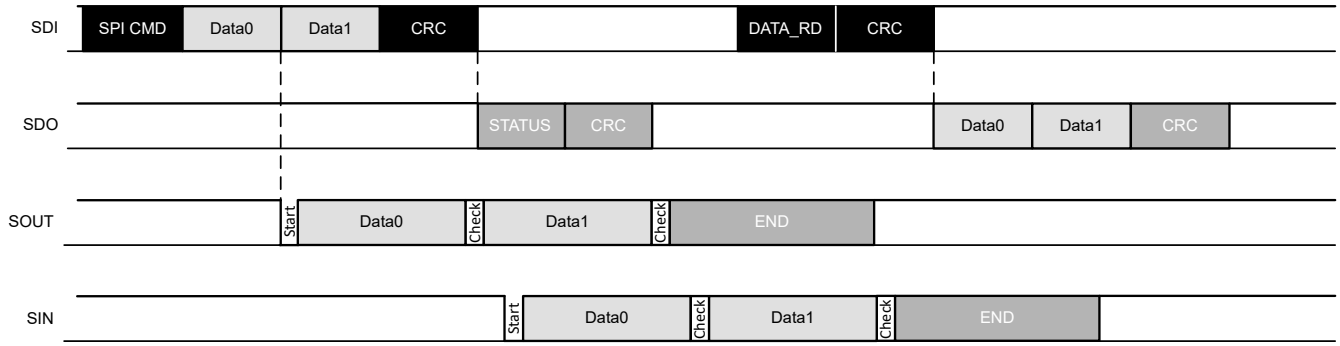


Figure 7-4. Example of insertion and removal of start bit and check bits

7.3.3 FIFO

The LP5899-Q1 has both a transmit and receive FIFO. The naming of the FIFOs are viewed from the Continuous Clock Serial Interface (CCSI). That means the transmit FIFO (TXFIFO) is the data that was received by the SPI peripheral and transmitted by the CCSI controller. The receive FIFO (RXFIFO) is the data received by the CCSI peripheral which can be read by the controller via SPI peripheral.

Both FIFOs are 16-bit-wide first-in-first-out memory buffers. The FIFOs are used to store data words to fullfil the timing requirements while the data is crossing between the SPI clock domain and CCSI clock domain. The TXFIFO holds the data during the crossover from the SPI clock to the CCSI clock domain. The RXFIFO holds the data during the crossover from the CCSI clock domain to the SPI clock domain.

When the SPI clock domain runs at a higher frequency than the CCSI clock domain, the TXFIFO stores data already received by the SPI peripheral which has not been transmitted yet by the CCSI controller. A counter (TXFFST) keeps track of the number of words currently stored in the TXFIFO. The example where the SPI peripheral runs at a higher clock frequency than the CCSI controller is depicted in Figure 7-5. Note that in this figure every data word is 16 bits. That means that when the width of the block is larger, the clock frequency is lower.

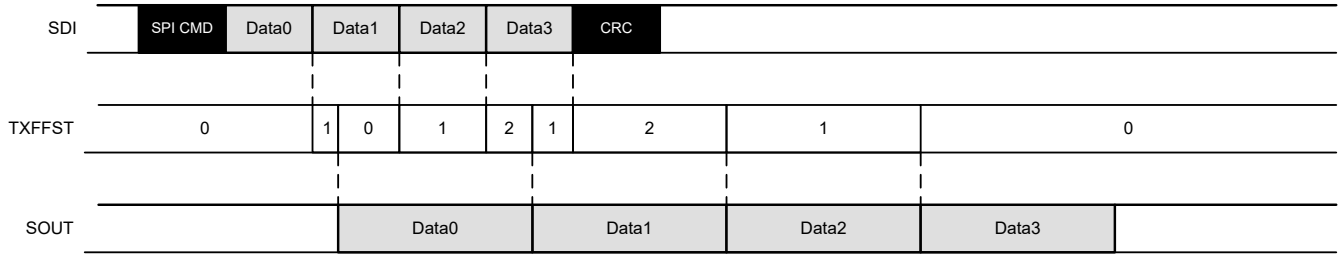


Figure 7-5. Example of SPI peripheral running at higher frequency than CCSI controller

When the SPI peripheral runs at a lower clock frequency than the CCSI controller, the TXFIFO is used to first store a number of data words received by the SPI peripheral before the transmission by the CCSI controller starts. Following this method, the data stream on the CCSI can be made continuous without requiring the continuous clock to stop because the data word was not received yet by the SPI peripheral. An example of this situation is depicted in Figure 7-6.

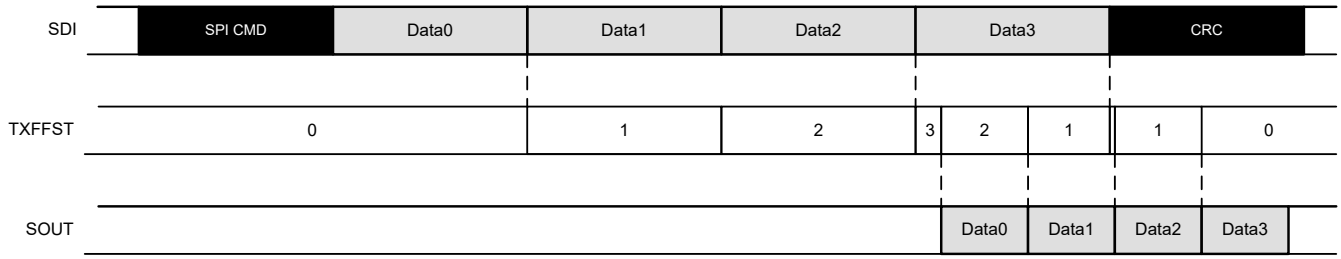


Figure 7-6. Example of SPI peripheral running at lower frequency than CCSI controller

For the RXFIFO, the CCSI peripheral receives the data and stores them on the RXFIFO. The SPI peripheral reads the data from the RXFIFO and transmits them to the SPI controller. Also for the RXFIFO a counter (RXFFST) exists to keep track of the number of data words currently stored.

Note that when an END byte is received, the storage stops. The END byte itself is not stored on the RXFIFO. Also the START bit and CHECK bits are not stored.

7.3.3.1 FIFO level and Data Ready (DRDY) Interrupt

The TXFIFO level (TXFFLVL) controls the start of the transmission of the CCSI controller for SPI forward commands that are independent of the SPI CRC. With correct setting of the FIFO level, FIFO overflow and underflow can be prevented. The setting is dependent on the difference between the SPI clock frequency and CCSI clock frequency, the accuracy of the clock provided to the SPI peripheral, accuracy of the clock of the CCSI controller, and the maximum length of data that is being forwarded.

The RXFIFO level (RXFFLVL) controls the Data Ready (DRDY) interrupt. When the number of data words on the RXFIFO exceed the RXFFLVL, the DRDY pin becomes logic LOW. This DRDY pin remains logic LOW until there are no more words on the RXFIFO. The RXFFLVL setting has the same dependencies as the TXFFLVL except the maximum length of data that is being forwarded is replaced by the maximum number of data words that is received by the CCSI peripheral. An example of the DRDY pin's behavior is depicted in Figure 7-7.

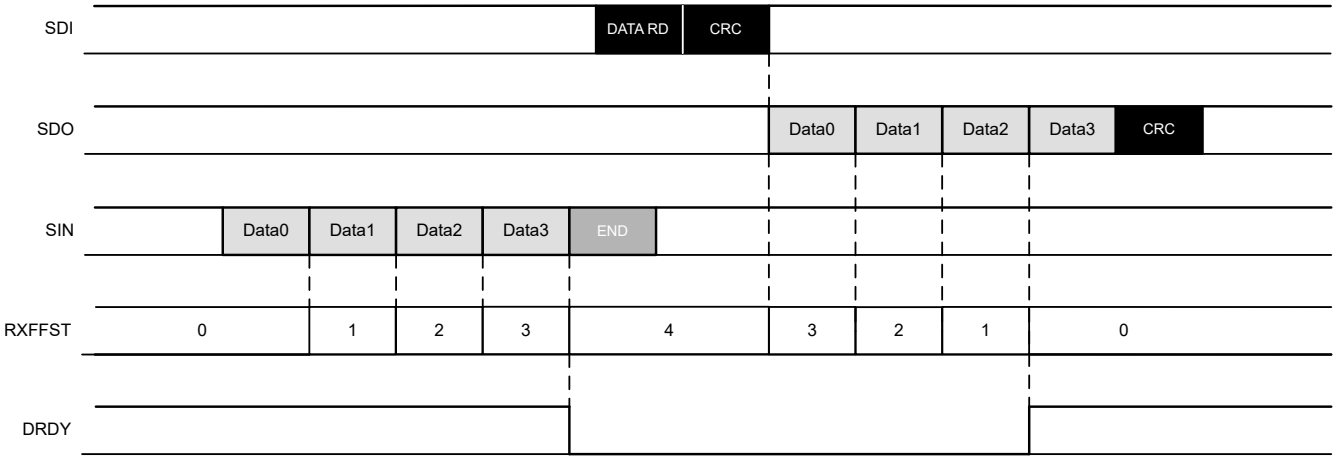


Figure 7-7. Example of DRDY pin with RXFFLVL register set to 3

The DRDY pin also becomes logic LOW when an END byte is detected and the number of words on the RXFIFO has not reached the RXFFLVL yet.

7.3.3.2 FIFO Clearance

To stop an ongoing CCSI transmission, the TXFIFO can be cleared by bit TXFFCLR in register TXFFLVL. This resets the TXFIFO counter (TXFFST) to 0. All the commands in the queue are cleared. The CCSI controller automatically inserts an END byte to reset the LED drivers. The CCSI peripheral continues to work as normal. The TXFFCLR bit automatically returns to 0.

The data on the RXFIFO can be cleared by bit RXFFCLR in register RXFFLVL. This resets the RXFIFO counter (RXFFST) to 0. If the CCSI peripheral is receiving data that needs to be stored on the RXFIFO, the storage is stopped for this command. The next CCSI command received by the CCSI peripheral follows the original request of the SPI command. The CCSI controller continues to work as normal. The RXFFCLR bit automatically returns to 0.

7.3.4 Diagnostics

The LP5899-Q1 provides both device internal and device external diagnostics. The device detects failures and reports the status out through the FAULT pin and the status registers. The SPI controller is required to take action to bring the device in a normal operating condition. Faults can be cleared by writing bit CLR_FLAG in the STATUS register. Only the OTP CRC error and Failsafe state flags cannot be cleared by this bit. The CLR_FLAG bit automatically returns to 0. If a fault remains, the error flag is set after the next detection.

7.3.4.1 Undervoltage Lockout

When VCC voltage drops below the UVLO threshold, the device enters Unpowered state. Upon voltage recovery, the device automatically switches to Initialization state with FLAG_POR and FLAG_ERR set to 1. The SPI controller can write 1 to register CLR_FLAG to clear the flags.

7.3.4.2 Oscillator Fault Diagnostics

The internal clock watchdog timer ($t_{WD,OSC}$) is automatically enabled upon exit from POR. If the internal oscillator stops toggling for more than $t_{WD,OSC}$, the watchdog expires and the FAULT pin is pulled low. The fault is latched and when the oscillator begins toggling again, the FLAG_OSC and FLAG_ERR are set to 1. The SPI controller can access the LP5899-Q1 and write 1 to CLR_FLAG to clear the flags.

7.3.4.3 SPI Communications Loss

The LP5899-Q1 monitors the SPI for communication with an internal watchdog timer. The device expects to receive a valid SPI command within the communications loss interval. The timer starts counting when the device enters the Normal state. The timer resets when a valid SPI command is detected. When the watchdog timer overflows, device automatically switches to Failsafe state and sets the DEV_STATE to 0x3 and FLAG_ERR is set to 1. The SPI controller can access the LP5899-Q1 and write 1 to EXIT_FS in register DEVCTRL to set the device to Normal state again when the communication recovers. The watchdog timer is programmable by 2-bit field SPI_WDT_CFG in register SPICTRL. Disabling the watchdog timer by setting SPI_WDT_CFG to 0x3 prevents the device from automatically entering into Failsafe state.

7.3.4.4 SPI Communications Error

7.3.4.4.1 Reset Timer

The LP5899-Q1 monitors the SPI for communication with an internal SPI reset timer. Once an SPI command is started, the timer starts and the device expects the full command (including reading of data) is completed before the timer overflows. The timer starts counting from the first clock pulse on the SCLK pin (with CS pin at active state) when the device is trying to detect the SPI command word. The timer is reset when the device starts to wait for the next SPI command word. If the watchdog timer overflows, the SPI peripheral is reset and starts to wait to receive the next SPI command word. In addition, the FLAG_SPI_TIMEOUT, FLAG_SPI, and FLAG_ERR are set to 1. The SPI controller can access the LP5899-Q1 and write 1 to CLR_FLAG to clear the flags. The SPI reset timer is programmable by 4-bit field SPI_RST_TIMEOUT_CFG in register SPICTRL. TI recommends to enable this timer when the CS pin is always tied to the active state.

7.3.4.4.2 Chip Select (CS) Reset

The SPI peripheral is reset by pulling the CS pin to logic HIGH. This is normally done when the whole SPI command has been completed and the SPI peripheral is waiting for the next command. In case the CS pin is pulled high after the SPI peripheral has received the SPI command word, but before the whole command is received, the FLAG_SPI_CS, FLAG_SPI, and FLAG_ERR are set to 1. The SPI controller can access the LP5899-Q1 and write 1 to CLR_FLAG to clear the flags.

7.3.4.4.3 CRC Error

The CRC word is the final word of a command the SPI controller transmits to make sure the LP5899-Q1 correctly has received all the words from SPI controller. The SPI controller must calculate the CRC value for all words including SPI command word and any data words. The LP5899-Q1 receives all words, calculates the CRC word and compares the calculated CRC word with received CRC word. If two CRC words do not match, the LP5899-Q1 sets FLAG_SPI_CRC and FLAG_ERR to 1. Dependent on the received command, the LP5899-Q1 ignores the command or continues processing the command. The SPI controller can access the device and write 1 to CLR_FLAG to clear the flags. Two different CRC algorithms are supported. The default algorithm is CCITT-FALSE. This can be changed to the CRC-16/XMODEM algorithm using the REG_WR SPI command. After changing the CRC algorithm, the next SPI command uses the new algorithm.

7.3.4.4.4 Register write failure

The CCSICTRL register is prohibted to be written while the CCSI controller is transmitting or CCSI peripheral is receiving. In that way the continuous clock output on CLK_O remains aligned with the data being transmitted on SOUT and received on SIN. When the user tries to write the CCSICTRL register during CCSI controller and/or peripheral activity, the device automatically detects this and sets FLAG_SPI_REG_WRITE to 1. The SPI controller can access the device and write 1 to CLR_FLAG to clear the flag.

7.3.4.5 CCSI Communications Loss

7.3.4.5.1 SIN Stuck-at Diagnostics

The data input (SIN) pin of the CCSI peripheral is monitored. After the CCSI controller starts transmitting (logic high to low transition on SOUT pin), the timer starts counting. If no toggling has been detected on the SIN pin before the timer overflows (after 5 milliseconds), the FLAG_CCSI_SIN, FLAG_CCSI, and FLAG_ERR are set to 1. The SPI controller can access the LP5899-Q1 and write 1 to CLR_FLAG to clear the flags.

When the FLAG_CCSI_SIN is set, the CCSI controller and CCSI peripheral are likely to get out of synchronization. Therefore, TI recommends to perform a SOFTRESET command after this flag has been set.

7.3.4.6 CCSI Communications Error

The CCSI peripheral diagnoses the received data. The check bit detection is checked on all received data while the data integrity is only checked for CCSI commands that did not add or modify data which was transmitted by the CCSI controller.

7.3.4.6.1 CHECK Bit Error

The CHECK (17th) bit of each CCSI data byte must be the *NOT* of the 16th bit. When the CHECK bit is the same as the 16th bit, the FLAG_CCSI_CHECK_BIT, FLAG_CCSI, and FLAG_ERR are set to 1. The SPI controller can access the LP5899-Q1 and write 1 to CLR_FLAG to clear the flags. The CCSI peripheral stops receiving the current CCSI command and waits until an END byte is received. Afterwards, the CCSI peripheral works normally independent of the status of the error flags.

7.3.4.6.2 Data Integrity Diagnostics

Data that is transmitted by the CCSI controller which is not modified or extended within the daisy chain of LED drivers is protected by the LP5899-Q1 device with a CRC. Over all the transmitted words of the CCSI command a CRC value is calculated. Once the command is received by the CCSI peripheral, another CRC is calculated over all the received words. When the CRC over the transmitted words does not match the CRC over the received words, the FLAG_CCSI_CRC, FLAG_CCSI, and FLAG_ERR are set to 1. The SPI controller can access the LP5899-Q1 and write 1 to CLR_FLAG to clear the flags.

When an SPI command starts with FWD (commands 0x2 to 0x7), the first data word of the SPI command is checked. When this word matches a write FC0 to FC15 (0xAA00 to 0xAA0F) or VSYNC (0xAAF0) CCSI command, the data integrity diagnostics is executed.

When this error flag is triggered consecutively, the CCSI controller and CCSI peripheral are likely out of synchronization. In that case, TI recommends to perform a SOFTRESET command.

7.3.4.6.3 CCSI Command Queue Overflow

The LP5899-Q1 provides a detection when there are too many commands in the queue to be transmitted by the CCSI controller or expected to be received by the CCSI peripheral. When the command queue is full and a new CCSI command is received by the SPI peripheral, the FLAG_CCSI_CMD_QUEUE_OVF, FLAG_CCSI, and FLAG_ERR are set to 1. In addition, the CCSI command queue and TXFIFO are cleared in the same way as TXFFCLR. The SPI controller can access the LP5899-Q1 and write 1 to CLR_FLAG to clear the flags. The error flag has to be cleared to be able to store new CCSI commands and the CCSI controller can start transmitting.

When the FLAG_CCSI_CMD_QUEUE_OVF is set, the CCSI controller and CCSI peripheral are likely to get out of synchronization. Therefore, TI recommends to perform a SOFTRESET command after this flag has been set.

7.3.4.7 FIFO Diagnostics

Both the TXFIFO and RXFIFO have their own overflow and underflow diagnostics. Below sections decribe these in more detail.

7.3.4.7.1 TXFIFO Overflow

When the TXFIFO is full (TXFFST = 0x1FF) and new data words are received by the SPI peripheral which have to be stored in the TXFIFO, the FLAG_TXFFOVF, FLAG_TXFF, and FLAG_ERR are set to 1. In addition, the TXFIFO is cleared in the same way as TXFFCLR. The SPI controller can access the LP5899-Q1 and write 1 to CLR_FLAG to clear the flags. The error flag has to be cleared to be able to store new CCSI data words on the TXFIFO and the CCSI controller can start transmitting.

7.3.4.7.2 TXFIFO Underflow

When the FIFO is empty (TXFFST = 0x0) and the CCSI controller tries to read a new word from the TXFIFO, the FLAG_TXFFUVF, FLAG_TXFF, and FLAG_ERR are set to 1. The ongoing transmission by the CCSI controller is stopped. The SPI controller can access the LP5899-Q1 and write 1 to CLR_FLAG to clear the flags. The error flag has to be cleared to be able to store new CCSI data words on the TXFIFO and the CCSI controller can start transmitting.

7.3.4.7.3 TXFIFO Single Error Detection (SED)

The TXFIFO is protected with a parity bit. When a single bit error is detected during a read operation from the TXFIFO, the FLAG_TXFFSED, FLAG_TXFF, and FLAG_ERR are set to 1. The ongoing transmission by the CCSI controller is stopped. However, the TXFIFO is not automatically cleared. The SPI controller can access the

LP5899-Q1 and write 1 to CLR_FLAG to clear the flags. The error flag has to be cleared to be able to store new CCSI data words on the TXFIFO and the CCSI controller can start transmitting.

7.3.4.7.4 RXFIFO Overflow

When the RXFIFO is full (RXFFST = 0x0FF) and new data words are received by the CCSI peripheral which have to be stored in the RXFIFO, the FLAG_RXFFOVF, FLAG_RXFF, and FLAG_ERR are set to 1. The RXFIFO is not cleared and data can still be accessed by the SPI controller. The SPI controller can access the LP5899-Q1 and write 1 to CLR_FLAG to clear the flags. The CCSI peripheral can only start storing new data in the RXFIFO after the error flag is cleared. The storage starts from the first CCSI head_byte that is received from a FWD_RD_END or FWD_RD_END_CRC SPI command.

7.3.4.7.5 RXFIFO Underflow

When the RXFIFO is empty (RXFFST = 0x0) and the SPI peripheral tries to read new data words from the RXFIFO, the FLAG_RXFFUVF, FLAG_RXFF, and FLAG_ERR are set to 1. The SPI controller can access the LP5899-Q1 and write 1 to CLR_FLAG to clear the flags. The CCSI peripheral can only start storing new data in the RXFIFO after the error flag is cleared. The storage starts from the first CCSI head_byte that is received from a FWD_RD_END or FWD_RD_END_CRC SPI command.

7.3.4.7.6 RXFIFO Single Error Detection (SED)

The RXFIFO is protected with a parity bit. When a single bit error is detected during a read operation from the RXFIFO, the FLAG_RXFFSED, FLAG_RXFF, and FLAG_ERR are set to 1. The SPI controller can access the LP5899-Q1 and write 1 to CLR_FLAG to clear the flags.

7.3.4.8 OTP CRC Error

The internal OTP is protected by an 8-bit CRC based on the polynomial $X^8 + X^2 + X + 1$. When the device powers up, the OTP is read and the read CRC is compared to the calculated CRC of all the read OTP bytes. When the CRC does not match, the FLAG_OTP_CRC and FLAG_ERR are set to 1. This flag cannot be cleared by the SPI controller. The device remains in Initialization state. Only powering down and up VCC can restart the reading of the OTP.

7.3.4.9 Fault Masking

The LP5899-Q1 provides fault masking capability using masking registers. The device is capable of masking faults by fault types. The fault masking does not disable diagnostics features but only prevents fault reporting to FLAG_ERR register and FAULT output. The below table gives the detailed description for each fault mask register.

Fault Detected	Mask Bit	Flag Name	FAULT Pin
SPI CRC error	MASK_SPI_CRC = 1	FLAG_SPI_CRC = 1 FLAG_ERR = 0	No action
	MASK_SPI_CRC = 0	FLAG_SPI_CRC = 1 FLAG_ERR = 1	Constant pulled down
SIN stuck error	MASK_CCSI_SIN = 1	FLAG_CCSI_SIN = 1 FLAG_CCSI = 1 FLAG_ERR = 0	No action
	MASK_CCSI_SIN = 0	FLAG_CCSI_CC = 1 FLAG_CCSI = 1 FLAG_ERR = 1	Constant pulled down
CCSI CHECK bit error	MASK_CCSI_CHECK_BIT = 1	FLAG_CCSI_CHECK_BIT = 1 FLAG_CCSI = 1 FLAG_ERR = 0	No action
	MASK_CCSI_CHECK_BIT = 0	FLAG_CCSI_CHECK_BIT = 1 FLAG_CCSI = 1 FLAG_ERR = 1	Constant pulled down
CCSI CRC error	MASK_CCSI_CRC = 1	FLAG_CCSI_CRC = 1 FLAG_CCSI = 1 FLAG_ERR = 0	No action
	MASK_CCSI_CRC = 0	FLAG_CCSI_CRC = 1 FLAG_CCSI = 1 FLAG_ERR = 1	Constant pulled down

7.3.4.10 Diagnostics Table

Table 7-1. Diagnostics Table

FAULT TYPE	DETECTION CRITERIA	CONDITIONS	FAULT ACTIONS	FAULT OUTPUT	FAULT PIN
VCC UVLO	$V_{CC} < V_{UVF}$		Device switch to Unpowered state	FLAG_POR FLAG_ERR	Constant pulled down
Oscillator error	$t_{WD,OSC}$ overflows		No action	FLAG_OSC FLAG_ERR	Constant pulled down
SPI communication loss fault	t_{SPI_WDT} overflows		Device enters FAILSAFE state	DEV_STATE = FAILSAFE FLAG_ERR	Constant pulled down
SPI command timeout fault	$t_{SPI\_RST\_TIMEOUT}$ overflows		Reset SPI logic	FLAG_SPI_TIMEOUT FLAG_SPI FLAG_ERR	Constant pulled down
SPI Chip Select (CS) fault	CS pin is pulled high in middle of SPI command		Reset SPI logic	FLAG_SPI_CS FLAG_SPI FLAG_ERR	Constant pulled down
SPI CRC error	Calculated CRC is different than received CRC		No action	FLAG_SPI_CRC FLAG_ERR (maskable)	Constant pulled down (maskable)
Register write failure	CCSICTRL is written during CCSI controller/peripheral activity		No action	FLAG_SPI_REG_WRITE	No action
SIN stuck error	$t_{WD,SIN}$ overflows		No action	FLAG_CCSI_SIN FLAG_CCSI FLAG_ERR (maskable)	Constant pulled down (maskable)
CCSI CHECK bit error	CHECK bit is not the inverted of the 16^{th} bit value		No action	FLAG_CCSI_CHECK_BIT FLAG_CCSI FLAG_ERR (maskable)	Constant pulled down (maskable)
CCSI CRC error	CCSI SOUT Head_bytes and Data_bytes_N result in a different CRC value than what is received on SIN	Head_bytes = VSYNC (0xAAF0) or write FCx (0xAA00 - 0xAA0F)	No action	FLAG_CCSI_CRC FLAG_CCSI FLAG_ERR (maskable)	Constant pulled down (maskable)
CCSI Command Queue overflow	Command queue is full and SPI receives new CCSI command		CCSI controller stops (if ongoing) and TXFFST is set to 0	FLAG_CCSI_CMD_QUEUE_OVF FLAG_CCSI FLAG_ERR	Constant pulled down
TXFIFO overflow	TXFFST = 511 and SPI data word needs to be stored	SPI command type starts with FWD	CCSI controller stops (if ongoing) and TXFFST is set to 0	FLAG_TXFFOVF FLAG_TXFF FLAG_ERR	Constant pulled down
TXFIFO underflow	TXFFST = 0 and CCSI controller requests a new word for transmission		CCSI controller stops	FLAG_TXFFUVF FLAG_TXFF FLAG_ERR	Constant pulled down

Table 7-1. Diagnostics Table (continued)

FAULT TYPE	DETECTION CRITERIA	CONDITIONS	FAULT ACTIONS	FAULT OUTPUT	FAULT PIN
TXFIFO single error detection	CCSI controller requests a new word for transmission and TXFIFO parity error		CCSI controller stops	FLAG_TXFFSED FLAG_TXFF FLAG_ERR	Constant pulled down
RXFIFO overflow	RXFFST = 255 and CCSI data word needs to be stored		CCSI peripheral does not store any words in RXFIFO	FLAG_RXFFOVF FLAG_RXFF FLAG_ERR	Constant pulled down
RXFIFO underflow	RXFFST = 0 and SPI peripheral requests a new word for transmission	SPI command type starts with DATA_READ	CCSI peripheral does not store any words in RXFIFO	FLAG_RXFFUVF FLAG_RXFF FLAG_ERR	Constant pulled down
RXFIFO single error detection	SPI peripheral requests a new word for transmission and RXFIFO parity error	SPI command type starts with DATA_READ	No action	FLAG_RXFFSED FLAG_RXFF FLAG_ERR	Constant pulled down
OTP CRC error	CALC_OTPCRC is different OTPCRC		No action	FLAG_OTP_CRC FLAG_ERR	Constant pulled down

7.4 Device Functional Modes

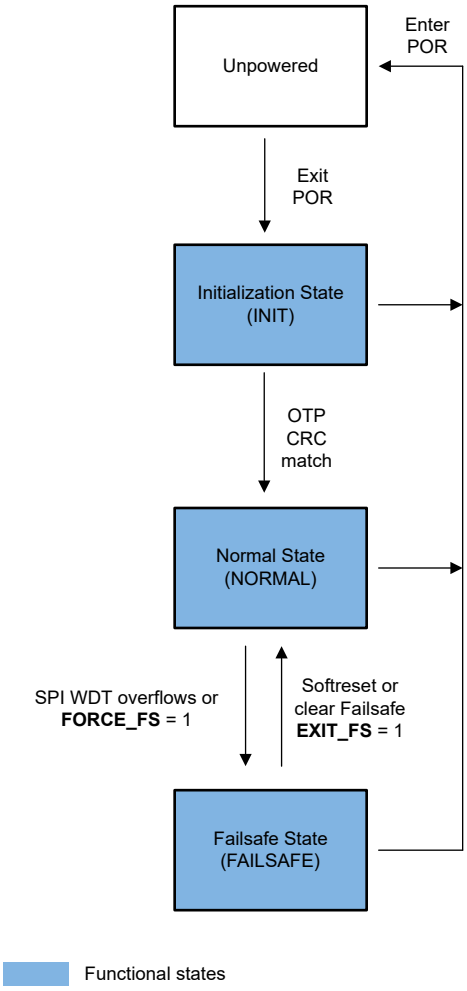


Figure 7-8. Device Functional Modes

7.4.1 Unpowered

As long as VCC is below the UVLO threshold, the device is kept in POR. All registers are kept in the reset state. If VCC falls below UVLO threshold in other states, the device immediately is kept in POR.

7.4.2 Initialization State

After VCC is above the UVLO threshold, the device enters initialization state. In this state the SPI peripheral is enabled, but the maximum supported frequency is lower than in Normal state. The continuous clock of the CCSI controller is enabled, but transmission can only start in Normal State. Also, the OTP is read and the read CRC is compared to the calculated CRC of all the read OTP bytes. If the CRC matches, the OTP registers are updated and the device enters Normal State.

7.4.3 Normal State

To enable the transmission by the CCSI controller, the FLAG_POR needs to be cleared. If the communications watchdog timer is enabled, and then expires due to a lack of communication, the device enters Failsafe state. The device can be also forced into Failsafe state anytime in Normal state by setting bit FORCE_FS in register DEVCTRL to 1. The FORCE_FS bit automatically returns to 0.

7.4.4 Failsafe State

When the device enters the Failsafe state, the TXFFCLR bit is set to stop any ongoing CCSI transmission.

The SPI peripheral is first reset when entering the Failsafe state. Afterwards, the SPI peripheral is kept alive to allow communication to the device. However, there is no control over the CCSI controller and CCSI peripheral. This means that when the SPI command starts with FWD, the data is ignored and not stored in the TXFIFO.

The device can quit from Failsafe to Normal state by setting bit EXIT_FS in register DEVCTRL to 1. The EXIT_FS bit automatically returns to 0. Another method to bring the device to Normal state is by sending the SOFTRESET_CRC SPI command.

7.5 Programming

The LP5899-Q1 has a serial peripheral interface (SPI) peripheral which is a high-speed synchronous serial input and output (I/O) port that allows a serial bit stream of 16 bits length to be shifted into and out of the device based on the externally provided clock rate. The bit stream shifted into the device provides access to the programmable functions and registers. The interface consists of 4 wires:

- Serial Data In (SDI)
- Serial Data Out (SDO)
- Serial Clock (SCLK)
- Chip Select (CS)

7.5.1 SPI Data Validity

The data on SDI wire must be stable at the rising edge of the SCLK wire. The data on SDO shifts out at the falling edge of the SCLK wire. SDO can be forced to be disabled by the bit SPI_SDO_DIS in the SPICTRL register. This is useful when the same command is broadcasted to multiple LP5899-Q1 devices on a single SPI bus. When no data is shifted into the device, the SCLK wire is expected to be logic LOW.

7.5.2 Chip Select (CS) and SPI Reset Control

The CS signal provides the ability to gate any spurious clock and data pulses. A HIGH logic signal on CS blocks the peripheral to receive data. This prevents the SPI peripheral from losing synchronization with the controller. TI does not recommend that the CS always be tied to the active state.

If the SPI peripheral does ever lose synchronization with the controller, providing a HIGH logic signal on CS resets SPI peripheral including the bit counter. Another method is to stop the SCLK and wait longer than the setting of the field SPI_RST_TIMEOUT_CFG in the SPICTRL register. This timeout starts counting from the first rising clock edge of SCLK when the SPI peripheral is expecting the command word.

7.5.3 SPI Command Format

Figure 7-9 and Table 7-2 define the format of the SPI command transmission. Each SPI command contains multiple 16-bit words. The different types of words are:

- **Command word:** The command word always includes an identifier of the command type. Dependent on the type, the command word also includes:
  - Start address to be written or read. When field address = 0 means address 0x00.
  - Length of the data that is transmitted or expected to be read. When the length field starts with opt, the data is optional. Therefore, opt_data_length = 0 means 0 data words. For fields that do not start with opt, data_length = 0 means 1 data word.
  - Number of extra END bytes to append when forwarding data. When field extra_end_bytes = 0 means 0 additional END bytes. A maximum of 127 extra END bytes can be appended with one SPI command.
  - Fixed data (in case of SOFTRESET_CRC command)
- **Data word:** Dependent of the command type this is data that needs to be forwarded (0 to N), register data that is written to (0 to N) or read from (N+1 to M) the device, or data read from (N+1 to M) the RXFIFO.
- **CRC word:** There are 2 different CRC words in each command:
  - CRC word that is generated by the SPI controller. This CRC is calculated over the SPI command word and all transmitted data words (0 to N)
  - CRC word that is generated by the SPI peripheral. This CRC is calculated over all the returned data words (N+1 to M).

  Two different CRC algorithms are supported. The default algorithm is CCITT-FALSE. This can be changed to the CRC-16/XMODEM algorithm using the REG_WR command. After changing the CRC algorithm, the next SPI command uses the new algorithm. Both algorithms are based on the polynomial $X^{16} + X^{12} + X^5 + 1$.

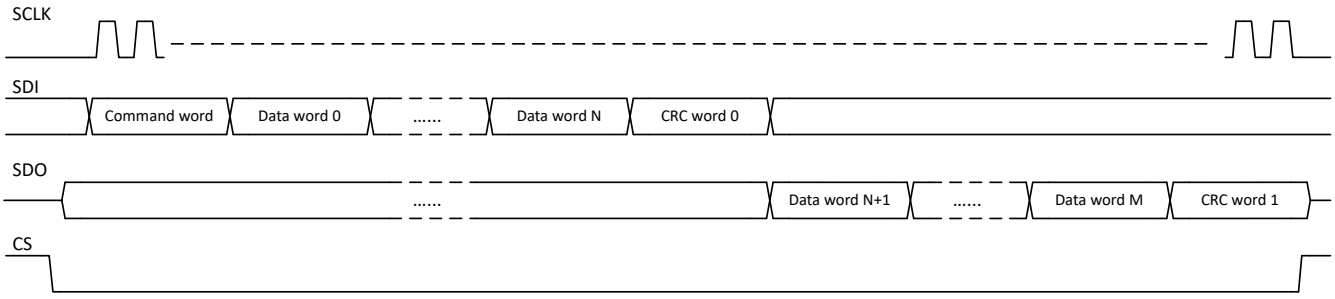


Figure 7-9. SPI Command Format

Table 7-2. SPI Command Detail

Command Type	Command Word												Data words	CRC word
	CMD[15:12]	11	10	9	8	7	6	5	4	3	2	1	0		
FWD_WR_CRC	0x2	0x0			data_length[8:0]									data word 0-data_length	CRC
FWD_WR	0x3	data_length[11:0]												data word 0-data_length	CRC
FWD_WR_END_CRC	0x4	opt_data_length[4:0]					extra_end_bytes[6:0]							data word 0-(opt_data_length-1)	CRC
FWD_WR_END	0x5	opt_data_length[4:0]					extra_end_bytes[6:0]							data word 0-(opt_data_length-1)	CRC
FWD_RD_END_CRC	0x6	data_length[4:0]					extra_end_bytes[6:0]							data word 0-data_length	CRC
FWD_RD_END	0x7	data_length[4:0]					extra_end_bytes[6:0]							data word 0-data_length	CRC
DATA_RD_CRC	0x8	0x0					data_length[7:0]							N/A	CRC
DATA_RD	0x9	0x0					data_length[7:0]							N/A	CRC
REG_WR_CRC	0xA	0x0		address[3:0]				0x0		data_length[3:0]				data word 0-data_length	CRC
REG_WR	0xB	0x0		address[3:0]				0x0		data_length[3:0]				data word 0-data_length	CRC
REG_RD_CRC	0xC	0x0		address[3:0]				0x0		data_length[3:0]				N/A	CRC
REG_RD	0xD	0x0		address[3:0]				0x0		data_length[3:0]				N/A	CRC
SOFTRESET_CRC	0xE	0x1E1												N/A	CRC

7.5.4 SPI Command Detail

For each command except SOFTRESET_CRC there are two versions. The version without CRC at the end of the type name is always executed even when the CRC value is incorrect. The version with CRC at the end of the type name is only executed when the CRC that is received matches the calculated CRC over the command word and data words.

The commands starting with FWD, forward the received data words by the CCSI controller. As long as the data length is larger than 0, the CCSI controller automatically inserts one start bit, the check bits, and one END byte. The SPI data words of one SPI command are therefore considered to be one CCSI command with 1 start bit before the first SPI data word, a check bit after every data word, and one END byte after the last SPI data word.

Commands starting with REG are used to write and read the register of the LP5899-Q1 device. The DATA_RD commands return the data stored on the RXFIFO.

Commands starting with FWD, REG_WR, and SOFTRESET_CRC return the STATUS register and the CRC calculated over the STATUS register. This acknowledgement can be disabled by bit SPI_ACK_DIS in the SPICTRL register. Care has to be taken when executing SOFTRESET_CRC while the acknowledgement is disabled. In this case, TI recommends to wait at least one SPI word before sending the next command.

Whenever the LP5899-Q1 device returns data to the controller on the SDO pin, the controller has to provide sufficient clock pulses on the SCLK pin to shift out the data. TI recommends to keep the SDI pin at logic HIGH while providing the clock pulses to shift out the data.

FWD_WR_CRC (Forward Write CRC command)

Return to the SPI Command Table

The FWD_WR_CRC command is used to transmit data words by the CCSI controller in the device. All the data words received by the SPI peripheral are stored on the TXFIFO. Only when the received CRC matches with the calculated CRC over the command word and data words, the CCSI controller starts to transmit. This means that the TXFFLVL does not impact the start of this transmission. Caution has to be taken by the SPI controller that the data length is less than the size of the TXFIFO. This SPI command supports up to 512 data words and returns the STATUS register and the CRC calculated over the STATUS register. An example of FWD_WR_CRC command forwarding 2 data words is depicted in Figure 7-10.

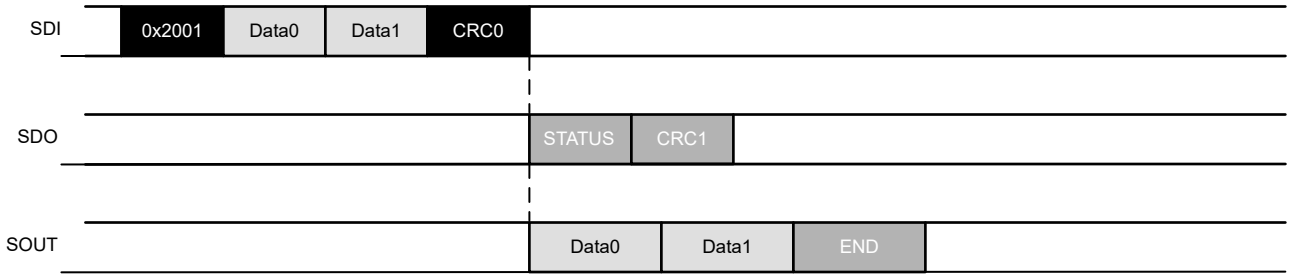


Figure 7-10. Example of FWD_WR_CRC command

FWD_WR (Forward Write command)

Return to the SPI Command Table

The FWD_WR command is used to transmit data words by the CCSI controller in the device. All the data words received by the SPI peripheral are stored on the TXFIFO. If one or more of the following conditions is met, the CCSI controller starts transmitting.

- The number of words stored on the TXFIFO reach TXFFLVL
- All the data words of the SPI command have been received

This means that the CRC does not impact the start of this transmission. When the received CRC does not match the calculated CRC over the command word and data words, the FAULT pin is pulled low (when not masked) and the flag FLAG_SPI_CRC is set. This SPI command supports up to 4096 data words and returns the STATUS register and the CRC calculated over the STATUS register. An example of FWD_WR command forwarding 3 words with TXFFLVL set to 2 data words is depicted in Figure 7-11.

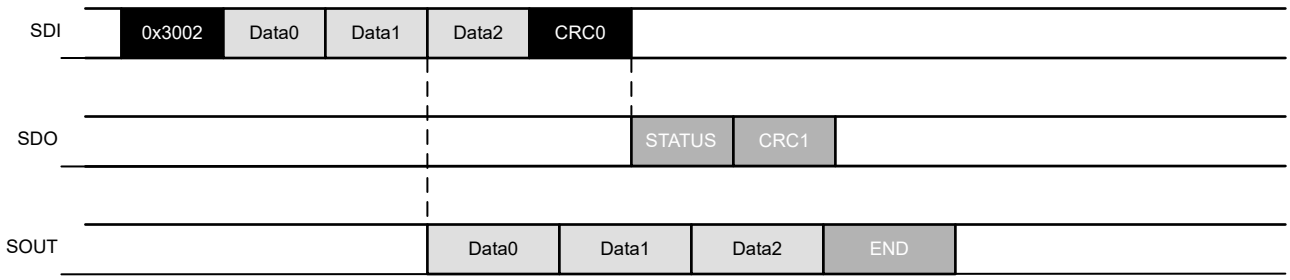


Figure 7-11. Example of FWD_WR command

FWD_WR_END_CRC (Forward Write CRC with END bytes command)

Return to the SPI Command Table

The FWD_WR_END_CRC command is used to transmit data words by the CCSI controller in the device. All the data words received by the SPI peripheral are stored on the TXFIFO. Only when the received CRC matches with the calculated CRC over the command word and data words, the CCSI controller starts to transmit. This means that the TXFFLVL does not impact the start of this transmission. After all the data words have been transmitted by the CCSI controller, the specified number of extra END bytes are appended. The transmission of data words and the transmission of the extra END bytes are considered as 2 separate CCSI commands. This SPI command supports up to 31 data words and returns the STATUS register and the CRC calculated over the STATUS register. An example of FWD_WR_END_CRC command forwarding 0 data words (and therefore does not insert one END byte) and 3 extra END bytes is depicted in Figure 7-12.

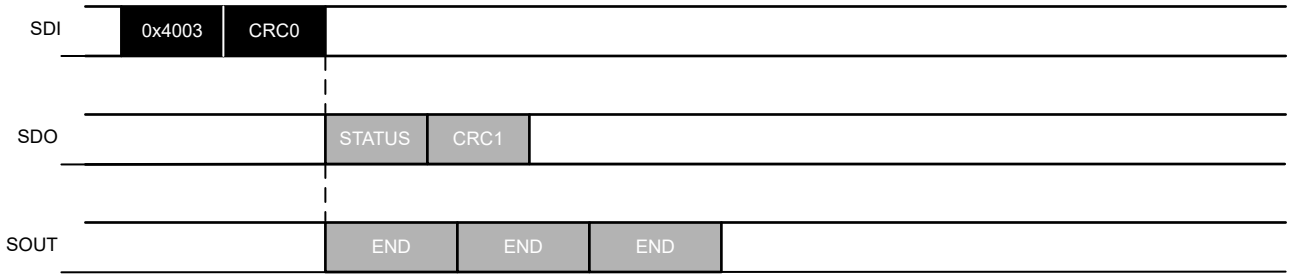


Figure 7-12. Example of FWD_WR_END_CRC command

FWD_WR_END (Forward Write with END bytes command)

Return to the SPI Command Table

The FWD_WR_END command is used to transmit data words by the CCSI controller in the device. All the data words received by the SPI peripheral are stored on the TXFIFO. If one or more of the following conditions is met, the CCSI controller starts transmitting.

- The number of words stored on the TXFIFO reach TXFFLVL
- All the data words of the SPI command have been received

This means that the CRC does not impact the start of this transmission. When the received CRC does not match the calculated CRC over the command word and data words, the FAULT pin is pulled low (when not masked) and the flag FLAG_SPI_CRC is set. After all the data words have been transmitted by the CCSI controller, the specified number of extra END bytes are appended. The transmission of data words and the transmission of the extra END bytes are considered as 2 separate CCSI commands. This SPI command supports up to 31 data words and returns the STATUS register and the CRC calculated over the STATUS register. An example of FWD_WR_END command forwarding 2 data words and 1 extra END bytes is depicted in Figure 7-13. Note that in this example the TXFFLVL is set to 2 words or higher.

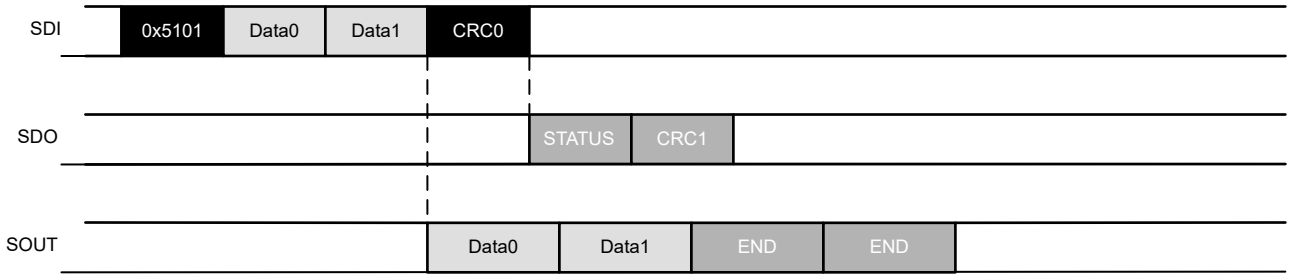


Figure 7-13. Example of FWD_WR_END command

FWD_RD_END_CRC (Forward Read CRC with END bytes command)

Return to the SPI Command Table

The FWD_RD_END_CRC command is used to transmit data words by the CCSI controller in the device. All the data words received by the SPI peripheral are stored on the TXFIFO. Only when the received CRC matches with the calculated CRC over the command word and data words, the CCSI controller starts to transmit. This means that the TXFFLVL does not impact the start of this transmission. After all the data words have been transmitted by the CCSI controller, the specified number of extra END bytes are appended. The transmission of data words and the transmission of the extra END bytes are considered as 2 separate CCSI commands. All the data words that are received by the CCSI peripheral for this command are stored on the RXFIFO. This SPI command supports up to 32 data words and returns the STATUS register and the CRC calculated over the STATUS register. An example of FWD_RD_END_CRC command forwarding 2 data words and 1 extra END bytes is depicted in Figure 7-14.

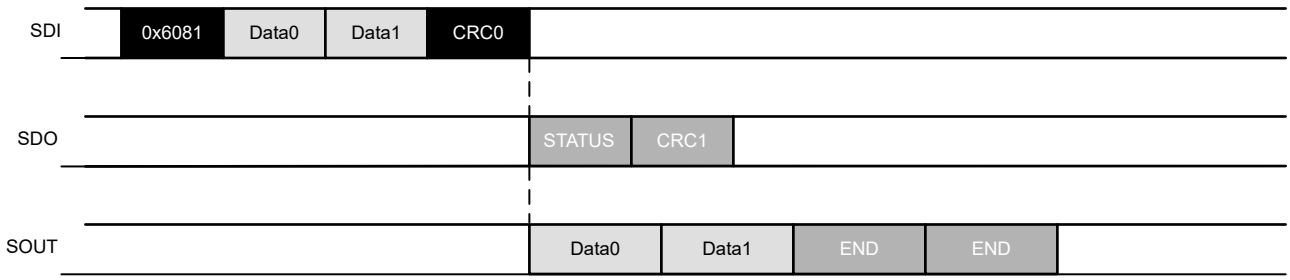


Figure 7-14. Example of FWD_RD_END_CRC command

FWD_RD_END (Forward Read with END bytes command)

Return to the SPI Command Table

The FWD_RD_END command is used to transmit data words by the CCSI controller in the device. All the data words received by the SPI peripheral are stored on the TXFIFO. If one or more of the following conditions is met, the CCSI controller starts transmitting.

- The number of words stored on the TXFIFO reach TXFFLVL
- All the data words of the SPI command have been received

This means that the CRC does not impact the start of this transmission. When the received CRC does not match the calculated CRC over the command word and data words, the FAULT pin is pulled low (when not masked) and the flag FLAG_SPI_CRC is set. After all the data words have been transmitted by the CCSI controller, the specified number of extra END bytes are appended. The transmission of data words and the transmission of the extra END bytes are considered as 2 separate CCSI commands. All the data words that are received by the CCSI peripheral for this command are stored on the RXFIFO. This SPI command supports up to 32 data words and returns the STATUS register and the CRC calculated over the STATUS register. An example of FWD_RD_END command forwarding 3 data words with TXFFLVL set to 2 data words and 2 extra END bytes is depicted in Figure 7-15.

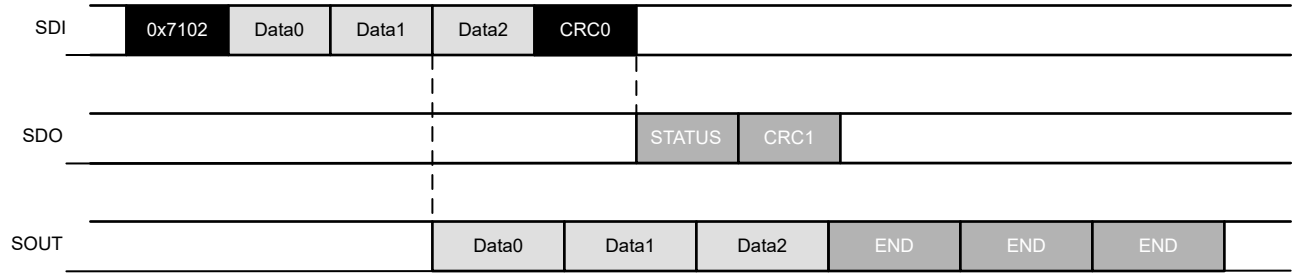


Figure 7-15. Example of FWD_RD_END command

DATA_RD_CRC (Data Read CRC command)

Return to the SPI Command Table

The DATA_RD_CRC command is used to read data words from the RXFIFO. Only when the received CRC matches with the calculated CRC over the command word, the device returns the requested number of data words and the CRC calculated over the data words. When the CRC fails, the SDO is kept at logic HIGH. An example of DATA_RD_CRC command requesting 4 data words is depicted in Figure 7-16.

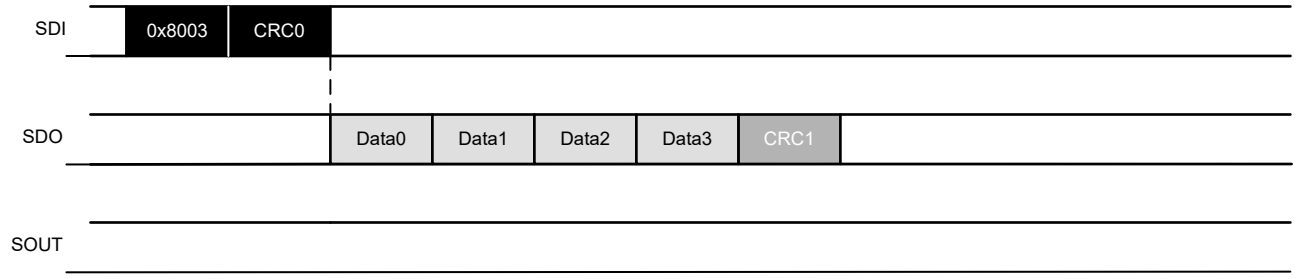


Figure 7-16. Example of DATA_RD_CRC command

DATA_RD (Data Read command)

Return to the SPI Command Table

The DATA_RD command is used to read data words from the RXFIFO. Even when the received CRC does not match with the calculated CRC over the command word, the device returns the requested number of data words and the CRC calculated over the data words. When the received CRC does not match the calculated CRC over the command word, the FAULT pin is pulled low (when not masked) and the flag FLAG_SPI_CRC is set. An example of DATA_RD command requesting 3 data words is depicted in Figure 7-17.

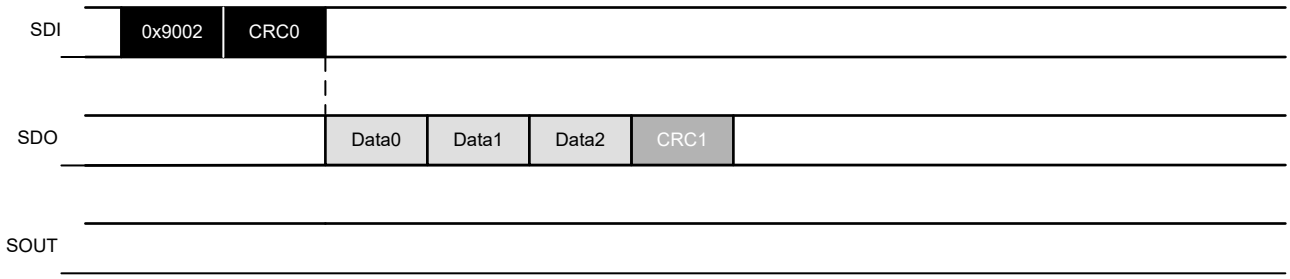


Figure 7-17. Example of DATA_RD command

REG_WR_CRC (Register Write CRC command)

Return to the SPI Command Table

The REG_WR_CRC command is used to write the internal registers of the LP5899-Q1 device. The command includes a field to indicate the address of the first register to be written. All the data words received by the SPI peripheral are stored in shadow registers. Only when the received CRC matches with the calculated CRC over the command word and data words, the registers are updated. This command returns the STATUS register and the CRC calculated over the STATUS register. An example of REG_WR_CRC command writing 3 registers is depicted in Figure 7-18.

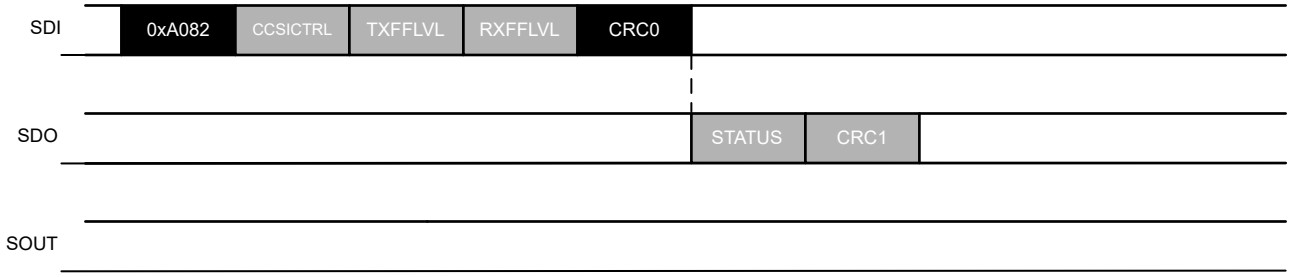


Figure 7-18. Example of REG_WR_CRC command

REG_WR (Register Write command)

Return to the SPI Command Table

The REG_WR command is used to write the internal registers of the LP5899-Q1 device. The command includes a field to indicate the address of the first register to be written. All the data words received by the SPI peripheral are directly written in registers. This means that the CRC does not impact the writing of registers. When the received CRC does not match the calculated CRC over the command word, the FAULT pin is pulled low (when not masked) and the flag FLAG_SPI_CRC is set. This command returns the STATUS register and the CRC calculated over the STATUS register. An example of REG_WR_CRC command writing 2 registers is depicted in Figure 7-19.

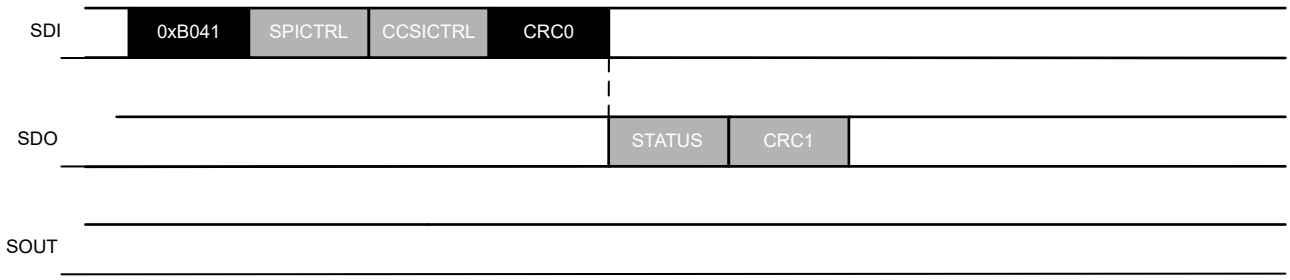


Figure 7-19. Example of REG_WR command

REG_RD_CRC (Register Read CRC command)

Return to the SPI Command Table

The REG_RD_CRC command is used to read the internal registers of the LP5899-Q1 device. The command includes a field to indicate the address of the first register to be read. Only when the received CRC matches with the calculated CRC over the command word, the device returns the requested number of register words and the CRC calculated over the register words. When the CRC fails, the SDO is kept at logic HIGH. An example of REG_RD_CRC command reading 1 register is depicted in Figure 7-20.

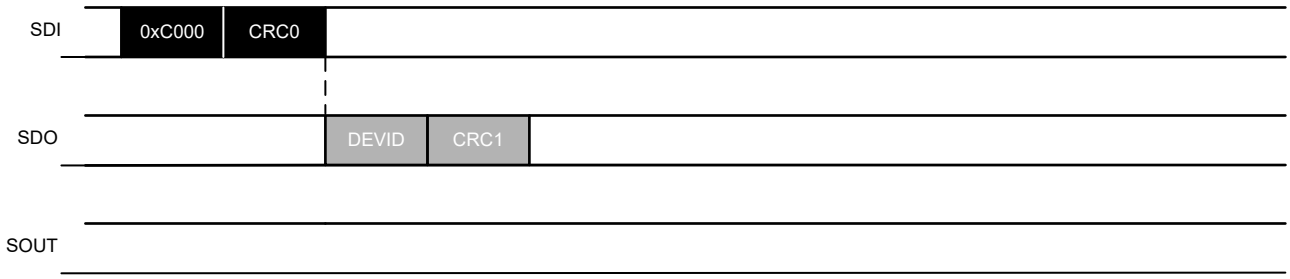


Figure 7-20. Example of REG_RD_CRC command

REG_RD (Register Read command)

Return to the SPI Command Table

The REG_RD command is used to read the internal registers of the LP5899-Q1 device. The command includes a field to indicate the address of the first register to be read. Even when the received CRC does not match with the calculated CRC over the command word, the device returns the requested number of register words and the CRC calculated over the register words. When the received CRC does not match the calculated CRC over the command word, the FAULT pin is pulled low (when not masked) and the flag FLAG_SPI_CRC is set. An example of REG_RD command reading 3 registers is depicted in Figure 7-21.

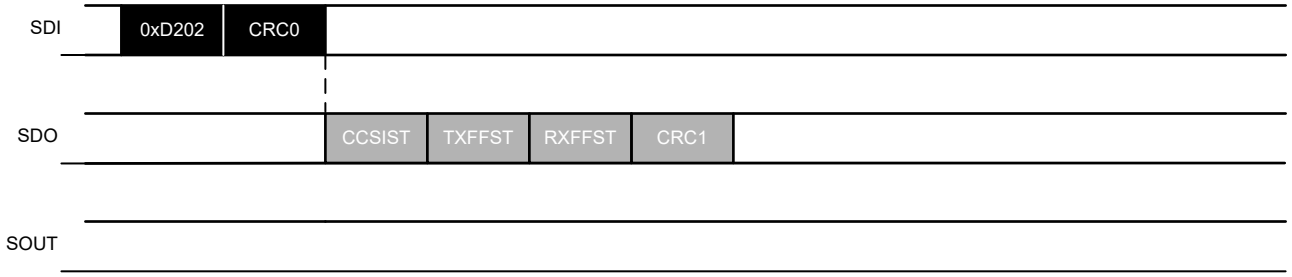


Figure 7-21. Example of REG_RD command

SOFTRESET_CRC (Softreset CRC command)

Return to the SPI Command Table

The SOFTRESET_CRC command is used to reset all internal registers to the default values and synchronize the CCSI controller and peripheral. The command is executed when:

- The received CRC matches with the calculated CRC over the command word, and
- The CCSI controller is not transmitting

The CRC value for the SOFTRESET_CRC command using CCITT-FALSE algorithm is 0xD383 and when using CRC-16/XMODEM algorithm 0xCE8C.

With a reset of all the internal registers, most of the fault flags that were previously set, are cleared. Only FLAG_POR and FLAG_ERR are reset to HIGH. In addition, all data stored on the RXFIFO becomes inaccessible. If there are CCSI commands in the LED daisy chain that have not been received yet by the CCSI peripheral, the CCSI CRC diagnostics cannot be checked anymore because the calculated CRC values have been cleared for the purpose of synchronization between the CCSI controller and CCSI peripheral. TI recommends to transmit the same number of END bytes as the number of LED drivers in the daisy chain after transmitting the SOFTRESET_CRC command. This clears any already transmitted CCSI command and therefore keeps the synchronization. When the device is in FAILSAFE mode, the SOFTRESET_CRC command brings the device to NORMAL mode. An unsuccessful SOFTRESET_CRC command is recorded in the bit FLAG_SRST in the STATUS register. An example of SOFTRESET_CRC command is depicted in Figure 7-22.

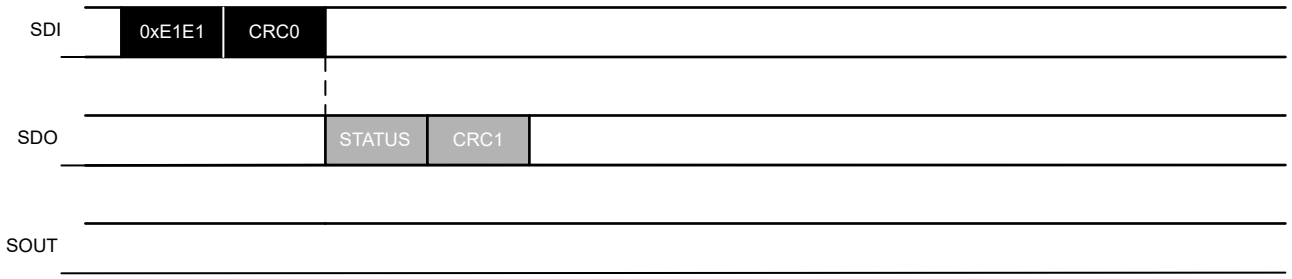


Figure 7-22. Example of SOFTRESET_CRC command

7.6 Device Registers

DEVICE Registers Summary Table lists the memory-mapped registers for the Device registers. All register offset addresses not listed in DEVICE Registers Summary Table should be considered as reserved locations and the register contents should not be modified.

Table 7-3. DEVICE Registers Summary Table

Address	Acronym	Description	Section
0x0	DEVID	Device Identification	Section 7.6.1
0x1	SPICTRL	Control for SPI	Section 7.6.2
0x2	CCSICTRL	Control for Continuous Clock Serial Interface (CCSI)	Section 7.6.3
0x3	TXFFLVL	Transmission FIFO level control	Section 7.6.4
0x4	RXFFLVL	Receive FIFO level control	Section 7.6.5
0x5	DEVCTRL	Control register for Device	Section 7.6.6
0x6	DIAGMASK	Diagnostic masking	Section 7.6.7
0x7	STATUS	Global device status	Section 7.6.8
0x8	IFST	Detail Interface status	Section 7.6.9
0x9	TXFFST	Detail Transmit FIFO status	Section 7.6.10
0xA	RXFFST	Detail Receive FIFO status	Section 7.6.11

Complex bit access types are encoded to fit into small table cells. Table 7-4 shows the codes that are used for access types in this section.

Table 7-4. Device Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
Reset or Default Value		
-n		Value after reset or the default value

7.6.1 DEVID Register (Address = 0x0) [Reset = 0xED99]

DEVID is shown in Figure 7-23 and described in Table 7-5.

Return to the DEVICE Registers Summary Table.

Figure 7-23. DEVID Register

15	14	13	12	11	10	9	8
DEVID							
R-0xED99							
7	6	5	4	3	2	1	0
DEVID							
R-0xED99							

Table 7-5. DEVID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	DEVID	R	0xED99	Device Identification

7.6.2 SPICTRL Register (Address = 0x1) [Reset = 0x00A0]

SPICTRL is shown in Figure 7-24 and described in Table 7-6.

Return to the DEVICE Registers Summary Table.

Figure 7-24. SPICTRL Register

15	14	13	12	11	10	9	8
RESERVED		SPI_WDT_CFG		RESERVED			
R/W-0x0		R/W-0x0		R/W-0x0			
7	6	5	4	3	2	1	0
SPI_RST_TIMEOUT_CFG				RESERVED	SPI_CRC_ALG	SPI_SDO_DIS	SPI_ACK_DIS
R/W-0xA				R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

Table 7-6. SPICTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	RESERVED	R/W	0x0	Reserved
13-12	SPI_WDT_CFG	R/W	0x0	Watchdog on SPI to into FAILSAFE state 0x0 = 40ms 0x1 = 20ms 0x2 = 10ms 0x3 = Disabled
11-8	RESERVED	R/W	0x0	Reserved
7-4	SPI_RST_TIMEOUT_CFG	R/W	0xA	Watchdog on SCLK to reset SPI after timeout 0x0 = Disabled 0x1 = 500us 0x2 = 1ms 0x3 = 2ms 0x4 = 3ms 0x5 = 4ms 0x6 = 5ms 0x7 = 10ms 0x8 = 15ms 0x9 = 20ms 0xA = 30ms 0xB = 40ms 0xC = 50ms 0xD = 85ms 0xE = 100ms 0xF = 200ms
3	RESERVED	R/W	0x0	Reserved
2	SPI_CRC_ALG	R/W	0x0	CRC algorithm used for SPI communication 0x0 = CCITT-FALSE is used 0x1 = CRC-16/XMODEM is used
1	SPI_SDO_DIS	R/W	0x0	Disable bit for SPI SDO 0x0 = SDO is driven when CS is low 0x1 = SDO is always High Impedance
0	SPI_ACK_DIS	R/W	0x0	Disable bit for SPI auto-reply of STATUS register 0x0 = Auto-reply is enabled 0x1 = Auto-reply is disabled

7.6.3 CCSICTRL Register (Address = 0x2) [Reset = 0x0000]

CCSICTRL is shown in Figure 7-25 and described in Table 7-7.

Return to the DEVICE Registers Summary Table.

Figure 7-25. CCSICTRL Register

15	14	13	12	11	10	9	8
RESERVED						CCSI_SS_CLKO	
R/W-0x0						R/W-0x0	
7	6	5	4	3	2	1	0
RESERVED				CCSI_DATA_RATE			
R/W-0x0				R/W-0x0			

Table 7-7. CCSICTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R/W	0x0	Reserved
9-8	CCSI_SS_CLKO	R/W	0x0	Spread spectrum setting for CLK_O pin 0x0 = disabled 0x1 = 2% 0x2 = 4% 0x3 = 8%
7-4	RESERVED	R/W	0x0	Reserved
3-0	CCSI_DATA_RATE	R/W	0x0	Data rate for CCSI 0x0 = 1Mbit/s 0x1 = 1.25Mbit/s 0x2 = 1.43Mbit/s 0x3 = 1.67Mbit/s 0x4 = 2Mbit/s 0x5 = 2.22Mbit/s 0x6 = 2.5Mbit/s 0x7 = 2.86Mbit/s 0x8 = 3.33Mbit/s 0x9 = 4Mbit/s 0xA = 5Mbit/s 0xB = 6.67Mbit/s 0xC = 8Mbit/s 0xD = 10Mbit/s 0xE = 13.33Mbit/s 0xF = 20Mbit/s

7.6.4 TXFFLVL Register (Address = 0x3) [Reset = 0x01FF]

TXFFLVL is shown in Figure 7-26 and described in Table 7-8.

Return to the DEVICE Registers Summary Table.

Figure 7-26. TXFFLVL Register

15	14	13	12	11	10	9	8
TXFFCLR	RESERVED						TXFFLVL
R/W1C-0x0	R/W-0x0						R/W-0x1FF
7	6	5	4	3	2	1	0
TXFFLVL							
R/W-0x1FF							

Table 7-8. TXFFLVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	TXFFCLR	R/W1C	0x0	Clear all data on Transmit FIFO
14-9	RESERVED	R/W	0x0	Reserved
8-0	TXFFLVL	R/W	0x1FF	TX FIFO level for start of transmission on CCSI in words with 0x0 meaning 1 word

7.6.5 RXFFLVL Register (Address = 0x4) [Reset = 0x00FF]

RXFFLVL is shown in Figure 7-27 and described in Table 7-9.

Return to the DEVICE Registers Summary Table.

Figure 7-27. RXFFLVL Register

15	14	13	12	11	10	9	8
RXFFCLR	RESERVED						
R/W1C-0x0	R/W-0x0						
7	6	5	4	3	2	1	0
RXFFLVL							
R/W-0xFF							

Table 7-9. RXFFLVL Register Field Descriptions

Bit	Field	Type	Reset	Description
15	RXFFCLR	R/W1C	0x0	Clear all data on Receive FIFO
14-8	RESERVED	R/W	0x0	Reserved
7-0	RXFFLVL	R/W	0xFF	RX FIFO level to pull down the DRDY pin when number of words is exceeded with 0x0 meaning 1 word

7.6.6 DEVCTRL Register (Address = 0x5) [Reset = 0x0000]

DEVCTRL is shown in Figure 7-28 and described in Table 7-10.

Return to the DEVICE Registers Summary Table.

Figure 7-28. DEVCTRL Register

15	14	13	12	11	10	9	8
RESERVED							
R/W-0x0							
7	6	5	4	3	2	1	0
RESERVED					FORCE_FS	RESERVED	EXIT_FS
R/W-0x0					R/W1C-0x0	R/W-0x0	R/W1C-0x0

Table 7-10. DEVCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R/W	0x0	Reserved
2	FORCE_FS	R/W1C	0x0	Switch the device from NORMAL state to FAILSAFE state 0x0 = Keep current state 0x1 = Bring device to FAILSAFE state
1	RESERVED	R/W	0x0	Reserved
0	EXIT_FS	R/W1C	0x0	Bring device out of FAILSAFE mode to NORMAL mode

7.6.7 DIAGMASK Register (Address = 0x6) [Reset = 0x0000]

DIAGMASK is shown in Figure 7-29 and described in Table 7-11.

Return to the DEVICE Registers Summary Table.

Figure 7-29. DIAGMASK Register

15	14	13	12	11	10	9	8
RESERVED				MASK_CCSI_CHECK_BIT	RESERVED	MASK_CCSI_CRC	MASK_CCSI_SIN
R/W-0x0				R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0
7	6	5	4	3	2	1	0
RESERVED							MASK_SPI_CRC
R/W-0x0							R/W-0x0

Table 7-11. DIAGMASK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0x0	Reserved
11	MASK_CCSI_CHECK_BIT	R/W	0x0	Mask CCSI check bit fault to set FLAG_ERR and pull down FAULT pin 0x0 = Fault reporting is enabled 0x1 = Fault reporting is disabled
10	RESERVED	R/W	0x0	Reserved
9	MASK_CCSI_CRC	R/W	0x0	Mask CCSI CRC fault to set FLAG_ERR and pull down FAULT pin 0x0 = Fault reporting is enabled 0x1 = Fault reporting is disabled
8	MASK_CCSI_SIN	R/W	0x0	Mask CCSI SIN stuck-at fault to set FLAG_ERR and pull down FAULT pin 0x0 = Fault reporting is enabled 0x1 = Fault reporting is disabled
7-1	RESERVED	R/W	0x0	Reserved
0	MASK_SPI_CRC	R/W	0x0	Mask SPI CRC fault to set FLAG_ERR and pull down FAULT pin 0x0 = Fault reporting is enabled 0x1 = Fault reporting is disabled

7.6.8 STATUS Register (Address = 0x7) [Reset = 0x0403]

STATUS is shown in Figure 7-30 and described in Table 7-12.

Return to the DEVICE Registers Summary Table.

Figure 7-30. STATUS Register

15	14	13	12	11	10	9	8
CLR_FLAG	FLAG_CCSI	RESERVED	FLAG_TXFF	FLAG_RXFF	DRDYST	FLAG_SRST	FLAG_SPI
R/W1C-0x0	R-0x0	R-0x0	R-0x0	R-0x0	R-0x1	R-0x0	R-0x0
7	6	5	4	3	2	1	0
FLAG_SPI_REG_WRITE	FLAG_SPI_CRC	DEV_STATE		FLAG_OTP_CRC	FLAG_OSC	FLAG_POR	FLAG_ERR
R-0x0	R-0x0	R-0x0		R-0x0	R-0x0	R-0x1	R-0x1

Table 7-12. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
15	CLR_FLAG	R/W1C	0x0	Write to clear all flags. 0x0 = Do not clear flags 0x1 = Clear all flags
14	FLAG_CCSI	R	0x0	CCSI error flag. 0x0 = No device error has been detected 0x1 = Device error has been detected. Check IFST for more details.
13	RESERVED	R	0x0	Reserved
12	FLAG_TXFF	R	0x0	Transmit FIFO error detection. 0x0 = No Transmit FIFO error has been detected 0x1 = Transmit FIFO error has been detected. Check TXFFST for more details.
11	FLAG_RXFF	R	0x0	Receive FIFO error detection. 0x0 = No Receive FIFO error has been detected 0x1 = Receive FIFO error has been detected. Check RXFFST for more details.
10	DRDYST	R	0x1	Status of DRDY pin. 0x0 = DRDY pin is logic low 0x1 = DRDY pin is logic high
9	FLAG_SRST	R	0x0	Unsuccessful SOFTRESET. Softreset cannot be executed while CCSI is transmitting. 0x0 = No SOFTRESET error has been detected 0x1 = SOFTRESET error has been detected
8	FLAG_SPI	R	0x0	SPI error flag. 0x0 = No device error has been detected 0x1 = Device error has been detected. Check IFST for more details.
7	FLAG_SPI_REG_WRITE	R	0x0	Unsuccessful SPI register write command. CCSICTRL cannot be written while CCSI is transmitting and/or receiving. 0x0 = No SPI register write error has been detected 0x1 = SPI register write error has been detected
6	FLAG_SPI_CRC	R	0x0	SPI communication CRC error has been detected. 0x0 = No CRC error has been detected 0x1 = CRC error has been detected
5-4	DEV_STATE	R	0x0	Device state. 0x0 = Device is in NORMAL state 0x1 = Device is in INIT state 0x2 = Device is in INIT state 0x3 = Device is in FAILSAFE state
3	FLAG_OTP_CRC	R	0x0	OTP CRC error detection. 0x0 = No OTP CRC error has been detected 0x1 = OTP CRC error has been detected

Table 7-12. STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	FLAG_OSC	R	0x0	Oscillator out of range detection. 0x0 = No oscillator error has been detected 0x1 = Oscillator error has been detected
1	FLAG_POR	R	0x1	Power-On-Reset flag 0x0 = No POR is triggered 0x1 = Device has triggered POR
0	FLAG_ERR	R	0x1	Global error flag. This is inverted status of FAULT pin. 0x0 = No error was detected 0x1 = One or more errors have been detected

7.6.9 IFST Register (Address = 0x8) [Reset = 0x0000]

IFST is shown in Figure 7-31 and described in Table 7-13.

Return to the DEVICE Registers Summary Table.

Figure 7-31. IFST Register

15	14	13	12	11	10	9	8
RESERVED						FLAG_SPI_CS	FLAG_SPI_TIMEOUT
R-0x0						R-0x0	R-0x0
7	6	5	4	3	2	1	0
RESERVED			FLAG_CCSI_CMD_QUEUE_OVF	FLAG_CCSI_CHECK_BIT	RESERVED	FLAG_CCSI_CRC	FLAG_CCSI_SIN
R-0x0			R-0x0	R-0x0	R-0x0	R-0x0	R-0x0

Table 7-13. IFST Register Field Descriptions

Bit	Field	Type	Reset	Description
15-10	RESERVED	R	0x0	Reserved
9	FLAG_SPI_CS	R	0x0	SPI Chip Select pin was pulled high in the middle of reception of command. 0x0 = No CS error has been detected 0x1 = CS error has been detected
8	FLAG_SPI_TIMEOUT	R	0x0	SPI timeout error has been detected. This will only be set when SPI_RST_TIMEOUT_CFG is enabled. 0x0 = No SPI timeout has been detected 0x1 = SPI timeout has been detected
7-5	RESERVED	R	0x0	Reserved
4	FLAG_CCSI_CMD_QUEUE_OVF	R	0x0	CCSI command queue overflow error has been detected. 0x0 = No overflow error has been detected 0x1 = Overflow error has been detected
3	FLAG_CCSI_CHECK_BIT	R	0x0	CCSI check bit error has been detected for CCSI received data. 0x0 = No check bit error has been detected 0x1 = Check bit error has been detected
2	RESERVED	R	0x0	Reserved
1	FLAG_CCSI_CRC	R	0x0	CRC error has been detected for CCSI data. 0x0 = No CRC error has been detected 0x1 = CRC error has been detected
0	FLAG_CCSI_SIN	R	0x0	Missing toggling on SIN. 0x0 = No missing toggling on SIN error has been detected 0x1 = Missing toggling on SIN error has been detected

7.6.10 TXFFST Register (Address = 0x9) [Reset = 0x0000]

TXFFST is shown in Figure 7-32 and described in Table 7-14.

Return to the DEVICE Registers Summary Table.

Figure 7-32. TXFFST Register

15	14	13	12	11	10	9	8
FLAG_TXFFOVF	FLAG_TXFFUVF	FLAG_TXFFSED	RESERVED				TXFFST
R-0x0	R-0x0	R-0x0	R-0x0				R-0x0
7	6	5	4	3	2	1	0
TXFFST							
R-0x0							

Table 7-14. TXFFST Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FLAG_TXFFOVF	R	0x0	Overflow error on Transmit FIFO
14	FLAG_TXFFUVF	R	0x0	Underflow error on Transmit FIFO
13	FLAG_TXFFSED	R	0x0	Single Error Detection on Transmit FIFO
12-9	RESERVED	R	0x0	Reserved
8-0	TXFFST	R	0x0	TX FIFO Status 0x0 = Transmit FIFO is empty. 0x1 = Transmit FIFO has 1 word. 0x2 = Transmit FIFO has 2 words. ... 0x1FE = Transmit FIFO has 510 words. 0x1FF = Transmit FIFO has 511 or 512 words.

7.6.11 RXFFST Register (Address = 0xA) [Reset = 0x0000]

RXFFST is shown in Figure 7-33 and described in Table 7-15.

Return to the DEVICE Registers Summary Table.

Figure 7-33. RXFFST Register

15	14	13	12	11	10	9	8
FLAG_RXFFOVF	FLAG_RXFFUVF	FLAG_RXFFSED	RESERVED				
R-0x0	R-0x0	R-0x0	R-0x0				
7	6	5	4	3	2	1	0
RXFFST							
R-0x0							

Table 7-15. RXFFST Register Field Descriptions

Bit	Field	Type	Reset	Description
15	FLAG_RXFFOVF	R	0x0	Overflow error on Receive FIFO
14	FLAG_RXFFUVF	R	0x0	Underflow error on Receive FIFO
13	FLAG_RXFFSED	R	0x0	Single Error Detection on Receive FIFO
12-8	RESERVED	R	0x0	Reserved
7-0	RXFFST	R	0x0	RX FIFO Status 0x0 = Receive FIFO is empty. 0x1 = Receive FIFO has 1 word. 0x2 = Receive FIFO has 2 words. ... 0xFE = Receive FIFO has 254 words. 0xFF = Receive FIFO has 255 or 256 words.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LP5899-Q1 is controlled using a standard SPI. The device is connected to a daisy chain of LP589x-Q1 devices which are controlled using a Continuous Clock Serial Interface (CCSI) provided by the LP5899-Q1 device. All the features of the LP5899-Q1 are accessed by programmable registers.

8.2 Typical Application

Figure 8-1 depicts a typical application with only one LP5899-Q1 connected to a Controller using one SPI bus and many LP589x-Q1 connected in a daisy chain using one CCSI bus.

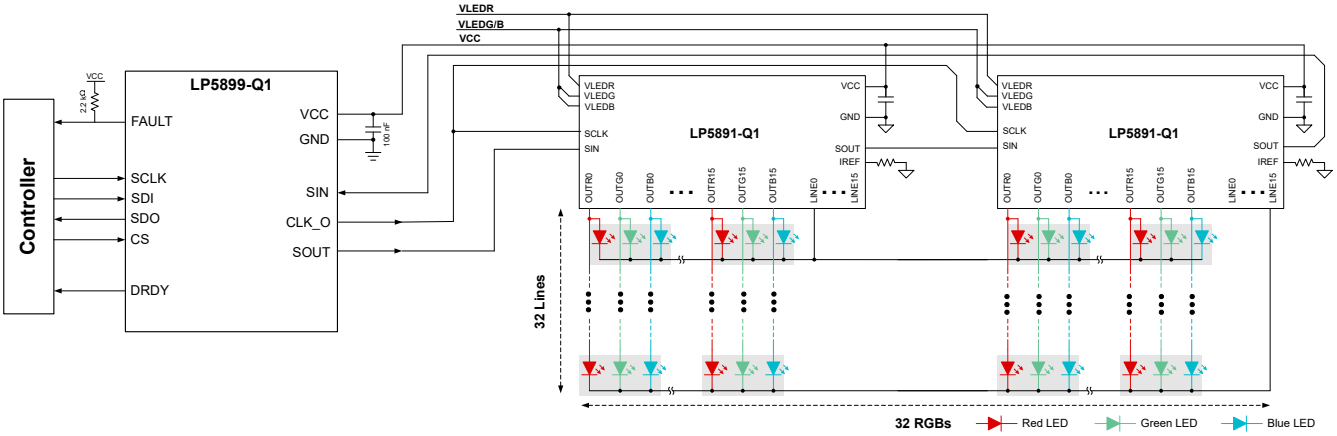


Figure 8-1. Typical Application Schematics

8.2.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER	VALUE
V_{CC}	2.8V
Frame rate	30Hz
Brightness resolution	16 bits
Cascaded devices number	6
Number of scan lines	30
f_{SPI}	8MHz

8.2.2 Detailed Design Procedure

At first the designer needs to determine the required CCSI data rate for the application. The minimum CCSI data rate is coming from the brightness information that needs to be transmitted to all the LED drivers within one frame period. The data sheet of the chosen LED driver gives more details about the minimum required CCSI data rate. In this application example the frame period is 33.33ms. There are 6 devices in the daisy chain (3 groups of 2 stackable mode) with 30 scan lines. When a data transmission efficiency of 70% is assumed (since there could be some idle time between transmitted CCSI commands), the minimum required CCSI data rate is 7.04Mbit/s. Therefore, the CCSI_DATA_RATE in register CCSICTRL is set to 8Mbit/s.

The SPI frequency is gerenally set to be in the similar range as the CCSI data rate. Therefore, in this application example the SPI frequency is set to 8MHz. The next step is to determine the TXFFLVL. TI recommends to set TXFFLVL larger than the maximum number of words that are forwarded for one CCSI command. The maximum number of words happen for a data write command with non-broadcast, e.g. write SRAM command. For this command, the number of words are equal to 3 times the number of cascaded devices plus one head byte. In this application example, the maximum number of words is 19 (3 x 6 + 1) words. Note that when SPI command FWD_WR_CRC is used, the TXFFLVL is ignored, and the forwarding only starts when the CRC word is correct. In addition, during the forwarding by the CCSI controller, the next SPI forward command can already be transmitted by the SPI controller because of the CCSI command queue in the LP5899-Q1.

8.2.2.1 Programming Procedure

Figure 8-2 depicts a typical device programming flow. The flow is similar to the LP589x-Q1 device family with several additional initialization steps to configure the LP5899-Q1. After power up VCC and waiting until the device is in Normal state (which means that the OTP CRC is correct), the LP5899-Q1 is initialized and the FLAG_POR has to be cleared (by setting CLR_FLAG) to allow forwarding of commands. Afterwards, the commands can be forwarded to the LP589x-Q1 daisy chain.

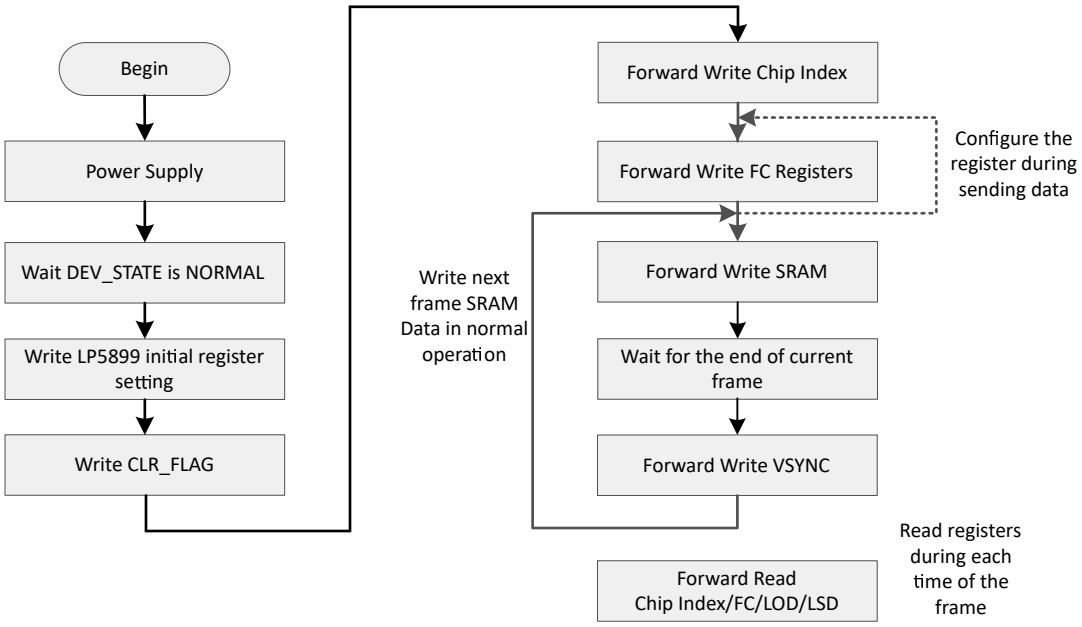


Figure 8-2. Programming Procedure

8.2.3 Application Curves

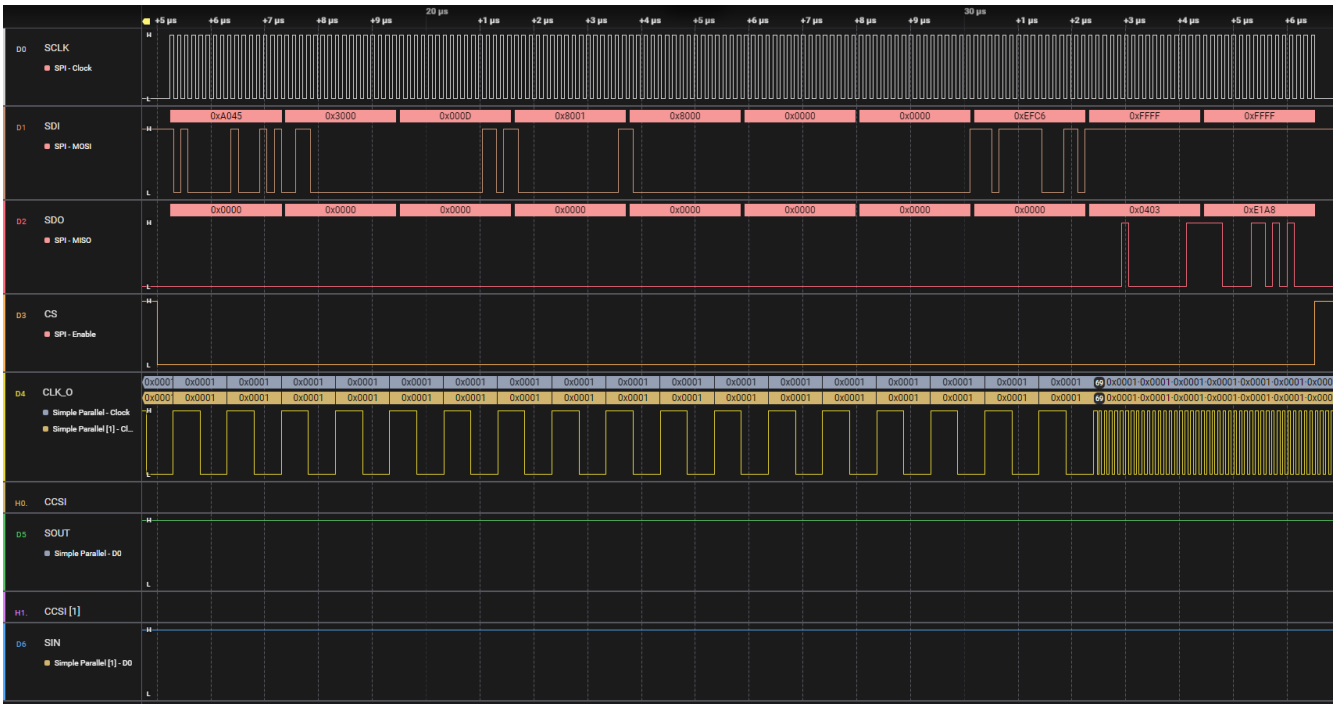


Figure 8-3. Write initial register settings example

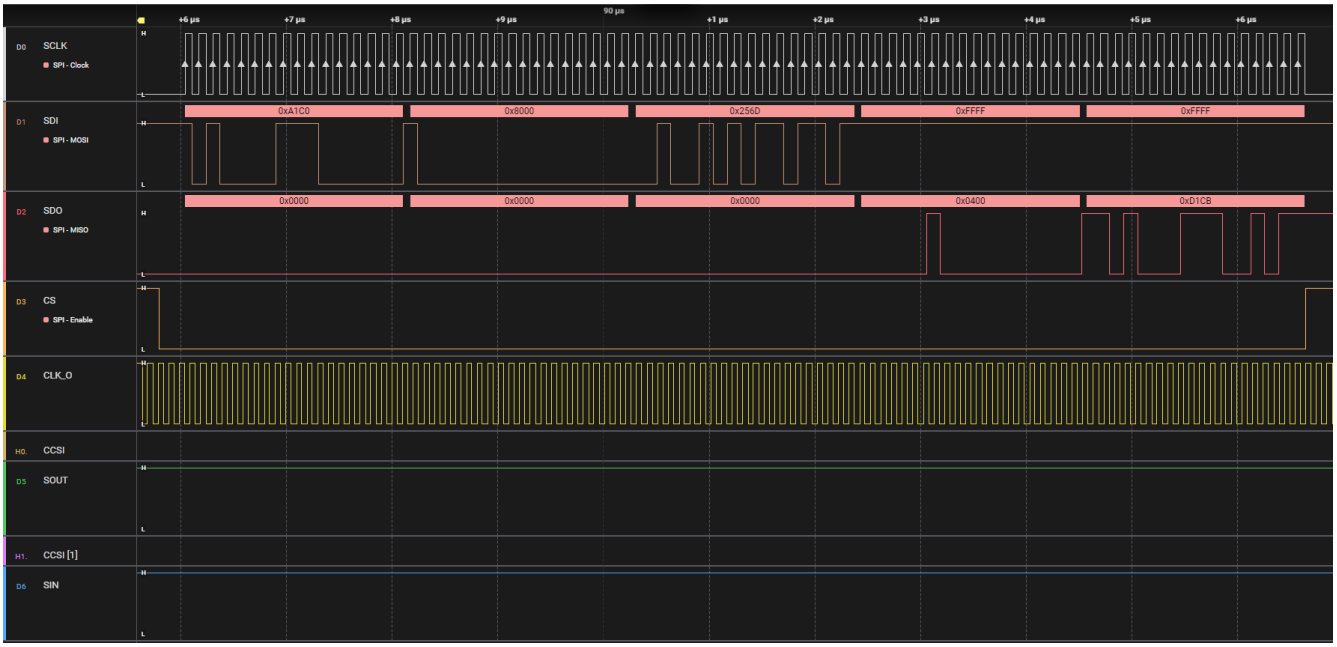


Figure 8-4. Write CLR_FLAG example

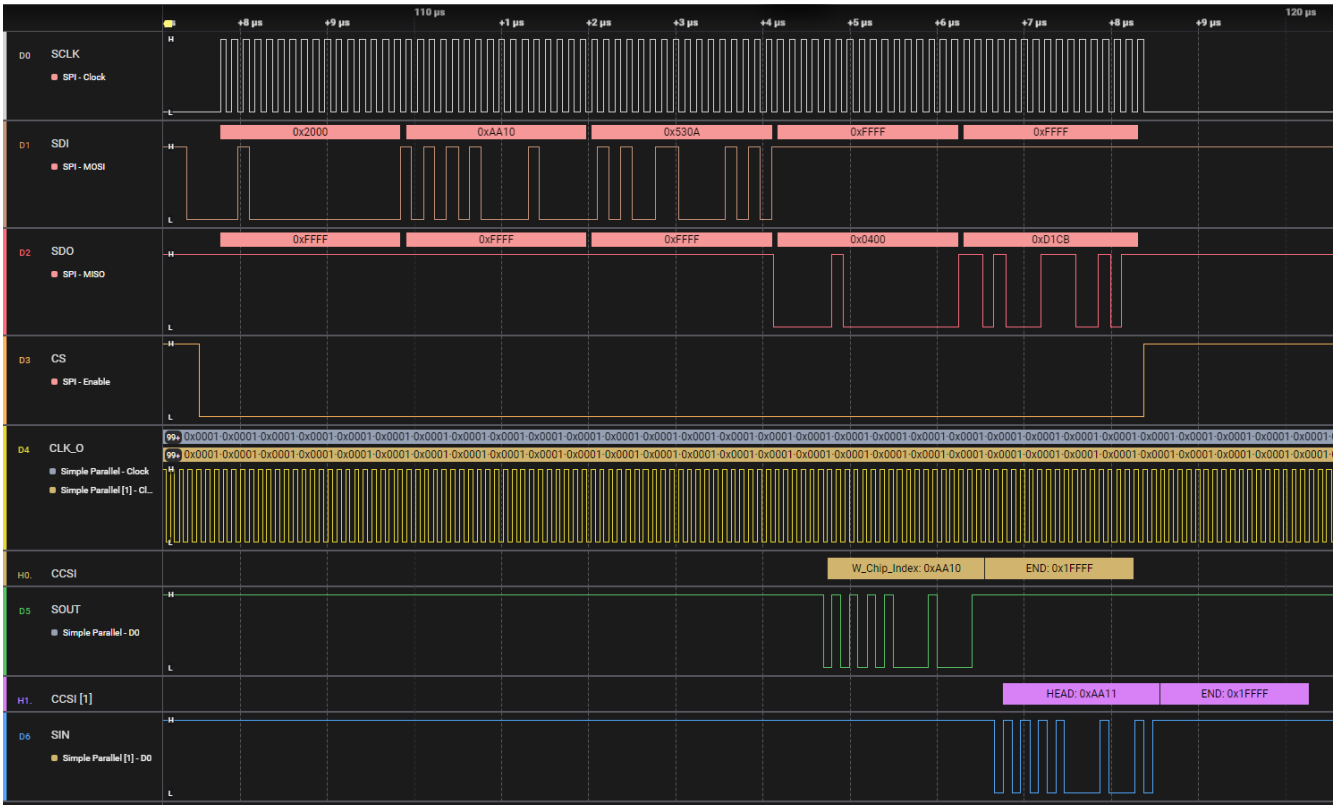


Figure 8-5. Forward Write Chip Index command for 1 LED driver in the daisy chain example

8.3 Power Supply Recommendations

The device is designed to operate from 2.5V to 5.5V VCC voltage supply. This input supply must be well regulated. The resistance of the VCC supply rail must be low enough that input current transient does not cause the device VCC supply voltage to drop below the maximum V_{UVR} voltage.

8.4 Layout

8.4.1 Layout Guidelines

The LP5899-Q1 only requires two external components. Place the capacitor for the VCC input as close as possible to the VCC pin. The FAULT pin is an open drain output. When the FAULT pin is connected to the Controller, an external pull-up resistor is required.

8.4.2 Layout Example

Figure 8-6 depicts an example of a layout for the DYY package. Both GND pins are connected together. The layout shows that pin 10 can be used for routing purposes. Also pin 5 can be used, but that is not shown in this example.

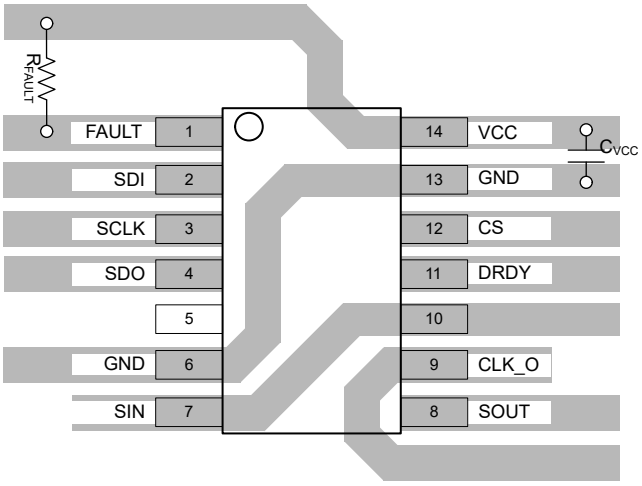


Figure 8-6. LP5899-Q1 Layout Example

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Support

9.2 Documentation Support

9.2.1 Related Documentation

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

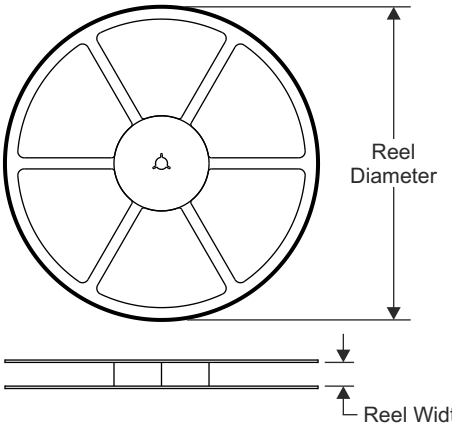
DATE	REVISION	NOTES
October 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

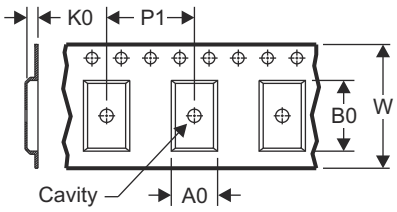
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information

REEL DIMENSIONS

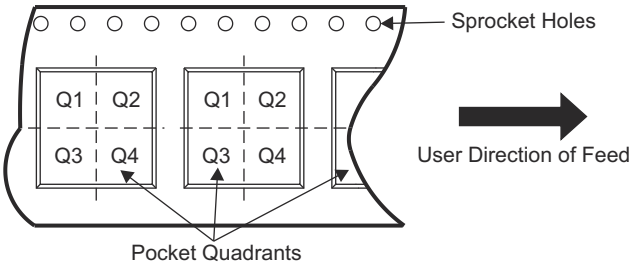


TAPE DIMENSIONS



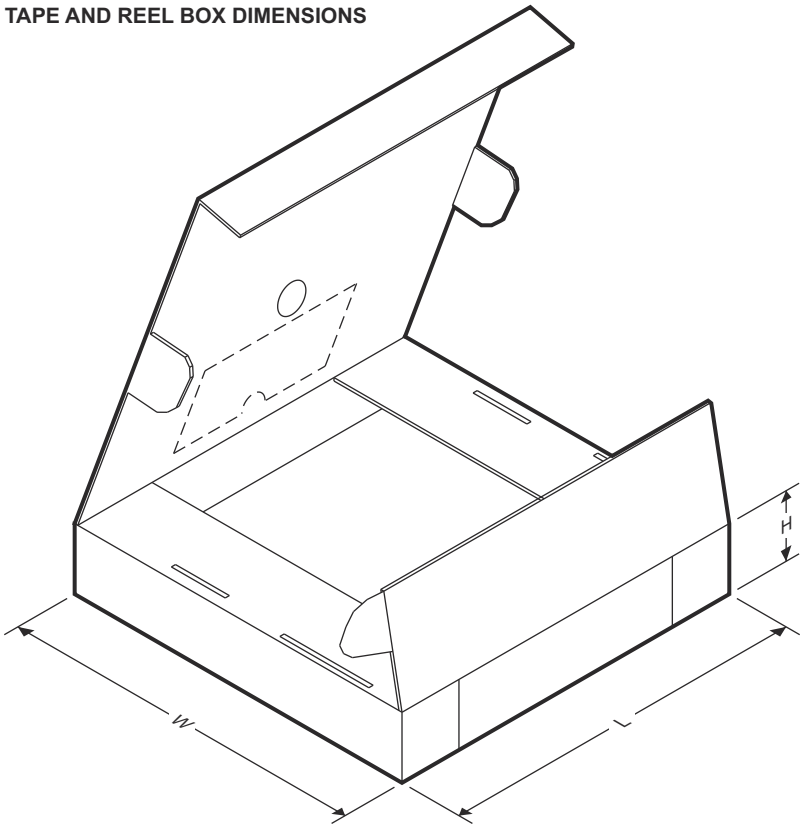
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP5899QDYYRQ1	SOT-23-THN	DYY	14									
LP5899QDRRRQ1	WSON	DRR	12									

TAPE AND REEL BOX DIMENSIONS



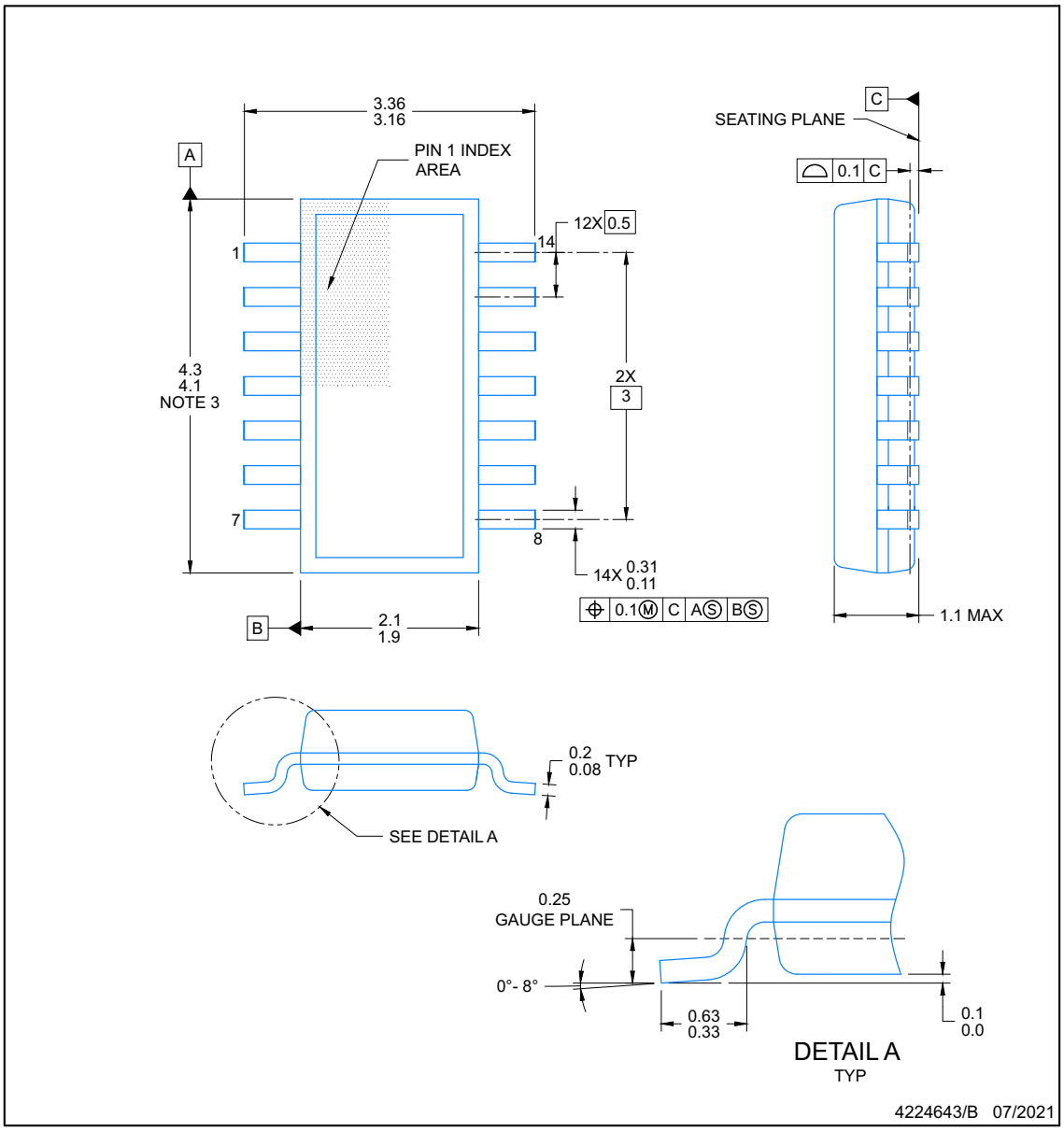
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP5899QDYYRQ1	SOT-23-THN	DYY	14				
LP5899QDRRRQ1	WSON	DRR	12				

11.2 Mechanical Data

PACKAGE OUTLINE

DYY0014A **SOT-23-THIN - 1.1 mm max height**

PLASTIC SMALL OUTLINE



NOTES:

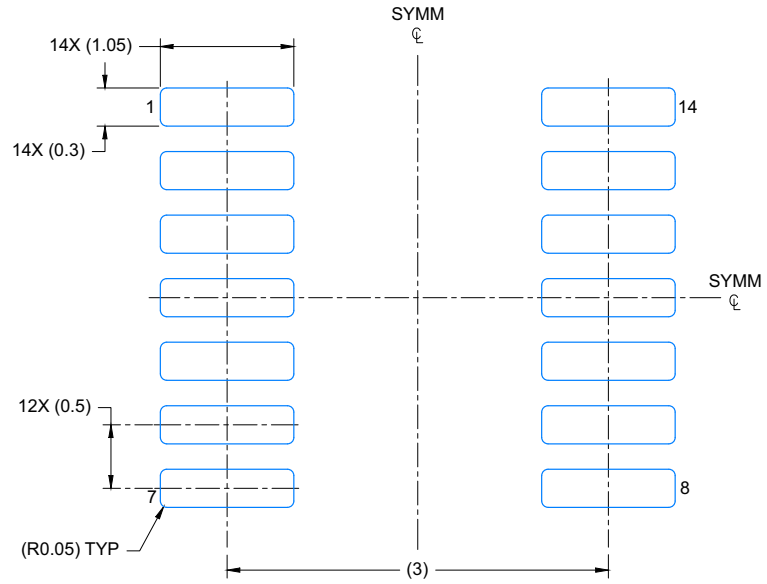
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB

EXAMPLE BOARD LAYOUT

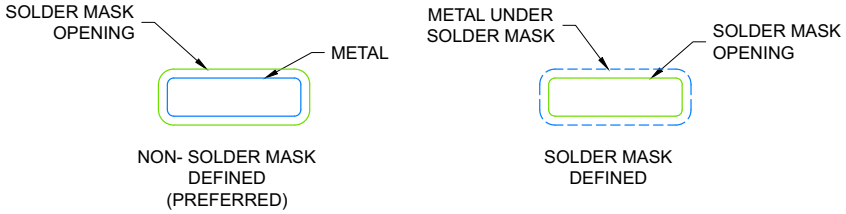
DYY0014A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224643/B 07/2021

NOTES: (continued)

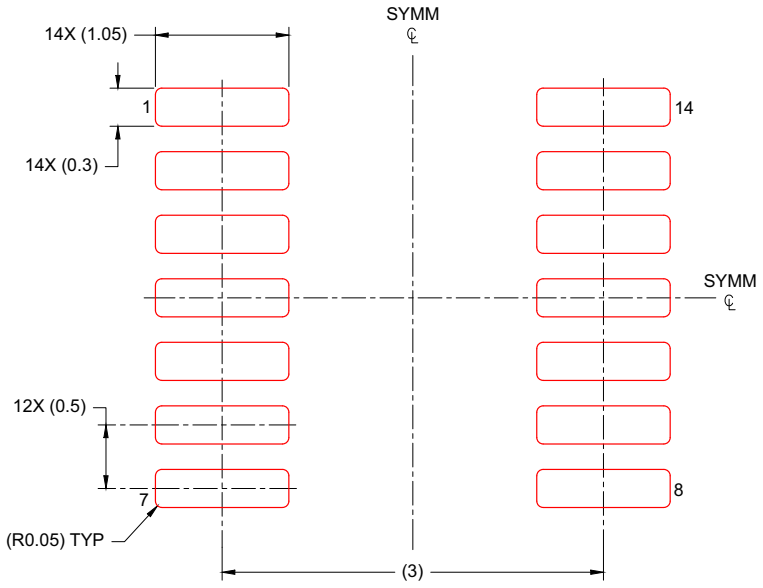
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DYY0014A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/B 07/2021

NOTES: (continued)

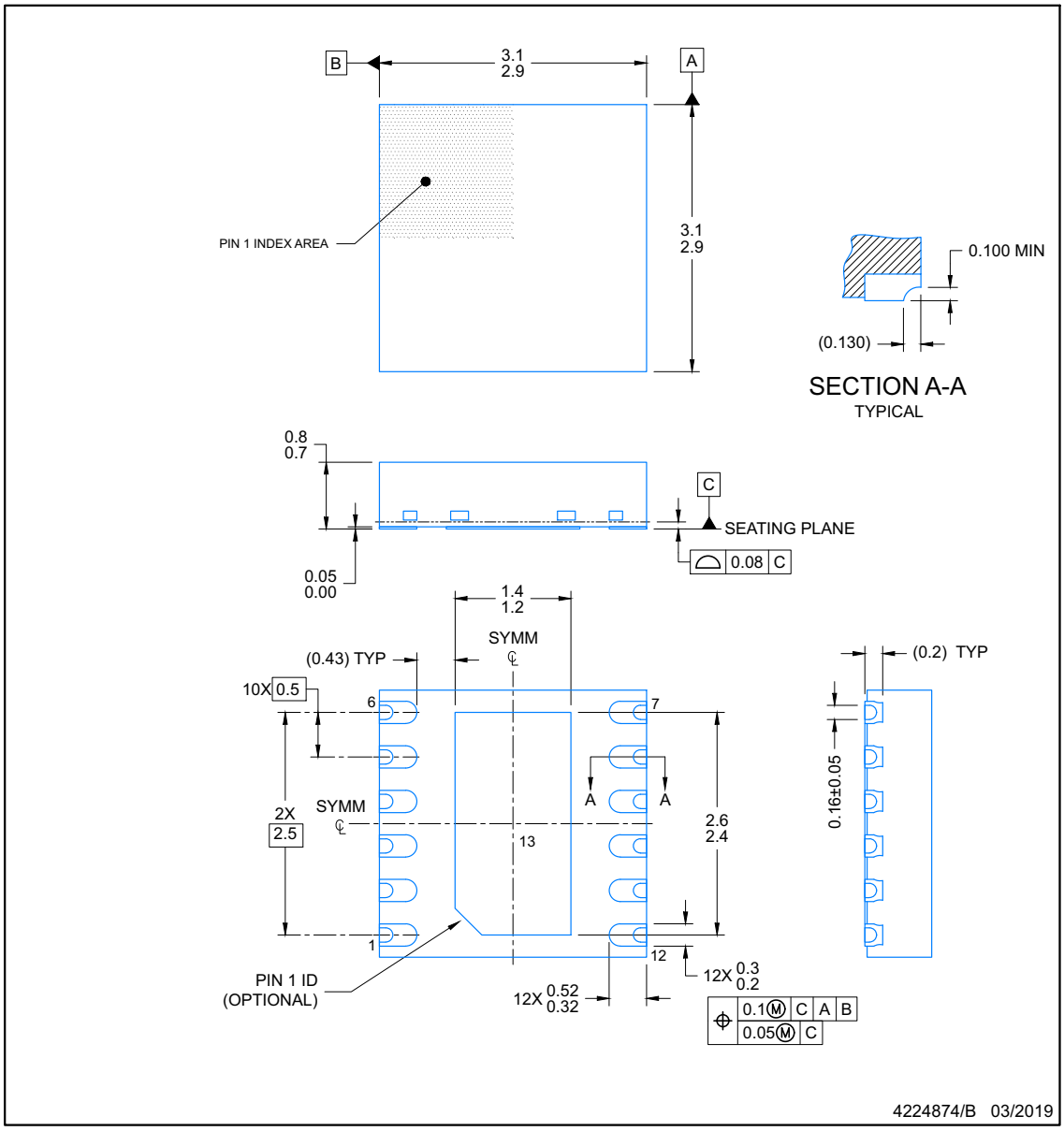
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRR0012E

WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

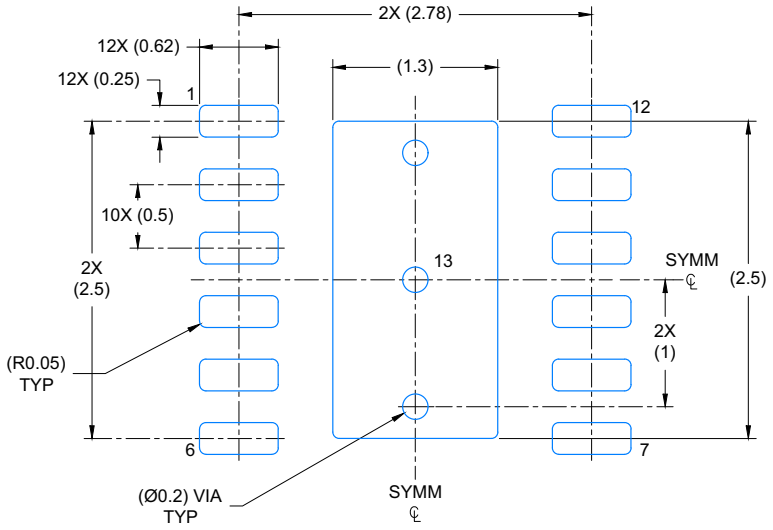
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

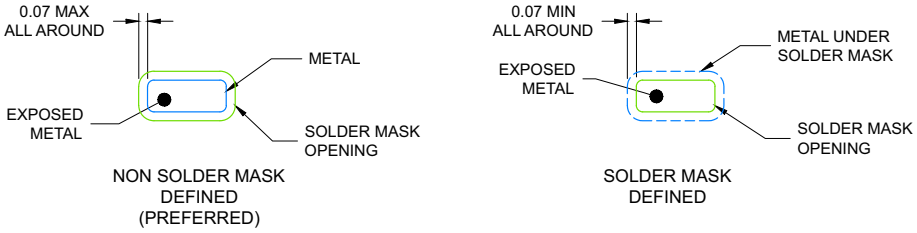
DRR0012E

WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224874/B 03/2019

NOTES: (continued)

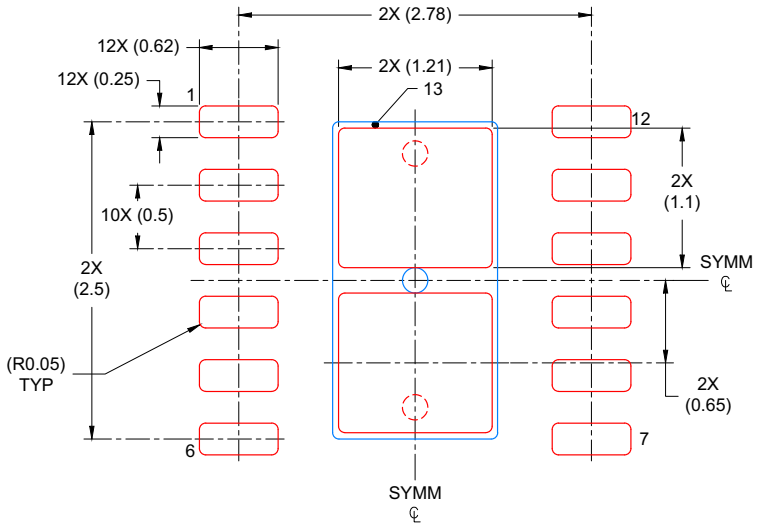
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRR0012E

WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED COVERAGE BY AREA
SCALE: 20X

4224874/B 03/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP5899QDRRRQ1	ACTIVE	WSON	DRR	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	5899NQ	Samples
LP5899QDYYRQ1	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L5899TQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

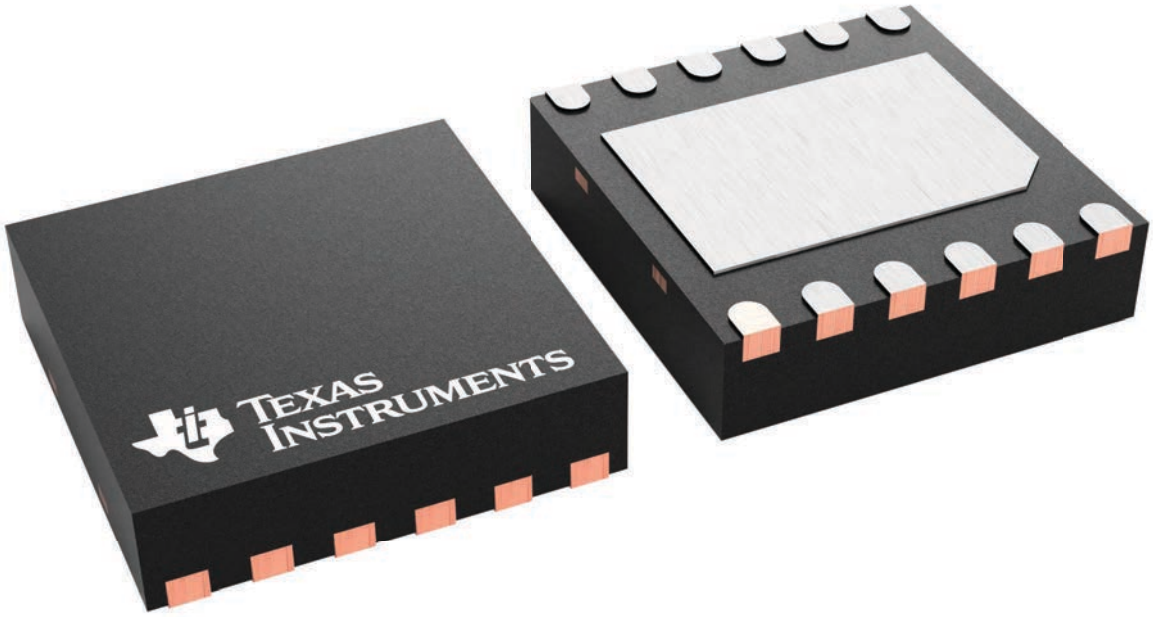
DRR 12

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



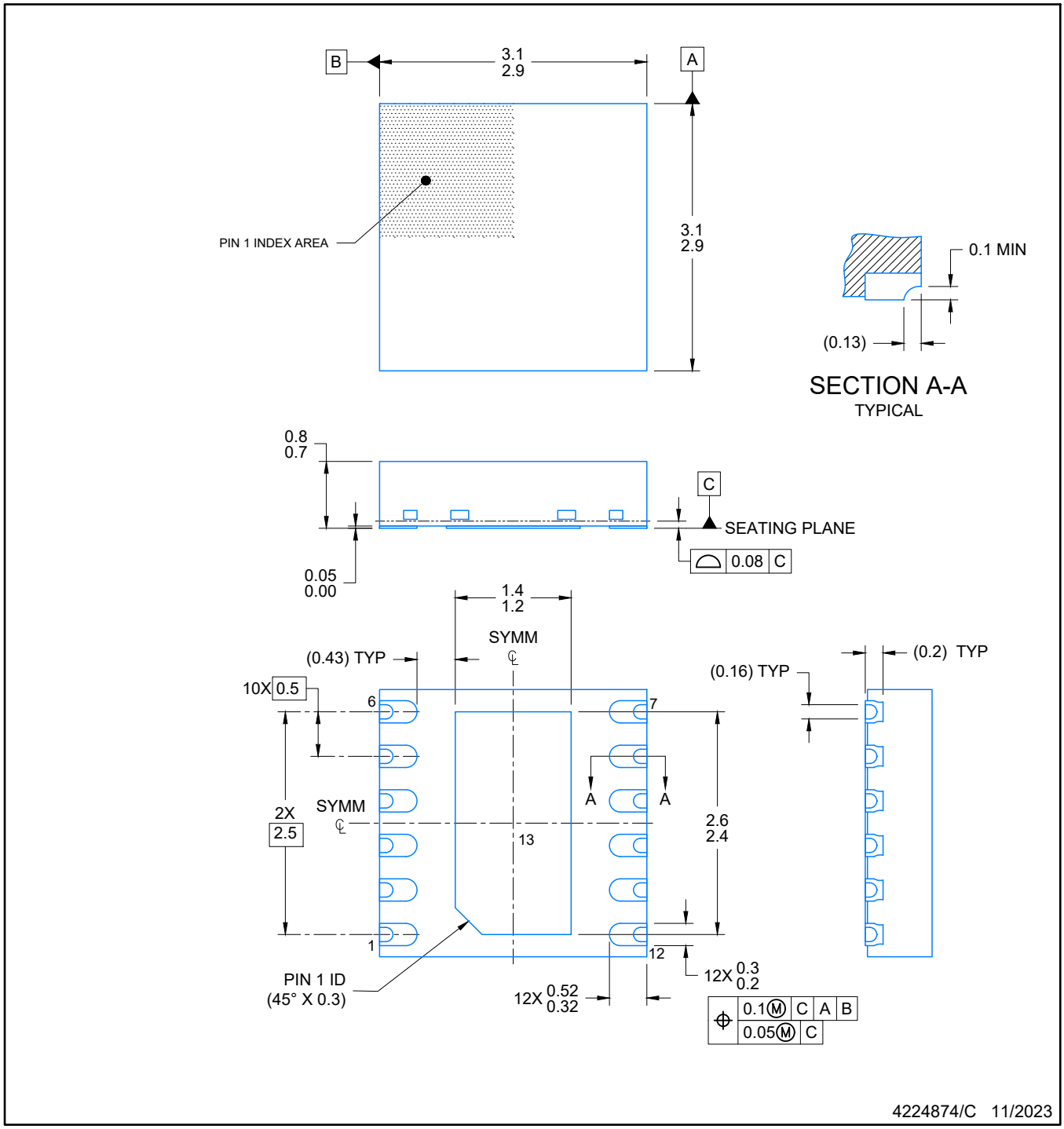
4223490/B

PACKAGE OUTLINE

DRR0012E

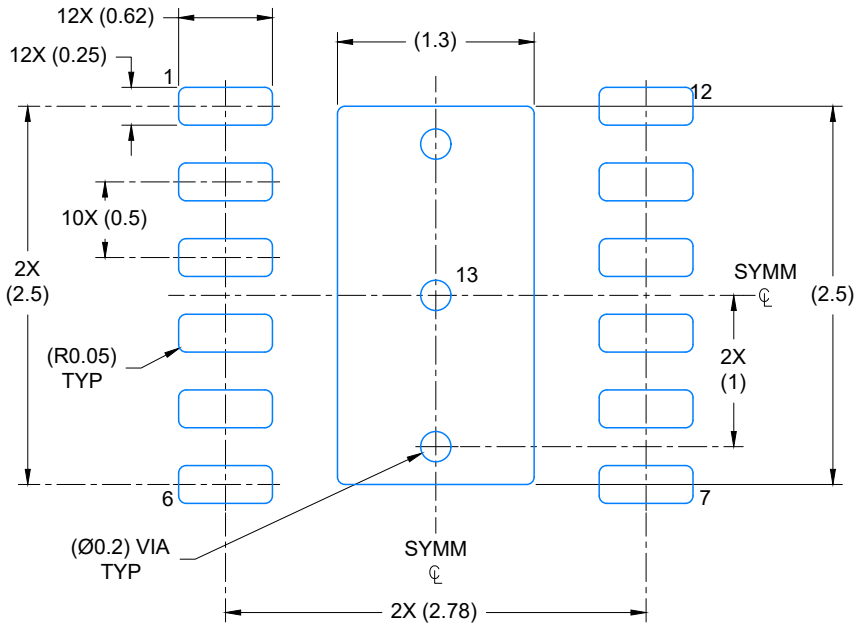
WSON - 0.8 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

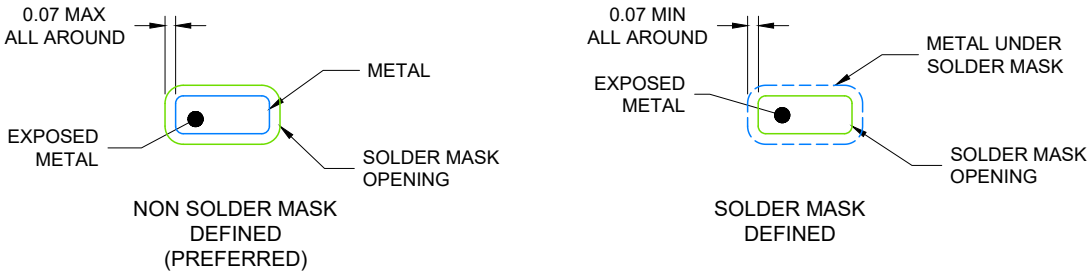


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

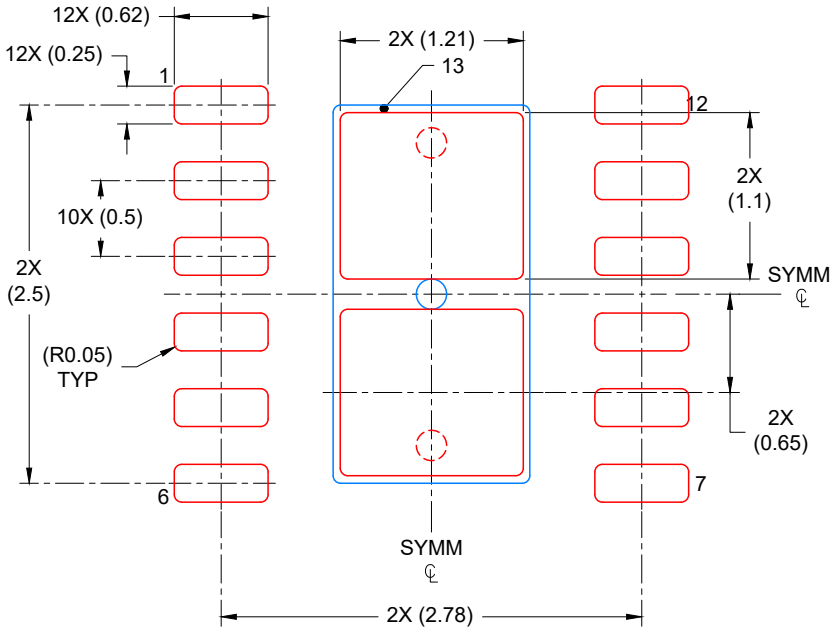


SOLDER MASK DETAILS

4224874/C 11/2023

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
82% PRINTED COVERAGE BY AREA
SCALE: 20X

4224874/C 11/2023

NOTES: (continued)

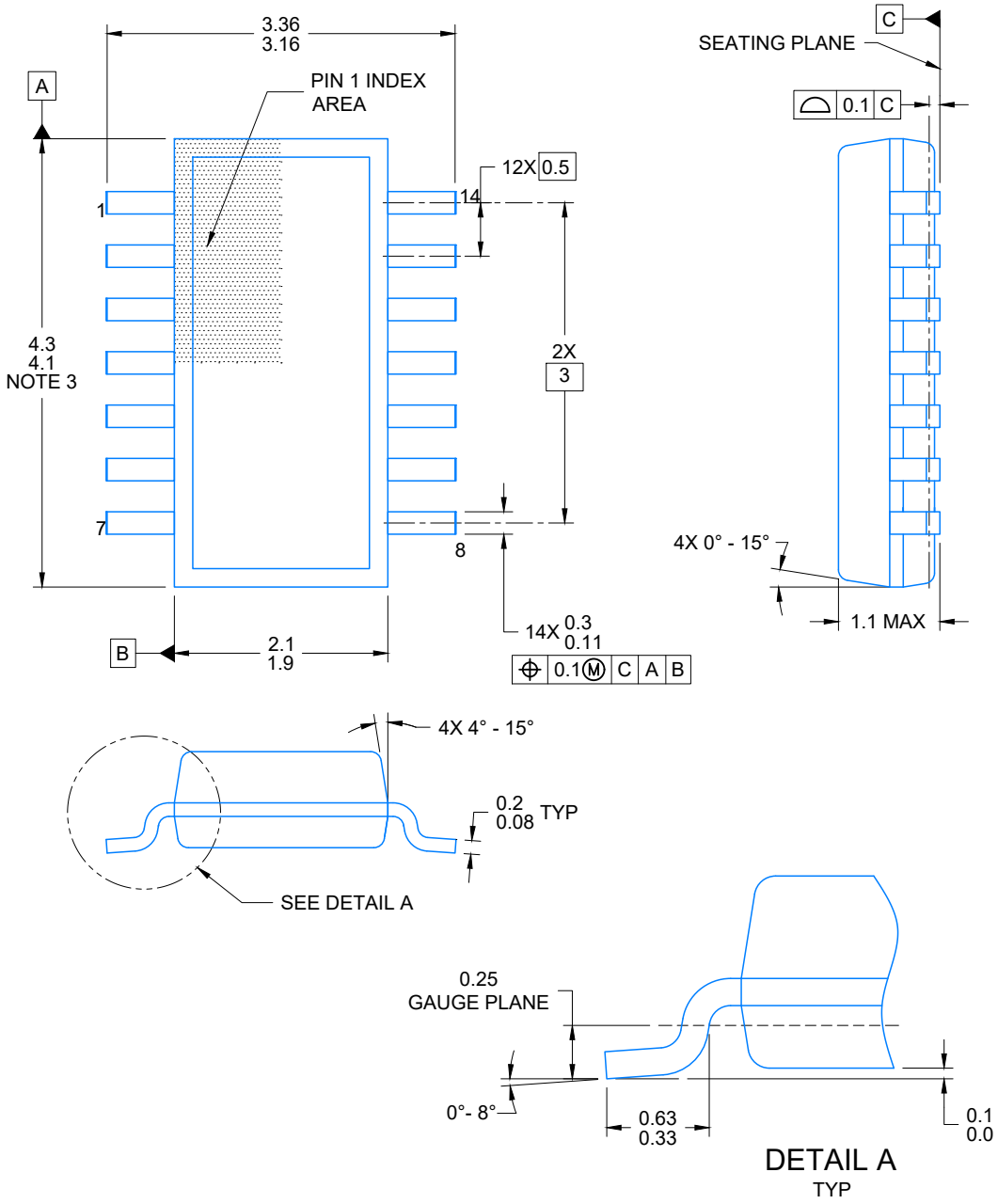
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYY0014A

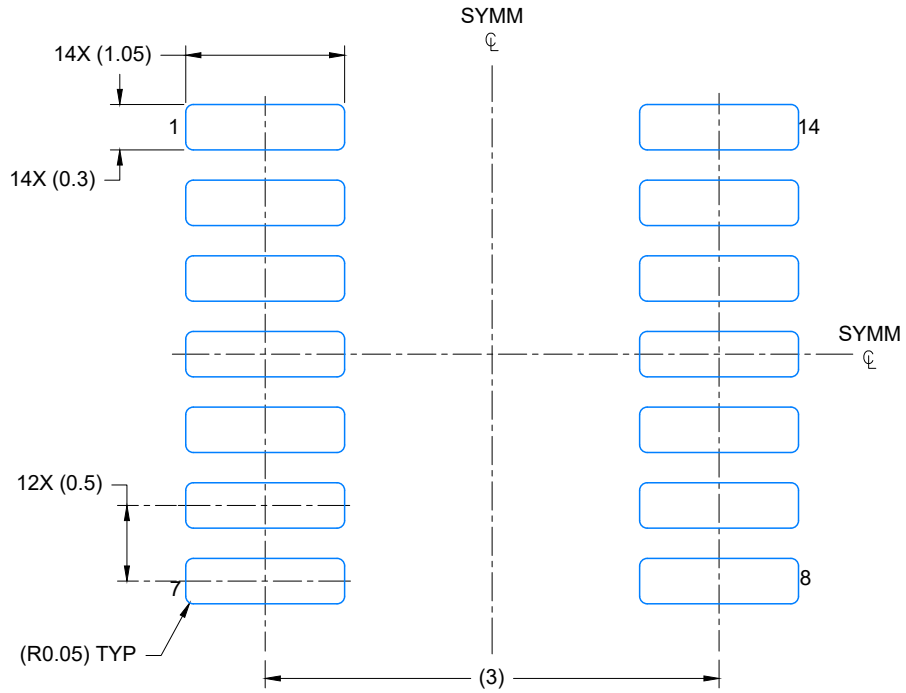
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

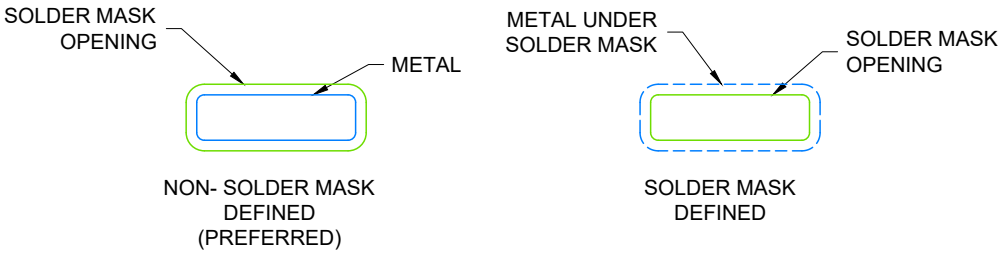


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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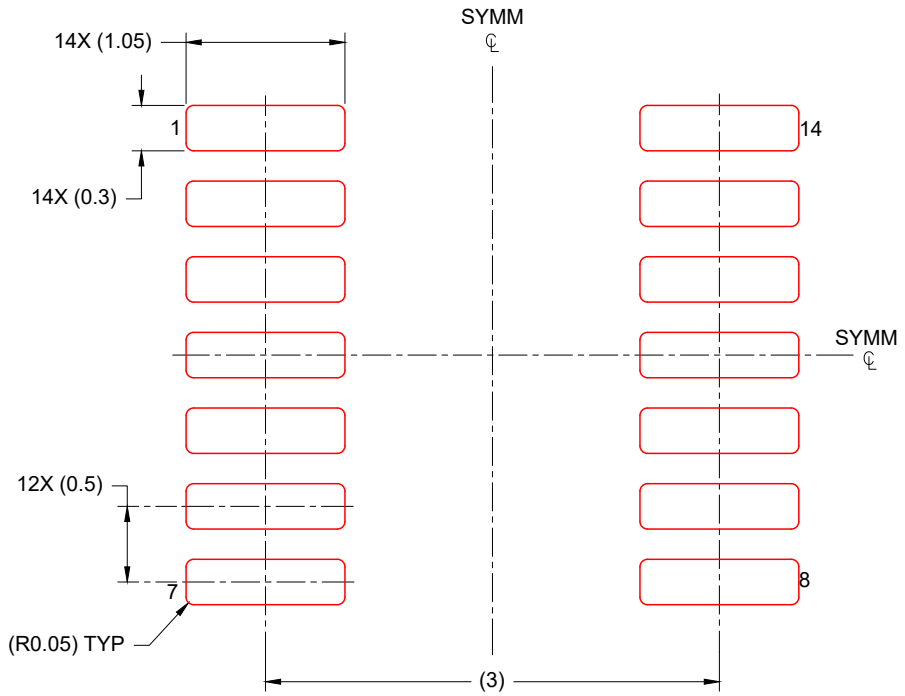
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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