TEXAS INSTRUMENTS
OPA388-Q1, OPA2388-Q1
SBOS989A – AUGUST 2020 – REVISED NOVEMBER 2021

OPAx388-Q1 Automotive, Precision, Zero-Drift, Zero-Crossover, True Rail-to-Rail, Input/Output Operational Amplifiers

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional-Safety Capable
  - Documentation available to aid functional safety system design (OPA388-Q1)
  - Documentation available to aid functional safety system design (OPA2388-Q1: VSSOP)
- Zero drift: ±0.005 µV/°C
- Zero crossover: 140-dB CMRR true RRIO
- Low noise: 7.0 nV/√Hz at 1 kHz
- No 1/f noise: 140 nV_{PP} (0.1 Hz to 10 Hz)
- Fast settling: 2 µs (1 V to 0.01%)
- Gain bandwidth: 10 MHz
- Single supply: 2.5 V to 5.5 V
- Dual supply: ±1.25 V to ±2.75 V
- True rail-to-rail input
- EMI and RFI filtered inputs
- Industry-standard packages: VSSOP-8, SOT-23-5

2 Applications

- HEV/EV inverter and motor control
- Battery management system (BMS)
- DC/DC converter
- Onboard (OBC) and wireless charger

3 Description

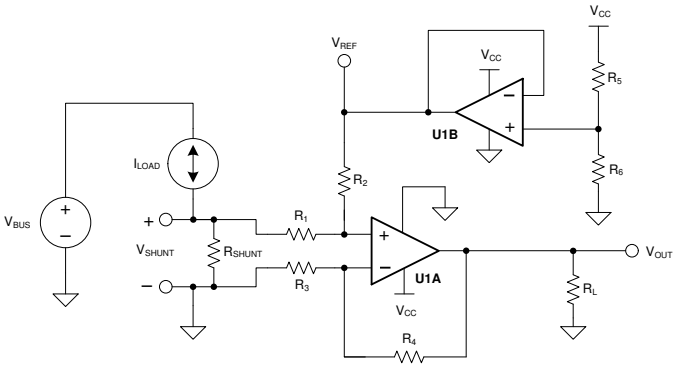
The OPA388-Q1 and OPA2388-Q1 (OPAx388-Q1) are automotive, low-noise, fast-settling, zero-drift, precision operational amplifiers that provide rail-to-rail input and output operation. Excellent ac performance, combined with only 0.25 µV of offset and 0.005 µV/°C of drift over temperature, make the OPAx388-Q1 a great choice for driving high-resolution, analog-to-digital converters (ADCs) with high accuracy. Zero-crossover technology minimizes any offset change over the common-mode range. The combination of low drift and very low 1/f noise allow the OPAx388-Q1 to monitor and detect faulty conditions without compromising signal integrity.

These devices are specified over the industrial temperature range of –40°C to +125°C.

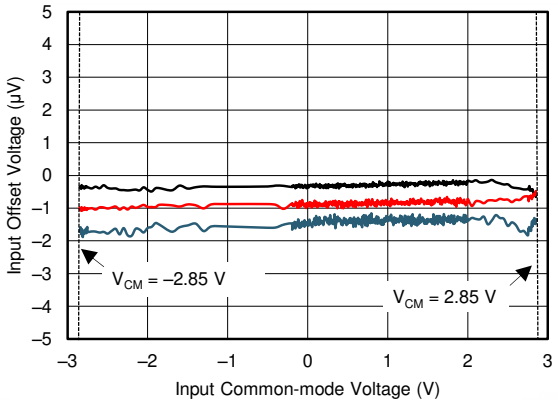
Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
OPA388-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
OPA2388-Q1	SOIC (8) - Preview	4.90 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



The OPA388-Q1 in a Bidirectional Current Shunt Monitor



The OPA388-Q1 Features Ultra-Low Offset Across the Full Common-Mode Range

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (August 2020) to Revision A (November 2021)	Page
• Added OPA2388-Q1 production data (active) device and associated content	1

5 Pin Configuration and Functions

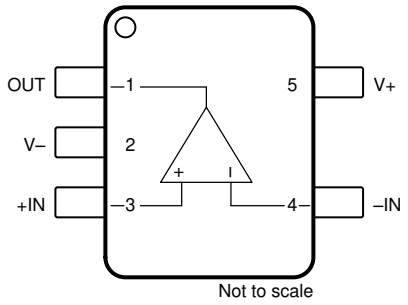


Figure 5-1. OPA388-Q1 DBV (5-Pin SOT-23) Package, Top View

Pin Functions: OPA388-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN	4	Input	Inverting input
+IN	3	Input	Noninverting input
NC	—	—	No internal connection (can be left floating)
OUT	1	Output	Output
V–	2	Power	Negative (lowest) power supply
V+	5	Power	Positive (highest) power supply

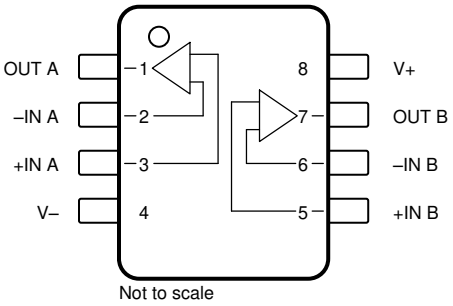


Figure 5-2. OPA2388-Q1 D (8-Pin SOIC, Preview) and DGK (8-Pin VSSOP) Packages, Top View

Pin Functions: OPA2388-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V–	4	Power	Negative (lowest) power supply
V+	8	Power	Positive (highest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single-supply		6	V
		Dual-supply		±3	
	Signal input pins voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Signal input pins current			±10	mA
	Output short circuit(2)		Continuous	Continuous	
T_A	Operating temperature		–55	150	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C5	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	Single-supply	2.5		5.5	V
		Dual-supply	±1.25		±2.75	
T_A	Specified temperature		–40		125	°C

6.4 Thermal Information: OPA388-Q1

THERMAL METRIC[1]		OPA388-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	145.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	24.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Thermal Information: OPA2388-Q1

THERMAL METRIC[1]		OPA2388-Q1 DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	165	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	87	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	85	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Electrical Characteristics

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, V_S = ±1.25 V to ±2.75 V (2.5 V to 5.5 V), and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OPA388-Q1			±0.25	±5	µV
		OPA2388-Q1			±1.5	±5	
		T_A = –40°C to +125°C				±7.5	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to +125°C			±0.005	±0.05	µV/°C
PSRR	Power-supply rejection ratio	T_A = –40°C to +125°C			±0.1	±1	µV/V
INPUT BIAS CURRENT							
I_B	Input bias current	R_{IN} = 100 kΩ			±30	±350	pA
			T_A = 0°C to +85°C			±400	
			T_A = –40°C to +125°C			±700	
I_{OS}	Input offset current	R_{IN} = 100 kΩ				±700	pA
			T_A = 0°C to +85°C			±800	
			T_A = –40°C to +125°C			±800	
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			0.14		$µV_{PP}$
e_N	Input voltage noise density	f = 10 Hz			7		nV/√Hz
		f = 100 Hz			7		
		f = 1 kHz			7		
		f = 10 kHz			7		
I_N	Input current noise density	f = 1 kHz			100		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V	V_S = ±1.25 V	124	138		dB
			V_S = ±2.75 V	124	140		
		(V–) < V_{CM} < (V+) + 0.1 V, T_A = –40°C to +125°C	V_S = ±1.25 V	114	134		
		(V–) – 0.05 V < V_{CM} < (V+) + 0.1 V, T_A = –40°C to +125°C	V_S = ±2.75 V	124	140		
INPUT IMPEDANCE							
z_{id}	Differential input impedance				100 || 2		MΩ || pF
z_{ic}	Common-mode input impedance				60 || 4.5		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.15 V < V_O < (V+) – 0.15 V		126	148		dB
			T_A = –40°C to +125°C	120	126		
		(V–) + 0.25 V < V_O < (V+) – 0.25 V, R_{LOAD} = 2 kΩ		126	148		
		(V–) + 0.30 V < V_O < (V+) – 0.30 V, R_{LOAD} = 2 kΩ	T_A = –40°C to +125°C	120	148		

6.6 Electrical Characteristics (continued)

at T_A = 25°C, V_{CM} = V_{OUT} = V_S / 2, V_S = ±1.25 V to ±2.75 V (2.5 V to 5.5 V), and R_{LOAD} = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE							
GBW	Unity-gain bandwidth				10		MHz
SR	Slew rate	G = 1, 4-V step			5		V/µs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 1 V_{RMS}			0.0005%		
t_S	Settling time	V_S = ±2.5 V, G = 1, 1-V step	To 0.1%		0.75		µs
			To 0.01%		2		
t_{OR}	Overload recovery time	V_{IN} × G = V_S			10		µs
OUTPUT							
V_O	Voltage output swing from rail	Positive rail	No load		1	15	mV
					5	20	
			R_{LOAD} = 2 kΩ		20	50	
		Negative rail	No load		5	15	
					10	20	
			R_{LOAD} = 2 kΩ		40	60	
		T_A = –40°C to +125°C, both rails, R_{LOAD} = 10 kΩ			10	25	
I_{SC}	Short-circuit current	V_S = 5.5 V			±60		mA
		V_S = 2.5 V			±30		
C_{LOAD}	Capacitive load drive				See Figure 6-25		
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A, see Figure 6-24			100		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = ±1.25 V (V_S = 2.5 V), I_O = 0 A			1.7	2.4	mA
			T_A = –40°C to +125°C		1.7	2.4	
		V_S = ±2.75 V (V_S = 5.5 V), I_O = 0 A			1.9	2.6	
			T_A = –40°C to +125°C		1.9	2.6	

6.7 Typical Characteristics

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

Table 6-1. Table of Graphs

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 6-1
Offset Voltage Drift Distribution From –40°C to +125°C	Figure 6-2
Offset Voltage vs Temperature	Figure 6-3
Offset Voltage vs Common-Mode Voltage	Figure 6-4
Offset Voltage vs Power Supply	Figure 6-5
Offset Voltage Long Term Drift	Figure 6-6
Open-Loop Gain and Phase vs Frequency	Figure 6-7
Closed-Loop Gain and Phase vs Frequency	Figure 6-8
Input Bias Current vs Common-Mode Voltage	Figure 6-9
Input Bias Current vs Temperature	Figure 6-10
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 6-11
CMRR and PSRR vs Frequency	Figure 6-12
CMRR vs Temperature	Figure 6-13
PSRR vs Temperature	Figure 6-14
0.1-Hz to 10-Hz Noise	Figure 6-15
Input Voltage Noise Spectral Density vs Frequency	Figure 6-16
THD+N Ratio vs Frequency	Figure 6-17
THD+N vs Output Amplitude	Figure 6-18
Spectral Content	Figure 6-19, Figure 6-20
Quiescent Current vs Supply Voltage	Figure 6-21
Quiescent Current vs Temperature	Figure 6-22
Open-Loop Gain vs Temperature	Figure 6-23
Open-Loop Output Impedance vs Frequency	Figure 6-24
Small-Signal Overshoot vs Capacitive Load (10-mV Step)	Figure 6-25
No Phase Reversal	Figure 6-26
Positive Overload Recovery	Figure 6-27
Negative Overload Recovery	Figure 6-28
Small-Signal Step Response (10-mV Step)	Figure 6-29, Figure 6-30
Large-Signal Step Response (4-V Step)	Figure 6-31 , Figure 6-32
Settling Time	Figure 6-33, Figure 6-34
Short-Circuit Current vs Temperature	Figure 6-35
Maximum Output Voltage vs Frequency	Figure 6-36
EMIRR vs Frequency	Figure 6-37

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

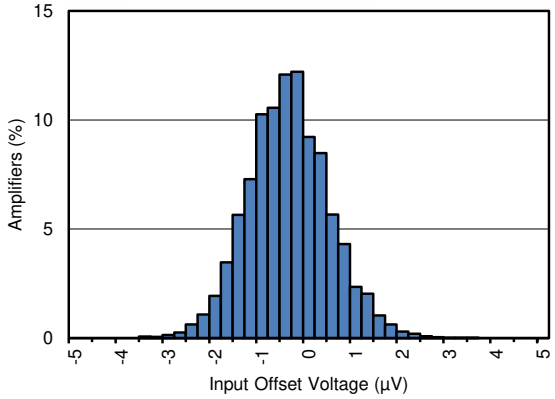
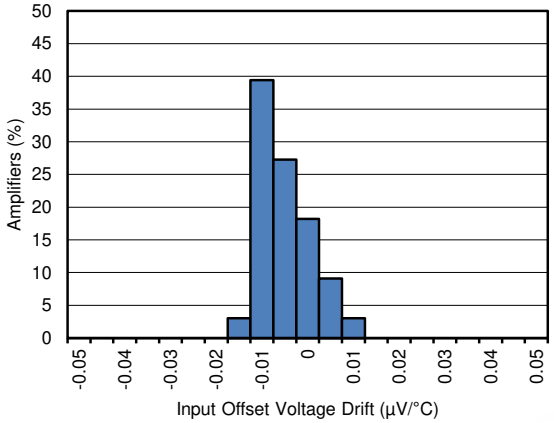


Figure 6-1. Offset Voltage Production Distribution



T_A = –40°C to +125°C

Figure 6-2. Offset Voltage Drift Distribution

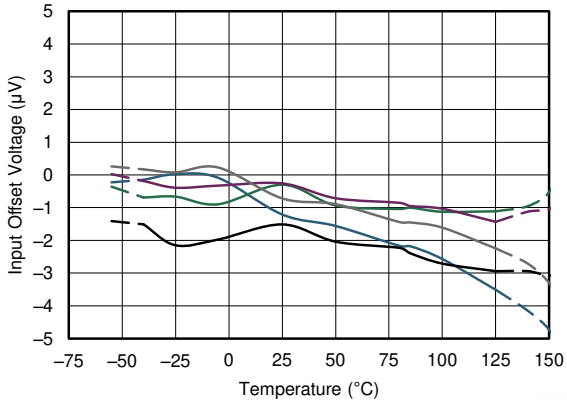


Figure 6-3. Offset Voltage vs Temperature

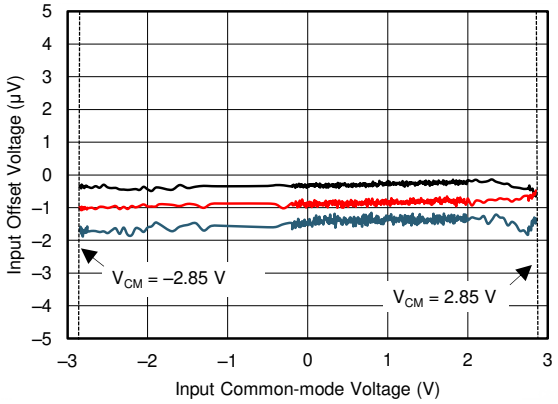


Figure 6-4. Offset Voltage vs Common-Mode Voltage

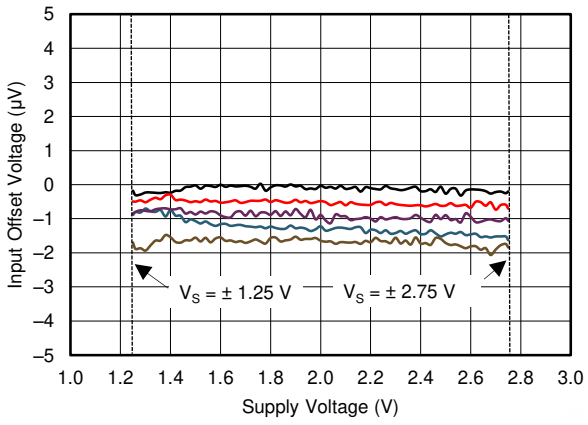
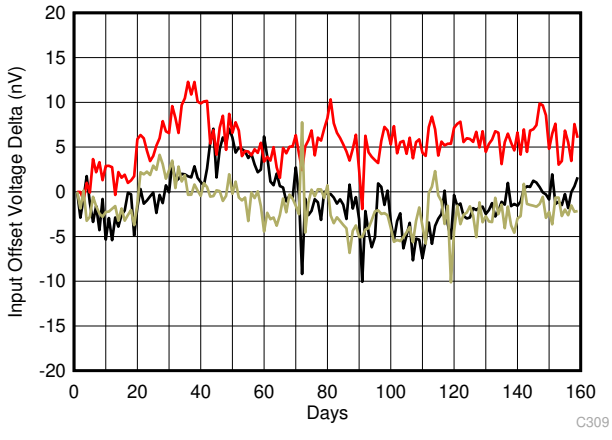


Figure 6-5. Offset Voltage vs Supply Voltage



3 typical units

Figure 6-6. Offset Voltage Long Term Drift

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

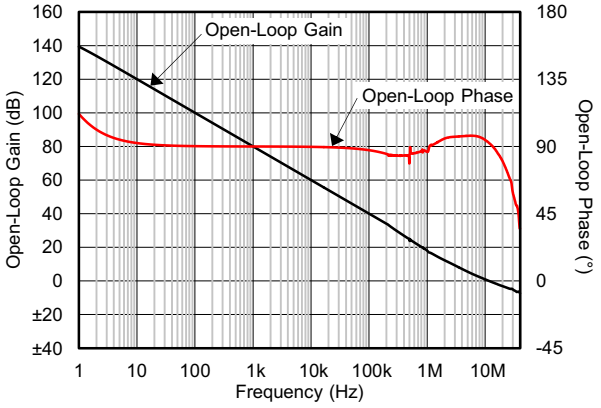


Figure 6-7. Open-Loop Gain and Phase vs Frequency

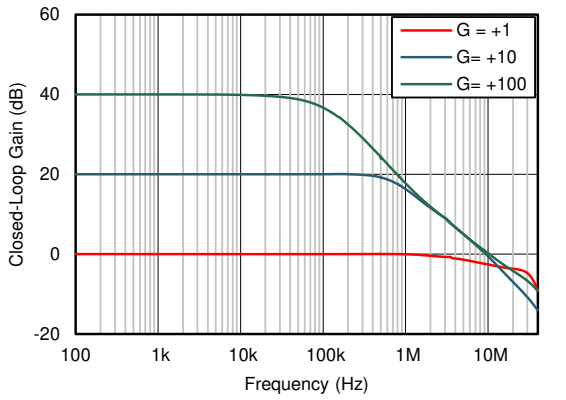


Figure 6-8. Closed-Loop Gain and Phase vs Frequency

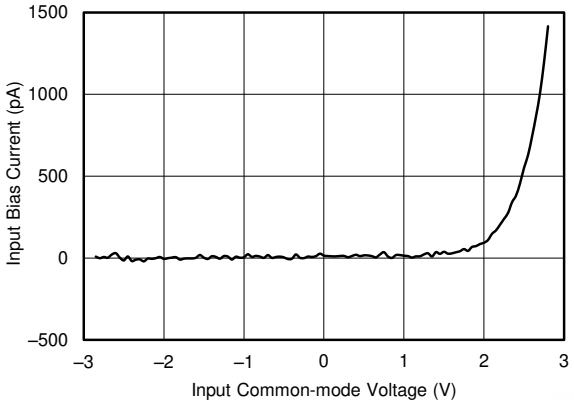


Figure 6-9. Input Bias Current vs Common-Mode Voltage

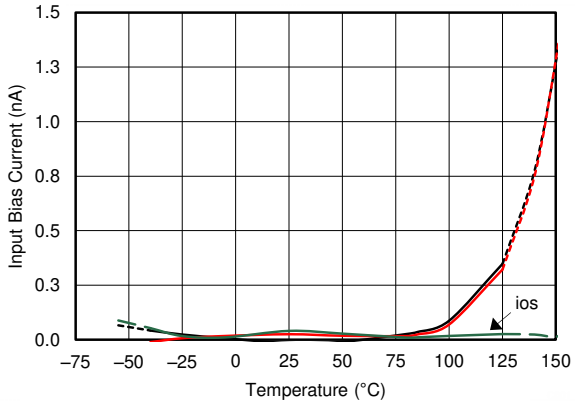


Figure 6-10. Input Bias Current vs Temperature

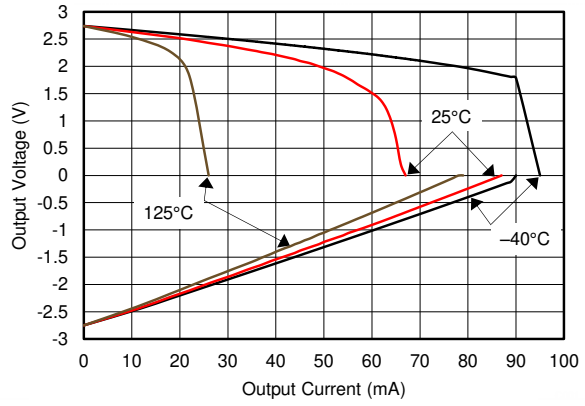


Figure 6-11. Output Voltage Swing vs Output Current (Maximum Supply)

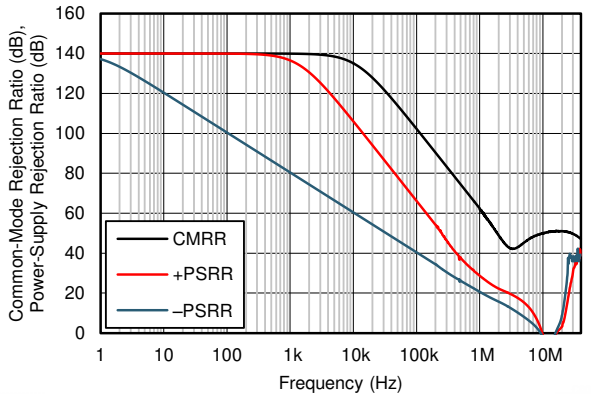


Figure 6-12. CMRR and PSRR vs Frequency

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

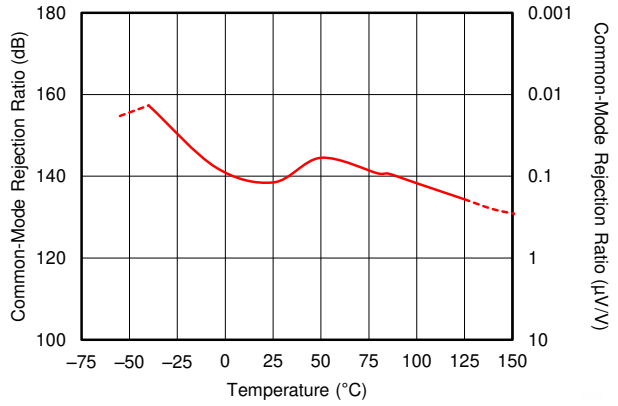


Figure 6-13. CMRR vs Temperature

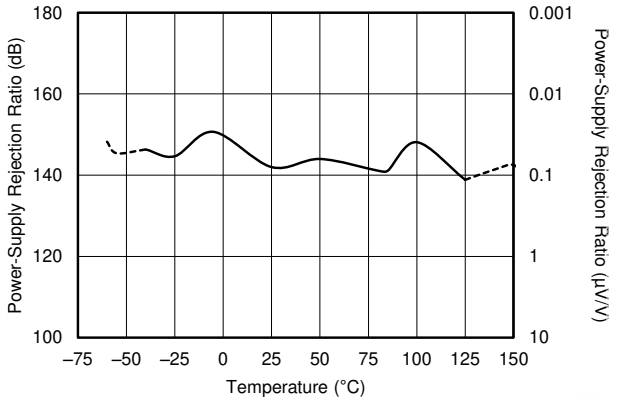


Figure 6-14. PSRR vs Temperature

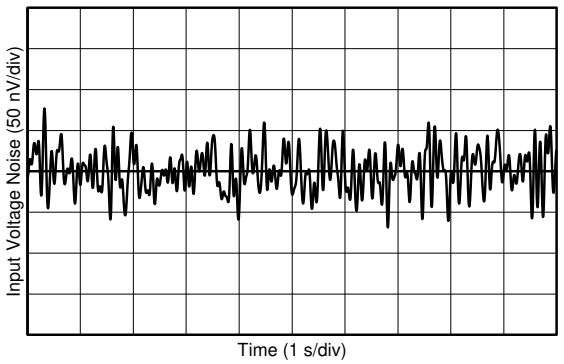


Figure 6-15. 0.1-Hz to 10-Hz Noise

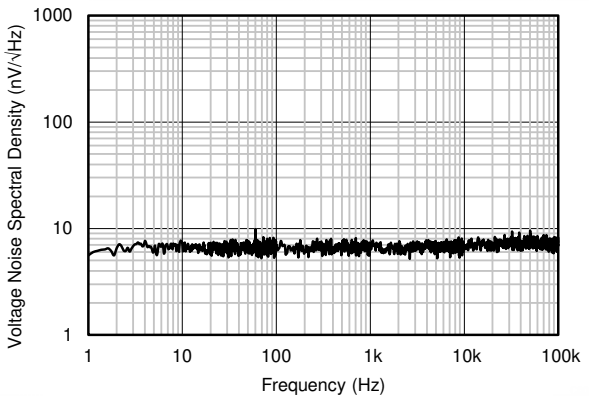


Figure 6-16. Input Voltage Noise Spectral Density vs Frequency

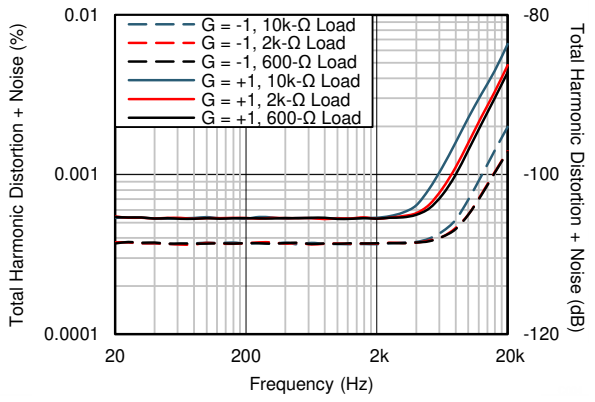


Figure 6-17. THD+N Ratio vs Frequency

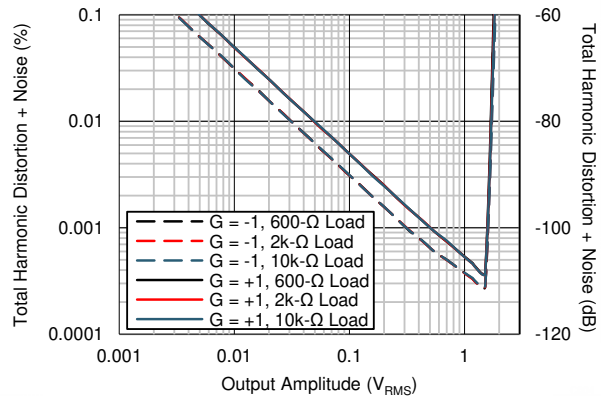
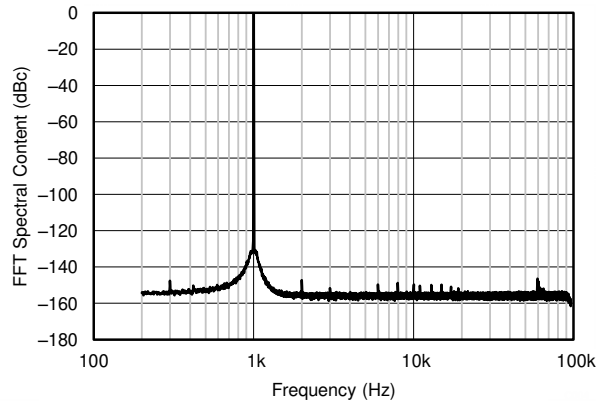


Figure 6-18. THD+N vs Output Amplitude

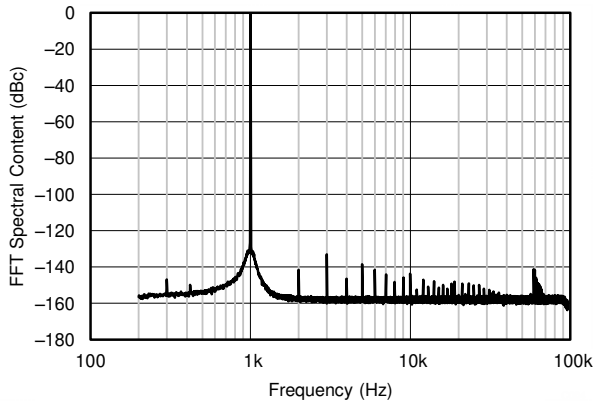
6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



G = +1, f = 1 kHz, V_O = 4.5 V_{PP}, R_L = 10 kΩ, BW = 90 kHz

Figure 6-19. Spectral Content (With 10-kΩ Load)



G = +1, f = 1 kHz, V_O = 4.5 V_{PP}, R_L = 2 kΩ, BW = 90 kHz

Figure 6-20. Spectral Content (With 2-kΩ Load)

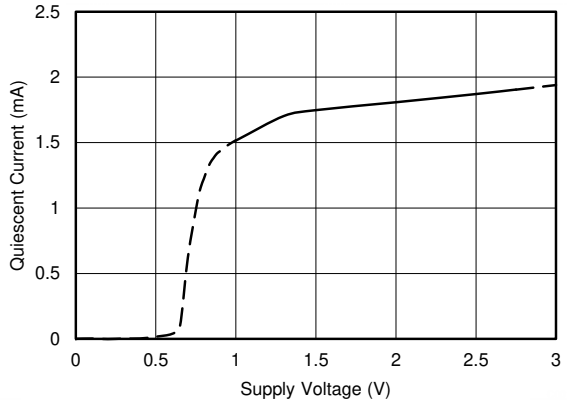


Figure 6-21. Quiescent Current vs Supply Voltage

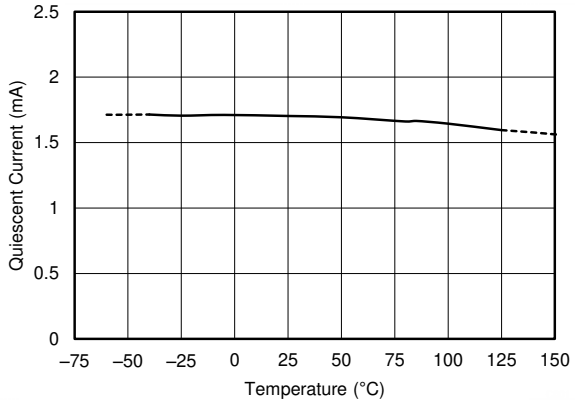


Figure 6-22. Quiescent Current vs Temperature

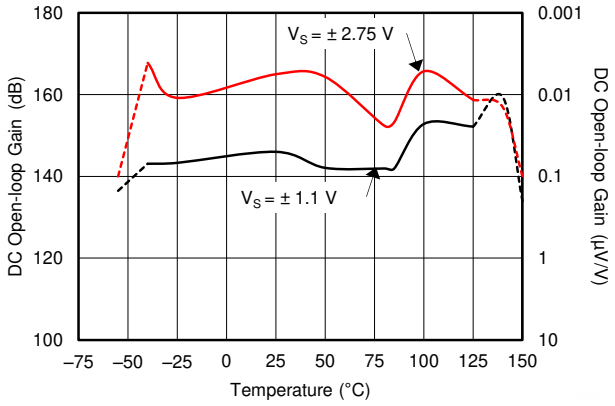


Figure 6-23. Open-Loop Gain vs Temperature

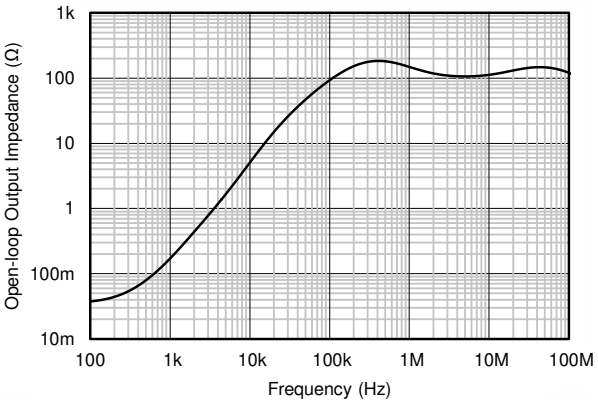


Figure 6-24. Open-Loop Output Impedance vs Frequency

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)

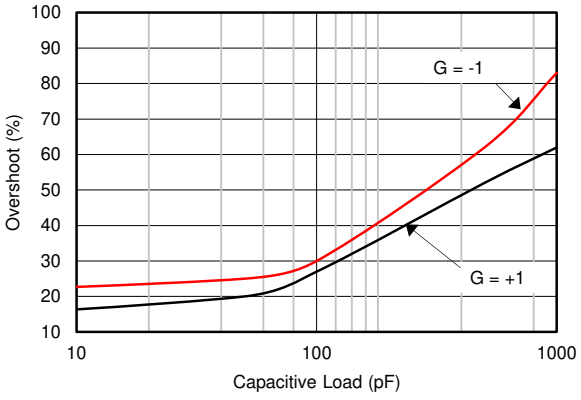


Figure 6-25. Small-Signal Overshoot vs Capacitive Load

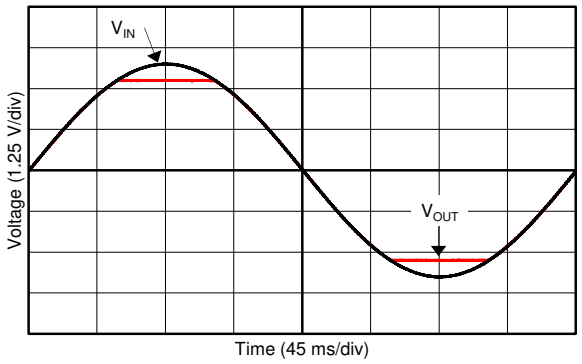


Figure 6-26. No Phase Reversal

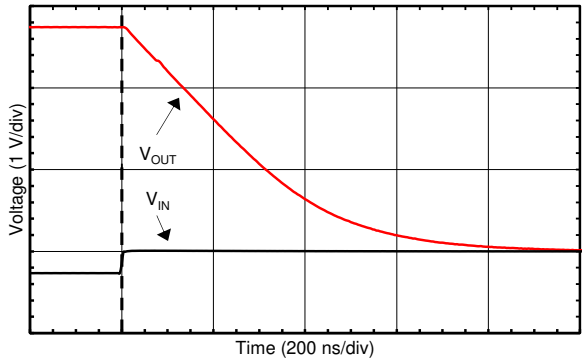


Figure 6-27. Positive Overload Recovery

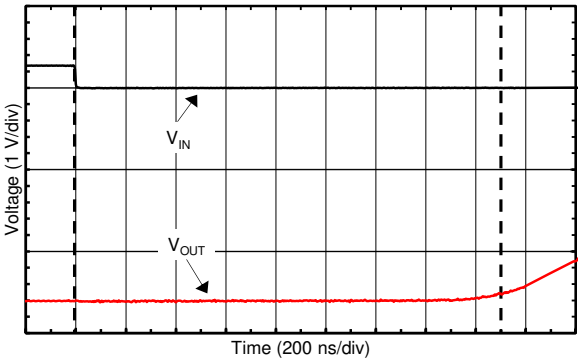
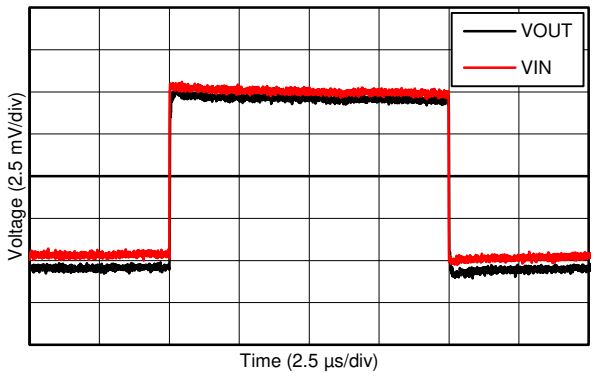
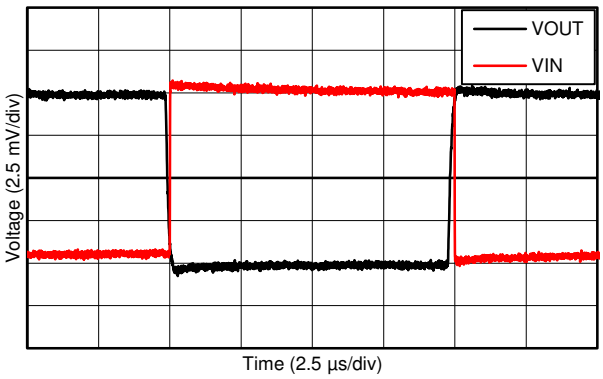


Figure 6-28. Negative Overload Recovery



G = +1, 10-mV step

Figure 6-29. Small-Signal Step Response

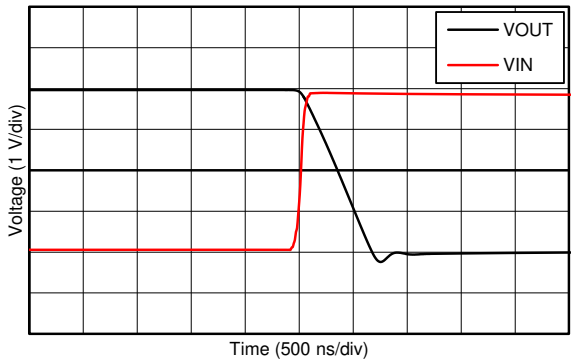


G = –1, 10-mV step

Figure 6-30. Small-Signal Step Response

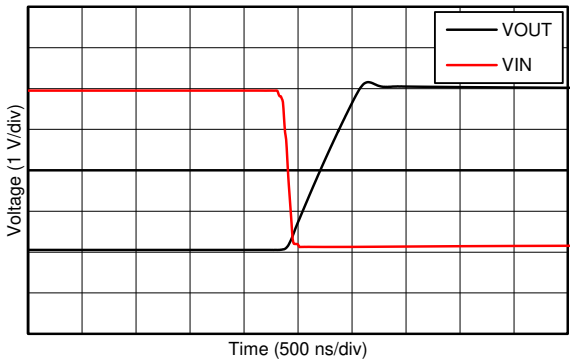
6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



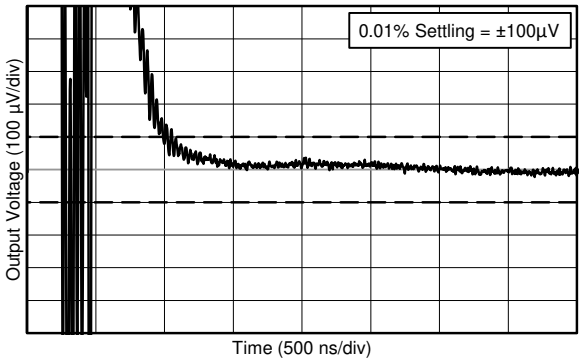
Falling output, 4-V Step

Figure 6-31. Large-Signal Step Response



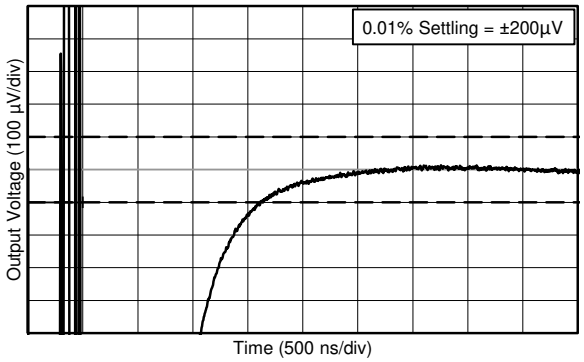
Rising output, 4-V step

Figure 6-32. Large-Signal Step Response



0.01% settling = ±100 µV, 1-V positive step

Figure 6-33. Settling Time



0.01% settling = ±200 µV, 1-V negative step

Figure 6-34. Settling Time

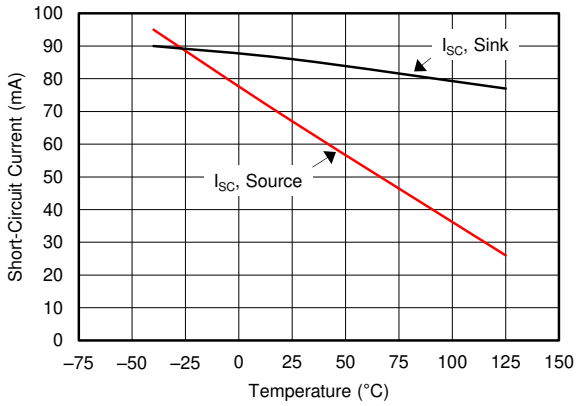


Figure 6-35. Short-Circuit Current vs Temperature

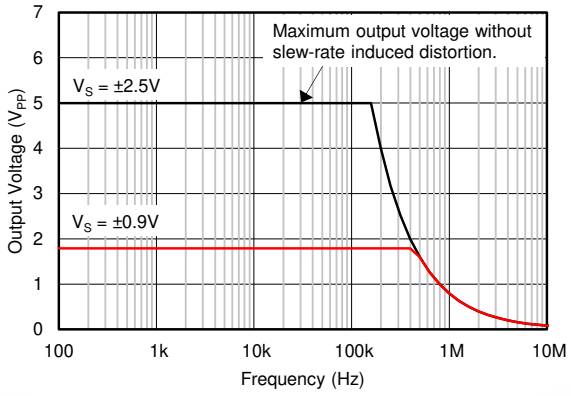
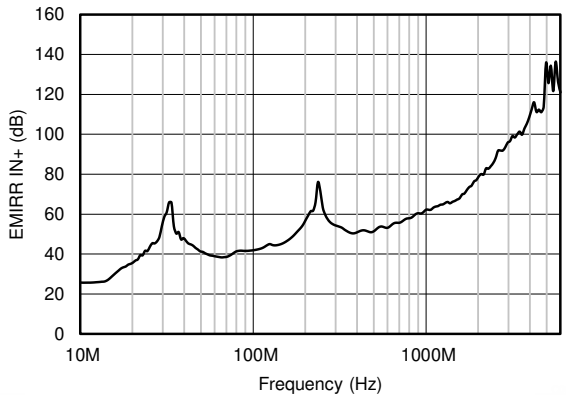


Figure 6-36. Maximum Output Voltage vs Frequency

6.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±2.5 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF (unless otherwise noted)



P_{RF} = –10 dBm

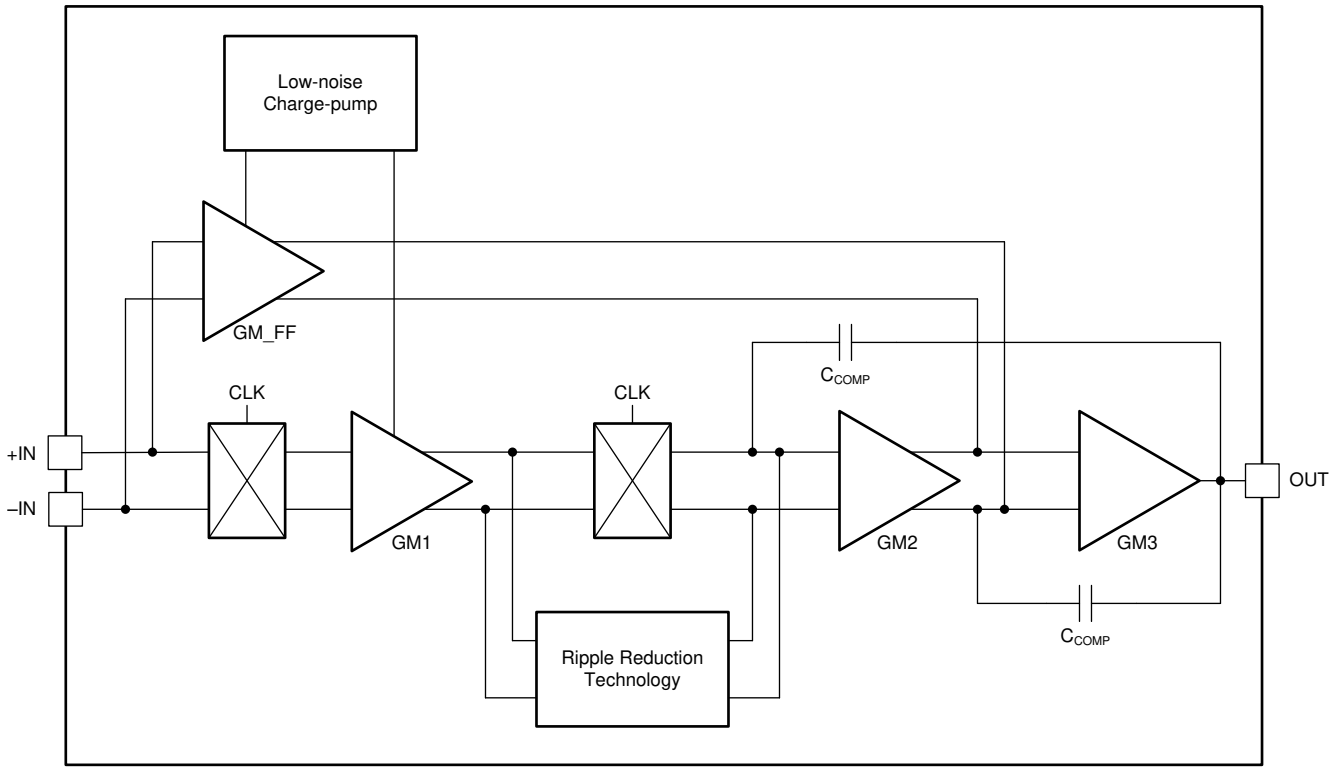
Figure 6-37. EMIRR vs Frequency

7 Detailed Description

7.1 Overview

The OPAx388-Q1 zero-drift amplifiers are engineered with the unique combination of a proprietary precision auto-calibration technique and a low-noise, low-ripple, input charge pump. These amplifiers offer ultra-low input offset voltage and drift and achieve excellent input and output dynamic linearity. The OPAx388-Q1 operate from 2.5 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose and precision applications. The integrated, low-noise charge pump allows true rail-to-rail input common-mode operation without distortion associated with complementary rail-to-rail input topologies (input crossover distortion). The OPAx388-Q1 strengths also include 10-MHz bandwidth, 7-nV/$\sqrt{\text{Hz}}$ noise spectral density, and no 1/f noise, making these devices an excellent choice for interfacing with sensor modules and buffering high-fidelity digital-to-analog converters (DACs).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input Voltage and Zero-Crossover Functionality

The OPAx388-Q1 input common-mode voltage range extends 0.1 V beyond the supply rails. This amplifier family is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers. Operating a complementary rail-to-rail input amplifier with signals traversing the transition region results in unwanted non-linear behavior and polluted spectral content. Figure 7-1 and Figure 7-2 contrast the performance of a traditional complementary rail-to-rail input stage amplifier with the performance of the zero-crossover OPAx388-Q1. Significant harmonic content and distortion is generated during the differential pair transition (such a transition does not exist in the OPAx388-Q1). Crossover distortion is eliminated through the use of a single differential pair coupled with an internal low-noise charge pump. The OPAx388-Q1 maintain noise, bandwidth, and offset performance throughout the input common-mode range, thus reducing printed circuit board (PCB) and bill of materials (BOM) complexity through the reduction of power-supply rails.

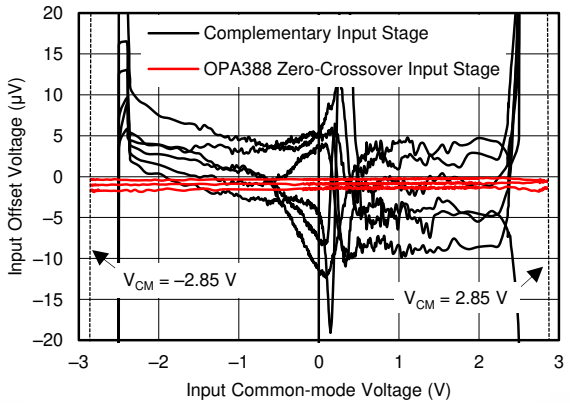


Figure 7-1. Input Crossover Distortion Nonlinearity

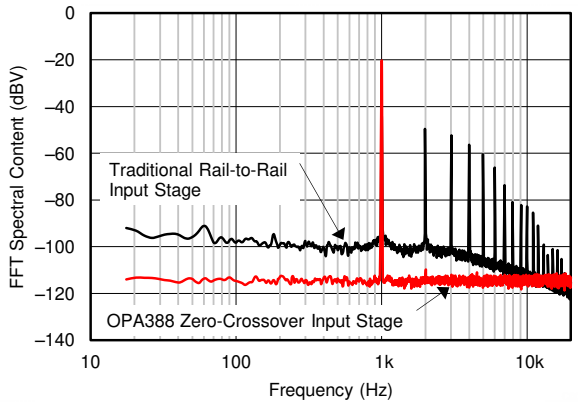


Figure 7-2. Input Crossover Distortion Spectral Content

Typically, input bias current is approximately ±30 pA. Input voltages exceeding the power supplies, however, can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor, as shown in Figure 7-3.

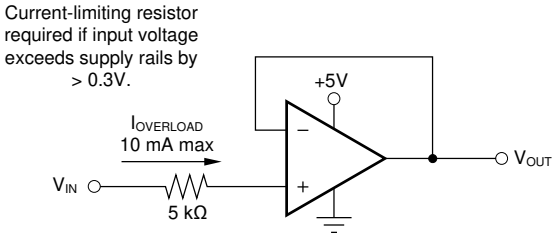


Figure 7-3. Input Current Protection

7.3.2 Input Differential Voltage

The typical input bias current of the OPAx388-Q1 during normal operation is approximately 30 pA. In overdriven conditions, the bias current can increase significantly. The most common cause of an overdriven condition occurs when an operational amplifier is outside of the linear range of operation. When the output of the operational amplifier is driven to one of the supply rails, the feedback loop requirements cannot be satisfied and a differential input voltage develops across the input pins. This differential input voltage results in activation of parasitic diodes inside the front-end input chopping switches that combine with 10-kΩ electromagnetic interference (EMI) filter resistors to create the equivalent circuit shown in Figure 7-4. Notice that the input bias current remains within specification in the linear region.

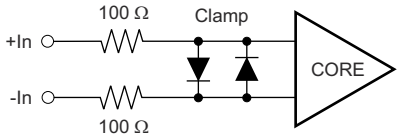


Figure 7-4. Equivalent Input Circuit

7.3.3 Internal Offset Correction

The OPAx388-Q1 operational amplifiers use an auto-calibration technique with a time-continuous, 200-kHz operational amplifier in the signal path. These amplifiers are zero-corrected every 5 µs using a proprietary technique. At power up, the amplifiers require approximately 1 ms to achieve the specified V_{OS} accuracy. This design has no aliasing or flicker noise.

7.3.4 EMI Susceptibility and Input Filtering

Operational amplifiers vary in susceptibility to EMI. If conducted EMI enters the operational amplifier, the dc offset at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPAx388-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. Both common-mode and differential-mode filtering are provided by the input filter. The filter is designed for a cutoff frequency of approximately 20 MHz (–3 dB), with a rolloff of 20 dB per decade.

7.4 Device Functional Modes

The OPAx388-Q1 have a single functional mode and are operational when the power-supply voltage is greater than 2.5 V (±1.25 V). The maximum specified power-supply voltage for the OPAx388-Q1 is 5.5 V (±2.75 V).

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The OPAx388-Q1 are unity-gain stable, precision operational amplifiers free from unexpected output and phase reversal. The use of proprietary zero-drift circuitry gives the benefit of low input offset voltage over time and temperature, as well as lowering the 1/f noise component. As a result of the high PSRR, these devices work well in applications that run directly from battery power without regulation. The OPAx388-Q1 are optimized for full rail-to-rail input, allowing for low-voltage, single-supply operation or split-supply use. These miniature, high-precision, low-noise amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the supplies without input crossover distortion and a rail-to-rail output that swings within 5 mV of the supplies under normal test conditions. The OPAx388-Q1 precision amplifiers are designed for upstream analog signal chain applications in low or high gains, as well as downstream signal chain functions such as DAC buffering.

8.2 Typical Application

This single-supply, low-side, bidirectional current-sensing design example detects load currents from –1 A to +1 A. The single-ended output spans from 110 mV to 3.19 V. This design uses the OPA388-Q1 because of the low offset voltage and rail-to-rail input and output. One of the amplifiers is configured as a difference amplifier and the other amplifier provides the reference voltage.

Figure 8-1 shows the circuit drawing.

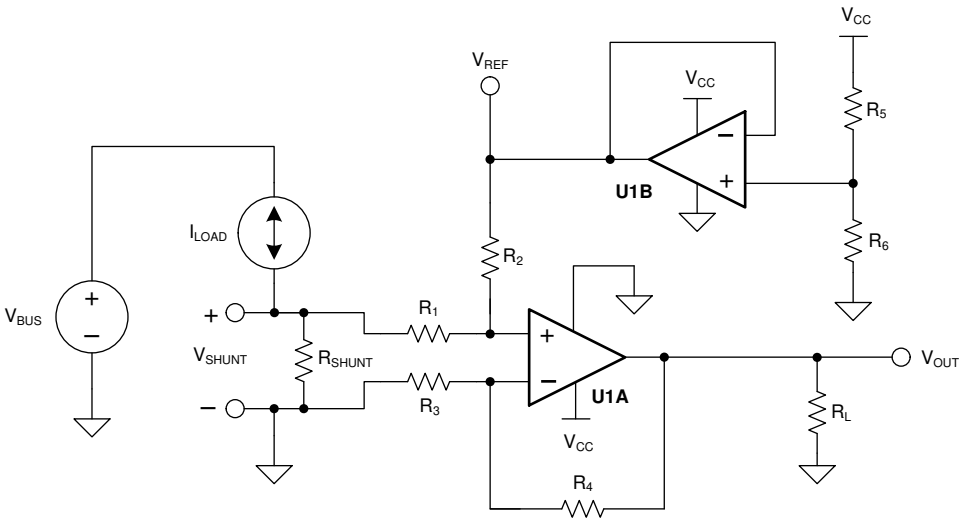


Figure 8-1. Bidirectional Current-Sensing

8.2.1 Design Requirements

This solution has the following requirements:

- Supply voltage: 3.3 V
- Input: –1 A to 1 A
- Output: 1.65 V ±1.54 V (110 mV to 3.19 V)

8.2.2 Detailed Design Procedure

The load current, I_{LOAD}, flows through the shunt resistor (R_{SHUNT}) to develop the shunt voltage, V_{SHUNT}. The shunt voltage is then amplified by the difference amplifier consisting of U1A and R_1 through R_4. The gain of the difference amplifier is set by the ratio of R_4 to R_3. To minimize errors, set $R_2 = R_4$ and $R_1 = R_3$. The reference voltage, V_{REF}, is supplied by buffering a resistor divider using U1B. The transfer function is given by Equation 1.

$$V_{OUT} = V_{SHUNT} \times Gain_{Diff\_Amp} + V_{REF} \quad (1)$$

where

- $V_{SHUNT} = I_{LOAD} \times R_{SHUNT}$
- $Gain_{Diff\_Amp} = \frac{R_4}{R_3}$
- $V_{REF} = V_{CC} \times \left(\frac{R_6}{R_5 + R_6} \right)$

There are two types of errors in this design: offset and gain. Gain errors are introduced by the tolerance of the shunt resistor and the ratios of R_4 to R_3 and, similarly, R_2 to R_1. Offset errors are introduced by the voltage divider (R_5 and R_6) and how closely the ratio of R_4 / R_3 matches R_2 / R_1. The latter value affects the CMRR of the difference amplifier, ultimately translating to an offset error.

The value of V_{SHUNT} is the ground potential for the system load because V_{SHUNT} is a low-side measurement. Therefore, a maximum value must be placed on V_{SHUNT}. In this design, the maximum value for V_{SHUNT} is set to 100 mV. Equation 2 calculates the maximum value of the shunt resistor given a maximum shunt voltage of 100 mV and maximum load current of 1 A.

$$R_{SHUNT(Max)} = \frac{V_{SHUNT(Max)}}{I_{LOAD(Max)}} = \frac{100\ mV}{1\ A} = 100\ m\Omega \quad (2)$$

The tolerance of R_{SHUNT} is directly proportional to cost. For this design, a shunt resistor with a tolerance of 0.5% was selected. If greater accuracy is required, select a 0.1% resistor or better.

The load current is bidirectional; therefore, the shunt voltage range is –100 mV to 100 mV. This voltage is divided down by R_1 and R_2 before reaching the operational amplifier, U1A. Make sure that the voltage present at the noninverting node of U1A is within the common-mode range of the device. Therefore, use an operational amplifier, such as the OPA388-Q1, that has a common-mode range that extends below the negative supply voltage. Finally, to minimize offset error, the OPA388-Q1 has a typical offset voltage of merely ±0.25 µV (±5 µV maximum).

Given a symmetric load current of –1 A to +1 A, the voltage divider resistors (R_5 and R_6) must be equal. To be consistent with the shunt resistor, a tolerance of 0.5% was selected. To minimize power consumption, 10-kΩ resistors are used.

To set the gain of the difference amplifier, the common-mode range and output swing of the OPA388-Q1 must be considered. Equation 3 and Equation 4 depict the typical common-mode range and maximum output swing, respectively, of the OPA388-Q1 given a 3.3-V supply.

$$-100\ \text{mV} < V_{CM} < 3.4\ \text{V} \tag{3}$$

$$100\ \text{mV} < V_{OUT} < 3.2\ \text{V} \tag{4}$$

The gain of the difference amplifier can now be calculated as shown in Equation 5.

$$\text{Gain}_{\text{Diff\_Amp}} = \frac{V_{\text{OUT\_Max}} - V_{\text{OUT\_Min}}}{R_{\text{SHUNT}} \times (I_{\text{MAX}} - I_{\text{MIN}})} = \frac{3.2\ \text{V} - 100\ \text{mV}}{100\ \text{m}\Omega \times [1\ \text{A} - (-1\text{A})]} = 15.5\ \frac{\text{V}}{\text{V}} \tag{5}$$

The resistor value selected for R_1 and R_3 was 1 kΩ. 15.4 kΩ was selected for R_2 and R_4 because this number is the nearest standard value. Therefore, the ideal gain of the difference amplifier is 15.4 V/V.

The gain error of the circuit primarily depends on R_1 through R_4. As a result of this dependence, 0.1% resistors were selected. This configuration reduces the likelihood that the design requires a two-point calibration. A simple one-point calibration, if desired, removes the offset errors introduced by the 0.5% resistors.

8.2.3 Application Curve

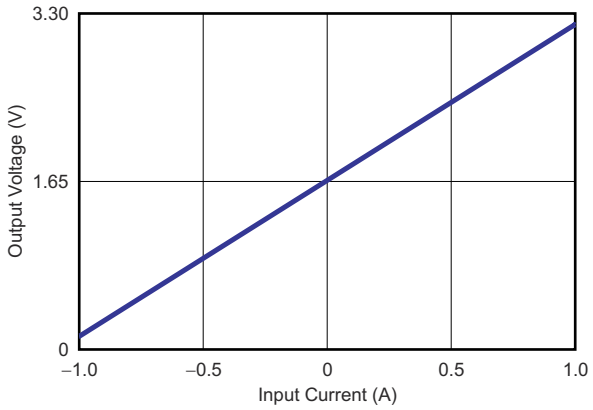


Figure 8-2. Bidirectional Current-Sensing Circuit Performance: Output Voltage vs Input Current

9 Power Supply Recommendations

The OPAx388-Q1 family of operational amplifiers can be used with single or dual supplies from an operating range of V_S = 2.5 V (±1.25 V) up to 5.5 V (±2.75 V). Key parameters that vary over the supply voltage or temperature range are shown in *Section 6.7*.

CAUTION
Supply voltages greater than 7 V can permanently damage the device (see Section 6.1).

10 Layout

10.1 Layout Guidelines

Pay attention to good layout practice. Keep traces short and, if possible, use a printed-circuit board (PCB) ground plane with surface-mount components placed as close as possible to the device pins. Place a 0.1-µF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

For lowest offset voltage and precision performance, optimize the circuit layout and mechanical conditions. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by making sure these potentials are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals).
- Thermally isolate components from power supplies or other heat sources.
- Shield operational amplifier and input circuitry from air currents, such as cooling fans.

Follow these guidelines to reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltage drift of 0.1 µV/°C or greater, depending on the materials used.

10.2 Layout Example

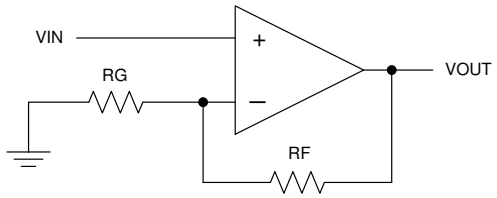


Figure 10-1. Schematic Representation

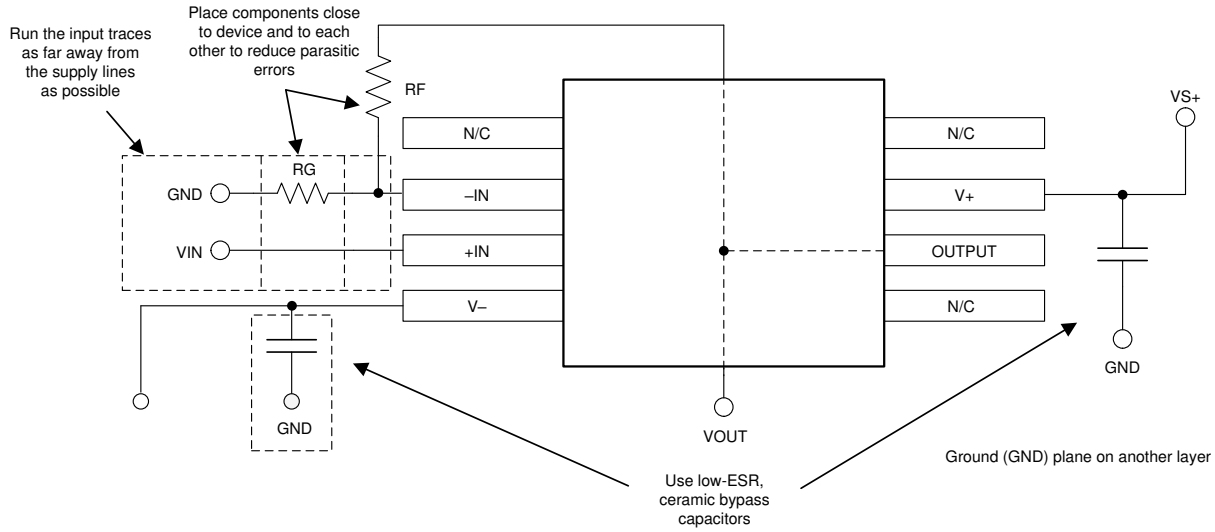


Figure 10-2. Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the TINA-TI™ software folder.

11.1.1.2 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

11.1.1.3 TI Precision Designs

The OPAx388-Q1 family is featured on TI Precision Designs, available online at www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following: Texas Instruments, *Circuit board layout techniques*

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

TINA-TI™ and TI E2E™ are trademarks of Texas Instruments.
TINA™ is a trademark of DesignSoft, Inc.
PSpice® is a registered trademark of Cadence Design Systems, Inc.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2388QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	O28Q	Samples
OPA388QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	388Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA2388-Q1, OPA388-Q1 :

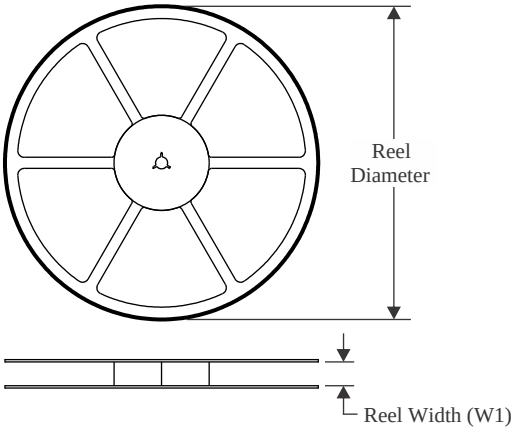
- Catalog : OPA2388, OPA388

NOTE: Qualified Version Definitions:

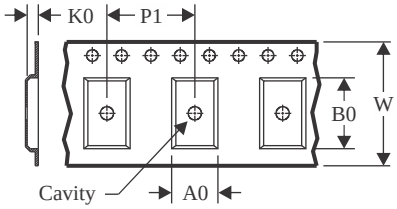
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

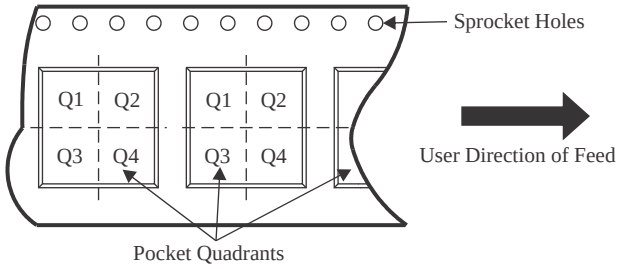


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

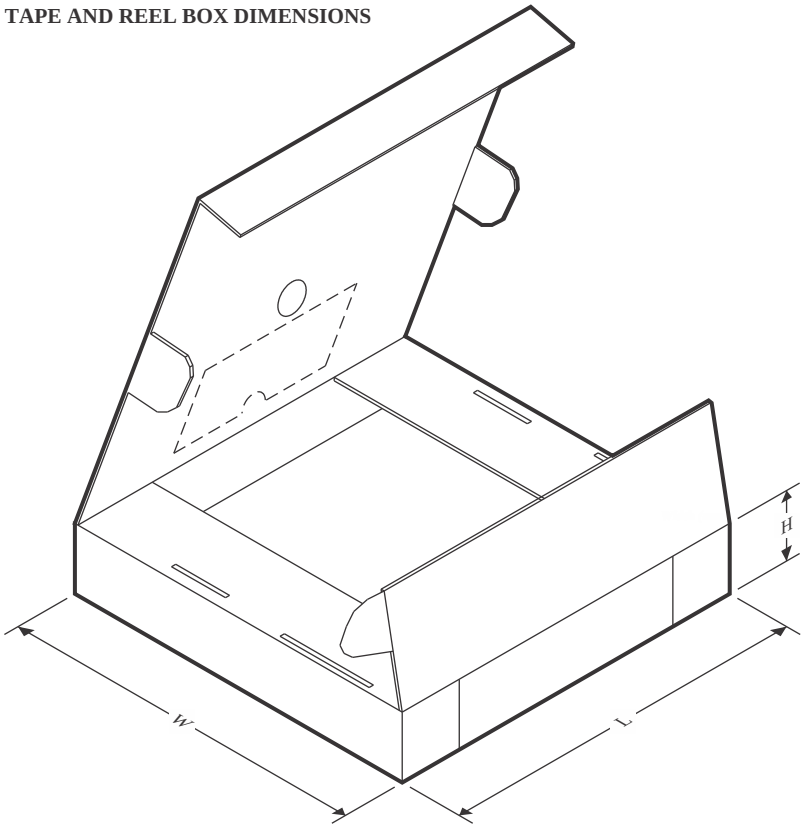
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2388QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA388QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

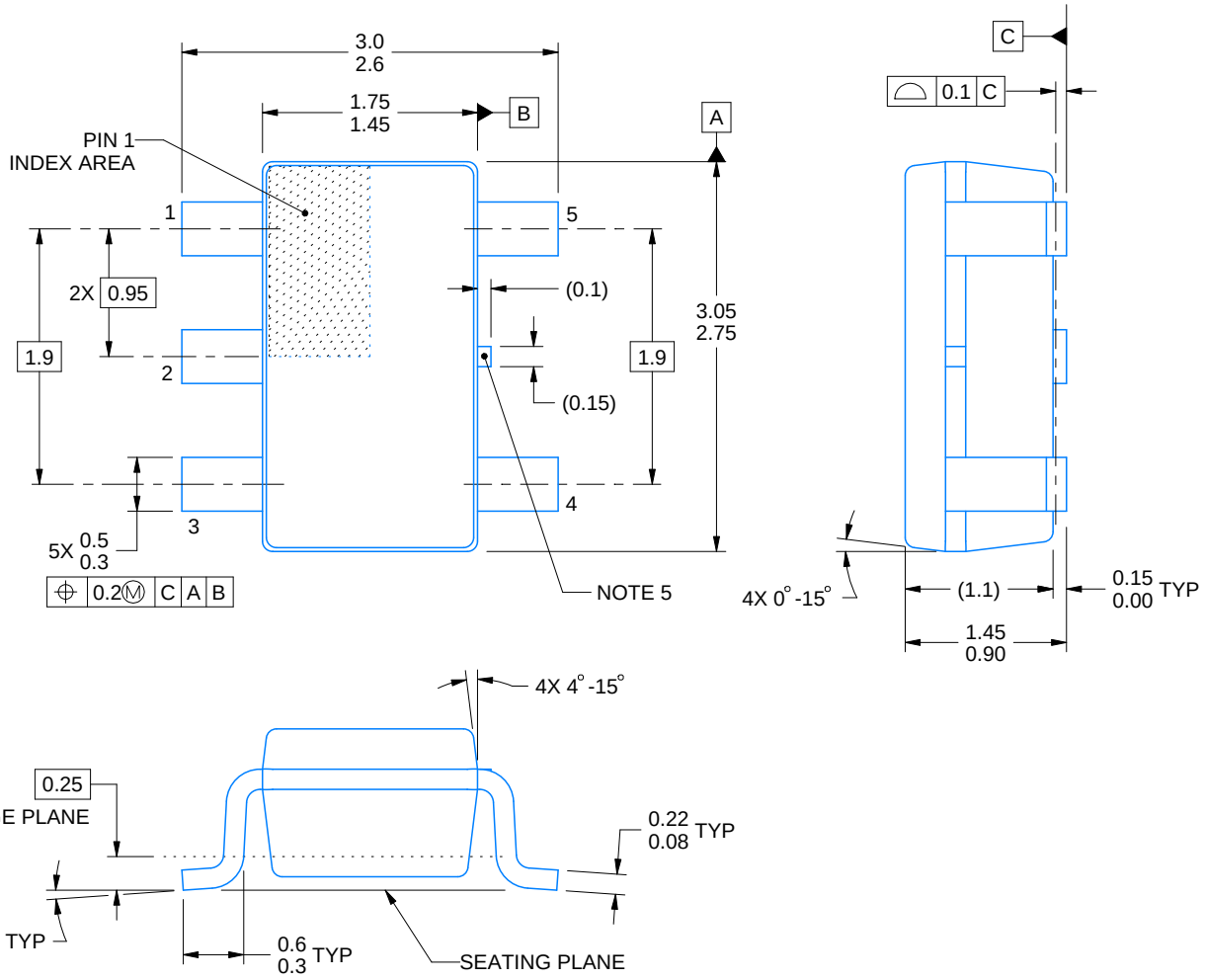
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2388QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA388QDBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

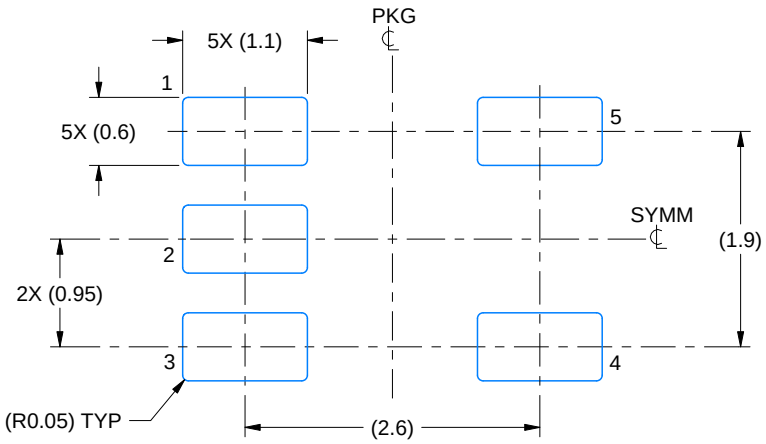
SMALL OUTLINE TRANSISTOR



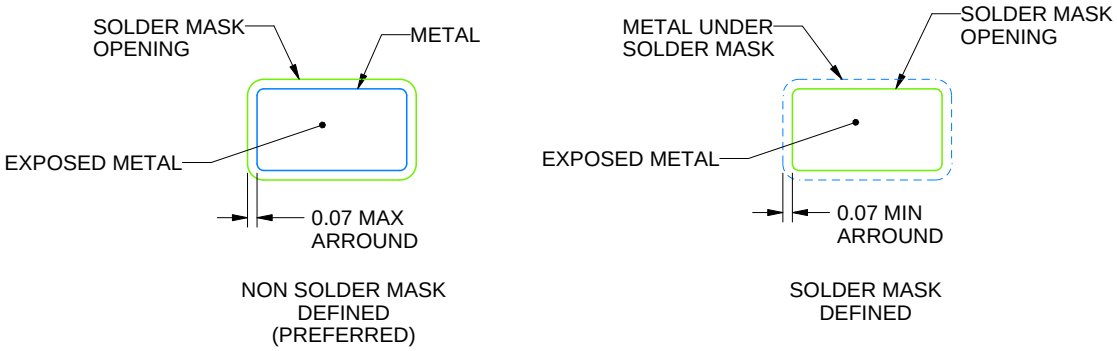
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

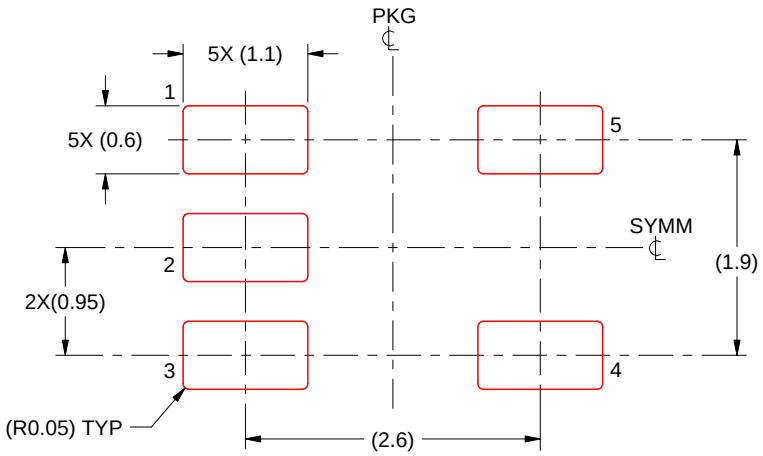


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

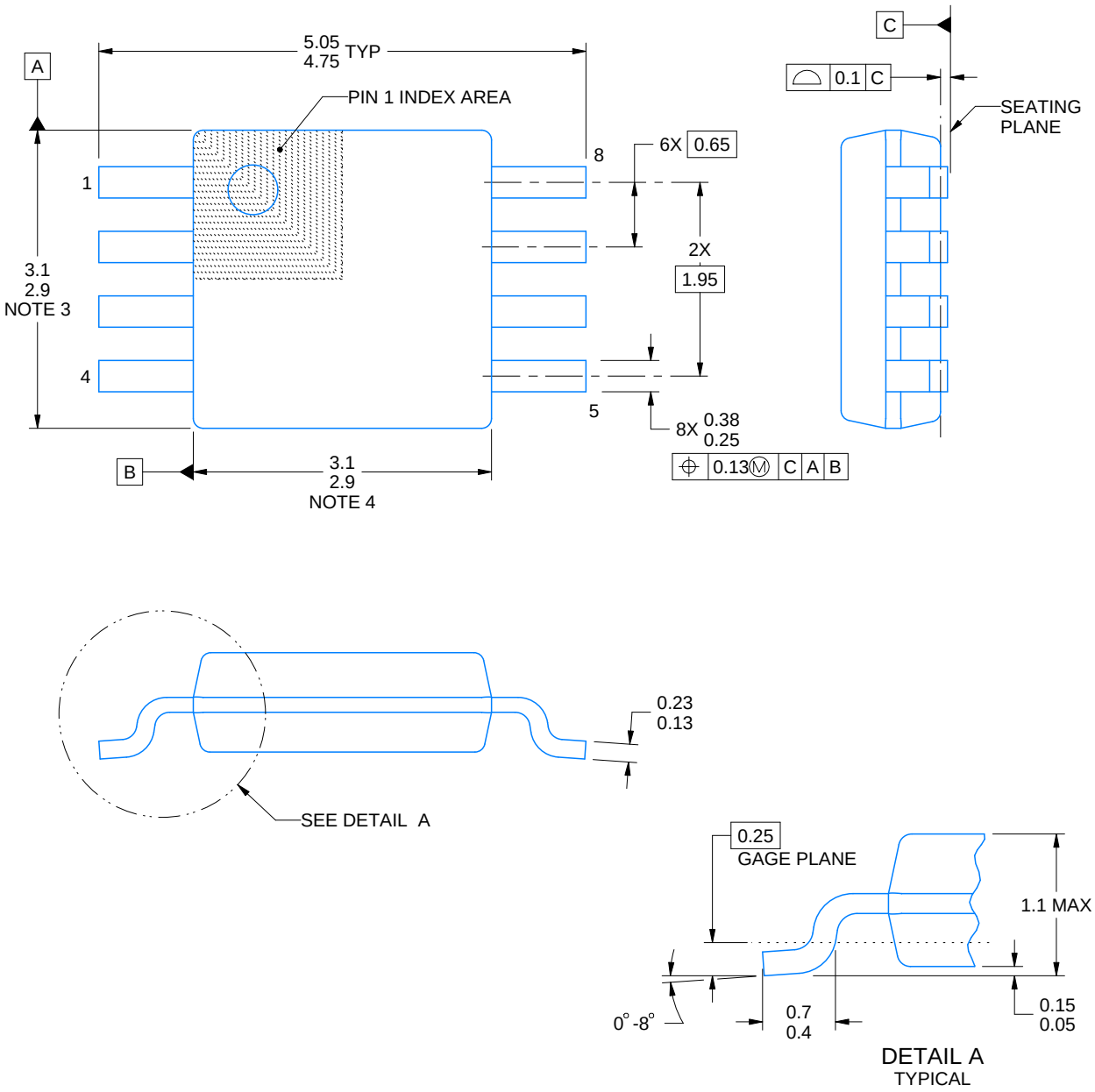
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

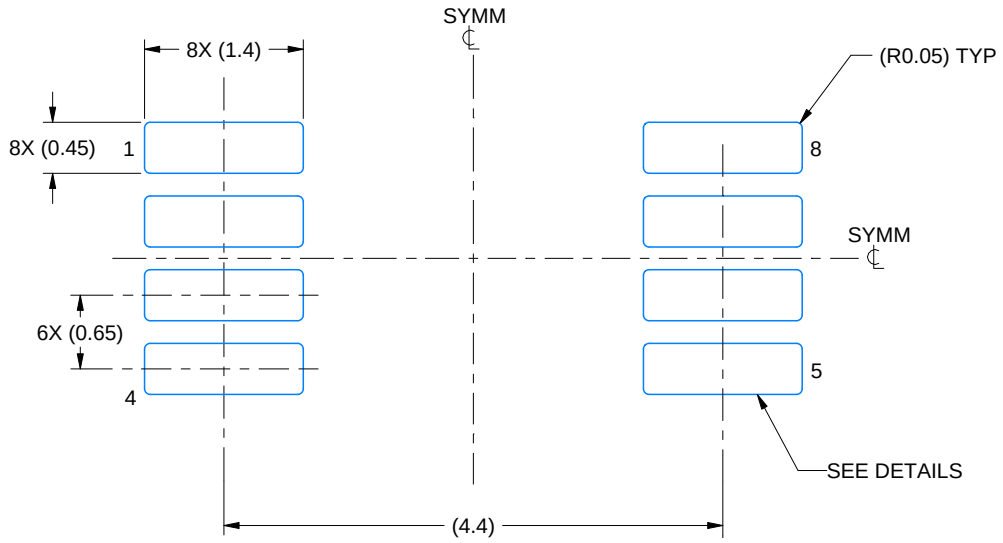
SMALL OUTLINE PACKAGE



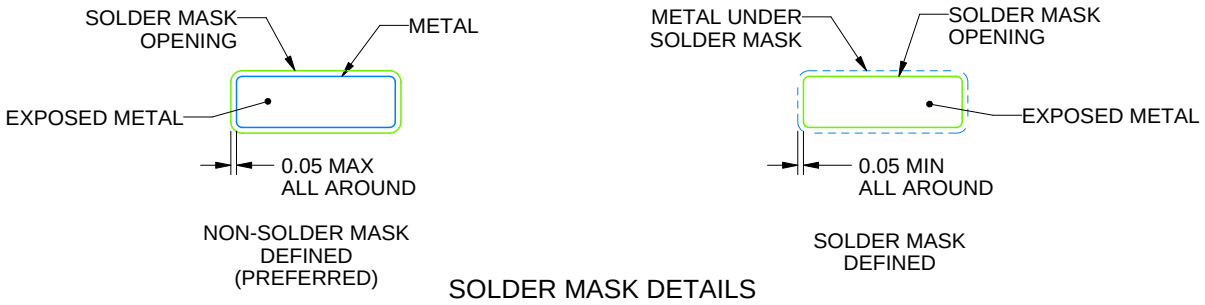
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

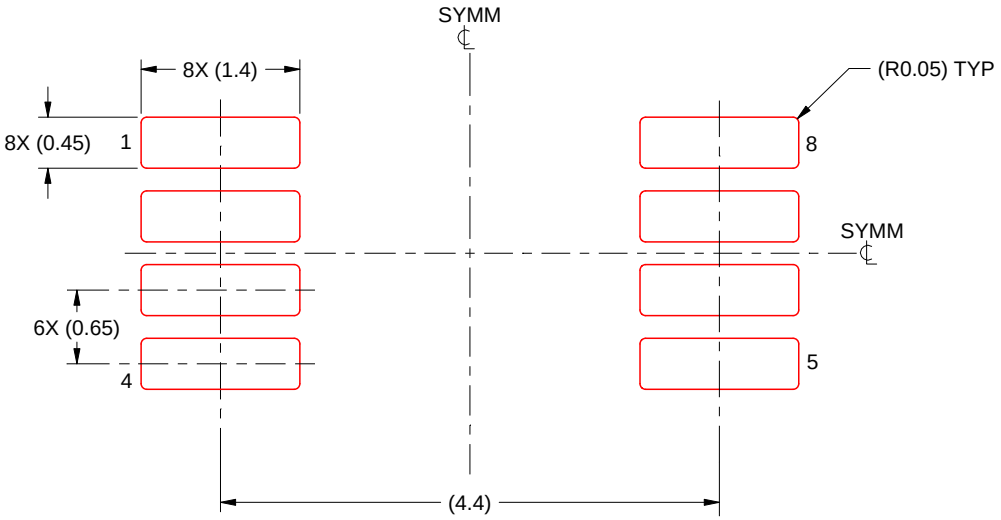


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265