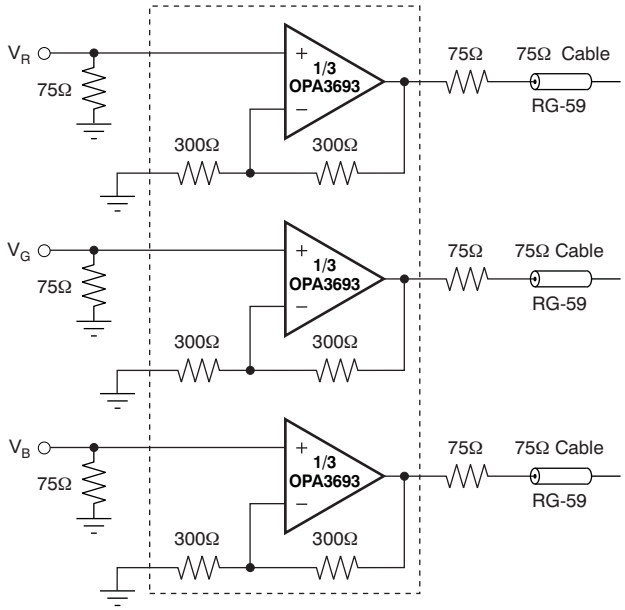
Triple, Ultra-Wideband, Fixed-Gain, VIDEO BUFFER with Disable

FEATURES

- **650MHz BANDWIDTH (G = +2)**
- **FIXED GAIN OF ±1 or +2**
- **OUTPUT VOLTAGE SWING: ±4.1V**
- **ULTRA-HIGH SLEW RATE: 2500V/µs**
- **3RD-ORDER INTERCEPT: > 40dBm (f < 50MHz)**
- **LOW POWER: 130mW/channel**
- **LOW DISABLED POWER: 0.4mW/channel**

APPLICATIONS

- **MULTIPLE LINE VIDEO DISTRIBUTION AMPLIFIER (DA)**
- **PORTABLE INSTRUMENTS**
- **BROADBAND VIDEO LINE DRIVERS**
- **ADC BUFFERS**
- **HIGH-FREQUENCY ACTIVE FILTERS**



DESCRIPTION

The OPA3693 provides an easy to use, broadband, triple, fixed-gain buffer amplifier. Depending on the external connections, the internal resistor network may be used to provide either a fixed gain of +2 video buffer or a gain of +1 or –1 voltage buffer. The OPA3693 offers a slew rate (2500V/µs) and bandwidth (> 800MHz) normally associated with a much higher supply current. A new output stage architecture delivers high output current with a minimal headroom and crossover distortion. This combination of features makes the OPA3693 an ideal RGB line driver or single-supply undersampling analog-to-digital converter (ADC) input driver.

The OPA3693 13mA/channel supply current is precisely trimmed at +25°C. This trim, along with a low temperature drift, gives lower system power over temperature. System power can be further reduced using the optional disable control pin. Leaving this pin open, or holding it HIGH, gives normal operation. If pulled LOW, the OPA3693 supply current drops to less than 130µA/channel. This power-saving feature, along with exceptional single +5V operation, make the OPA3693 ideal for portable applications. The OPA3693 is available in an SSOP-16 package.

OPA3693 RELATED PRODUCTS

FEATURE	SINGLES	DUALS	TRIPLES
Voltage Feedback	OPA690	OPA2690	OPA3690
Current Feedback	OPA691	OPA2691	OPA3691
Fixed Gain	OPA692	—	OPA3692
Fixed Gain	OPA693	—	—
>900MHz	OPA695	OPA2695	OPA3695

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA3693	SSOP-16	DBQ	–40°C to +85°C	OP3693	OPA3693IDBQ	Rail, 75
					OPA3693IDBQR	Tape and Reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

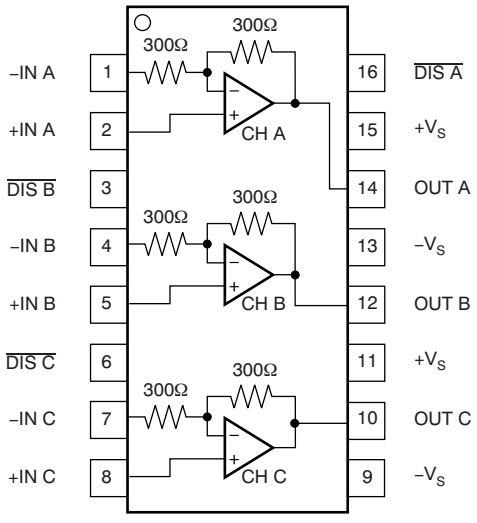
Power Supply		$\pm 6.5 V_{DC}$
Internal Power Dissipation		See Thermal Analysis
Differential Input Voltage		±1.2V
Input Common-Mode Voltage Range		$\pm V_S$
Storage Temperature Range		–65°C to +125°C
Lead Temperature (soldering, 10s)		+300°C
Maximum Junction Temperature, T_J	Peak	+150°C
	Continuous Operation, Long-Term Reliability	+140°C
ESD Rating	Human Body Model (HBM)	1500V
	Charge Device Model (CDM)	1000V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these and any other conditions beyond those specified is not supported.

Top View

OPA3693

SSOP



ELECTRICAL CHARACTERISTICS: V_S = ±5V

Boldface limits are tested at **+25°C.**
At G = +2 (–IN grounded) and R_L = 100Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3693IDBQ						TEST LEVEL (1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C (2)	0°C to +70°C (3)	–40°C to +85°C (3)	UNITS	MIN/ MAX	
AC PERFORMANCE								
Small-Signal Bandwidth (V_O = 1.0V_{PP})	G = +1	800				MHz	typ	C
	G = +2	650	500	480	470	MHz	min	B
	G = –1	650	500	480	470	MHz	min	B
Bandwidth for 0.2dB Gain Flatness	V_O = 1.0V_{PP}	320	120	110	105	MHz	min	B
Peaking at a Gain of +1	V_O = 1.0V_{PP}	3	4.3	5.3	5.7	dB	max	B
Large-Signal Bandwidth	V_O = 4V_{PP}	380				MHz	typ	C
Slew Rate	V_O = 4V Step	2500	2200	2100	2000	V/µs	min	B
Rise-and-Fall Time	V_O = 0.5V Step	0.6	0.8	0.8	0.9	ns	max	B
	V_O = 5V Step	1.2	1.3	1.3	1.4	ns	max	B
Settling Time to 0.02%	V_O = 2V Step	16				ns	typ	C
Settling Time to 0.1%	V_O = 2V Step	12				ns	typ	C
Harmonic Distortion	f = 10MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω	–75	–66	–65	–64	dBc	max	B
	R_L ≥ 500Ω	–80	–78	–77	–76	dBc	max	B
3rd-Harmonic	R_L = 100Ω	–78	–75	–65	–64	dBc	max	B
	R_L ≥ 500Ω	–84	–80	–79	–76	dBc	max	B
Input Voltage Noise	f > 1MHz	1.8	2	2.7	2.9	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	18	19	21	22	pA/√Hz	max	B
Inverting Input Current Noise (internal)	f > 1MHz	22	24	26	27	pA/√Hz	max	B
Differential Gain	NTSC, R_L = 150Ω	0.03				%	typ	C
	NTSC, R_L = 37.5Ω	0.03				%	typ	C
Differential Phase	NTSC, R_L = 150Ω	0.01				deg	typ	C
	NTSC, R_L = 37.5Ω	0.1				deg	typ	C
Crosstalk (2 channels driven)	f = 10MHz	–65				dBc	typ	C
DC PERFORMANCE (4)								
Gain Error	G = +1	±0.7				%	typ	C
	G = +2	±0.6	**±1.0**	1.1	1.2	%	max	A
	G = –1, R_s = 0Ω	±0.5	±0.9	1.0	1.1	%	max	B
Internal R_F and R_G								
Maximum		300	**341**	345	347	Ω	max	A
Minimum		300	**264**	260	258	Ω	min	A
Input Offset Voltage	V_{CM} = 0V	±0.6	**±3.5**	±3.7	±4.0	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±8	±8	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	+15	**±35**	±43	±45	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 0V			170	170	nA/°C	max	B
Inverting Input Bias Current (internal)	V_{CM} = 0V	±20	**±50**	±52	±54	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V			50	60	nA/°C	max	B

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limits; junction temperature = ambient +27°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of pin.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

Boldface limits are tested at **+25°C.**

At G = +2 (–IN grounded) and R_L = 100Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3693IDBQ						TEST LEVEL (1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C (2)	0°C to +70°C (3)	–40°C to +85°C (3)	UNITS	MIN/ MAX	
INPUT								
Common-Mode Input Voltage Range (CMIR)		±3.4	±3.3	±3.2	±3.2	V	min	B
Noninverting Input Impedance		300 || 1.2				kΩ || pF	typ	C
OUTPUT								
Voltage Output Swing	No Load	±4.1	**±3.9**	±3.9	±3.8	V	min	A
	100Ω Load	±3.8	**±3.7**	±3.7	±3.7	V	min	A
Current Output: Sinking, Sourcing	V_O = 0	±100	**±85**	±80	±70	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.18				Ω	typ	C
DISABLE (Disabled LOW)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0, All Channels	–390	**–600**	–650	–665	µA	typ	A
Disable Time	V_{IN} = ±0.25V_{DC}	1				µs	typ	C
Enable Time	V_{IN} = ±0.25V_{DC}	25				ns	typ	C
Off Isolation	G = +2, 10MHz	70				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn-On Glitch	G = +2, V_{IN} = 0	±100				mV	typ	C
Turn-Off Glitch	G = +2, V_{IN} = 0	±20				mV	typ	C
Enable Voltage		3.3	**3.5**	3.6	3.7	V	min	A
Disable Voltage		1.8	**1.7**	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0, Each Channel	75	**130**	143	149	µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Minimum Operating Voltage			±1.75	±1.8	±1.9	V	min	B
Maximum Operating Voltage			**±6**	±6	±6	V	max	A
Maximum Quiescent Current	V_S = ±5V	39	**41**	42.2	43.5	mA	max	A
Minimum Quiescent Current	V_S = ±5V	39	**37.5**	34.8	33	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input-Referred, f < 100kHz	62	**52**	50	49	dB	typ	A
TEMPERATURE RANGE								
Specification: IDBQ		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
DBQ SSOP-16		80				°C/W	typ	C

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**
At G = +2 (–IN grounded) and R_L = 100Ω to V_S/2, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3693IDBQ						TEST LEVEL (1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C (2)	0°C to +70°C (3)	–40°C to +85°C (3)	UNITS	MIN/ MAX	
AC PERFORMANCE (see Figure 29)								
Small-Signal Bandwidth (V_O = 0.5V_{PP})	G = +1	600				MHz	typ	C
	G = +2	500	400	390	380	MHz	min	B
	G = –1	450						C
Bandwidth for 0.2dB Gain Flatness	V_O < 0.5V_{PP}	280	110	100	96	MHz	min	B
Peaking at a Gain of +1	V_O < 0.5V_{PP}	2.2	2.9	3.9	4.2	dB	max	B
Large-Signal Bandwidth	V_O = 2V_{PP}	425				MHz	typ	C
Slew Rate	2V Step	1500	1200	1100	1000	V/µs	min	B
Rise-and-Fall Time	V_O = 0.5V Step	0.8				ns	typ	C
	V_O = 2V Step	1.0				ns	typ	C
Settling Time to 0.02%	V_O = 2V Step	16				ns	typ	C
Settling Time to 0.1%	V_O = 2V Step	12				ns	typ	C
Harmonic Distortion	f = 10MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω to V_S/2	–72	–62	–62	–61	dBc	max	B
	R_L ≥ 500Ω to V_S/2	–73	–67	–66	–66	dBc	max	B
3rd-Harmonic	R_L = 100Ω to V_S/2	–67	–62	–61	–60	dBc	max	B
	R_L ≥ 500Ω to V_S/2	–67	–62	–61	–60	dBc	max	B
Input Voltage Noise	f > 1MHz	1.8	2	2.7	2.9	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	18	19	21	22	pA/√Hz	max	B
Inverting Input Current Noise (internal)	f > 1MHz	22	24	26	27	pA/√Hz	max	B
DC PERFORMANCE (4)								
Gain Error	G = +1	±0.8				%	typ	C
	G = +2	±0.6	**± 1.2**	±1.3	±1.4	%	max	A
	G = –1, R_s = 0Ω	±0.5	±1.1	±1.2	±1.3	%	max	B
Internal R_F and R_G								
Maximum		300	**341**	345	347	Ω	max	A
Minimum		300	**264**	260	258	Ω	min	A
Input Offset Voltage	V_{CM} = V_S/2	±0.6	**±3.5**	±4.0	±4.2	mV	max	A
Average Offset Voltage Drift	V_{CM} = V_S/2			±12	±12	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = V_S/2	±5	**±25**	±33	±35	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = V_S/2			±170	±170	nA/°C	max	B
Inverting Input Bias Current (internal)	V_{CM} = V_S/2	±20	**±50**	±52	±54	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = V_S/2			±50	±60	nA/°C	max	B

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limits; junction temperature = ambient +14°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of pin.

ELECTRICAL CHARACTERISTICS: V_S = +5V (continued)

Boldface limits are tested at **+25°C.**

At G = +2 (–IN grounded) and R_L = 100Ω to V_S/2, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3693IDBQ						TEST LEVEL (1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C (2)	0°C to +70°C (3)	–40°C to +85°C (3)	UNITS	MIN/ MAX	
INPUT								
Least Positive Input Voltage		1.6	1.7	1.8	1.8	V	max	B
Most Positive Input Voltage		3.4	3.3	3.2	3.2	V	min	B
Noninverting Input Impedance		300 || 1.2				kΩ || pF	typ	C
OUTPUT								
Most Positive Output Voltage	No Load	4.2	**4.0**			V	min	A
	R_L = 100Ω Load to V_S/2	4.0	**3.9**			V	min	A
Least Positive Output Voltage	No Load	0.8	**1.0**			V	max	A
	R_L = 100Ω Load to V_S/2	1.0	**1.1**			V	max	A
Current Output Sourcing, Sinking	V_O = V_S/2	±100	**±85**	±80	±70	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.18				Ω	typ	C
DISABLE (Disabled LOW)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0, All Channels	–400	–550	-600	-625	µA	typ	C
Disable Time		1				µs	typ	C
Enable Time		25				ns	typ	C
Off Isolation	G = +2, 10MHz	70				dB	typ	C
Output Capacitance in Disable		4				pF	typ	C
Turn-On Glitch	G = +2, V_{IN} = V_S/2	±100				mV	typ	C
Turn-Off Glitch	G = +2, V_{IN} = V_S/2	±20				mV	typ	C
Enable Voltage		3.3	3.5	3.6	3.7	V	min	B
Disable Voltage		1.8	1.7	1.6	1.5	V	max	B
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0, Each Channel	75	130	143	149	µA	typ	C
POWER SUPPLY								
Specified Single-Supply Operating Voltage		5				V	typ	C
Minimum Operating Voltage			+3.5	+3.6	+3.8	V	min	B
Maximum Single-Supply Operating Voltage			**+12**	+12	+12	V	max	A
Maximum Quiescent Current	V_S = +5V	34.5	**36.5**	38	39.2	mA	max	A
Minimum Quiescent Current	V_S = +5V	34.5	**32**	28.1	27.2	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input-Referred	53				dB	typ	C
TEMPERATURE RANGE								
Specification: IDBQ		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
DBQ SSOP-16		80				°C/W	typ	C

TYPICAL CHARACTERISTICS: ±5V

At G = +2 (–IN grounded) and R_L = 100Ω, unless otherwise noted.

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

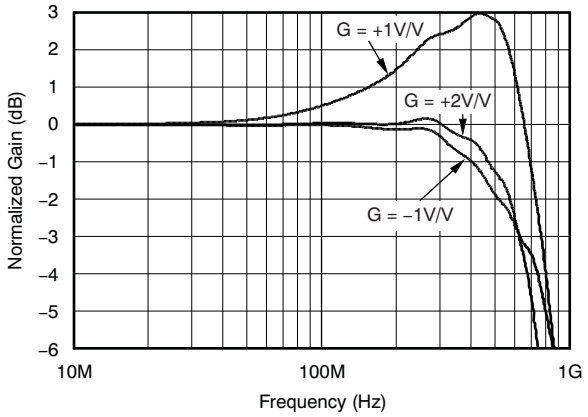


Figure 1.

NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE

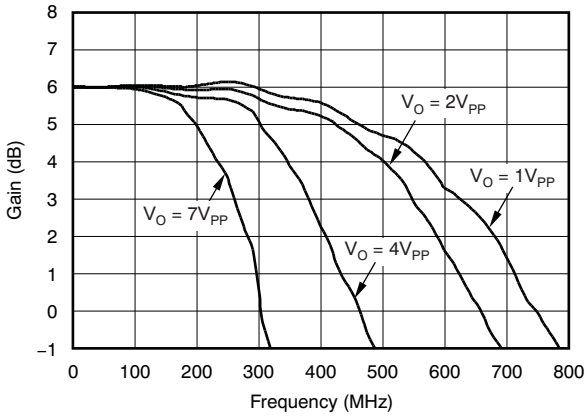


Figure 2.

FREQUENCY RESPONSE FLATNESS vs LOAD

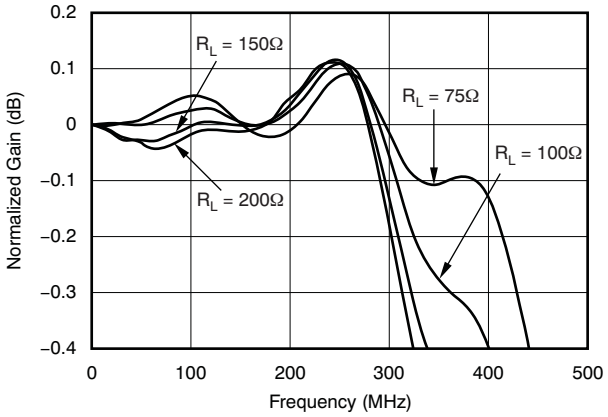


Figure 3.

DEVIATION FROM LINEAR PHASE

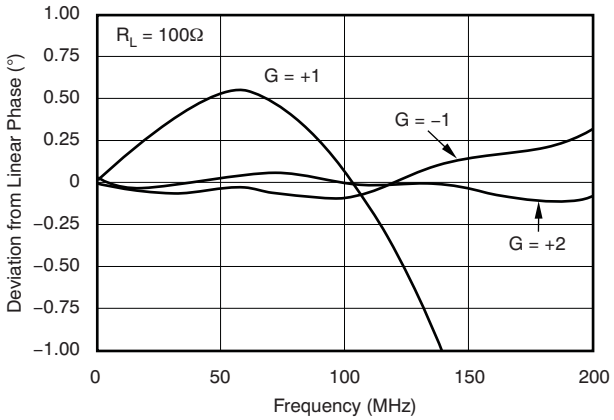


Figure 4.

GAIN OF +2 PULSE RESPONSE

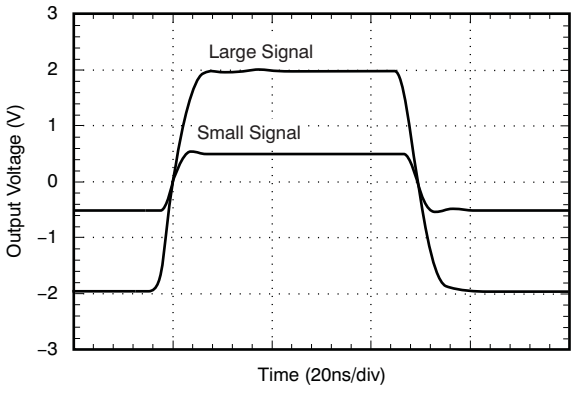


Figure 5.

GAIN OF +1 PULSE RESPONSE

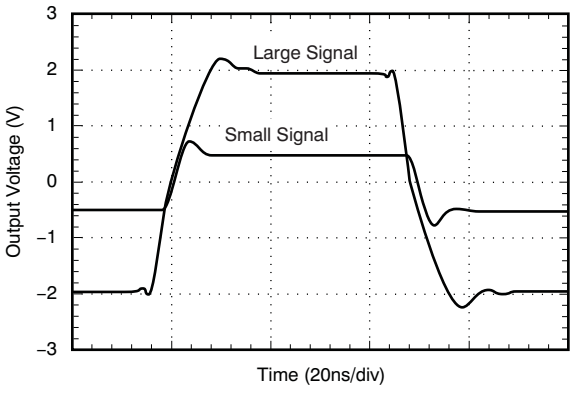


Figure 6.

TYPICAL CHARACTERISTICS: ±5V (continued)

At G = +2 (–IN grounded) and R_L = 100Ω, unless otherwise noted.

10MHz HARMONIC DISTORTION vs LOAD RESISTANCE

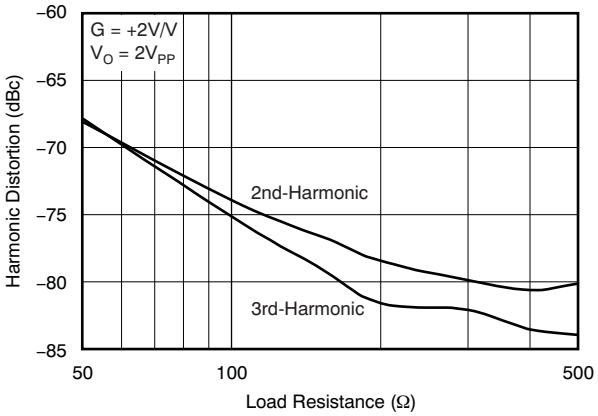


Figure 7.

10MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

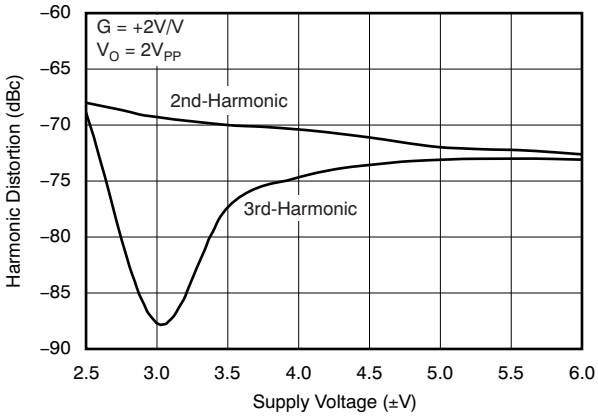


Figure 8.

10MHz HARMONIC DISTORTION vs OUTPUT VOLTAGE

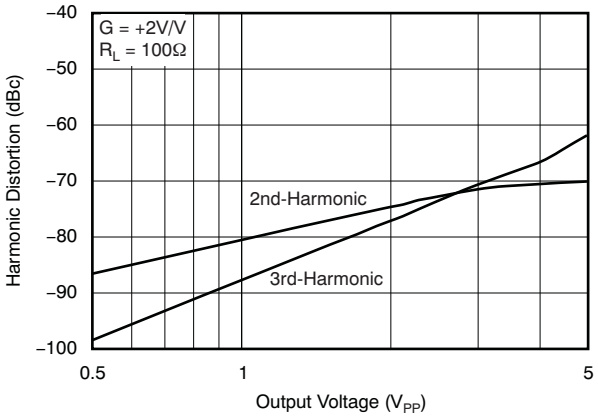


Figure 9.

G = +2 HARMONIC DISTORTION vs FREQUENCY

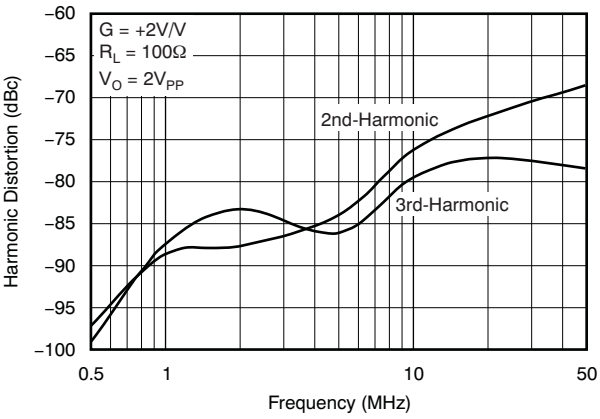


Figure 10.

G = +1 HARMONIC DISTORTION vs FREQUENCY

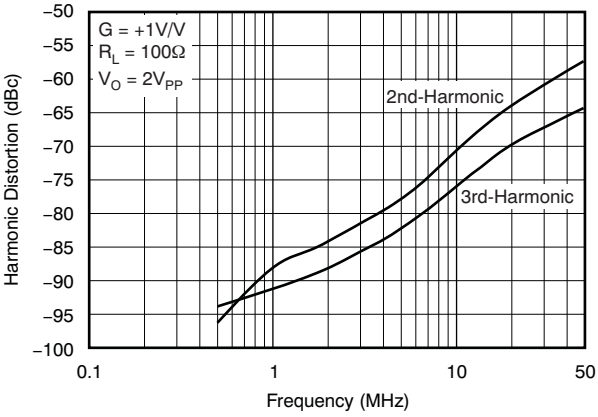


Figure 11.

G = –1 HARMONIC DISTORTION vs FREQUENCY

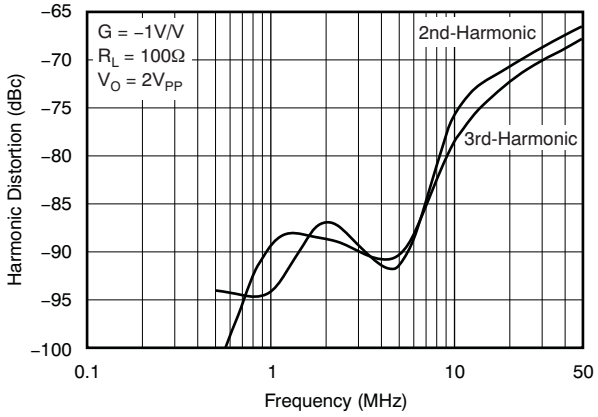


Figure 12.

TYPICAL CHARACTERISTICS: ±5V (continued)

At G = +2 (–IN grounded) and R_L = 100Ω, unless otherwise noted.

2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

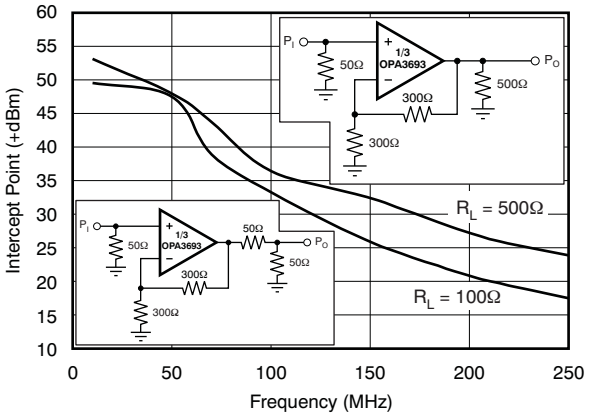


Figure 13.

INPUT VOLTAGE vs CURRENT NOISE DENSITY

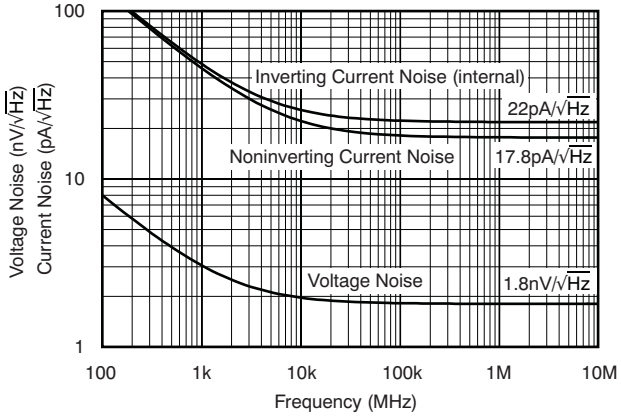


Figure 14.

RECOMMENDED R_S vs CAPACITIVE LOAD

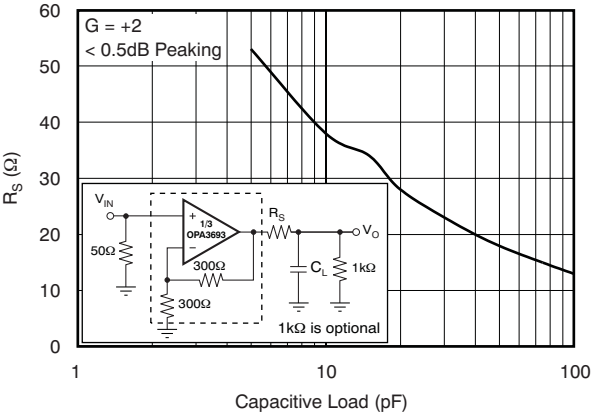


Figure 15.

SMALL-SIGNAL FREQUENCY RESPONSE vs CAPACITIVE LOAD

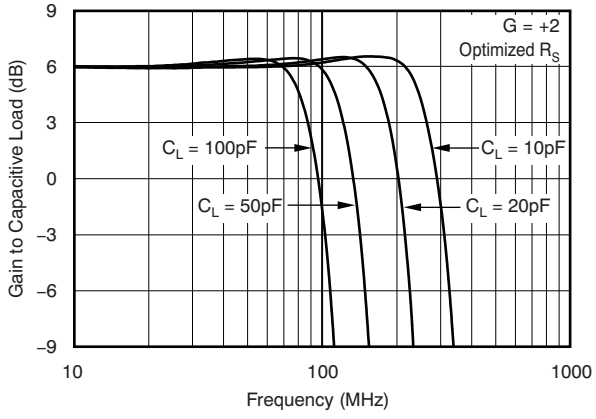


Figure 16.

SETTLING TIME

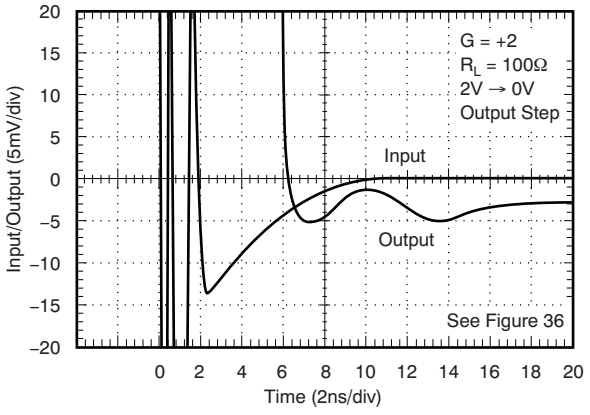


Figure 17.

DISABLED FEEDTHROUGH vs FREQUENCY

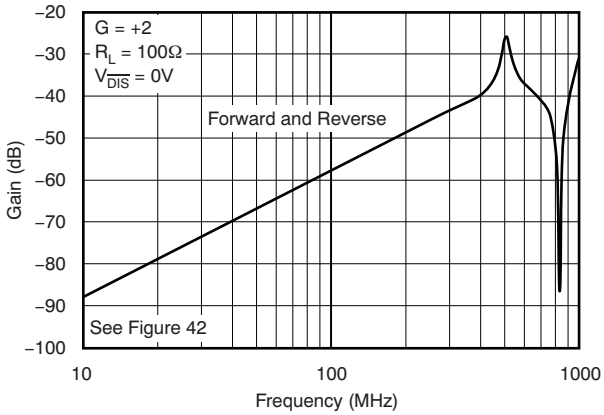


Figure 18.

TYPICAL CHARACTERISTICS: ±5V (continued)

At G = +2 (–IN grounded) and R_L = 100Ω, unless otherwise noted.

PSRR vs FREQUENCY

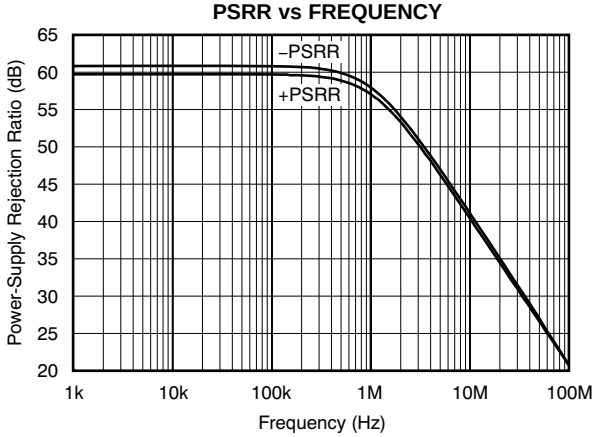


Figure 19.

CLOSED-LOOP OUTPUT IMPEDANCE

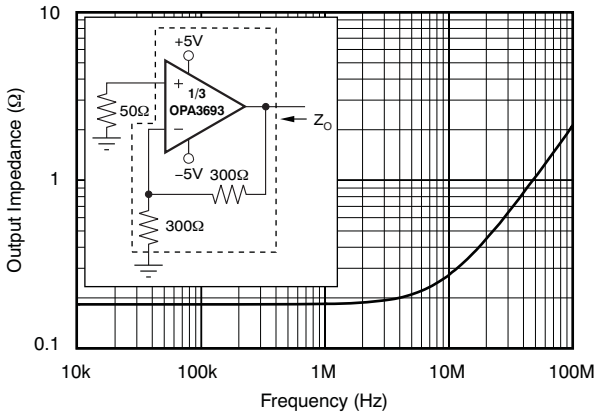


Figure 20.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

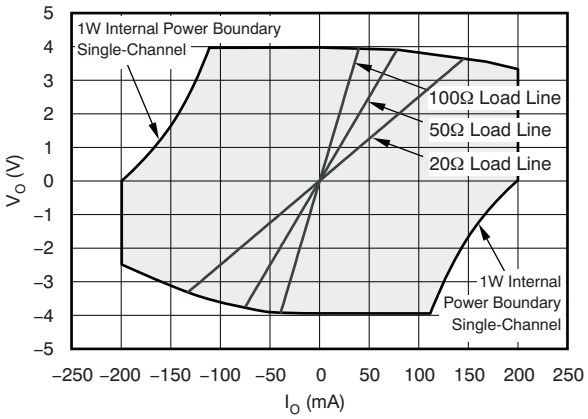


Figure 21.

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE

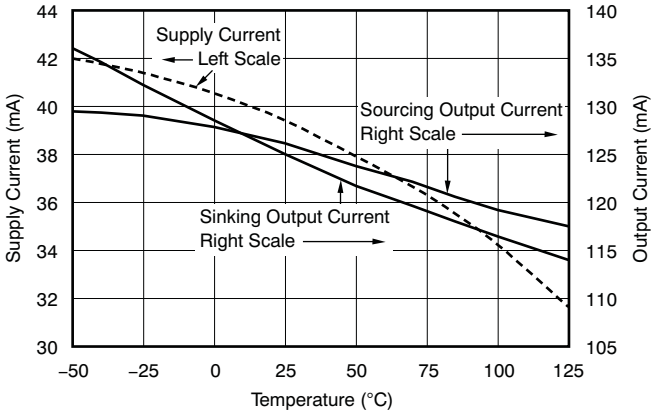


Figure 22.

NONINVERTING OVERDRIVE RECOVERY

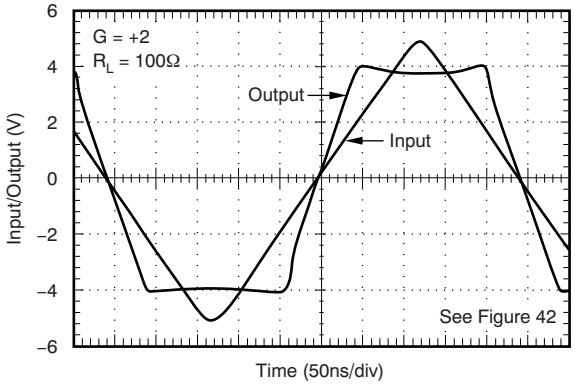


Figure 23.

INVERTING OVERDRIVE RECOVERY

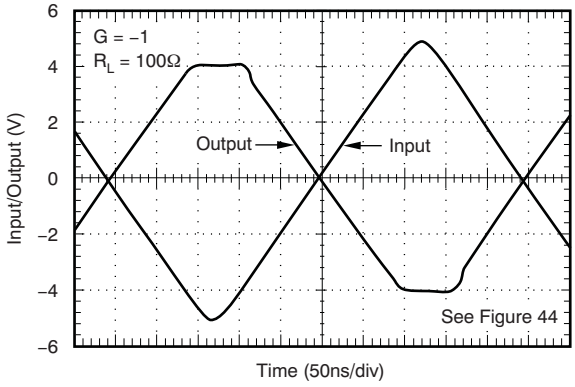


Figure 24.

TYPICAL CHARACTERISTICS: ±5V (continued)

At G = +2 (–IN grounded) and R_L = 100Ω, unless otherwise noted.

TYPICAL DC DRIFT OVER TEMPERATURE

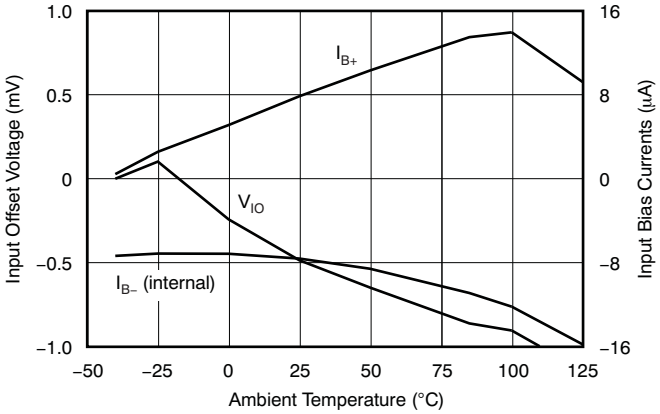


Figure 25.

COMMON-MODE INPUT AND OUTPUT SWING vs SUPPLY VOLTAGE

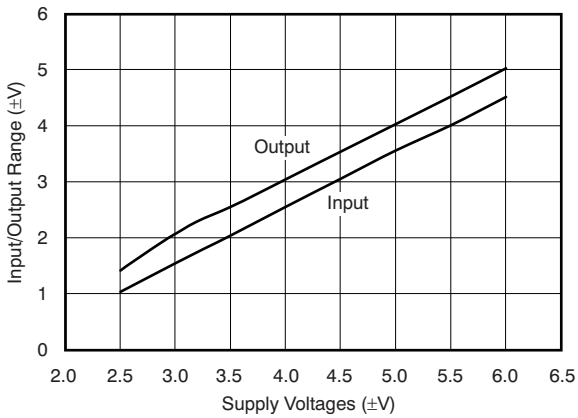


Figure 26.

COMPOSITE VIDEO dG/dP

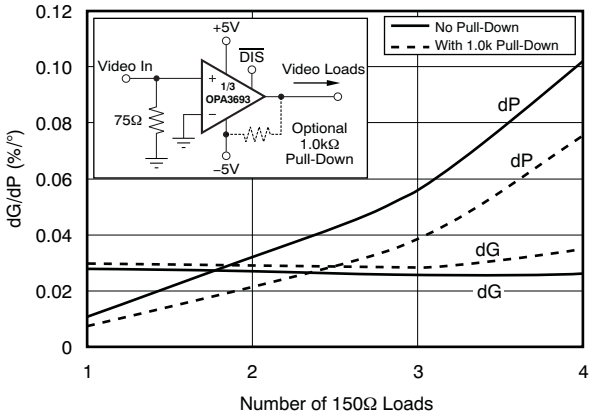


Figure 27.

LARGE-SIGNAL DISABLE/ENABLE RESPONSE

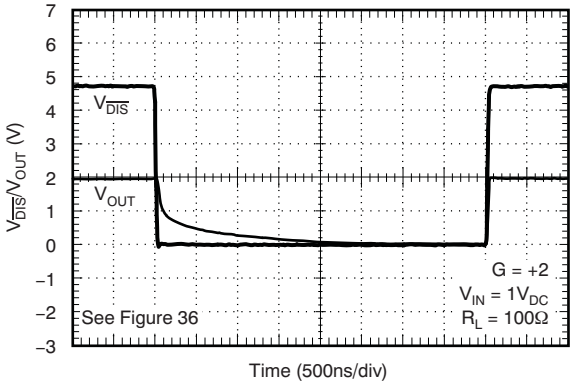


Figure 28.

INPUT RETURN LOSS vs FREQUENCY (S11)

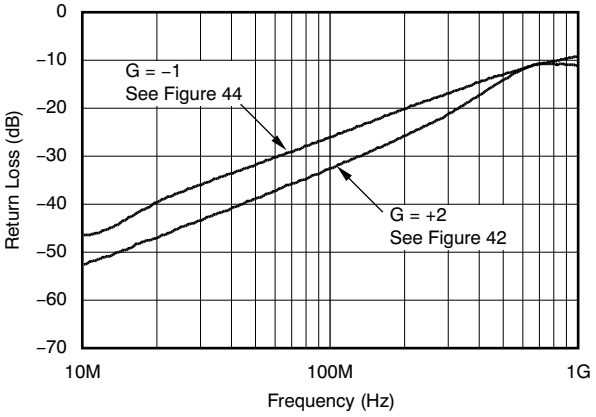


Figure 29.

OUTPUT RETURN LOSS vs FREQUENCY (S22)

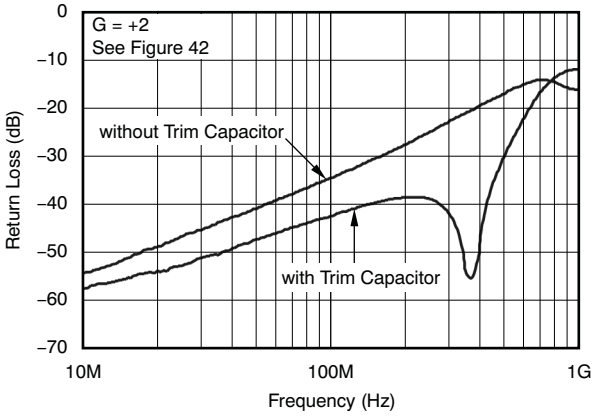


Figure 30.

TYPICAL CHARACTERISTICS: ±5V (continued)

At G = +2 (–IN grounded) and R_L = 100Ω, unless otherwise noted.

ALL HOSTILE CROSSTALK

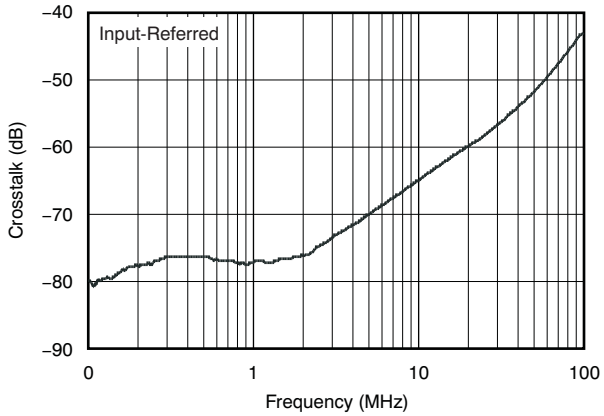


Figure 31.

TYPICAL CHARACTERISTICS: +5V

At G = +2V/V (–IN grounded) and R_L = 100Ω to V_S/2, unless otherwise noted.

NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE

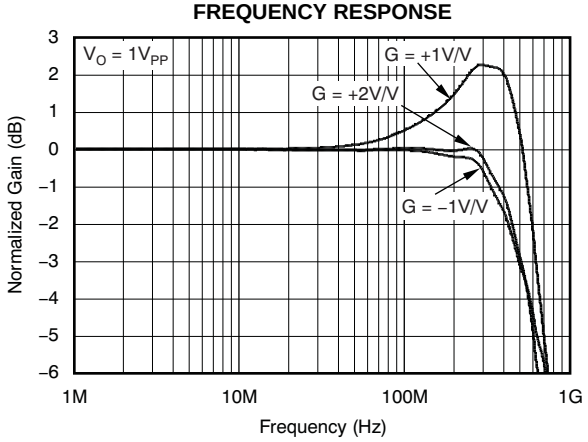


Figure 32.

LARGE-SIGNAL FREQUENCY RESPONSE

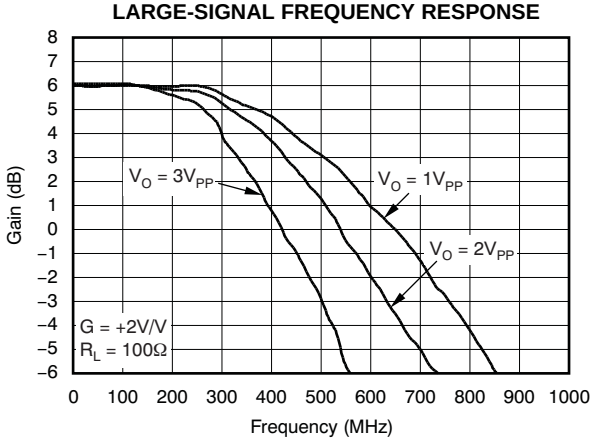


Figure 33.

FREQUENCY RESPONSE FLATNESS vs LOAD

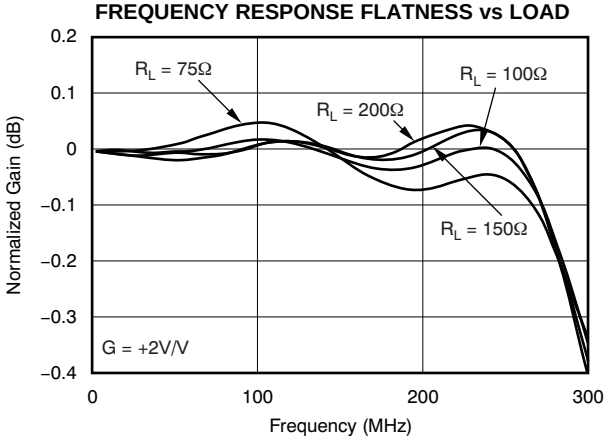


Figure 34.

SMALL-SIGNAL BANDWIDTH vs SINGLE-SUPPLY VOLTAGE

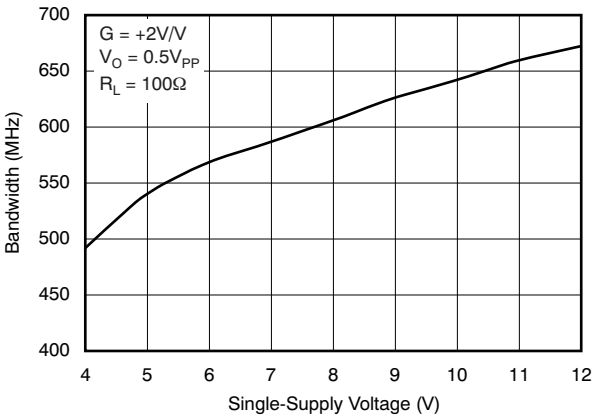


Figure 35.

GAIN OF +2 PULSE RESPONSE

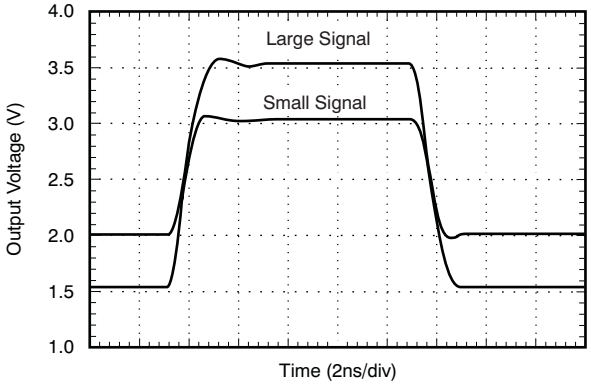


Figure 36.

GAIN OF +1 PULSE RESPONSE

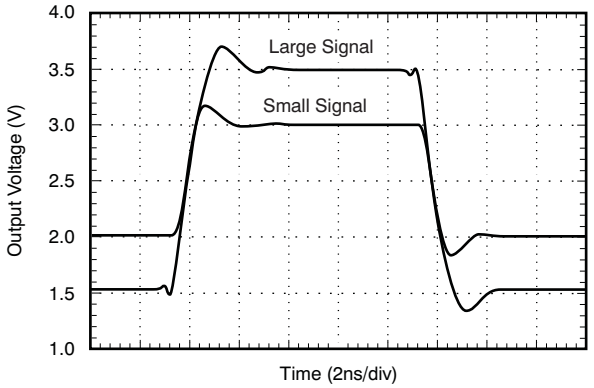


Figure 37.

TYPICAL CHARACTERISTICS: +5V (continued)

At G = +2V/V (–IN grounded) and R_L = 100Ω to V_S/2, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY (G = +2)

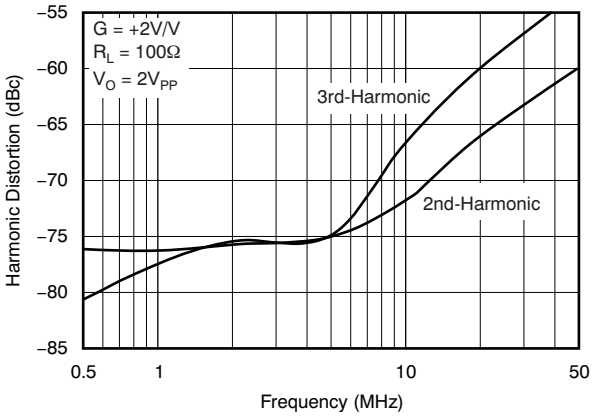


Figure 38.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

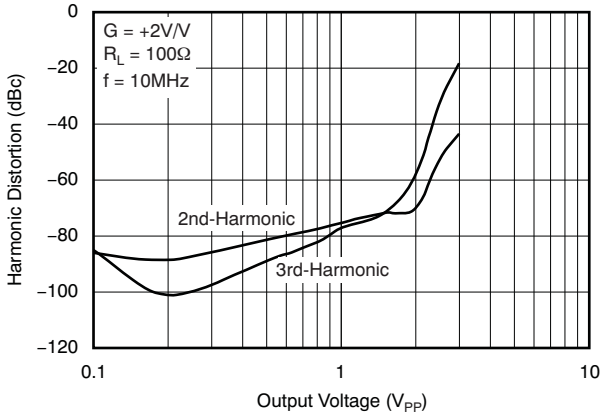


Figure 39.

HARMONIC DISTORTION vs LOAD RESISTANCE

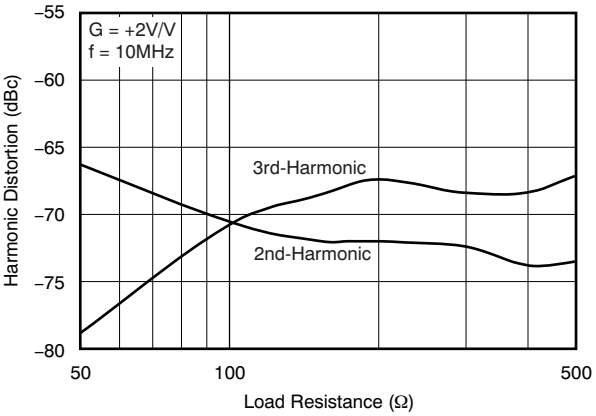


Figure 40.

2-TONE, 3RD-ORDER INTERMODULATION INTERCEPT

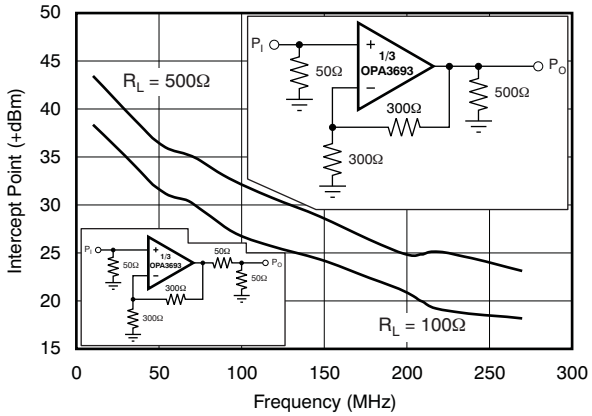


Figure 41.

APPLICATION INFORMATION

WIDEBAND BUFFER OPERATION

The OPA3693 gives the exceptional ac performance of a wideband current-feedback op amp with a highly linear output stage. It features internal R_F and R_G resistors, making it a simple matter to select a gain of +2V/V, +1V/V, or –1V/V with no external resistors. Requiring only 13mA/ch supply current, the OPA3693 output swings to within 1V of either supply with > 650MHz small-signal bandwidth and > 250MHz delivering $7V_{PP}$ into a 100Ω load. This low output headroom in a very high-speed amplifier gives remarkable single +5V operation. The OPA3693 delivers $2V_{PP}$ swing with > 400MHz bandwidth operating on a single +5V supply. The primary advantage of a current-feedback fixed-gain video buffer (as opposed to a slew-enhanced, low-gain, stable voltage-feedback implementation) is a higher slew rate with lower quiescent power and output noise.

Figure 42 shows the dc-coupled, gain of +2V/V, dual power-supply circuit configuration used as the basis for the ±5V Electrical Characteristics table and Typical Characteristics curves. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins while load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 42, the total effective load is 100Ω || 600Ω = 85.7Ω. The disable control line ($\overline{DIS}$) is typically left open to ensure normal amplifier operation. In addition to the usual power-supply decoupling capacitors to ground, a 0.01µF capacitor can be included between the two power-supply pins. This optional added capacitor typically improves the 2nd-harmonic distortion performance by 3dB to 6dB.

Figure 43 shows the DC-coupled, gain of +1V/V buffer configuration used as a starting point for the gain of +5V Typical Characteristic curves. In this case, the inverting input resistor, R_G, is left open giving a very broadband gain of +1V/V performance. While the test circuit shows a 50Ω input resistor, a buffer application is typically transforming from a source that cannot drive a heavy load to a 100Ω load, such as shown in Figure 43. The noninverting input impedance of the OPA3693 is typically 100kΩ || 2pF. Driving directly into the noninverting input provides this very light load to the source. However, the source must provide the noninverting input bias current required by the input stage to operate. An alternative approach to a gain of +1 buffer is described in the Wideband Unity-Gain Buffer section of this data sheet.

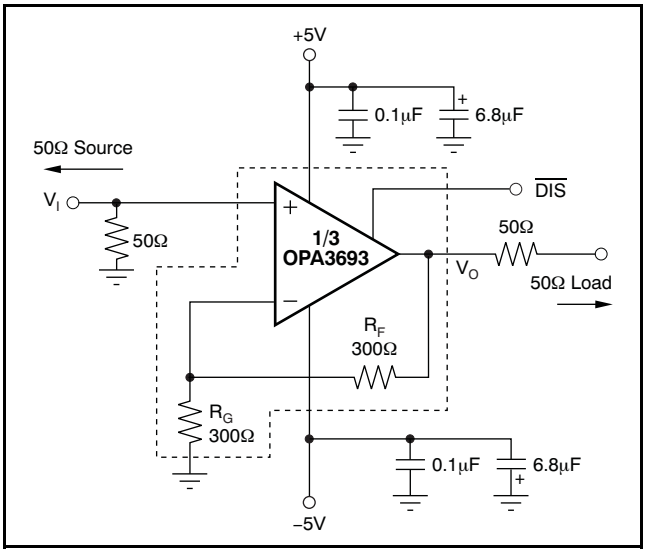


Figure 42. DC-Coupled, G = +2, Bipolar-Supply, Specification and Test Circuit

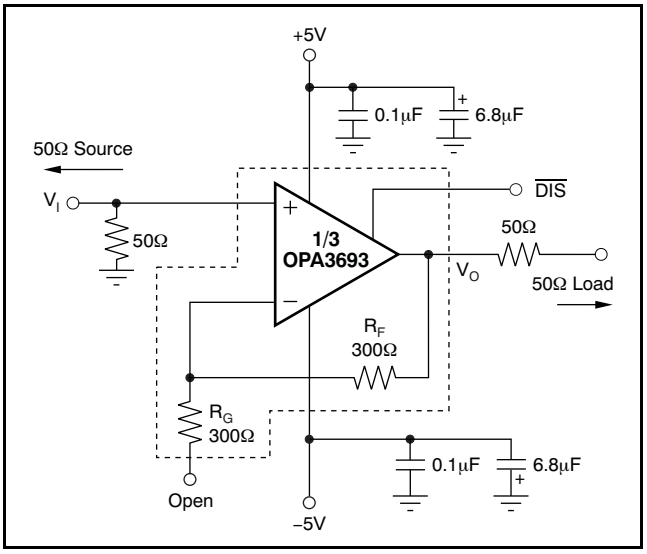


Figure 43. DC-Coupled, G = +1V/V, Bipolar-Supply, Specification and Test Circuit

Figure 44 shows the DC-coupled, gain of –1V/V buffer configuration used as a starting point for the gain of –1V/V Typical Characteristic curves. The input impedance is set to 50Ω using the parallel combination of an external 60.4Ω resistor and the internal 300Ω R_G resistor. The noninverting input is tied directly to ground. Since the internal design for the OPA3693 is current-feedback, trying to get improved dc accuracy by including a resistor on the noninverting input to ground is ineffective. Using a direct short to ground on the noninverting input reduces both the contribution of the dc bias current and noise current to the output error. While the external 60.4Ω is used here to match to the 50Ω source from the test equipment, the maximum input impedance in this configuration is limited to the 300Ω R_G resistor even with the R_M resistor removed. Unlike the noninverting unity gain buffer application, removing R_M does not strongly impact the dc operating point because the short on the noninverting input of Figure 44 provides the dc operating voltage. This application of the OPA3693 provides a very broadband, high-output, signal inverter.

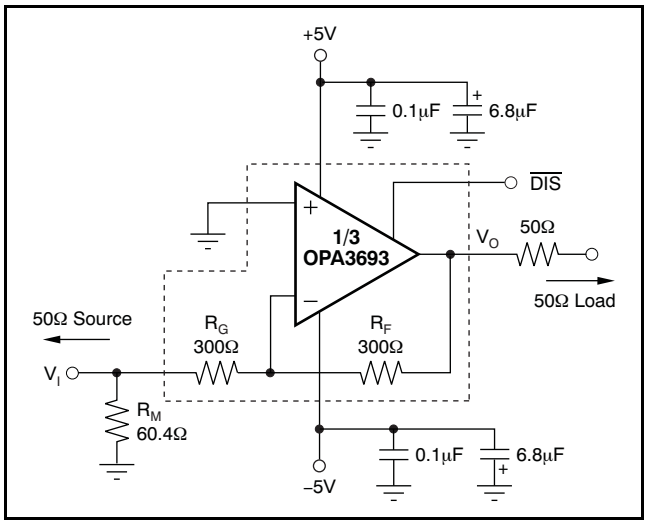


Figure 44. DC-Coupled, G = –1V/V, Bipolar-Supply Specification and Test Circuit

SINGLE-SUPPLY OPERATION

The OPA3693 may be used over a single-supply range of +3.5V to +12V. Though not a rail-to-rail output design, the OPA3693 requires minimal input and output voltage headroom compared to other very-wideband video buffer amplifiers. As illustrated in the single +5V Typical Characteristic curves, the OPA3693 provides > 300MHz bandwidth driving a $3V_{PP}$ swing into a 100Ω load. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the useable voltage ranges at both the input and the output.

The circuit of Figure 45 shows the AC-coupled, gain of +2V/V, video buffer circuit used as the basis for the Electrical Characteristics table and Typical Characteristics curves. The circuit of Figure 45 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 604Ω resistors). The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 1.6V of either supply pin, giving a $1.8V_{PP}$ input signal range centered between the supply pins. The input impedance matching resistor (60.4Ω) used for testing is adjusted to give a 50Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a dc gain of +1V/V, which puts the input dc bias voltage (2.5V) on the output as well. Again, on a single +5V supply, the output voltage can swing to within 1V of either supply pin while delivering more than 85mA output current. A demanding 100Ω load to a midpoint bias is used in this characterization circuit. The new output stage used in the OPA3693 can deliver large bipolar output current into this midpoint load with minimal crossover distortion, as illustrated by the +5V supply, 3rd-harmonic distortion plots.

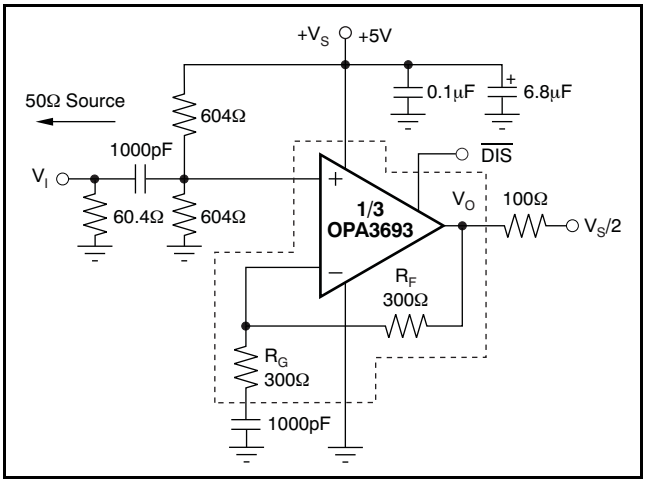


Figure 45. AC-Coupled, G = +2V/V, Single-Supply Specification and Test Circuit

While the circuit of Figure 45 shows +5V single-supply operation, this same circuit may be used for single supplies ranging as high as +12V nominal. The noninverting input bias resistors are relatively low in Figure 45 to minimize output dc offset as a result of noninverting input bias current. At higher signal-supply voltage, these resistors should be increased to limit the added supply current drawn through this path.

Figure 46 shows the AC-coupled, G = +1V/V, single-supply specification and test circuit. In this case, the gain setting resistor, R_G, is simply left open to get a gain of +1V for ac signals. Once again, the noninverting input is dc biased at midsupply, putting that same $V_S/2$ at the output pin. The signal is AC-coupled into this midpoint with an added termination resistor on the source side of the blocking capacitor.

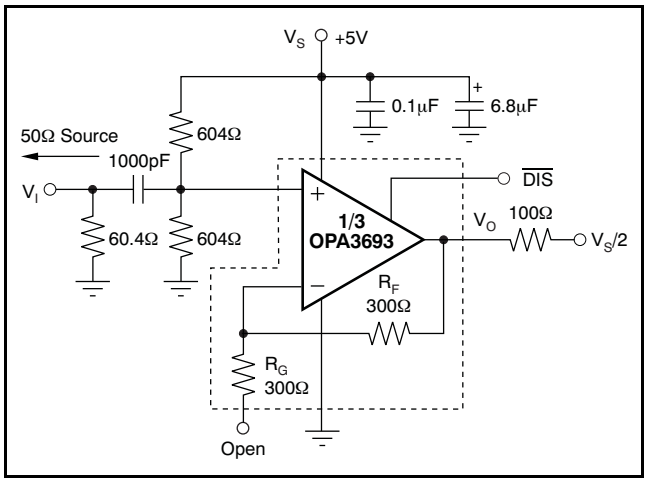


Figure 46. AC-Coupled, G = +1V/V, Single-Supply Specification and Test Circuit

WIDEBAND UNITY-GAIN BUFFER WITH IMPROVED FLATNESS

As shown in the Typical Characteristic curves, the unity-gain buffer configuration of Figure 43 illustrates a peaking in the frequency response exceeding 2dB. This configuration gives the slight amount of overshoot and ringing apparent in the gain of +1V/V pulse response curves. A similar circuit that holds a flatter frequency response, giving improved pulse fidelity, is shown in Figure 47. This circuit removes the peaking by bootstrapping out any parasitic effects on R_G.

The input impedance is still set by R_M as the apparent impedance looking into R_G is very high. R_M may be increased to show a higher input impedance, but larger values begin to impact dc output offset voltage.

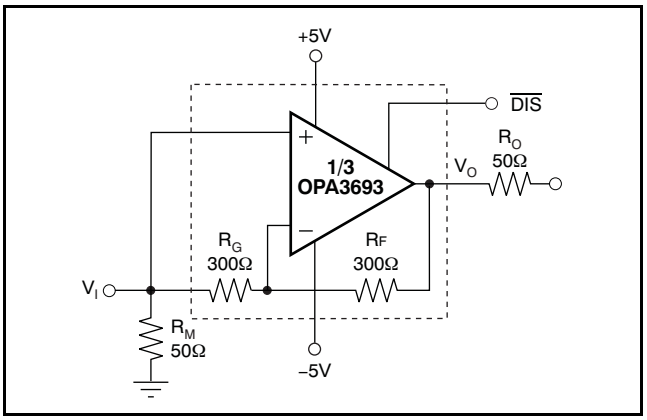


Figure 47. Improved Unity-Gain Buffer

This circuit creates an additional input offset voltage as the difference in the two input bias currents times the impedance to ground at V_I. Figure 48 shows a comparison of small-signal frequency response for the unity-gain buffer of Figure 43 compared to the improved approach shown in Figure 47.

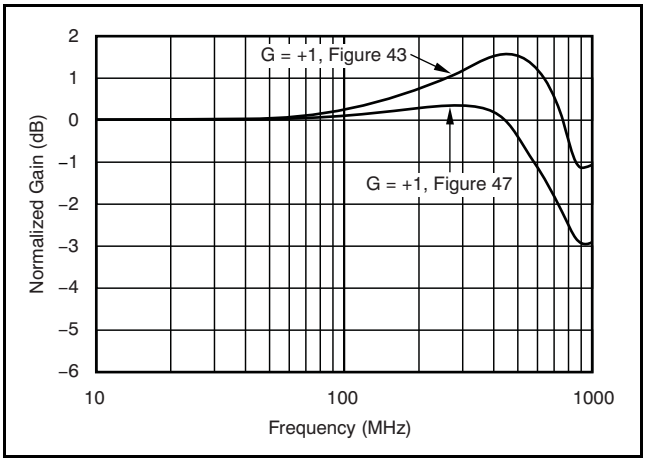


Figure 48. Buffer Frequency Response Comparison

HIGH-FREQUENCY ACTIVE FILTERS

The extremely wide bandwidth of the OPA3693 allows a wide range of active filter topologies to be implemented with minimal amplifier bandwidth interaction in the filter shape. Sallen-Key filters, for example, using either a gain of +1V/V or gain of +2V/V amplifier, may be easily implemented with no external gain setting elements. In general, given a desired filter ω_O, the amplifier should have at least 20X that ω_O to minimize filter interaction with the amplifier frequency response. Figure 49 illustrates an example gain of +2 line driver using the OPA3693 that incorporates a 40MHz low-pass Butterworth response with just a few external components. The filter resistor values have been adjusted slightly here from an ideal filter analysis to account for parasitic effects.

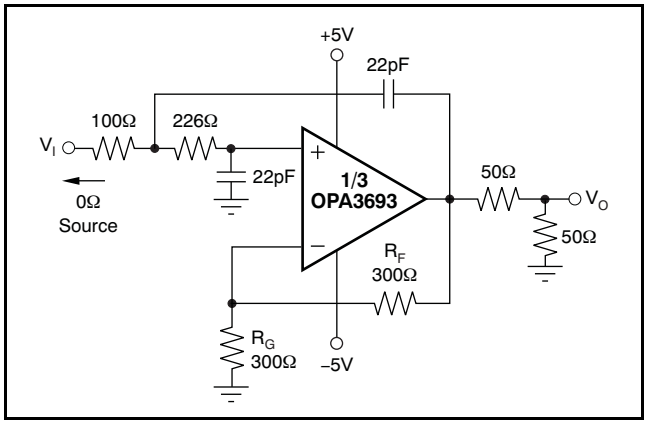


Figure 49. Line Driver with 40MHz Low-Pass Active Filter

This type of filter depends on a low output impedance from the amplifier through very high frequencies to continue to provide an increasing attenuation with frequency. As the amplifier output impedance rises with frequency, any input signal or noise starts to feed directly through to the output via the feedback capacitor. Because the OPA3693 used in Figure 49 has a 650MHz bandwidth, the active filter continues to rolloff through frequencies exceeding 200MHz. Figure 50 shows the frequency response for the filter of Figure 49, where the desired 40MHz cutoff is achieved and a 40dB/dec roll-off is held through very high frequencies.

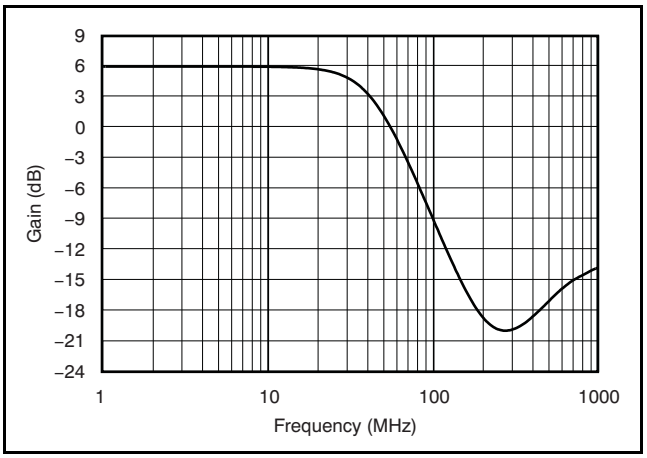


Figure 50. 40MHz Low-Pass Active Filter Response

HIGH-SPEED INSTRUMENTATION AMPLIFIER

Figure 51 shows an instrumentation amplifier based on the OPA3693. The offset matching between inputs makes this configuration an attractive input stage for this application. The differential-to-single-ended gain for this circuit is 2V/V. The inputs are high-impedance, with only 1.2pF to ground at each input. The loads on the OPA3693 outputs are equal for the best harmonic distortion possible.

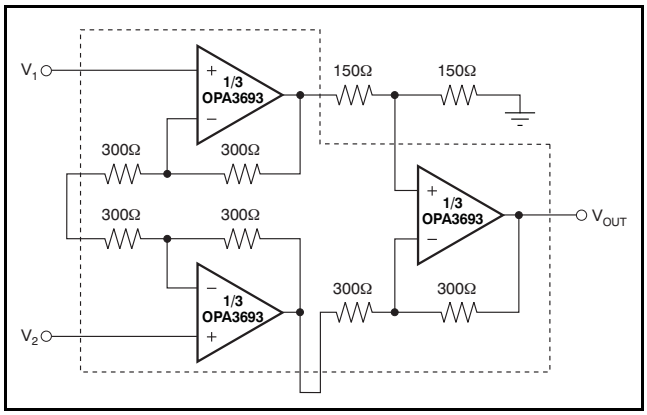


Figure 51. High-Speed Instrumentation Amplifier

As shown in Figure 52, the OPA3693 used as an instrumentation amplifier has a 420MHz, –3dB bandwidth. This plot has been made for a $1V_{PP}$ output signal using a low-impedance differential input source.

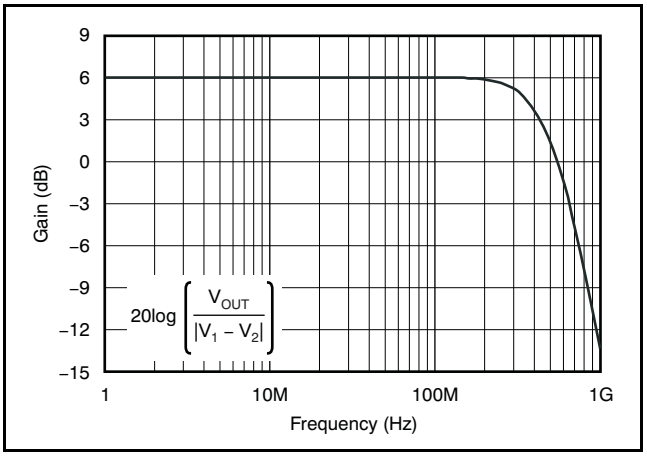


Figure 52. High-Speed Instrumentation Amplifier Response

MULTIPLEXED CONVERTER DRIVER

The converter driver in Figure 53 multiplexes among the three input signals. The OPA3693 enable and disable times support multiplexing among video signals. The make-before-break disable characteristic of the OPA3693 ensures that the output is always under control. To avoid large switching glitches, switch during the sync or retrace portions of the video signal—the two inputs should be almost equal at these times. The output is always under control, so the switching glitches for two 0V inputs are < 20mV. With standard video signals levels at the inputs, the maximum differential voltage across the disabled inputs does not exceed the ±1.2V maximum allowed.

The output resistors isolate the outputs from each other when switching between channels. The feedback network of the disabled channels forms part of the load seen by the enabled amplifier, attenuating the signal slightly.

LOW-PASS FILTER

The circuit in Figure 54 realizes a 7th-order Butterworth low-pass filter with a –3dB bandwidth of 20MHz. This filter is based on the KRC active filter topology that uses an amplifier with the fixed gain ≥ 1. The OPA3693 makes a good amplifier for this type of filter. The component values have been adjusted to compensate for the parasitic effects of the op amp.

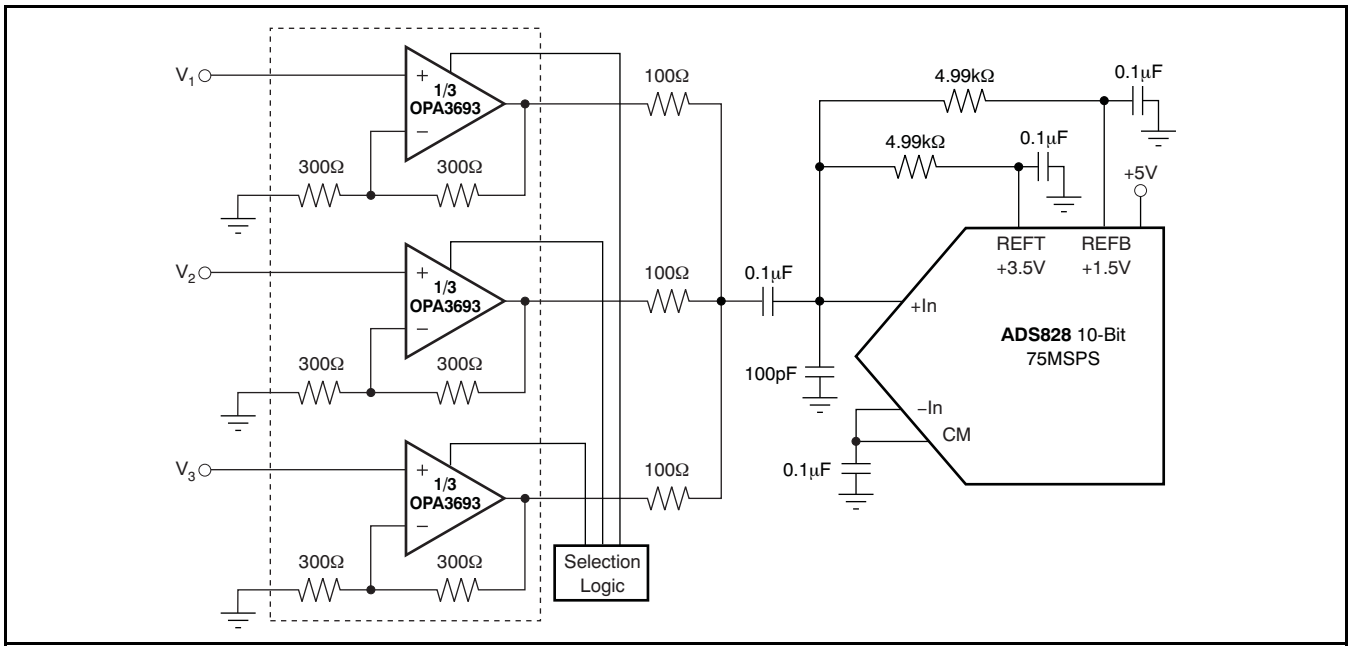


Figure 53. Multiplexed Converter Driver

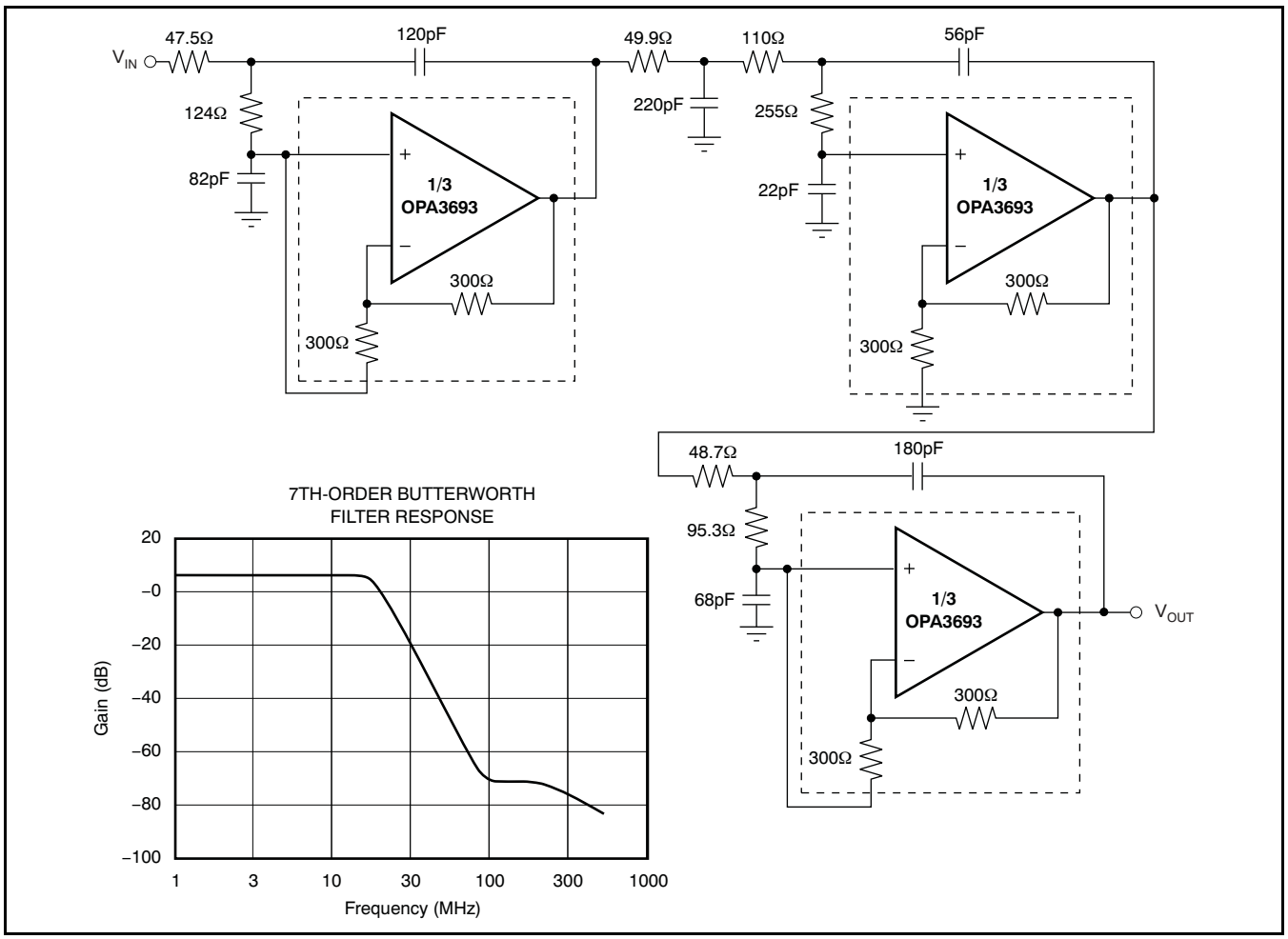


Figure 54. 7th-Order Butterworth Filter

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA3693. The fixture is offered free of charge as an unpopulated PCB, delivered with a user's guide. The summary information for this fixture is shown in Table 2.

Table 2. Demonstration Fixture

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA3693IDBQ, Noninverting	SSOP-16	DEM-OPA-SSOP-3C	SBOU047
OPA3693IDBQ, Inverting	SSOP-16	DEM-OPA-SSOP-3D	SBOU046

The demonstration fixture can be requested at the Texas Instruments web site (www.ti.com) through the OPA3693 product folder.

OPERATING SUGGESTIONS

GAIN SETTING

Setting the gain for the OPA3693 is very easy. For a gain of +2, ground the –IN pin and drive the +IN pin with the signal. For a gain of +1, either leave the –IN pin open and drive the +IN pin or drive both the +IN and –IN pins (see Figure 47). For a gain of –1, ground the +IN pin and drive the –IN pin with the input signal. An external resistor may be used in series with the –IN pin to reduce the gain. However, because the internal resistors (R_F and R_G) have a tolerance and temperature drift different than the external resistor, the absolute gain accuracy and gain drift over temperature are relatively poor compared to the previously described standard gain connections using no external resistor.

OUTPUT CURRENT AND VOLTAGE

The OPA3693 provides output voltage and current capabilities that can easily support multiple video loads and/or 100Ω loads with very low distortion. Under no-load conditions at +25°C, the output voltage typically swings to 1V of either supply rail; the tested swing limit is within 1.2V of either rail. Into a 15Ω load (the minimum tested load), it is tested to deliver more than ±90mA.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage × current, or V-I product, which is more relevant to circuit operation. Refer to the Output Voltage and Current Limitations plot (Figure 21) in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA3693 output drive capabilities, noting that the graph is bounded by a *Safe Operating Area* of 1W maximum internal power dissipation. Superimposing resistor load lines onto the plot shows that the OPA3693 can drive ±3.4V into 20Ω or ±3.7V into 50Ω without exceeding either the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test-circuit load) shows full ±3.8V output swing capability, as shown in the Typical Characteristics.

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the over-temperature min/max specifications. As the output transistors deliver power, their junction temperatures increase, which decreases their V_{BE}s (increasing the available output voltage swing) and increases their current gains (increasing the available output current). In steady-state operation, the available output voltage and current is always greater than that shown in the over-temperature characteristics since the output stage junction temperatures are higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This configuration is not normally a problem, since most applications include a series matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to an adjacent positive power-supply pin, in most cases, destroys the amplifier. If additional protection to a power-supply short is required, consider a small series resistor in the power-supply leads. Under heavy output loads, this reduces the available output voltage swing. A 5Ω series resistor in each supply lead limits the internal power dissipation to < 1W for an output short while decreasing the available output voltage swing only 0.5V, for up to 100mA desired load currents. Always place the 0.1µF power-supply decoupling capacitors after these supply-current limiting resistors directly on the device supply pins.

DRIVING CAPACITIVE LOADS

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an analog-to-digital converter (ADC), including additional external capacitance, which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA3693 can be very susceptible to decreased stability and may give

closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This resistor does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show a *Recommended R_S vs Capacitive Load* curve (Figure 15) to help the designer pick a value to give < 0.5dB peaking to the load. The resulting frequency response curves show a 0.5dB peaked response for several selected capacitive loads and recommended R_S combinations. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA3693. Long PCB traces, unmatched cables, and connections to other amplifier inputs can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA3693 output pin (see the Board Layout Guidelines section).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load (< 0.5dB peaking). For the OPA3693 operating at a gain of +2V/V, the frequency response at the output pin is very flat to begin with, allowing relatively small values of R_S to be used for low capacitive loads.

DISTORTION PERFORMANCE

The OPA3693 provides good distortion performance into a 100Ω load on ±5V supplies. Relative to alternative solutions, the OPA3693 holds much lower distortion at higher frequencies (> 20MHz) than alternative solutions. Generally, until the fundamental signal reaches very high-frequency or power levels, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration (see Figure 42), this value is the sum of $R_F + R_G$, while in the inverting configuration it is just R_F (see Figure 44). Also, providing an additional supply decoupling capacitor (0.01µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

The OPA3693 has an extremely low 3rd-order harmonic distortion. This feature also produces a high two-tone, 3rd-order intermodulation intercept. Two graphs for this intercept are given in the in the Typical Characteristics; one for ±5V and one for +5V. The lower curve shown in each graph is defined at the 50Ω load when driven through a 50Ω matching resistor, to allow direct comparisons to RF MMIC devices. The higher curve in each graph shows the intercept if the output is taken directly at the output pin with a 500Ω load, to allow prediction of the 3rd-order spurious level when driving a lighter load, such as an ADC input. The output matching resistor attenuates the voltage swing from the output pin to the load by 6dB. If the OPA3693 drives directly into the input of a high-impedance device, such as an ADC, this 6dB attenuation is not taken and the intercept increases, as shown in the 500Ω load typical characteristic.

The intercept is used to predict the intermodulation spurious levels for two closely-spaced frequencies. If the two test frequencies (f1 and f2) are specified in terms of average and delta frequency, $f_O = (f1 + f2)/2$ and $\Delta f = |f2 – f1|/2$, then the two, 3rd-order, close-in spurious tones appear at $f_O \pm 3 \times \Delta f$. The difference between two equal test tone power levels and these intermodulation spurious power levels is given by $\Delta dBc = 2 \times (IM3 – P_O)$, where IM3 is the intercept taken from the Typical Characteristics and P_O is the power level in dBm at the 50Ω load for one of the two closely-spaced test frequencies. For instance, at 50MHz, the OPA3693 at a gain of +2 has an intercept of 47dBm at a matched 50Ω load. If the full envelope of the two frequencies needs to be $2V_{PP}$ at this load, this requires each tone to be 4dBm ($1V_{PP}$). The 3rd-order intermodulation spurious tones will then be 2 × (47 – 4) = 83dBc below the test tone power level (–79dBm). If this same $2V_{PP}$ two-tone envelope were delivered directly into a lighter 500Ω load, the intercept would increase to the 48dBm shown in the Typical Characteristics. With the same output signal and gain conditions, but now driving directly into a light load with no matching loss, the 3rd-order spurious tones will then be at least 2 × (48 – 4) = 92dBc below the 4dBm test tone power levels centered on 50MHz (–88dBm). We are still using a 4dBm for the $1V_{PP}$ output swing into this 500Ω load. While not strictly correct from a power standpoint, this does give the correct prediction for spurious level. The class AB output stage for the OPA3693 is much more voltage-swing-dependent on output distortion than strictly power-dependent. To use the 500Ω intercept curve, use the single-tone voltage swing as if it were driving a 50Ω load to compute the P_O used in the intercept equation.

GAIN ACCURACY AND LINEARITY

The OPA3693 provides improved absolute gain accuracy and dc linearity over earlier fixed gain of two line drivers. Operating at a gain of +2V/V by tying the –IN pin to ground, the OPA3693 shows a maximum gain error of ±1% at +25°C. The dc gain therefore lies between 1.98V/V and 2.02V/V at room temperature. Over the specified temperature ranges, this gain tolerance expands only slightly due to the matched temperature drift for R_F and R_G. Achieving this gain accuracy requires a very low impedance ground at –IN. Typical production lots show a much tighter distribution in gain than this ±1% specification. Figure 55 shows a typical distribution in measured gain at the gain of +2V/V configuration, in this case showing a slight drop in the mean (0.25%) from the nominal but with a very tight distribution.

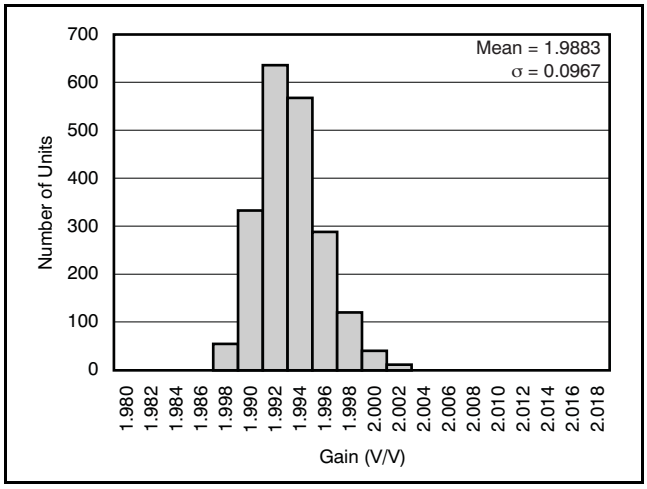


Figure 55. Typical +2V/V Gain Distribution

The exceptionally linear output stage (as illustrated by the high 3rd-order intermodulation intercept) and low thermal gradient induced errors for the OPA3693 give an extremely linear output over large voltage swings and heavy loads. Figure 56 shows the tested deviation (in % of peak-to-peak) from linearity for a range of symmetrical output swings and loads. Below $4V_{PP}$, for either a 100Ω or a 500Ω load, the OPA3693 delivers greater than 14-bit linear output response.

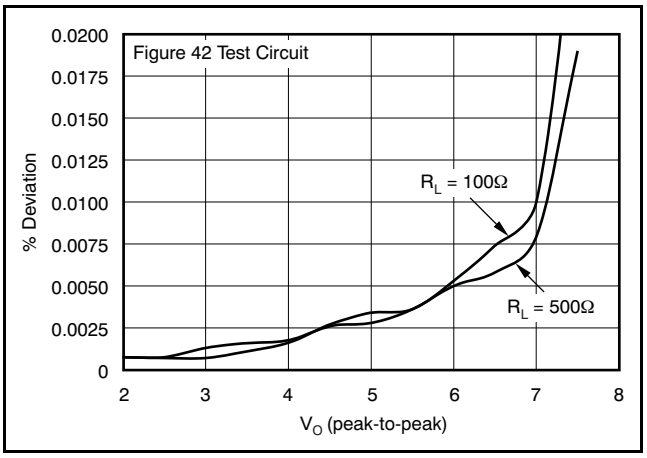


Figure 56. DC Linearity vs Output Swing and Loads

NOISE PERFORMANCE

The OPA3693 offers an excellent balance between voltage and current noise terms to achieve a low output noise under a variety of operating conditions. The inverting node noise current (internal) appears at the output multiplied by the relatively low 300Ω feedback resistor. The input noise voltage (1.8nV/√Hz) is extremely low for a unity-gain stable amplifier. This low input voltage noise was achieved at the price of higher noninverting input current noise (17.8pA/√Hz). As long as the ac source impedance looking out of the noninverting input is less than 100Ω, this current noise does not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise for the each of the three gain settings available using the OPA3693. Figure 57 shows the op amp noise analysis model with all of the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

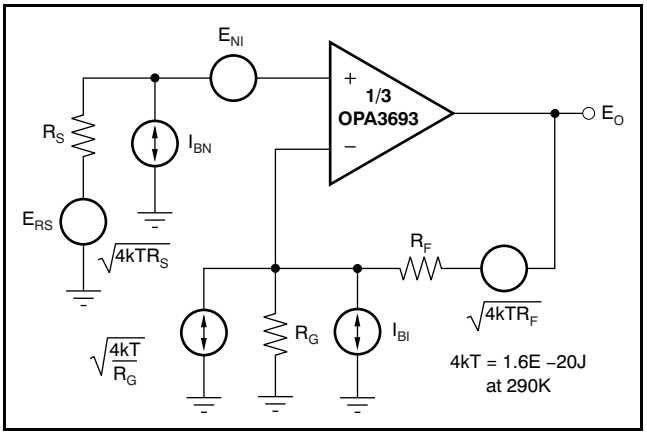


Figure 57. Op Amp Noise Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 57.

$$E_O = \sqrt{\left[E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right] NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \quad (1)$$

Dividing this expression through by noise gain (NG = 1 + R_F/R_G) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 2.

$$E_N = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (2)$$

Evaluating the output noise and input noise expressions for the two noninverting gain configurations, and with two different values for the noninverting source impedance, gives output and input-referred spot noise voltages of Table 3.

Table 3. Total Output and Input-Referred Noise

CONFIGURATION	R_S (Ω)	OUTPUT SPOT NOISE E_O (nV/√Hz)	TOTAL INPUT SPOT NOISE E_N (nV/√Hz)
G = +2 (Figure 42)	25	8.3	4.15
G = +2 (Figure 42)	300	14	7
G = +1 (Figure 43)	25	7.3	7.3
G = +1 (Figure 43)	300	9.2	9.2

The output noise is being dominated by the inverting current noise times the internal feedback resistor. This gives a total input-referred noise voltage that exceeds the 1.8nV voltage term for the amplifier itself.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp such as the OPA3693 provides exceptional bandwidth and slew rate giving fast pulse settling but only moderate dc accuracy. The Electrical Characteristics show an input offset voltage comparable to high-speed voltage-feedback amplifiers. However, the two input bias currents are somewhat higher and are unmatched. Whereas bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output dc offset for wideband current-feedback op amps. Since the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 42, using worst-case +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$\pm(NG \times V_{OS}) + (I_{BN} \times R_S/2 \times NG) \pm (I_{BI} \times R_F)$
$= \pm(2 \times 3.5mV) + (35\mu A \times 25\Omega \times 2) \pm (50\mu A \times 300\Omega)$
$= \pm 7mV \pm 1.75mV \pm 15mV$
$= \pm 23.75mV$

where NG = noninverting signal gain.

Minimizing the resistance seen by the noninverting input also minimizes the output dc error. For improved dc precision in a wideband low-gain amplifier, consider the OPA842 where a bipolar input is acceptable (low source resistance) or the OPA656 where a JFET input is required.

DISABLE OPERATION

The OPA3693 provides an optional disable feature that can be used to reduce system power. If the $V_{\overline{DIS}}$ control pin is left unconnected, the OPA3693 operates normally. This shutdown is intended only as a power-savings feature. Forward path isolation when disabled is very good for small signals for gains of +1 or +2. Large-signal isolation is not ensured. Using this feature to multiplex two or more outputs together is not recommended. Large signals applied to the disabled output stages can turn on parasitic devices degrading signal linearity for the desired channel.

Turn-on time is very quick from the shutdown condition (typically < 60ns). Turn-off time strongly depends on the selected gain configuration and load, but is typically 3µs for the circuit of Figure 42.

To shutdown, the control pin must be asserted low. This logic control is referenced to the positive supply, as the simplified circuit of Figure 58 shows.

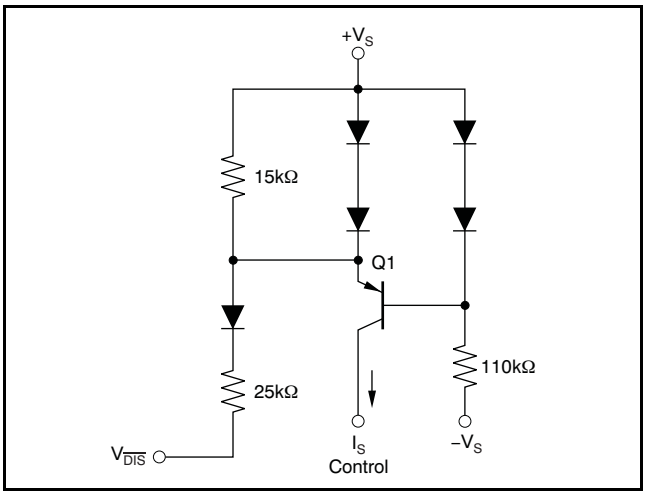


Figure 58. Simplified Disable Control Circuit

In normal operation, base current to Q1 is provided through the 110kΩ resistor while the emitter current through the 15kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in the Q1 emitter. As $V_{\overline{DIS}}$ is pulled LOW, additional current is

pulled through the 15kΩ resistor, eventually turning on these two diodes (≈ 80μA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately 0V. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the shutdown mode is only that required to operate the circuit of Figure 58.

The shutdown feature for the OPA3693 is a positive supply referenced, current-controlled interface. Open-collector (or drain) interfaces are most effective, as long as the controlling logic can sustain the resulting voltage (in the open mode) that appears at the $V_{\overline{DIS}}$ pin. That voltage is one diode below the positive supply voltage applied to the OPA3693. For voltage output logic interfaces, the on/off voltage levels described in the Electrical Characteristics apply only for a +5V positive supply on the OPA3693. An open-drain interface is recommended for shutdown operation using a higher positive supply for the OPA3693 and/or logic families with inadequate high-level voltage swings.

THERMAL ANALYSIS

The OPA3693 does not require heatsinking or airflow in most applications. Maximum desired junction temperature sets the maximum allowed internal power dissipation as described here. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this worst-case condition, $P_{DL} = V_S^2/(4 \times R_L)$ where R_L includes feedback network loading. This value is the absolute highest power that can be dissipated for a given R_L. All actual applications dissipate less power in the output stage.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA3693IDBQ (SSOP-16 package) in the circuit of Figure 42 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω load at $V_S/2$. Maximum internal power is:

$$P_D = 10V \times 43.5mA + 3 \times 5^2/(4 \times (100\Omega \parallel 600\Omega)) = 654mW$$

$$\text{Maximum } T_J = +85°C + (0.654W \times 80°C/W) = 137°C$$

All actual applications operate at a lower junction temperature than the +137°C computed above. Compute your actual output stage power to get an accurate estimate of maximum junction temperature, or use the results shown here as an absolute maximum.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier such as the OPA3693 requires careful attention to PCB layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, create a window around the signal I/O pins in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequency, should also be used on the supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components preserve the high-frequency performance of the OPA3693. Use resistors that have low reactance at high frequencies. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the series output resistor, if any, as close as possible to the output pin. Because the inverting input node is internal for the OPA3693, it is more robust to layout issues than amplifiers with similar speed but external feedback and gain

resistors. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Good axial metal film or surface-mount resistors have approximately 0.2pF in shunt with the resistor. For resistor values > 2.0kΩ, this parasitic capacitance can add a pole and/or zero below 400MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load driving considerations.

d) Connections to other wideband devices on the PCB may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *Recommended R_S vs Capacitive Load* (Figure 15). Low parasitic capacitive loads (< 4pF) may not need an R_S since the OPA3693 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment improves distortion, as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA3693 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as illustrated in the plot of Figure 15. This configuration does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part such as the OPA3693 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA3693 directly onto the board.

INPUT AND ESD PROTECTION

The OPA3693 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 59.

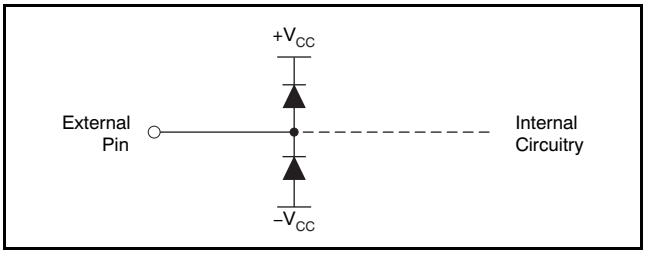


Figure 59. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA3693), current limiting series resistors may be added on the noninverting input. Keep this resistor value as low as possible since high values degrade both noise performance and frequency response. The inverting input already has a 300Ω resistor from the external pin to the internal summing junction for the op amp. This resistor provides considerable protection for that node.

Revision History

Changes from Original (December 2006) to Revision A	Page
• Changed storage temperature range rating in *Absolute Maximum Ratings* table from –40°C to +125°C to –65°C to +125°C	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA3693IDBQ	ACTIVE	SSOP	DBQ	16	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OP3693	Samples
OPA3693IDBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		OP3693	Samples
OPA3693IDBQRG4	ACTIVE	SSOP	DBQ	16	2500	TBD	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

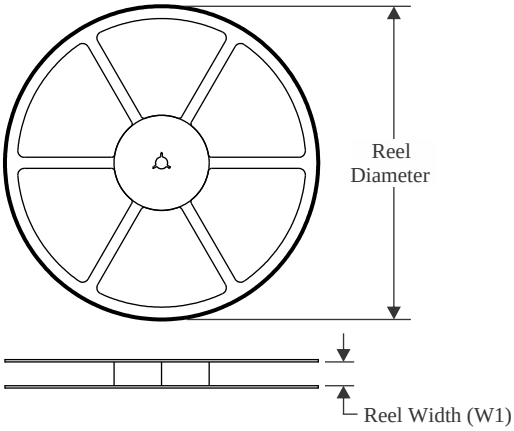
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

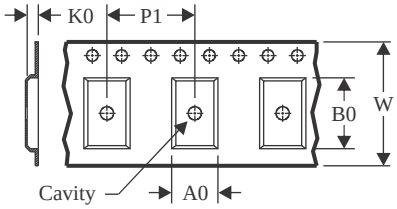
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

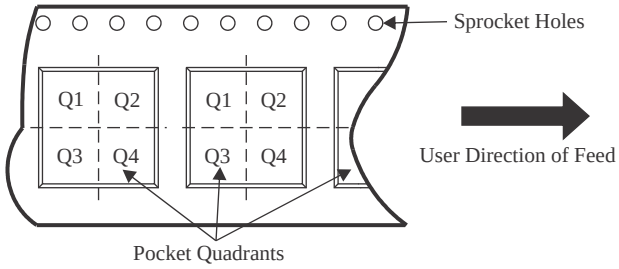


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

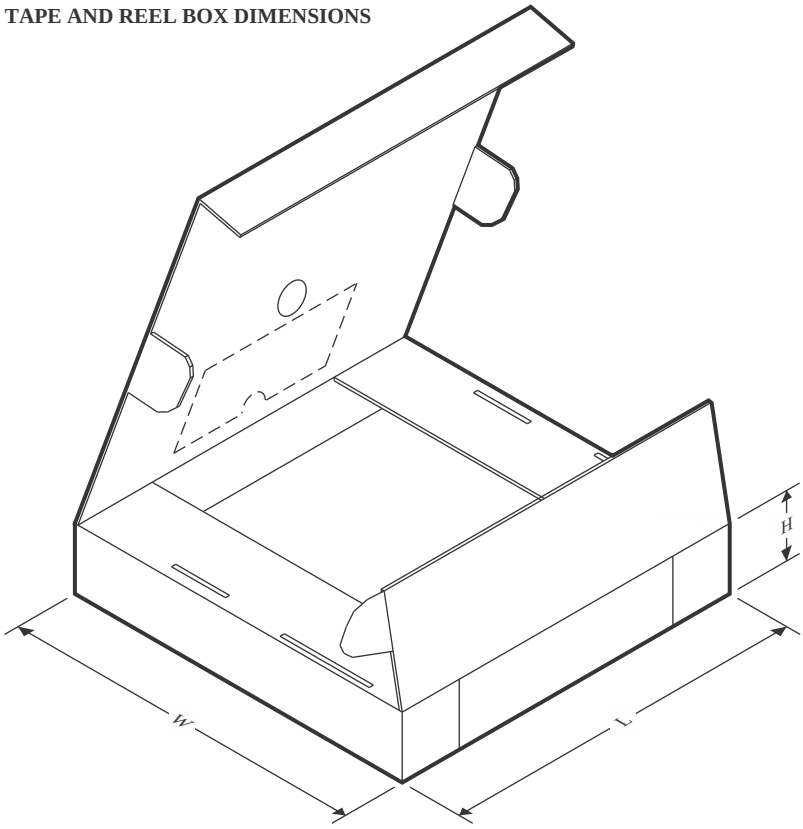
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA3693IDBQR	SSOP	DBQ	16	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

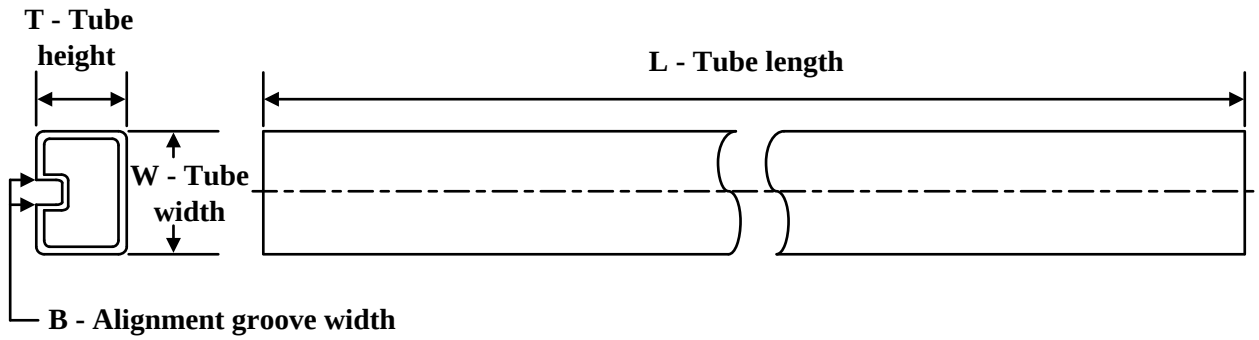
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

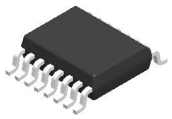
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA3693IDBQR	SSOP	DBQ	16	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA3693IDBQ	DBQ	SSOP	16	75	506.6	8	3940	4.32

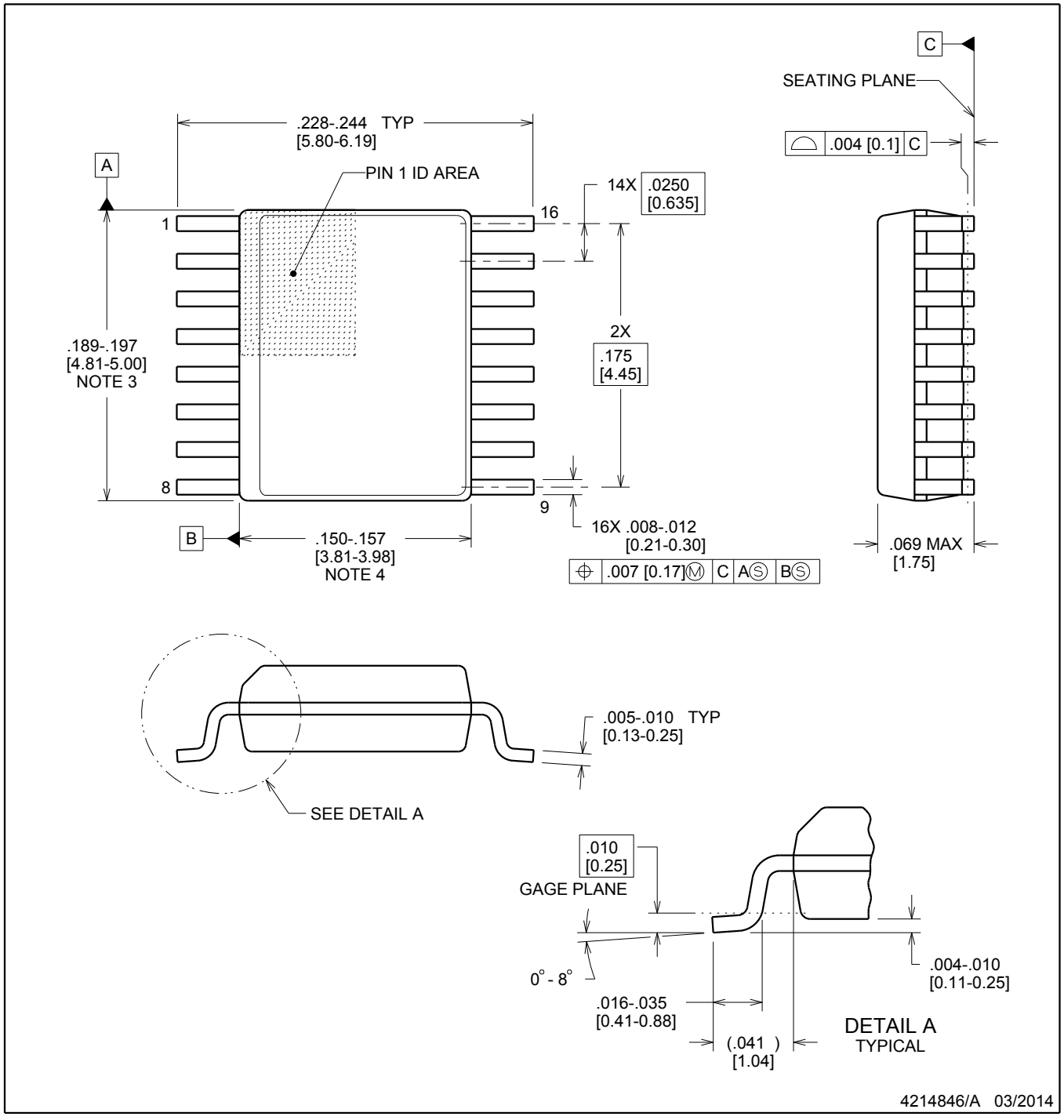


PACKAGE OUTLINE

DBQ0016A

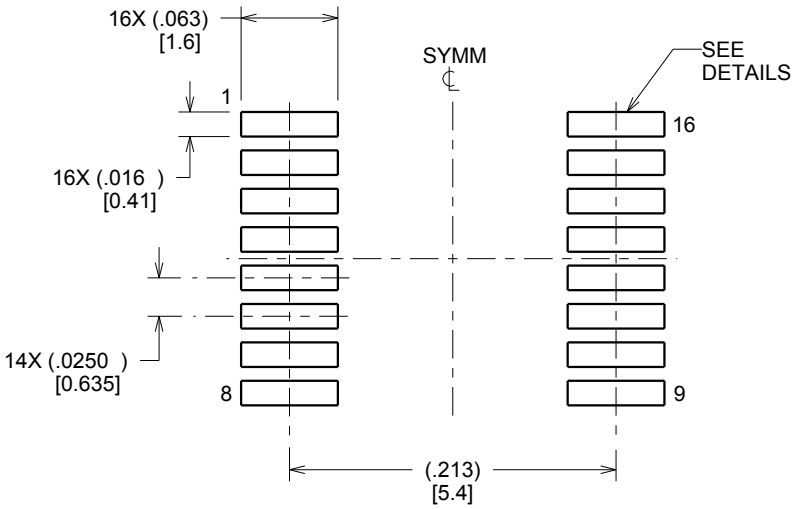
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

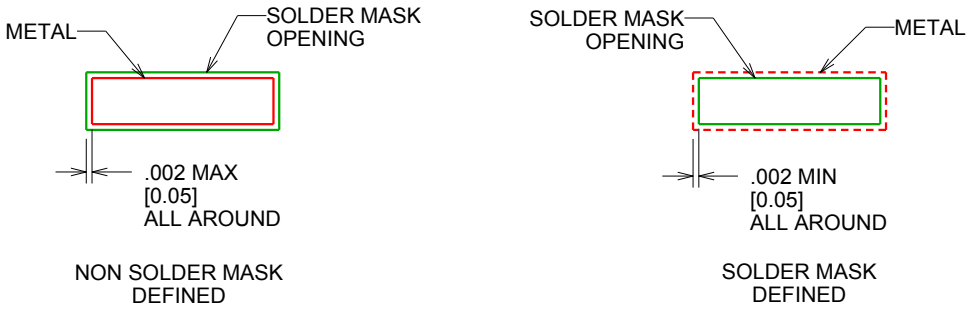


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

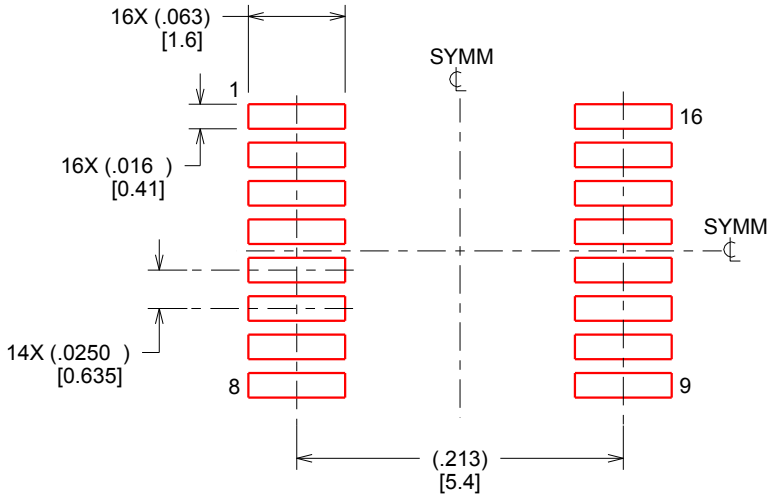
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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