Triple, Low-Power, High-Speed, Fixed-Gain Operational Amplifier

FEATURES

- **HIGH BANDWIDTH: 80MHz (G = +2)**
- **LOW SUPPLY CURRENT: 3.9mA/ch (V_S = +5V)**
- **FLEXIBLE SUPPLY RANGE:**
  ±1.5V to ±5.5V Dual Supply
  +3V to +11V Single Supply
- **INPUT RANGE INCLUDES GROUND ON SINGLE SUPPLY**
- **4.9V_{PP} OUTPUT SWING ON +5V SUPPLY**
- **HIGH SLEW RATE: 350V/µs**
- **LOW INPUT VOLTAGE NOISE: 9.3nV/√Hz**

APPLICATIONS

- **SINGLE-SUPPLY VIDEO LINE DRIVERS**
- **CCD IMAGING CHANNELS**
- **LOW-POWER ULTRASOUND**
- **PORTABLE CONSUMER ELECTRONICS**

DESCRIPTION

The OPA3832 is a triple, low-power, high-speed, fixed-gain amplifier designed to operate on a single +3V to +11V supply. Operation on ±1.5V to ±5.5V supplies is also supported. The input range extends below ground and to within 1.7V of the positive supply.

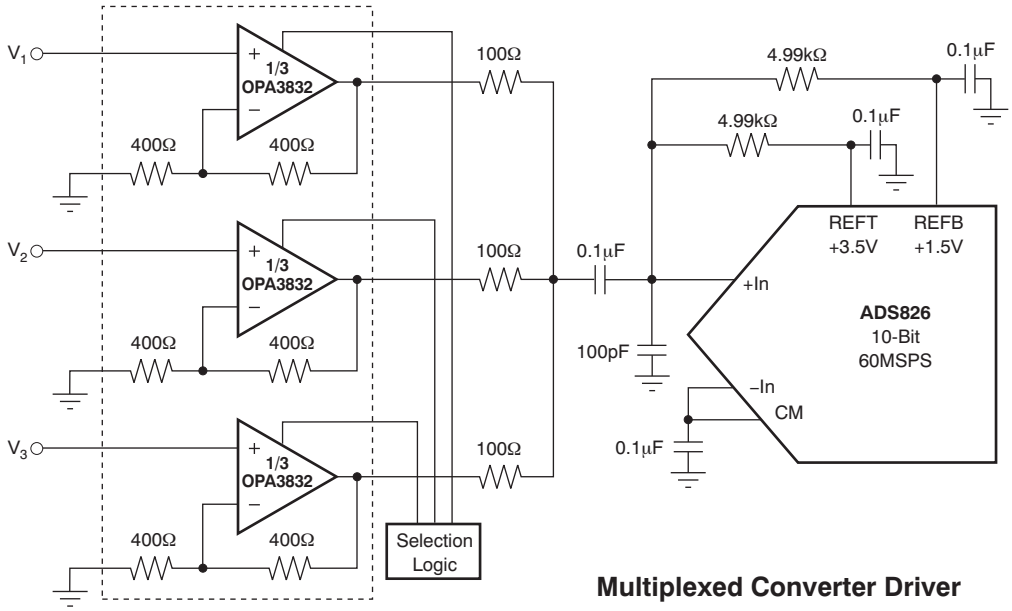
Using complementary common-emitter outputs provides an output swing to within 30mV of ground and 60mV of the positive supply. The high output drive current and low differential gain and phase errors also make it ideal for single-supply consumer video products.

Low distortion operation is ensured by high bandwidth (80MHz) and slew rate (350V/µs), making the OPA3832 an ideal input buffer stage to 3V and 5V CMOS converters. Unlike earlier low-power, single-supply amplifiers, distortion performance improves as the signal swing is decreased. A low 9.3nV/√Hz input voltage noise supports wide dynamic range operation.

The OPA3832 is available in an industry-standard SO-14 package or a small TSSOP-14 package.

RELATED PRODUCTS

DESCRIPTION	SINGLES	DUALS	TRIPLES	QUADS
Rail-to-Rail Output	OPA830	OPA2830	—	OPA4830
Rail-to-Rail Fixed-Gain	OPA832	OPA2832	—	—
General-Purpose (1800V/µs slew rate)	OPA690	OPA2690	OPA3690	—
Low-Noise, High dc Precision	OPA820	OPA2822	—	OPA4820



Multiplexed Converter Driver

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA3832	SO-14	D	–40°C to +85°C	OPA3832	OPA3832ID	Rails, 50
					OPA3832IDR	Tape and Reel, 2500
OPA3832	TSSOP-14	PW	–40°C to +85°C	OPA3832	OPA3832IPW	Rails, 90
					OPA3832IPWR	Tape and Reel, 2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

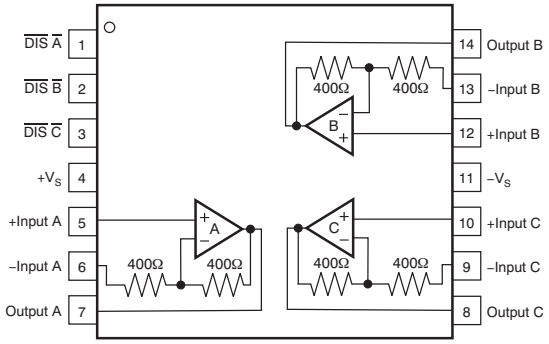
ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	$12V_{DC}$
Internal Power Dissipation	See Thermal Characteristics
Differential Input Voltage(2)	±1.2V
Input Voltage Range	–0.5V to $\pm V_S$ + 0.3V
Storage Voltage Range: D, PW	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Maximum Junction Temperature (T_J)	+150°C
Maximum Junction Temperature: Continuous Operation, Long Term Reliability	+140°C
ESD Rating:	
Human Body Model (HBM)	2000V
Charge Device Model (CDM)	1000V
Machine Model (MM)	200V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Noninverting input to internal inverting mode.

PIN ASSIGNMENT

D, PW PACKAGES
SO-14, TSSOP-14
(TOP VIEW)



ELECTRICAL CHARACTERISTICS: V_S = ±5V

Boldface limits are tested at **+25°C**.

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to GND, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3832ID, IPW				UNITS	MIN/ MAX	TEST LEVEL(3)
		+25°C	+25°C(1)	0°C to +70°C(2)	–40°C to +85°C(2)			
AC PERFORMANCE								
Small-Signal Bandwidth	G = +1, V_O ≤ 0.5V_{PP}	250				MHz	typ	C
	G = +2, V_O ≤ 0.5V_{PP}	80	55	54	54	MHz	min	B
	G = –1, V_O ≤ 0.5V_{PP}	110	57	56	55	MHz	min	B
Peaking at a Gain of +1	V_O ≤ 0.5V_{PP}	6				dB	typ	C
Slew Rate	G = +2, 2V Step	325	220	210	200	V/µs	min	B
Rise Time	0.5V Step	5.0	5.8	6.0	6.0	ns	max	B
Fall Time	0.5V Step	5.0	5.8	6.0	6.0	ns	max	B
Settling Time to 0.1%	G = +2, 1V Step	45	63	65	66	ns	max	B
Harmonic Distortion	V_O = 2V_{PP}, 5MHz							
2nd-Harmonic	R_L = 150Ω	–57	–54	–52	–50	dBc	max	B
	R_L = 500Ω	–65	–62	–61	–60	dBc	max	B
3rd-Harmonic	R_L = 150Ω	–60	–50	–49	–48	dBc	max	B
	R_L = 500Ω	–75	–64	–60	–57	dBc	max	B
Input Voltage Noise	f > 1MHz	9.2				nV/√Hz	typ	C
Input Current Noise	f > 1MHz	2.2				pA/√Hz	typ	C
NTSC Differential Gain	R_L = 150Ω	0.10				%	typ	C
NTSC Differential Phase	R_L = 150Ω	0.16					typ	C
All Hostile Crosstalk, Input Referred	2 Channels Driven at 5MHz, 1V_{PP} 3rd Channel Measured	–55				dBc	typ	C
DC PERFORMANCE(4)								
Gain Error	G = +2	±0.3	**±1.5**	±1.6	±1.7	%	min	A
	G = –1	±0.2	±1.5	±1.6	±1.7	%	max	B
Internal R_F and R_G								
Maximum		400	**455**	460	462	Ω	max	B
Minimum		400	**345**	340	338	Ω	max	B
Average Drift				±0.1	±0.1	%/°C	max	B
Input Offset Voltage		±1.4	**±8.0**	±9.3	±9.7	mV	max	A
Average Offset Voltage Drift		—		±27	±27	µV/°C	max	B
Input Bias Current		+5.5	**+10**	+12	+13	µA	max	A
Input Bias Current Drift		—		±45	±45	nA/°C	max	B
Input Offset Current		±0.1	**±1.5**	±2	±2.5	µA	max	A
Input Offset Current Drift		—		±10	±10	nA/°C	max	B
INPUT								
Negative Input Voltage Range		–5.4	–5.2	–5.0	–4.9	V	max	B
Positive Input Voltage Range		3.2	3.1	3.0	2.9	V	min	B
Input Impedance								
Differential Mode		10 || 2.1				kΩ || pF	typ	C
Common-Mode		400 || 1.2				kΩ || pF	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +13°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

Boldface limits are tested at **+25°C**.

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to GND, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3832ID, IPW				UNITS	MIN/ MAX	TEST LEVEL(3)
		+25°C	+25°C(1)	0°C to +70°C(2)	–40°C to +85°C(2)			
OUTPUT								
Output Voltage Swing	R_L = 1kΩ to GND	±4.9	**±4.8**	±4.75	±4.75	V	max	A
	R_L = 150Ω to GND	±4.6	**±4.5**	±4.45	±4.4	V	max	A
Current Output, Sinking and Sourcing		±82	**±63**	±58	±53	mA	min	A
Short-Circuit Current	Output Shorted to Either Supply	120				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.2				Ω	typ	C
DISABLE (Disabled LOW)								
Power Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0, All Channels	0.95	**2.5**	2.6	2.7	mA	max	A
DIsable Time	V_{IN} = 1V_{DC}	40				µs	typ	C
Enable Time	V_{IN} = 1V_{DC}	20				ns	typ	C
Off Isolation	G = +2V/V, 5MHz	–75				dB	typ	C
Output Capacitance in Disable						pF	typ	C
Turn-On Glitch	G = +2V/V, R_L = 150Ω, V_{IN} = 0V	8				mV	typ	C
Turn-Off Glitch	G = +2V/V, R_L = 150Ω, V_{IN} = 0V	2				mV	typ	C
Enable Voltage			**4.5**	4.5	4.5	V	min	A
Disable Voltage			**3.0**	3.0	3.0	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0V, Each Channel	125	**300**	350	400	µA	max	A
POWER SUPPLY								
Minimum Operating Voltage		±1.4				V	min	B
Maximum Operating Voltage		—	**±5.5**	±5.5	±5.5	V	max	A
Maximum Quiescent Current	All Channels, V_S = ±5V	12.75	**14.4**	16.1	17.9	mA	max	A
Minimum Quiescent Current	All Channels, V_S = ±5V	12.75	**12**	10.8	9.3	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input-Referred	66	**61**	60	59	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID, IPW		–40 to +85				°C	typ	C
Thermal Resistance								
D SO-14		85				°C/W	typ	C
PW TSSOP-14		100				°C/W	typ	C

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C**.

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3832ID, IPW				UNITS	MIN/ MAX	TEST LEVEL(3)
		+25°C	+25°C(1)	0°C to +70°C(2)	–40°C to +85°C(2)			
AC PERFORMANCE								
Small-Signal Bandwidth	G = +1, $V_O \le 0.5V_{PP}$	210				MHz	typ	C
	G = +2, $V_O \le 0.5V_{PP}$	80	56	55	55	MHz	min	B
	G = –1, $V_O \le 0.5V_{PP}$	105	60	58	58	MHz	min	B
Peaking at a Gain of +1	$V_O \le 0.5V_{PP}$	7				dB	typ	C
Slew Rate	G = +2, 2V Step	350	230	220	220	V/µs	min	B
Rise Time	0.5V Step	5.2	5.8	5.8	5.9	ns	max	B
Fall Time	0.5V Step	5.2	5.8	5.8	5.9	ns	max	B
Settling Time to 0.1%	G = +2, 1V Step	46	64	66	67	ns	max	B
Harmonic Distortion	$V_O = 2V_{PP}$, 5MHz							
2nd-Harmonic	R_L = 150Ω	–54	–51	–50	–49	dBc	max	B
	R_L = 500Ω	–60	–57	–55	–54	dBc	max	B
3rd-Harmonic	R_L = 150Ω	–57	–50	–49	–47	dBc	max	B
	R_L = 500Ω	–79	–65	–62	–58	dBc	max	B
Input Voltage Noise	f > 1MHz	9.3				nV/√Hz	typ	C
Input Current Noise	f > 1MHz	2.3				pA/√Hz	typ	C
NTSC Differential Gain	R_L = 150Ω	0.11				%	typ	C
NTSC Differential Phase	R_L = 150Ω	0.14					typ	C
DC PERFORMANCE(4)								
Gain Error	G = +2	±0.3	**±1.5**	±1.6	±1.7	%	min	A
	G = –1	±0.2	±1.5	±1.6	±1.7	%	max	B
Internal R_F and R_G, Maximum		400	**455**	460	462	Ω	max	A
Minimum		400	**345**	340	338	Ω	max	A
Average Drift				±0.1	±0.1	%/°C	max	B
Input Offset Voltage		±1.5	**±6.5**	±7.5	±8.0	mV	max	A
Average Offset Voltage Drift		—		±25	±25	µV/°C	max	B
Input Bias Current	V_{CM} = 2.0V	+5.5	**+10**	+12	+13	µA	max	A
Input Bias Current Drift		—		±45	±45	nA/°C	max	B
Input Offset Current	V_{CM} = 2.0V	±0.1	**±1.5**	±2	±2.5	µA	max	A
Input Offset Current Drift		—		±10	±10	nA/°C	max	B
INPUT								
Least Positive Input Voltage		–0.5	–0.2	0	+0.1	V	max	B
Most Positive Input Voltage		3.3	3.2	3.1	3.0	V	min	B
Input Impedance, Differential Mode		10 || 2.1				kΩ || pF	typ	C
Common-Mode		400 || 1.2				kΩ || pF	typ	C
OUTPUT								
Least Positive Output Voltage	R_L = 1kΩ to 2.0V	0.03	**0.16**	0.18	0.20	V	max	A
	R_L = 150Ω to 2.0V	0.18	**0.3**	0.35	0.40	V	max	A
Most Positive Output Voltage	R_L = 1kΩ to 2.0V	4.94	**4.8**	4.6	4.4	V	min	A
	R_L = 150Ω to 2.0V	4.86	**4.6**	4.5	4.4	V	min	A
Current Output, Sinking and Sourcing		±75	**±58**	±53	±50	mA	min	A
Short-Circuit Output Current	Output Shorted to Either Supply	100				mA	typ	C
Closed-Loop Output Impedance	G = +2, f ≤ 100kHz	0.2				Ω	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +6°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node.

ELECTRICAL CHARACTERISTICS: V_S = +5V (continued)

Boldface limits are tested at **+25°C**.

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3832ID, IPW				UNITS	MIN/ MAX	TEST LEVEL(3)
		+25°C	+25°C(1)	0°C to +70°C(2)	–40°C to +85°C(2)			
DISABLE (Disabled LOW)								
Power Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0, All Channels	0.7	**1.4**	1.5	1.5	mA	max	A
DIsable Time	V_{IN} = 1V_{DC}	40				µs	typ	C
Enable Time	V_{IN} = 1V_{DC}	20				ns	typ	C
Off Isolation	G = +2V/V, 5MHz	–75				dB	typ	C
Output Capacitance in Disable						pF	typ	C
Turn-On Glitch	G = +2V/V, R_L = 150Ω, V_{IN} = 0V	2				mV	typ	C
Turn-Off Glitch	G = +2V/V, R_L = 150Ω, V_{IN} = 0V	6				mV	typ	C
Enable Voltage			**4.5**	4.5	4.5	V	min	A
Disable Voltage			**3.0**	3.0	3.0	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0V, Each Channel	125	**300**	350	400	µA	max	A
POWER SUPPLY								
Minimum Operating Voltage		+2.8				V	typ	C
Maximum Operating Voltage		—	**+11**	+11	+11	V	max	A
Maximum Quiescent Current	All Channels, V_S = +5V	11.7	**12.6**	14.7	16.8	mA	max	A
Minimum Quiescent Current	All Channels, V_S = +5V	11.7	**11.1**	10.5	9	mA	min	A
Power-Supply Rejection Ratio (PSRR)	Input-Referred	66	**61**	60	59	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID, IPW		–40 to +85				°C	typ	C
Thermal Resistance								
D SO-14		85				°C/W	typ	C
PW TSSOP-14		100				°C/W	typ	C

ELECTRICAL CHARACTERISTICS: V_S = +3.3V

Boldface limits are tested at **+25°C**.

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 0.75V, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3832ID, IPW			UNITS	MIN/ MAX	TEST LEVEL(3)
		+25°C	+25°C(1)	0°C to +70°C(2)			
AC PERFORMANCE							
Small-Signal Bandwidth	G = +1, V_O ≤ 0.5V_{PP}	180			MHz	typ	C
	G = +2, V_O ≤ 0.5V_{PP}	90	59	57	MHz	min	B
	G = –1, V_O ≤ 0.5V_{PP}	100	63	61	MHz	min	B
Peaking at a Gain of +1	V_O ≤ 0.5V_{PP}	8			dB	typ	C
Slew Rate	1V Step	150	110	100	V/µs	min	B
Rise Time	0.5V Step	4.4	5.6	5.7	ns	max	B
Fall Time	0.5V Step	4.4	5.6	5.7	ns	max	B
Settling Time to 0.1%	1V Step	48	70	80	ns	max	B
Harmonic Distortion	5MHz						
2nd-Harmonic	R_L = 150Ω	–60	–54	–51	dBc	max	B
	R_L = 500Ω	–67	–63	–57	dBc	max	B
3rd-Harmonic	R_L = 150Ω	–66	–60	–55	dBc	max	B
	R_L = 500Ω	–80	–66	–62	dBc	max	B
Input Voltage Noise	f > 1MHz	9.4			nV/√Hz	typ	C
Input Current Noise	f > 1MHz	2.4			pA/√Hz	typ	C
DC PERFORMANCE(4)							
Gain Error	G = +2	±0.3	**±1.5**	±1.6	%	min	A
	G = –1	±0.2	±1.5	±1.6	%	max	B
Internal R_F and R_G							
Maximum		400	455	460	Ω	max	B
Minimum		400	345	340	Ω	max	B
Average Drift				±0.1	%/°C	max	B
Input Offset Voltage		±1.4	**±6.5**	±7.7	mV	max	A
Average Offset Voltage Drift		—		±27	µV/°C	max	B
Input Bias Current	V_{CM} = 0.75V	+5.5	**+10**	+12	µA	max	A
Input Bias Current Drift		—		±45	nA/°C	max	B
Input Offset Current	V_{CM} = 0.75V	±0.1	**±1.5**	±2	µA	max	A
Input Offset Current Drift		—		±10	nA/°C	max	B
INPUT							
Least Positive Input Voltage		–0.5	–0.3	–0.2	V	max	B
Most Positive Input Voltage		1.5	1.4	1.3	V	min	B
Input Impedance							
Differential Mode		10 || 2.1			kΩ || pF	typ	C
Common-Mode		400 || 1.2			kΩ || pF	typ	C
OUTPUT							
Least Positive Output Voltage	R_L = 1kΩ to 0.75V	0.03	0.16	0.18	V	max	B
	R_L = 150Ω to 0.75V	0.1	0.3	0.35	V	max	B
Most Positive Output Voltage	R_L = 1kΩ to 0.75V	3	2.8	2.6	V	min	B
	R_L = 150Ω to 0.75V	3	2.8	2.6	V	min	B
Current Output, Sinking and Sourcing		±35	**±25**	±20	mA	min	A
Short-Circuit Output Current	Output Shorted to Either Supply	80			mA	typ	C
Closed-Loop Output Impedance	See Figure 2, f < 100kHz	0.2			Ω	typ	C

(1) Junction temperature = ambient for +25°C specifications.
(2) Junction temperature = ambient at low temperature limits; junction temperature = ambient +4°C at high temperature limit for over temperature specifications.
(3) Test levels: (A) 100% tested at +25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(4) Current is considered positive out of node.

ELECTRICAL CHARACTERISTICS: V_S = +3.3V (continued)

Boldface limits are tested at **+25°C**.

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 0.75V, unless otherwise noted.

PARAMETER	CONDITIONS	OPA3832ID, IPW			UNITS	MIN/ MAX	TEST LEVEL(3)
		+25°C	+25°C(1)	0°C to +70°C(2)			
DISABLE (Disabled LOW)							
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0, All Channels	0.4	0.8	0.85	mA	max	A
DIsable Time	V_{IN} = 1V_{DC}	40			µs	typ	C
Enable Time	V_{IN} = 1V_{DC}	20			ns	typ	C
Off Isolation	G = +2V/V, 5MHz	–75			dB	typ	C
Output Capacitance in Disable					pF	typ	C
Turn-On Glitch	G = +2V/V, R_L = 150Ω, V_{IN} = 0V	2			mV	typ	C
Turn-Off Glitch	G = +2V/V, R_L = 150Ω, V_{IN} = 0V	6			mV	typ	C
Enable Voltage			**2.8**	2.8	V	min	A
Disable Voltage			**1.3**	1.3	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0V, Each Channel	73	**130**	140	µA	max	A
POWER SUPPLY							
Minimum Operating Voltage		+2.8			V	typ	C
Maximum Operating Voltage		—	**+11**	+11	V	max	A
Maximum Quiescent Current	All Channels, V_S = +3.3V	11.4	**12.2**	14.5	mA	max	A
Minimum Quiescent Current	All Channels, V_S = +3.3V	11.4	**10.2**	9.5	mA	min	A
Power-Supply Rejection Ratio (PSRR)	Input-Referred	60			dB	typ	C
THERMAL CHARACTERISTICS							
Specification: ID, IPW		–40 to +85			°C	typ	C
Thermal Resistance							
D SO-14		85			°C/W	typ	C
PW TSSOP-14		100			°C/W	typ	C

TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to GND, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

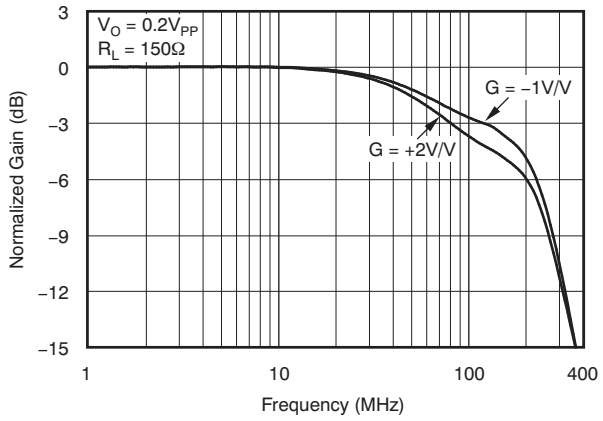


Figure 1.

LARGE-SIGNAL FREQUENCY RESPONSE

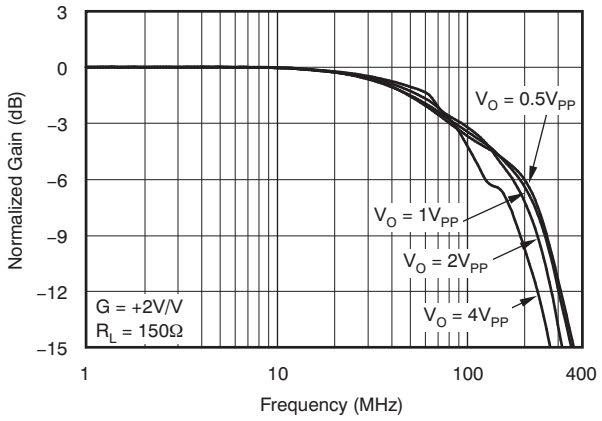


Figure 2.

NONINVERTING PULSE RESPONSE

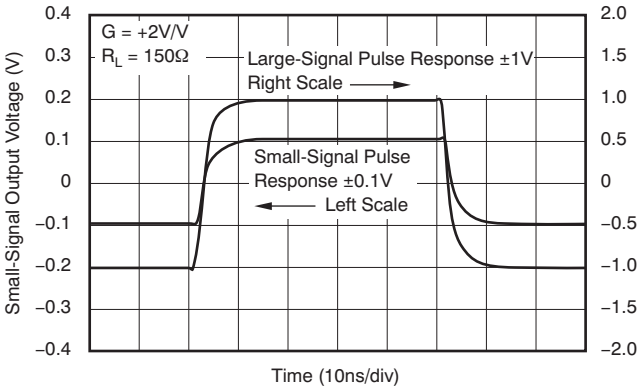


Figure 3.

INVERTING PULSE RESPONSE

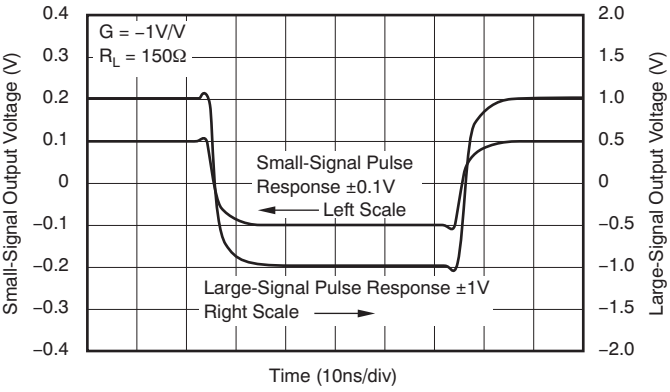


Figure 4.

REQUIRED R_S vs CAPACITIVE LOAD

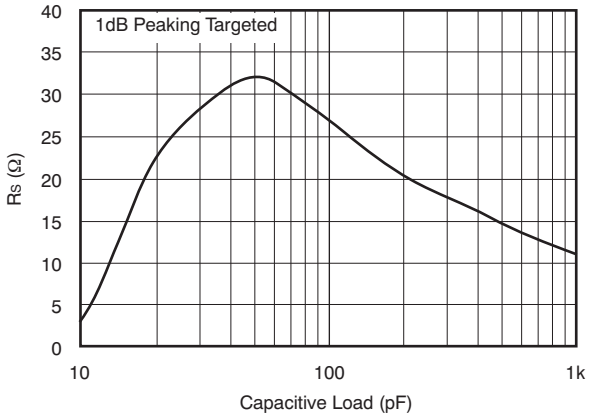


Figure 5.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

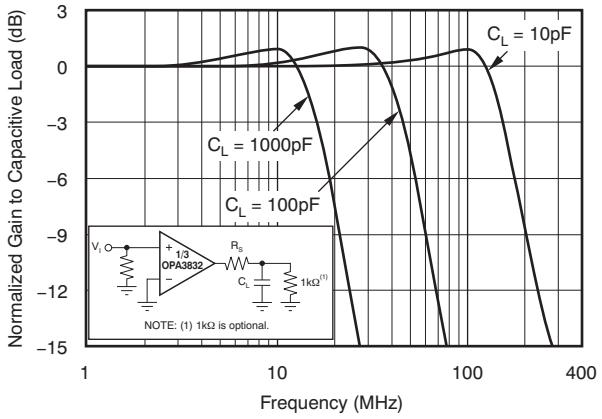


Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to GND, unless otherwise noted.

HARMONIC DISTORTION vs LOAD RESISTANCE

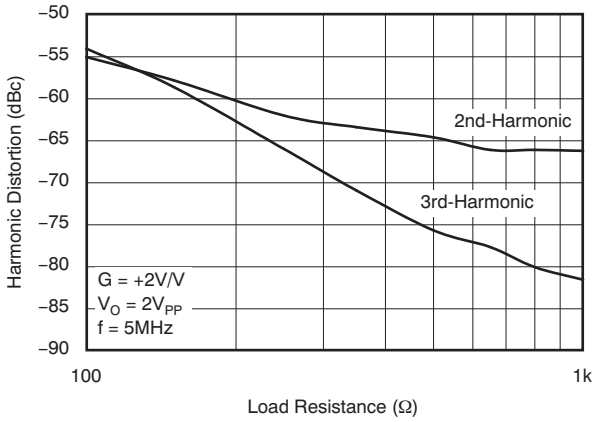


Figure 7.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

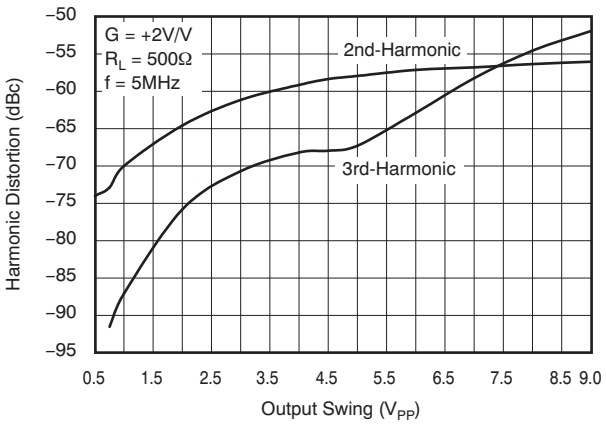


Figure 8.

HARMONIC DISTORTION vs FREQUENCY

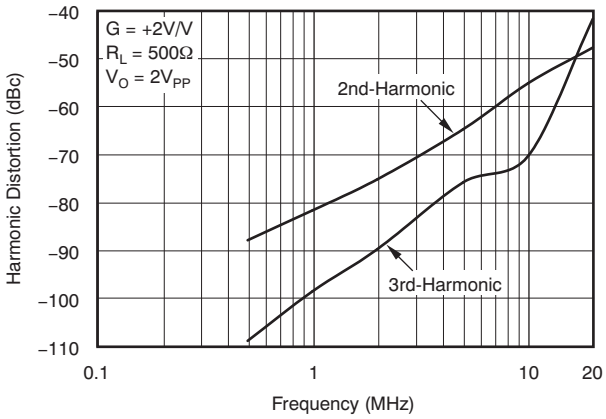


Figure 9.

2-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

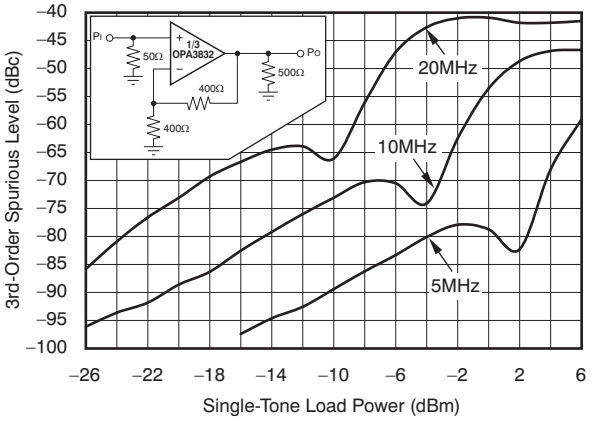


Figure 10.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

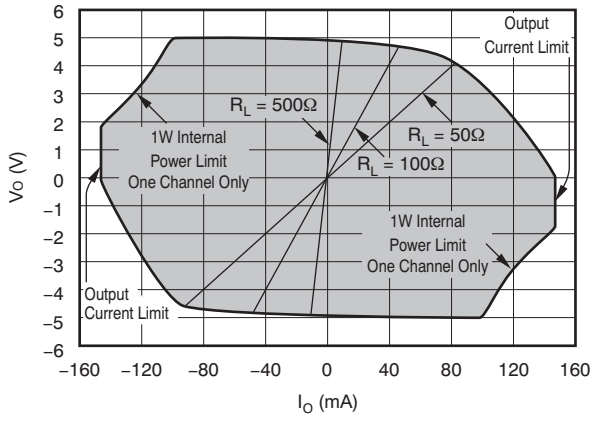


Figure 11.

OUTPUT SWING vs LOAD RESISTANCE

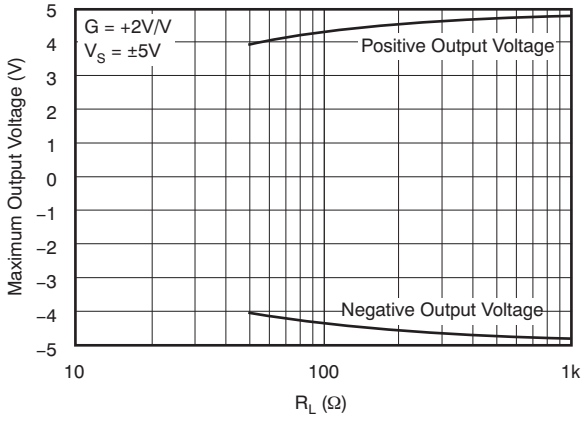


Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to GND, unless otherwise noted.

COMPOSITE VIDEO dG/dP

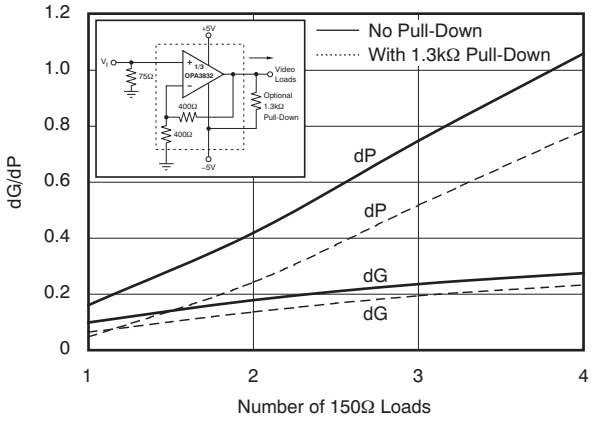


Figure 13.

CHANNEL-TO-CHANNEL CROSSTALK REJECTION
ALL HOSTILE CROSSTALK REJECTION

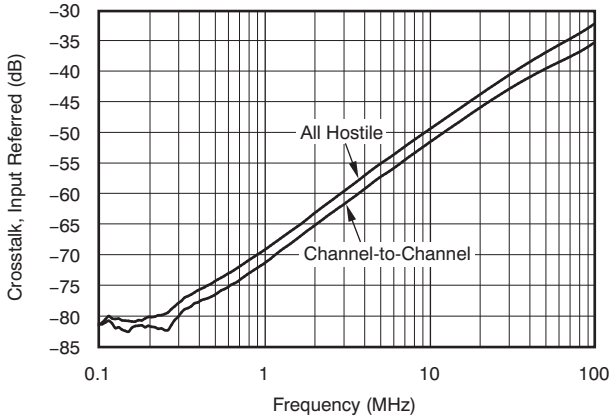


Figure 14.

TYPICAL CHARACTERISTICS: V_S = +5V

At T_A = +25°C, Differential Gain = +2V/V, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

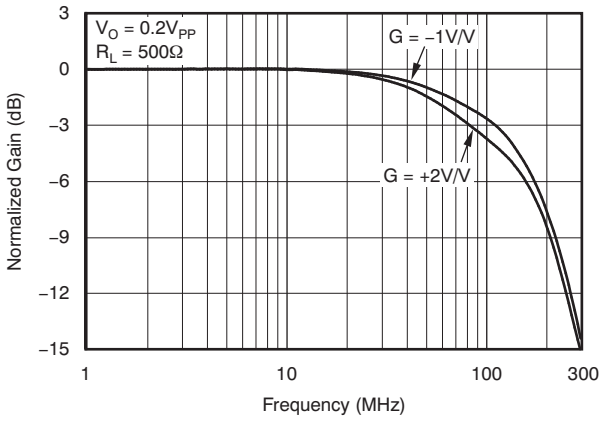


Figure 15.

LARGE-SIGNAL FREQUENCY RESPONSE

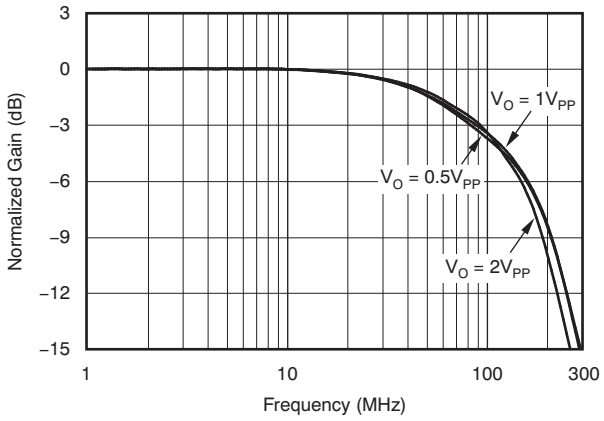


Figure 16.

NONINVERTING PULSE RESPONSE

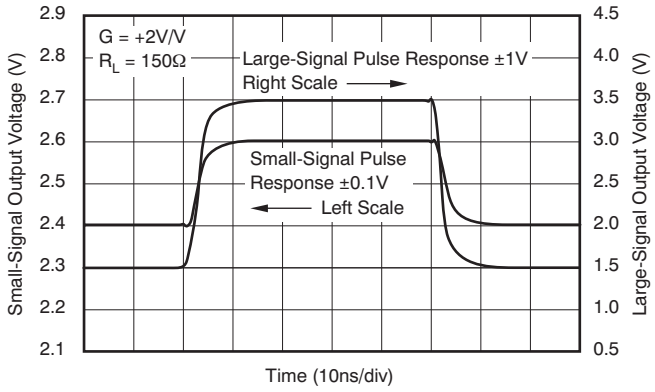


Figure 17.

INVERTING PULSE RESPONSE

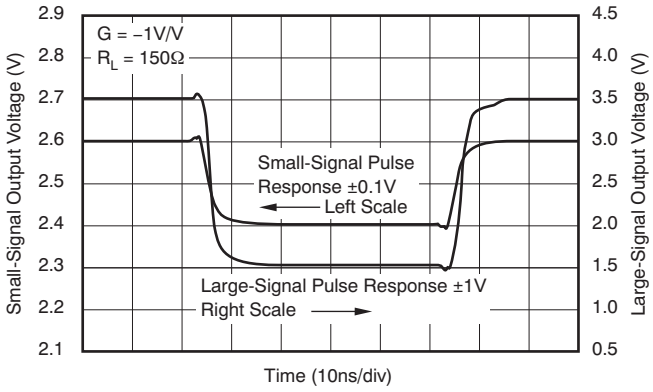


Figure 18.

COMPOSITE VIDEO dG/dP

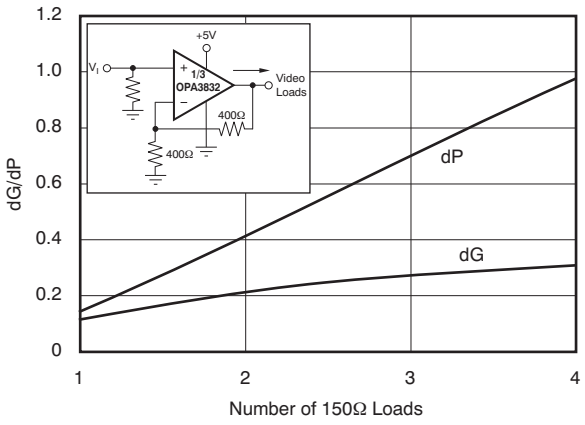
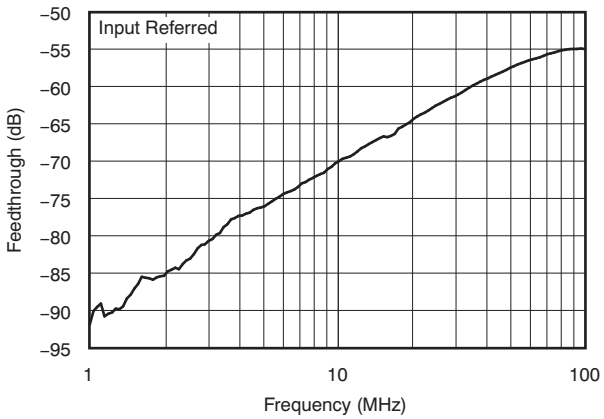


Figure 19.

DISABLE FEEDTHROUGH vs FREQUENCY



TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, Differential Gain = +2V/V, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted.

HARMONIC DISTORTION vs LOAD RESISTANCE

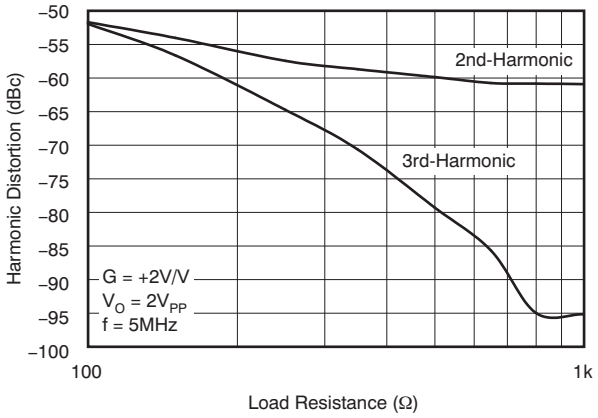


Figure 20.

5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

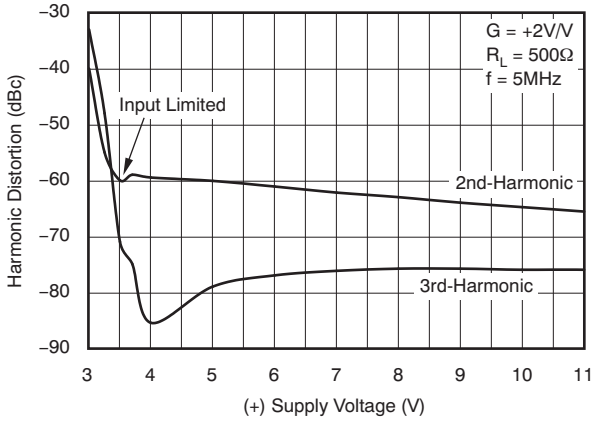


Figure 21.

G = +2V/V, HARMONIC DISTORTION vs FREQUENCY

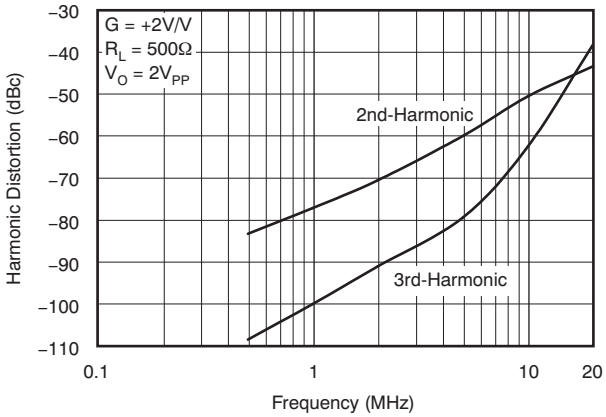


Figure 22.

G = –1V/V, HARMONIC DISTORTION vs FREQUENCY

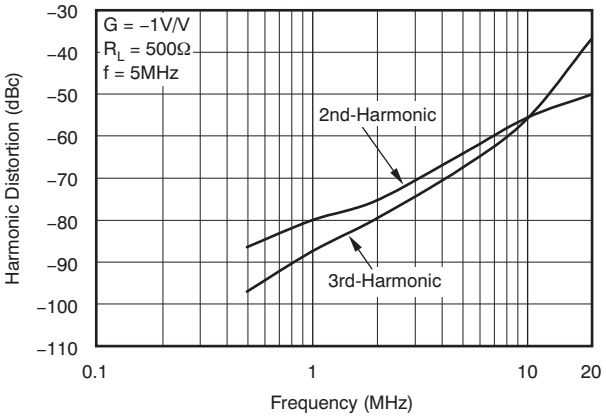


Figure 23.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

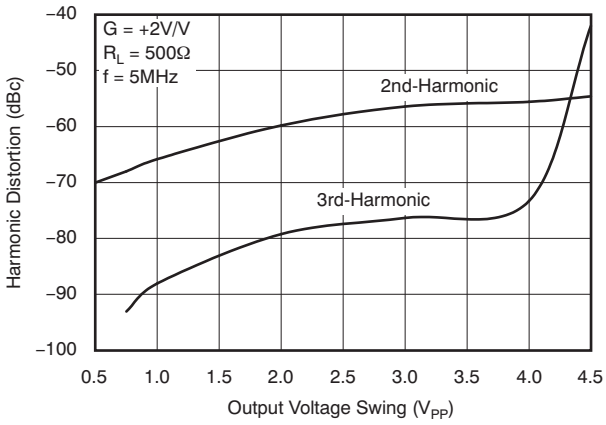


Figure 24.

2-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

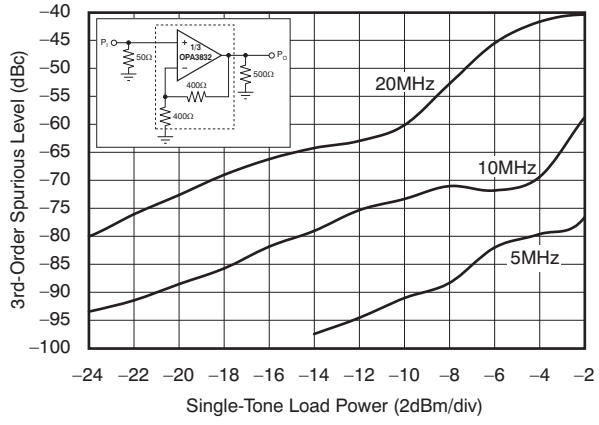


Figure 25.

TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, Differential Gain = +2V/V, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted.

INPUT VOLTAGE AND CURRENT NOISE

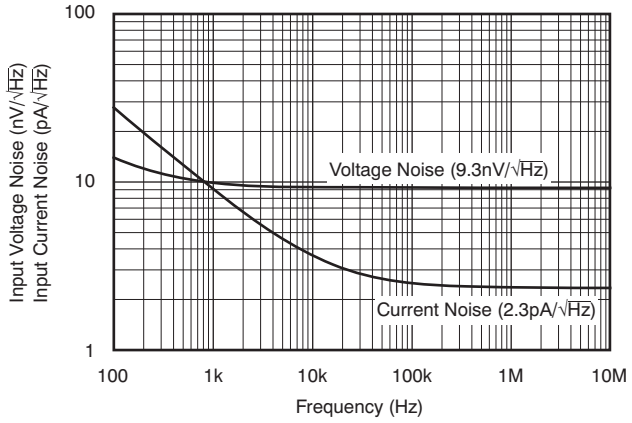


Figure 26.

POWER-SUPPLY REJECTION RATIO AND COMMON-MODE REJECTION RATIO VS FREQUENCY

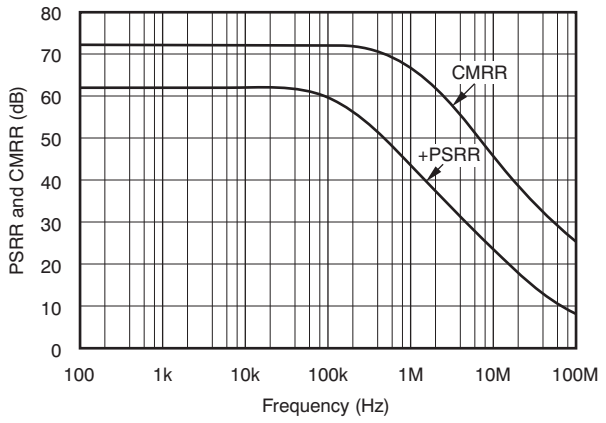


Figure 27.

OUTPUT SWING vs LOAD RESISTANCE

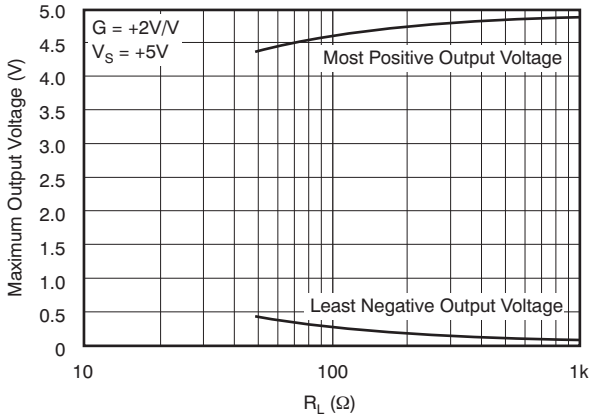


Figure 28.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

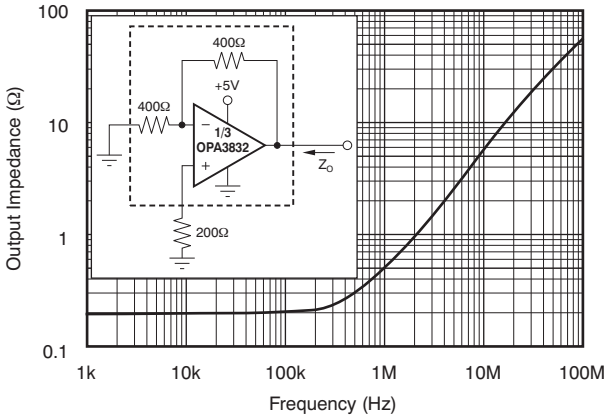


Figure 29.

VOLTAGE RANGES vs TEMPERATURE

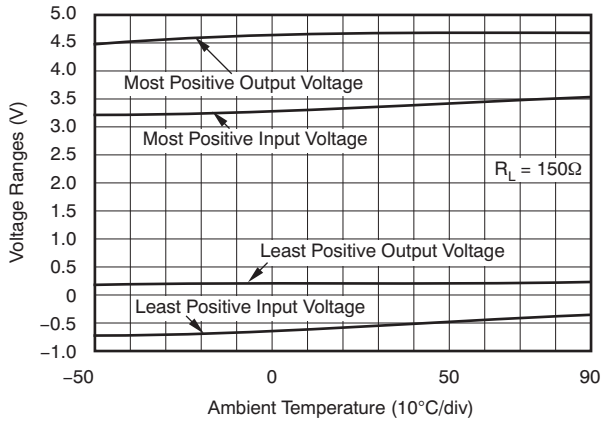


Figure 30.

TYPICAL DC DRIFT OVER TEMPERATURE

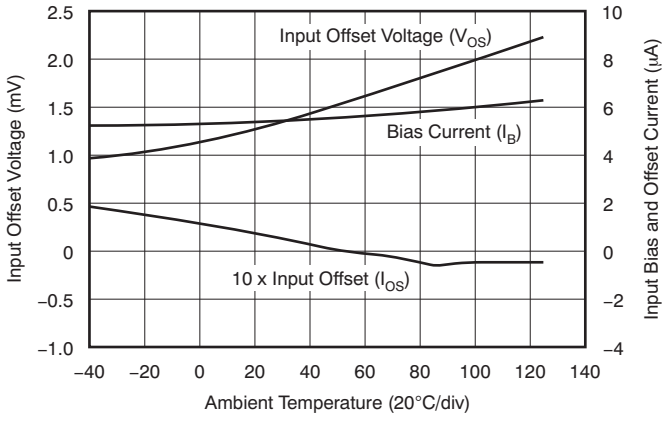


Figure 31.

TYPICAL CHARACTERISTICS: V_S = +5V (continued)

At T_A = +25°C, Differential Gain = +2V/V, and R_L = 150Ω to V_{CM} = 2V, unless otherwise noted.

SUPPLY AND OUTPUT CURRENT vs TEMPERATURE

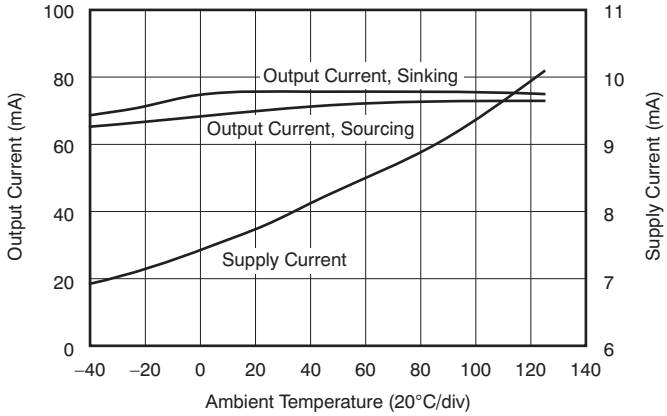


Figure 32.

LARGE-SIGNAL DISABLE/ENABLE RESPONSE

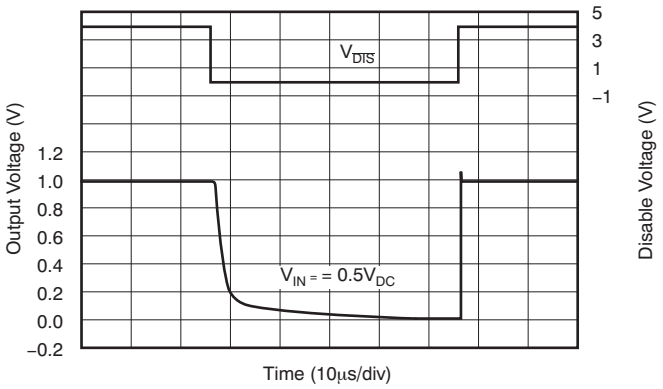


Figure 33.

DISABLE/ENABLE GLITCH

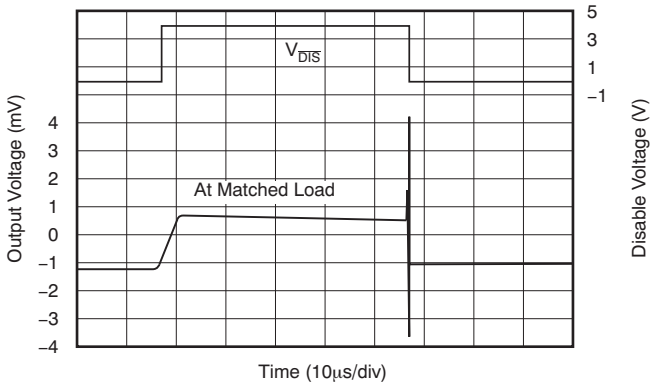


Figure 34.

TYPICAL CHARACTERISTICS: V_S = +3.3V

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 0.75V, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

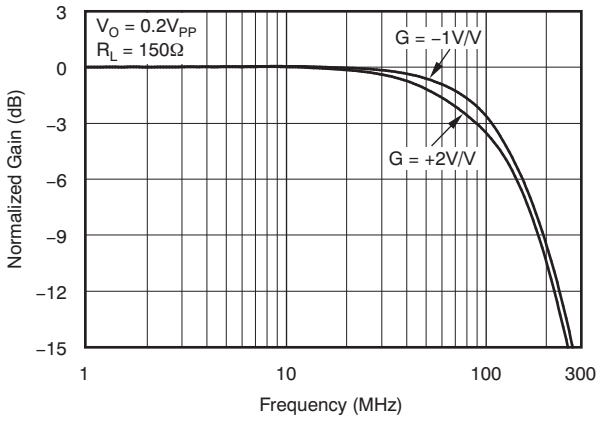


Figure 35.

LARGE-SIGNAL FREQUENCY RESPONSE

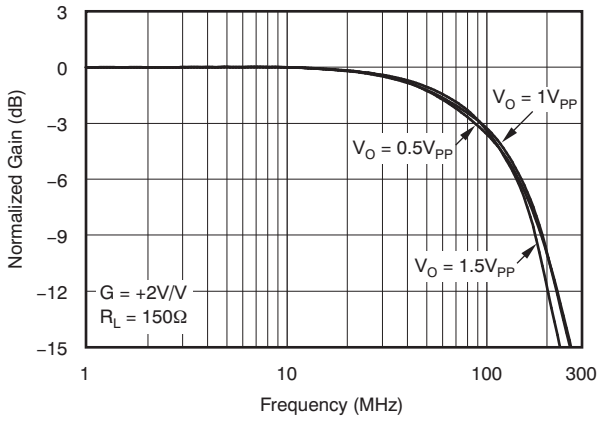


Figure 36.

NONINVERTING PULSE RESPONSE

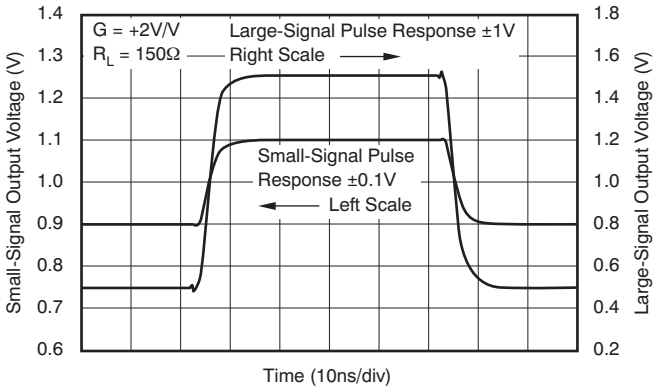


Figure 37.

INVERTING PULSE RESPONSE

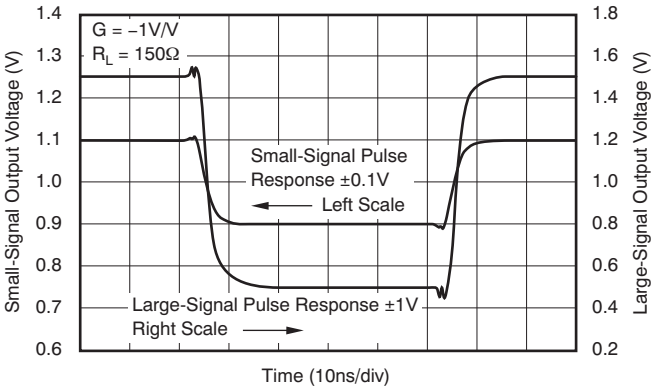


Figure 38.

REQUIRED R_S vs CAPACITIVE LOAD

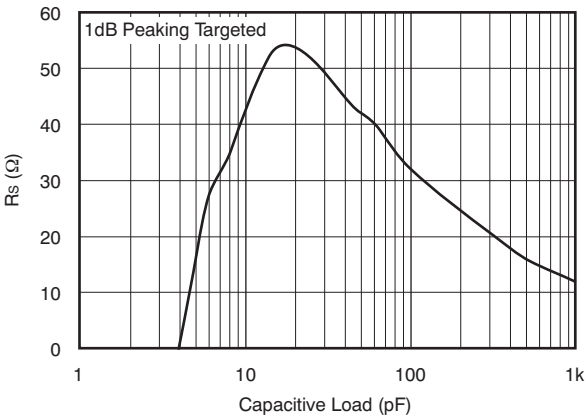


Figure 39.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

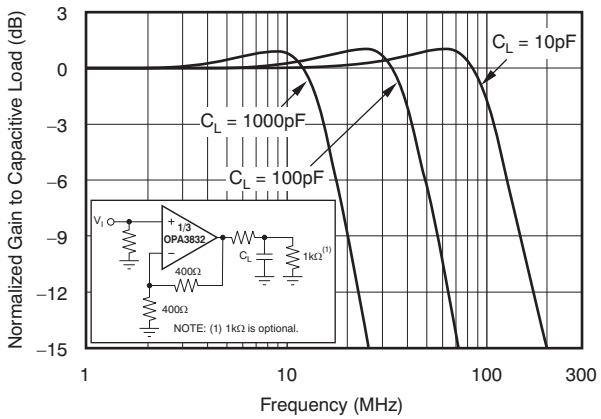


Figure 40.

TYPICAL CHARACTERISTICS: V_S = +3.3V (continued)

At T_A = +25°C, G = +2V/V, and R_L = 150Ω to V_{CM} = 0.75V, unless otherwise noted.

HARMONIC DISTORTION vs LOAD RESISTANCE

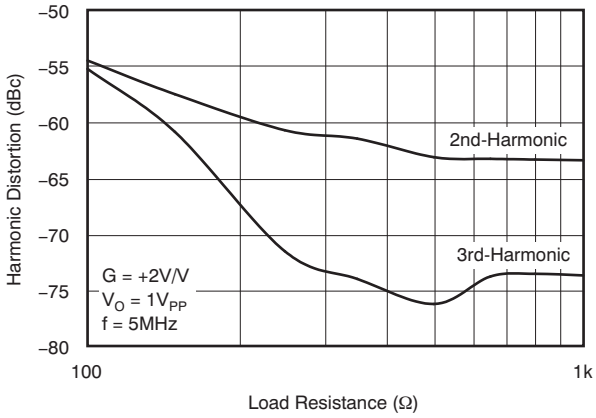


Figure 41.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

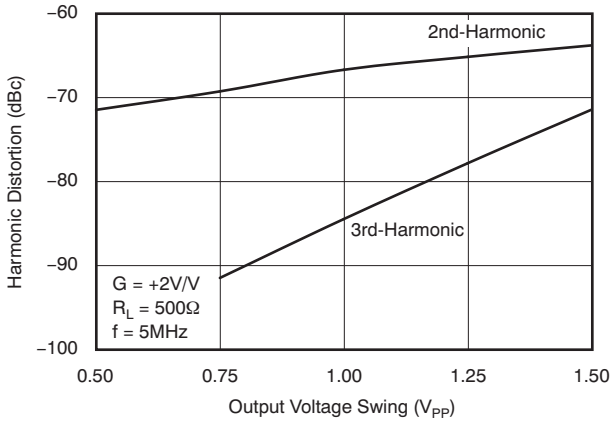


Figure 42.

HARMONIC DISTORTION vs FREQUENCY

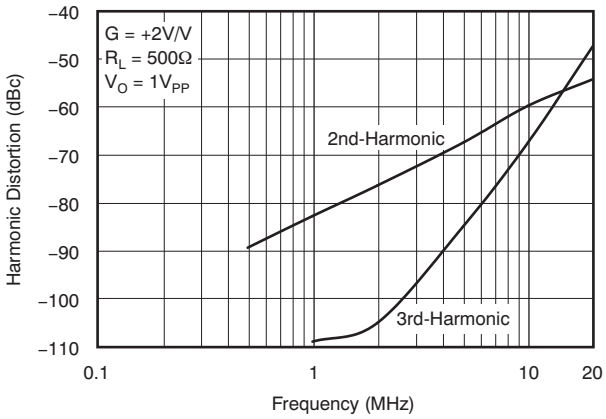


Figure 43.

TWO-TONE, 3RD-ORDER INTERMODULATION SPURIOUS

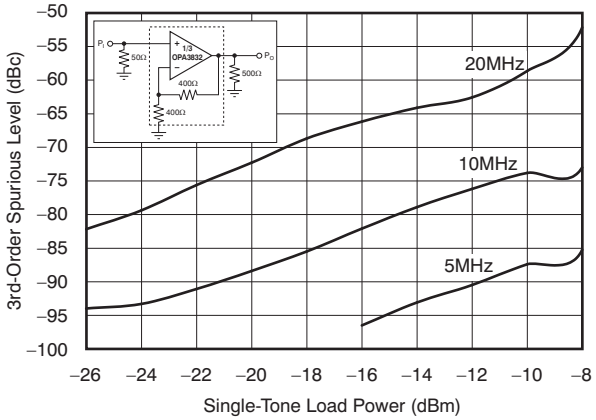


Figure 44.

OUTPUT SWING vs LOAD RESISTANCE

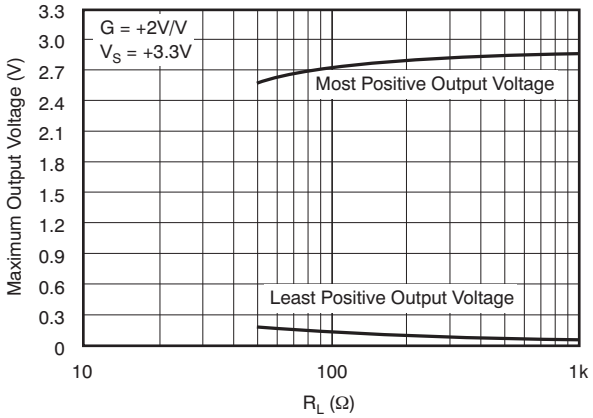


Figure 45.

APPLICATION INFORMATION

WIDEBAND VOLTAGE-FEEDBACK OPERATION

The OPA3832 is a unity-gain stable, very high-speed voltage-feedback op amp designed for single-supply operation (+3V to +11V). The input stage supports input voltages below ground and to within 1.7V of the positive supply. The complementary common-emitter output stage provides an output swing to within 25mV of ground and the positive supply. The OPA3832 is compensated to provide stable operation with a wide range of resistive loads.

Figure 46 shows the ac-coupled, gain of +2V/V configuration used for the +5V Specifications and Typical Characteristic Curves. For test purposes, the input impedance is set to 50Ω with the 66.7Ω resistor to ground in parallel with the 200Ω bias network. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins. For the circuit of Figure 46, the total effective load on the output at high frequencies is 150Ω || 800Ω. The 332Ω and 505Ω resistors at the noninverting input provide the common-mode bias voltage. This parallel combination equals the dc resistance at the inverting input (R_F), reducing the dc output offset resulting from input bias current.

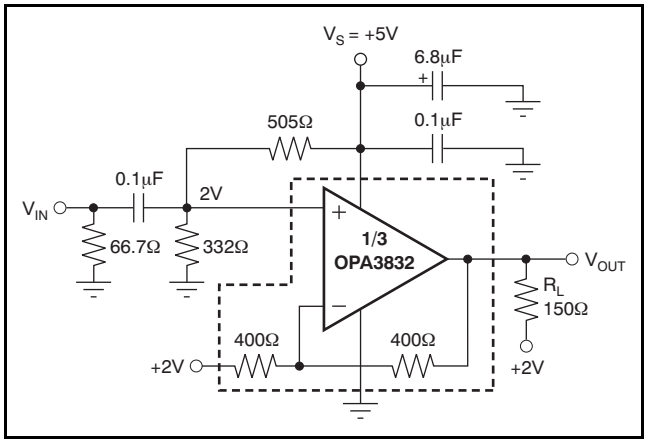


Figure 46. AC-Coupled, G = +2, +5V Single-Supply Specification and Test Circuit

Figure 47 shows the ac-coupled, gain of +2V/V configuration used for the +3.3V Specifications and Typical Characteristic Curves. For test purposes, the input impedance is set to 66.5Ω with a resistor to ground. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins. For the circuit of Figure 47, the total effective load on the output at high frequencies is 150Ω || 800Ω. The 255Ω and 1.13kΩ resistors at the noninverting input provide the common-mode bias voltage. This parallel combination equals the dc resistance at the inverting input (R_F), reducing the dc output offset arising from input bias current.

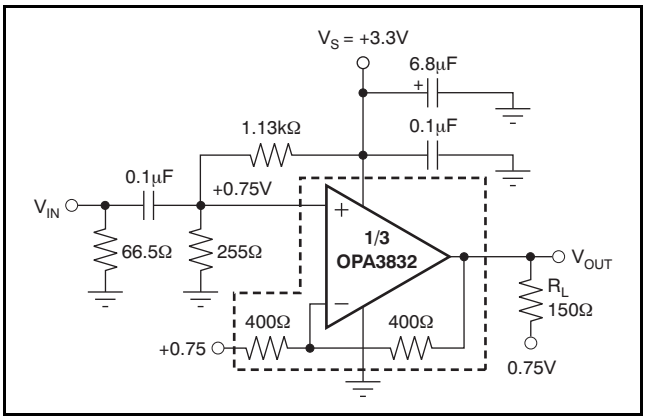


Figure 47. AC-Coupled, G = +2, +3.3V Single-Supply Specification and Test Circuit

Figure 48 shows the dc-coupled, gain of +2, dual power-supply circuit configuration used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 150Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins. For the circuit of Figure 48, the total effective load will be 150Ω || 800Ω. Two optional components are included in Figure 48. An additional resistor (175Ω) is included in series with the noninverting input. Combined with the 25Ω dc source resistance looking back towards the signal generator, this configuration gives an input bias current cancelling resistance that matches the 200Ω source resistance seen at the inverting input (see the *DC Accuracy and Offset Control* section). In addition to the usual power-supply decoupling capacitors to ground, a 0.01µF capacitor is included between the two power-supply pins. In practical printed circuit board (PCB) board layouts, this optional capacitor will typically improve the 2nd-harmonic distortion performance by 3dB to 6dB.

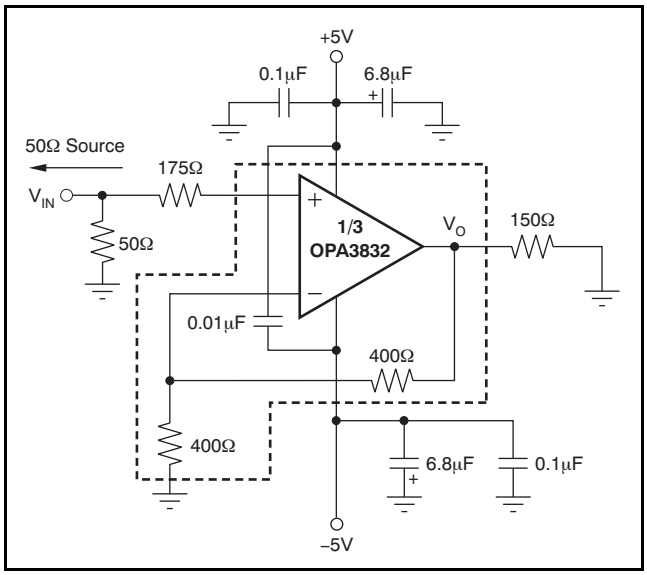


Figure 48. DC-Coupled, G = +2, Bipolar Supply Specification and Test Circuit

SINGLE-SUPPLY ACTIVE FILTER

The OPA3832, while operating on a single +3.3V or +5V supply, lends itself well to high-frequency active filter designs. Again, the key additional requirement is to establish the dc operating point of the signal near the supply midpoint for highest dynamic range. Figure 50 shows an example design of a 1MHz low-pass Butterworth filter using the Sallen-Key topology.

Both the input signal and the gain setting resistor are ac-coupled using 0.1μF blocking capacitors (actually giving bandpass response with the low-frequency pole set to 3.2kHz for the component values shown). As discussed for Figure 46, this configuration allows the midpoint bias formed by one 2kΩ and one 3kΩ resistor to appear at both the input and output pins. The midband signal gain is set to +2 (6dB) in this case. The capacitor to ground on the noninverting input is intentionally set larger to dominate input parasitic terms. At a gain of +2, the OPA3832 on a single supply will show 80MHz small- and large-signal bandwidth. The resistor values have been slightly adjusted to account for this limited bandwidth in the amplifier stage. Tests of this circuit, shown in Figure 49, illustrate a precise 1MHz, –3dB point with a maximally-flat passband (above the 3.2kHz ac-coupling corner), and a maximum stop band attenuation of 36dB.

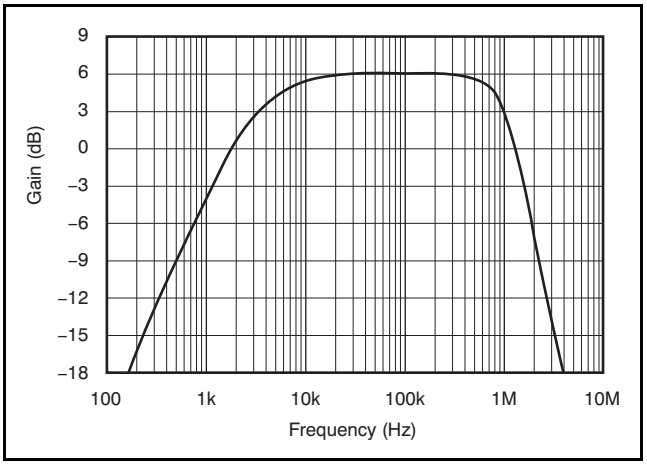


Figure 49. 1MHz, 2nd-Order, Butterworth Low-Pass Filter

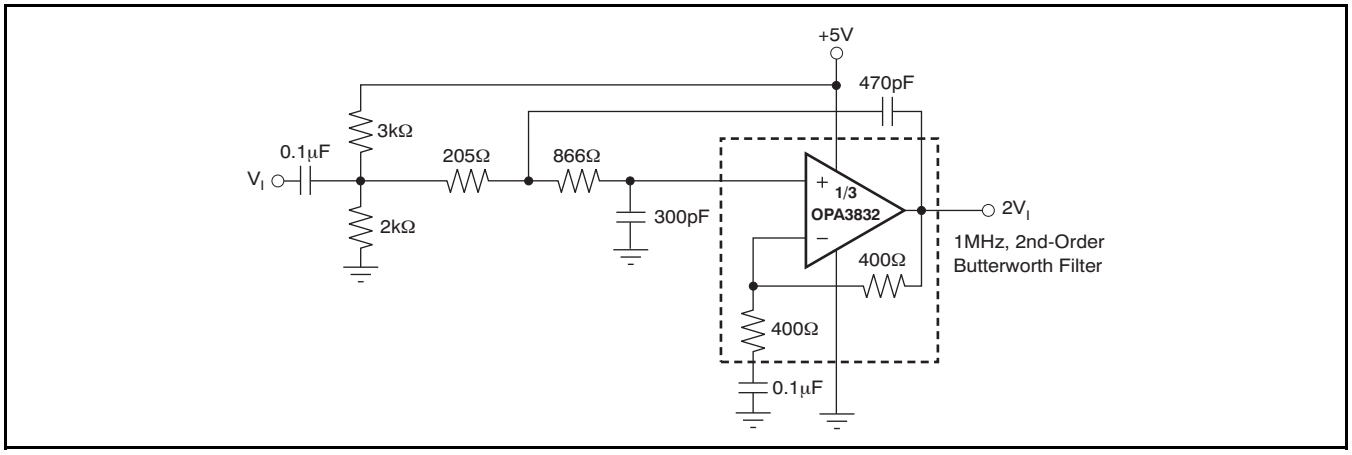


Figure 50. Single-Supply, High-Frequency Active Filter

HIGH-SPEED INSTRUMENTATION AMPLIFIER

Figure 51 shows an instrumentation amplifier based on the OPA3832. The offset matching between inputs makes this an attractive input stage for this application. The differential-to-single-ended gain for this circuit is 2.0V/V. The inputs are high impedance, with only 1pF to ground at each input. The loads on the OPA3832 outputs are equal for the best harmonic distortion possible.

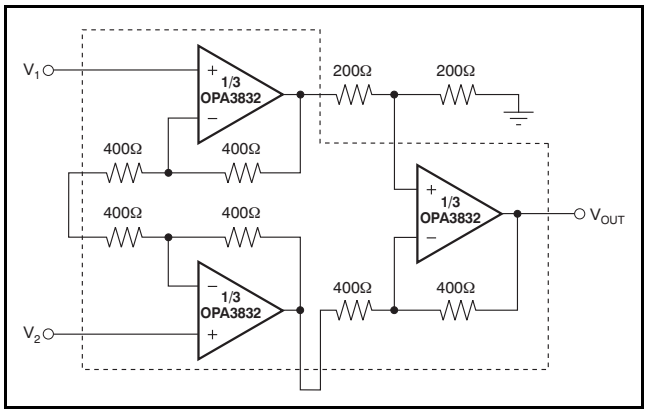


Figure 51. High-Speed Instrumentation Amplifier

As shown in Figure 52, the OPA3832 used as an instrumentation amplifier has a 55MHz, –3dB bandwidth. This data plots a $1V_{PP}$ output signal using a low-impedance differential input source.

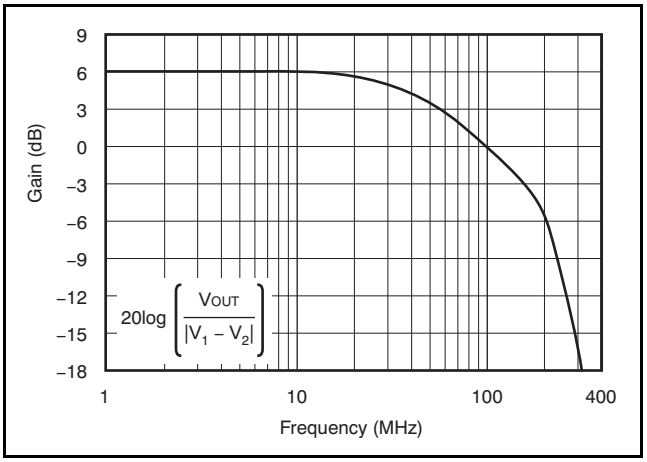


Figure 52. High-Speed Instrumentation Amplifier Response

MULTIPLEXED CONVERTER DRIVER

The converter driver in Figure 53 multiplexes among the three input signals. The OPA3832s enable and disable times support multiplexing among video signals. The make-before-break disable characteristic of the OPA3832 ensures that the output is always under control. To avoid large switching glitches, switch during the sync or retrace portions of the video signal—the two inputs should be almost equal at these times. The output is always under control, so the switching glitches for two 0V inputs are < 20mV. With standard video signals levels at the inputs, the maximum differential voltage across the disabled inputs will not exceed the ±1.2V maximum rating.

The output resistors isolate the outputs from each other when switching between channels. The feedback network of the disabled channels forms part of the load seen by the enabled amplifier, attenuating the signal slightly.

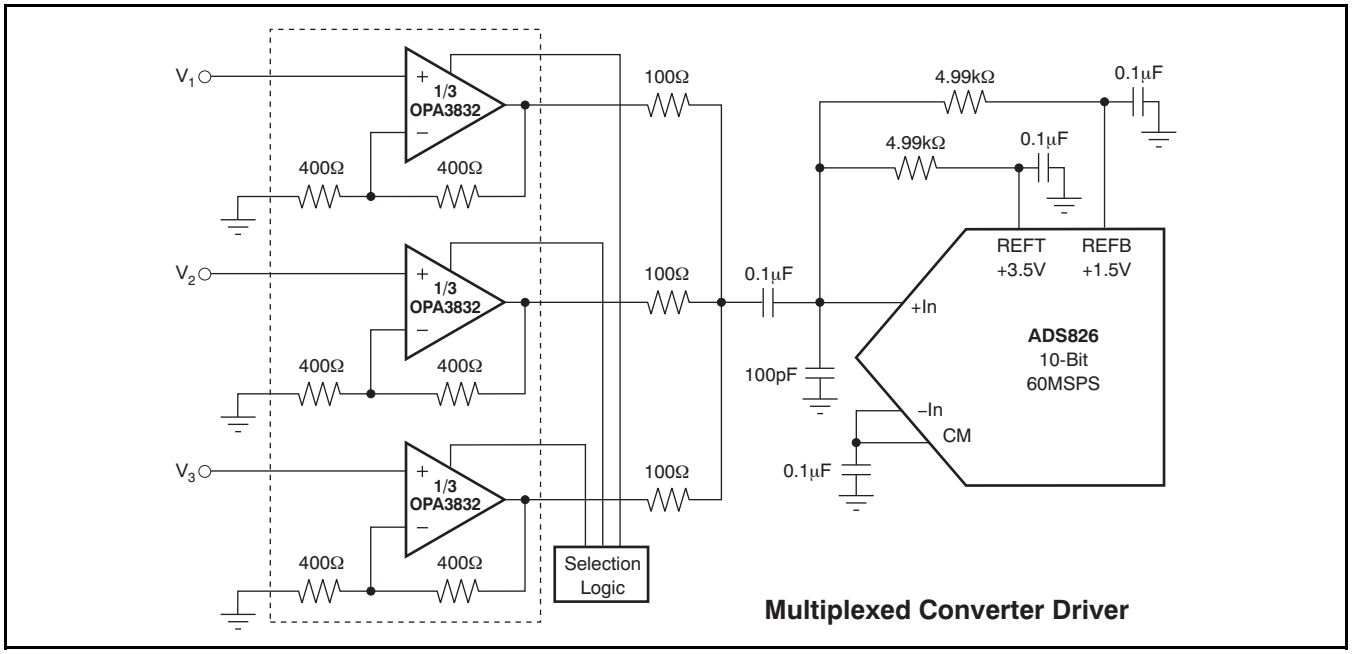


Figure 53. Multiplexed Converter Driver

LOW-PASS FILTER

The circuit in Figure 54 realizes a 7th-order Butterworth low-pass filter with a –3dB bandwidth of 2MHz. This filter is based on the KRC active filter topology that uses an amplifier with the fixed gain ≥ 1. The OPA3832 makes a good amplifier for this type of filter. The component values have been adjusted to compensate of the parasitic effects of the op amp.

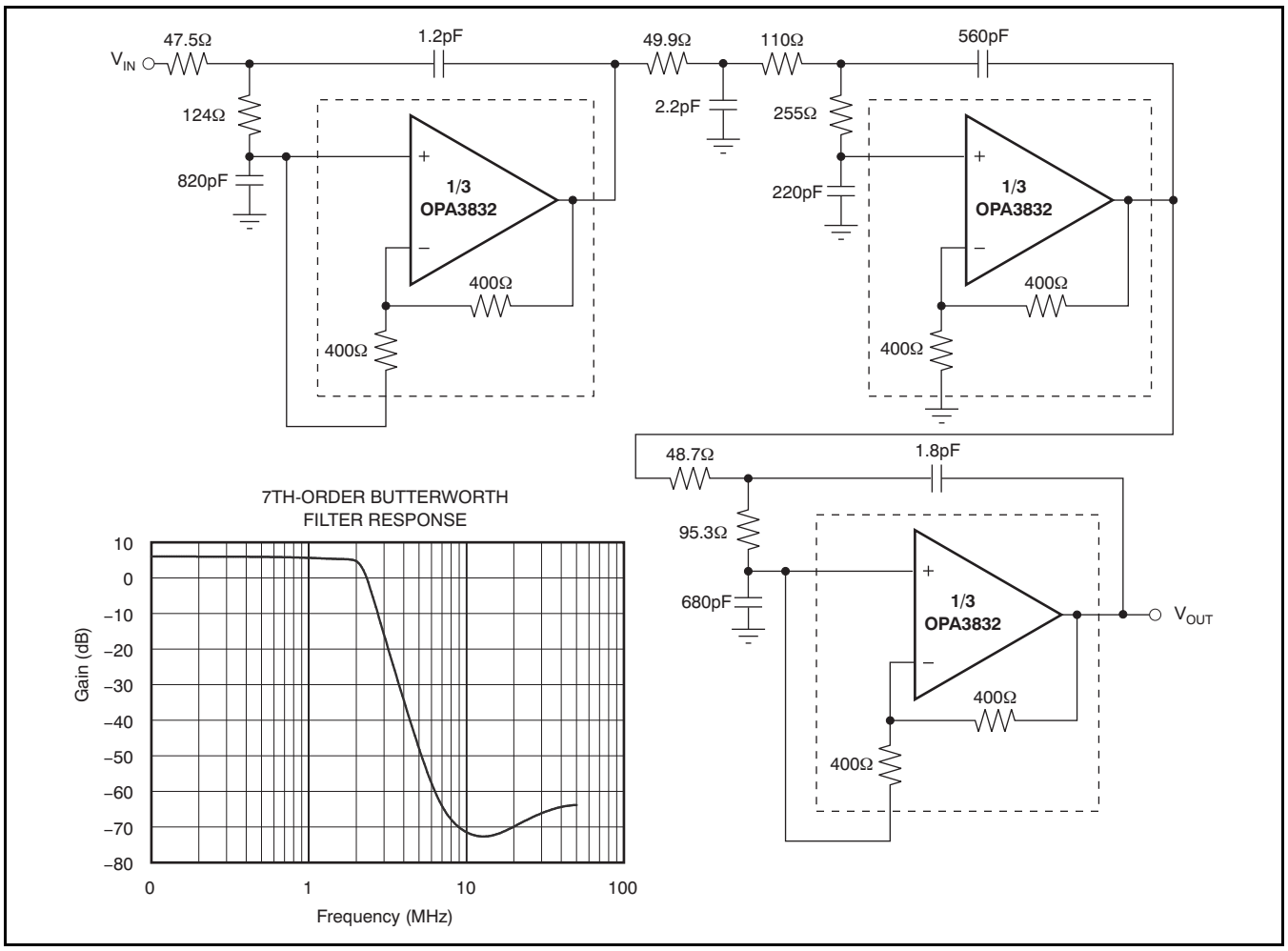


Figure 54. 7th-Order Butterworth Filter

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA3832 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table 1.

Table 1. Demonstration Fixtures by Package

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA3832ID	SO-14	DEM-OPA-SO-3B	SBOU018
OPA3832IPW	TSSOP-14	DEM-OPA-SSOP-3B	SBOU019

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA3832 product folder.

MACROMODEL AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA3832 and its circuit designs. This is particularly true for video and RF amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA3832 is available through the TI web page (www.ti.com). The applications department is also available for design assistance. These models predict typical small signal ac, transient steps, dc performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the data sheet. These models do not attempt to distinguish between the package types in their small-signal ac performance.

OPERATING SUGGESTIONS

OUTPUT CURRENT AND VOLTAGES

The OPA3832 provides outstanding output voltage capability. For the +5V supply, under no-load conditions at +25°C, the output voltage typically swings closer than 90mV to either supply rail.

The minimum specified output voltage and current specifications over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the ensured tables. As the output transistors deliver power, the junction temperatures will increase, decreasing the V_{BE}s (increasing the available output voltage swing) and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications, because the output stage junction temperatures will be higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short-circuit protection is provided. This configuration will not normally be a problem, since most applications include a series matching resistor at the output that will limit the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin (8-pin packages) will, in most cases, destroy the amplifier. If additional short-circuit protection is required, consider a small series resistor in the power-supply leads. This resistor will reduce the available output voltage swing under heavy output loads.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an Analog-to-Digital Converter (ADC)—including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA3832 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load.

The Typical Characteristic curves show the recommended R_S versus capacitive load and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA3832. Long PCB traces, unmatched cables, and connections to multiple devices can easily exceed this value. Always consider this effect carefully, and add the recommended series resistor as close as possible to the output pin (see the *Board Layout Guidelines* section).

The criterion for setting this R_S resistor is a maximum bandwidth, flat frequency response at the load. For a gain of +2, the frequency response at the output pin is already slightly peaked without the capacitive load, requiring relatively high values of R_S to flatten the response at the load. Increasing the noise gain will also reduce the peaking.

DISTORTION PERFORMANCE

The OPA3832 provides good distortion performance into a 150Ω load. Relative to alternative solutions, it provides exceptional performance into lighter loads and/or operating on a single +3.3V supply. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic will dominate the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network; in the noninverting configuration (see Figure 47) this is the sum of $R_F + R_G$, while in the inverting configuration, only R_F needs to be included in parallel with the actual load.

NOISE PERFORMANCE

High slew rate, unity-gain stable, voltage-feedback op amps usually achieve their slew rate at the expense of a higher input noise voltage. The 9.2nV/√Hz input voltage noise for the OPA3832, however, is much lower than comparable amplifiers. The input-referred voltage noise and the two input-referred current noise terms (2.2pA/√Hz) combine to give low output noise under a wide variety of operating conditions. Figure 55 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

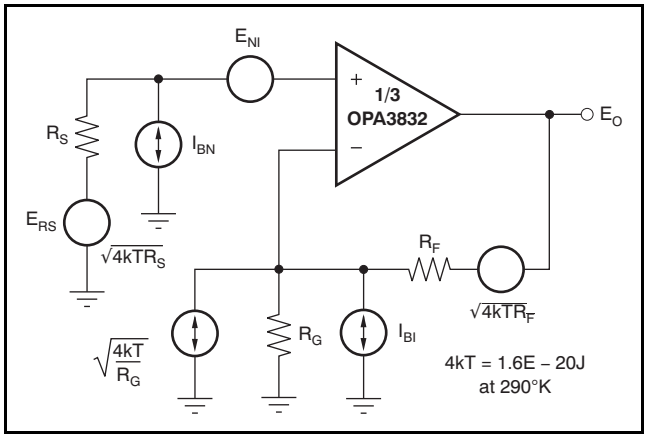


Figure 55. Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 1 shows the general form for the output noise voltage using the terms shown in Figure 55:

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (1)$$

Dividing this expression by the noise gain ($NG = (1 + R_F/R_G)$) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Figure 55:

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (2)$$

Evaluating these two equations for the circuit and component values shown in Figure 46 gives a total output spot noise voltage of 18.8nV/√Hz and a total equivalent input spot noise voltage of 9.42nV/√Hz. This total includes the noise added by the resistors. This total input-referred spot noise voltage is not much higher than the 9.2nV/√Hz specification for the op amp voltage noise alone.

DC ACCURACY AND OFFSET CONTROL

The balanced input stage of a wideband voltage-feedback op amp allows good output dc accuracy in a wide variety of applications. The power-supply current trim for the OPA3832 gives even tighter control than comparable products. Although the high-speed input stage does require relatively high input bias current (typically 5µA out of each input terminal), the close matching between them may be used to reduce the output dc error caused by this current. This configuration matches the dc source resistances appearing at the two inputs. Evaluating the configuration of Figure 48 (which has matched dc input resistances), using worst-case +25°C input offset voltage and current specifications, gives a worst-case output offset voltage equal to:

- (NG = noninverting signal gain at dc)
- $\pm(NG \times V_{OS(MAX)}) + R_F \times I_{OS(MAX)})$
- $= \pm(2 \times 80mV) + (400\Omega \times 1.5\mu A)$
- = –15.4mV to +16.6mV

A fine-scale output offset null, or dc operating point adjustment, is often required. Numerous techniques are available for introducing dc offset control into an op amp circuit. Most of these techniques are based on adding a dc current through the feedback resistor. In selecting an offset trim method, one key consideration is the impact on the desired signal path frequency response. If the signal path is intended to be noninverting, the offset control is best applied as an inverting summing signal to avoid interaction with the signal source. If the signal path is intended to be inverting, applying the offset control to the noninverting input may be considered. Bring the dc offsetting current into the inverting input node through resistor values that are much larger than the signal path resistors. This configuration ensures that the adjustment circuit has minimal effect on the loop gain and thus the frequency response.

THERMAL ANALYSIS

Maximum desired junction temperature sets the maximum allowed internal power dissipation, as described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load, though for resistive loads connected to midsupply ($V_S/2$), P_{DL} is at a maximum when the output is fixed at a voltage equal to $V_S/4$ or $3V_S/4$. Under this condition, $P_{DL} = V_S^2/(4 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage, and not into the load, that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA3832 (TSSOP-14 package) in the circuit of Figure 48 operating at the maximum specified ambient temperature of +85°C and driving both channels at a 150Ω load at mid-supply.

$$P_D = 10V \times 12.75mA + \frac{3 \times 5^2}{\left(4 \times \left(150\Omega \parallel 800\Omega\right)\right)} = 276mV$$

$$\text{Maximum } T_J = +85°C + \left(0.276W \times 100°C/W\right) = 113°C$$

Although this value is still well below the specified maximum junction temperature, system reliability considerations may require lower ensured junction temperatures. The highest possible internal dissipation will occur if the load requires current to be forced into the output at high output voltages or sourced from the output at low output voltages. This condition puts a high current through a large internal voltage drop in the output transistors.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier such as the OPA3832 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Each power-supply connection should always be decoupled with one of these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components will preserve the high-frequency performance. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB traces as short as possible. Never use wire-wound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the typical characteristic curve, Figure 5. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA3832 is nominally compensated to operate with a 2pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary onboard, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined (based on board material and trace dimensions), a matching series resistor into the trace from the output of the OPA3832 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the typical characteristic curve, Figure 5. This configuration will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation as a result of the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA3832 directly onto the board.

INPUT AND ESD PROTECTION

The OPA3832 is built using a very high-speed, complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins are protected with internal ESD protection diodes to the power supplies, as shown in Figure 56.

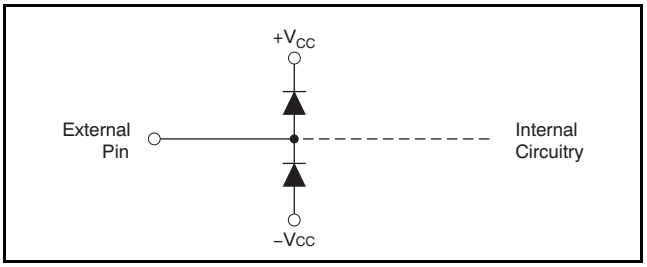


Figure 56. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (that is, in systems with ±15V supply parts driving into the OPA3832), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible, since high values degrade both noise performance and frequency response.

Revision History

Changes from Original (December 2006) to Revision A **Page**

- Deleted grey from rows labelled as *D* in the package designator rows in the *Ordering Information* table 2
- Deleted footnote (2) from the *Ordering Information* table 2
- Changed storage voltage range row in *Absolute Maximum Ratings* table to storage temperature range with a rating of –65°C to +125°C 2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA3832ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA3832	Samples
OPA3832IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA3832	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

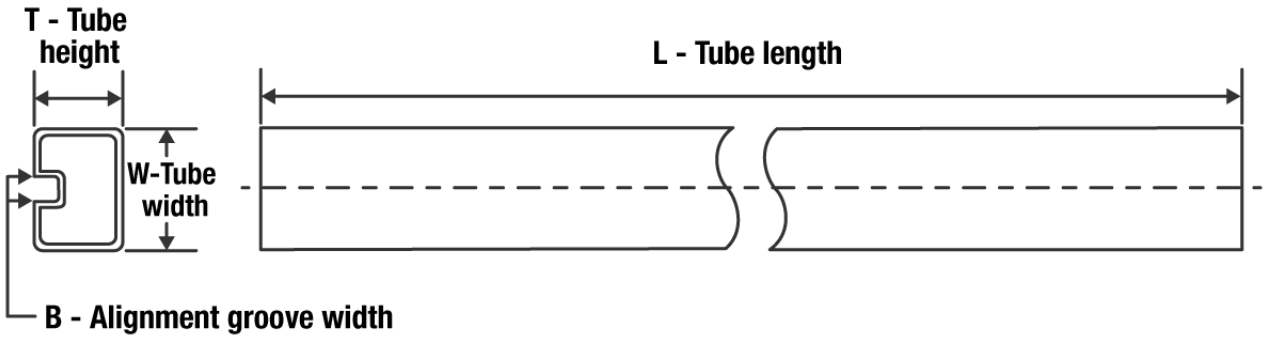
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

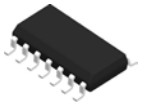
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA3832ID	D	SOIC	14	50	506.6	8	3940	4.32
OPA3832IPW	PW	TSSOP	14	90	530	10.2	3600	3.5

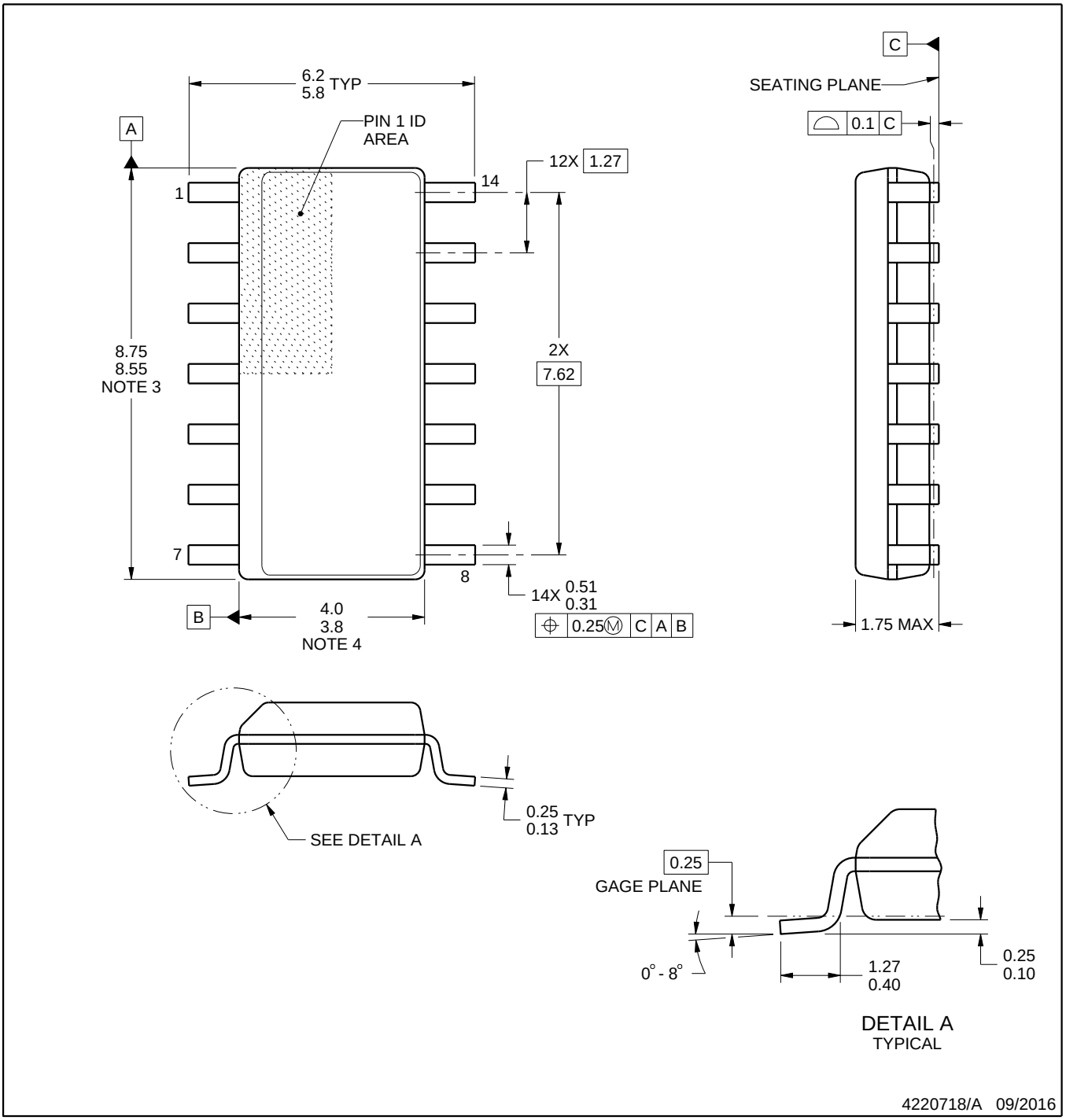


PACKAGE OUTLINE

D0014A

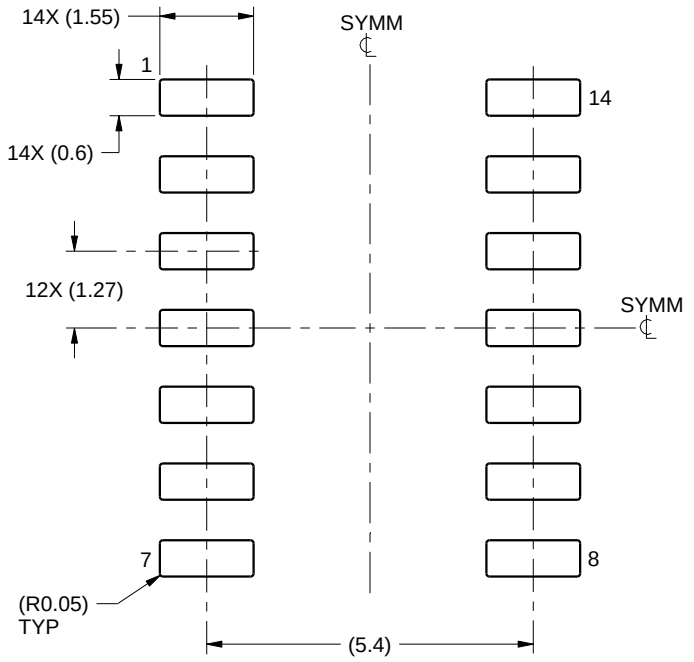
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

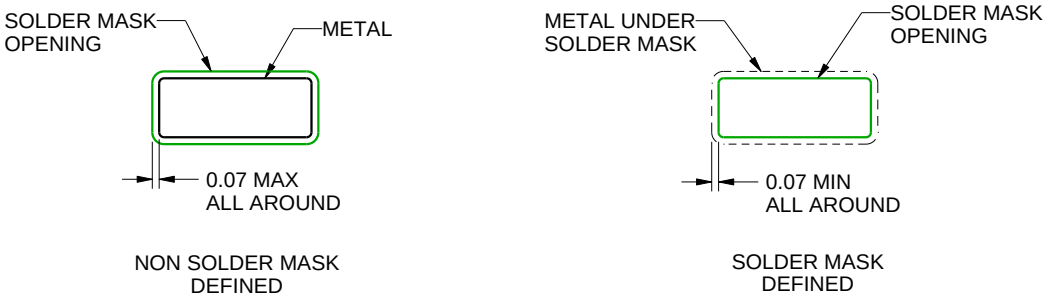


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

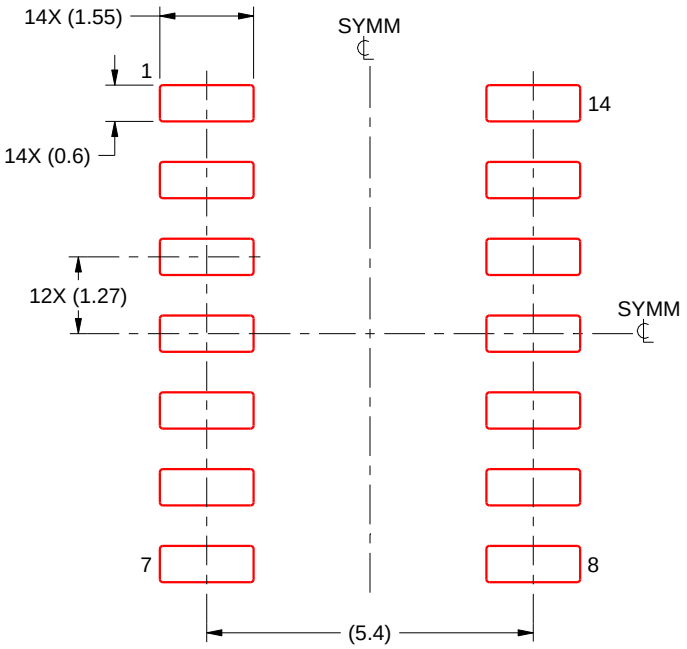
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

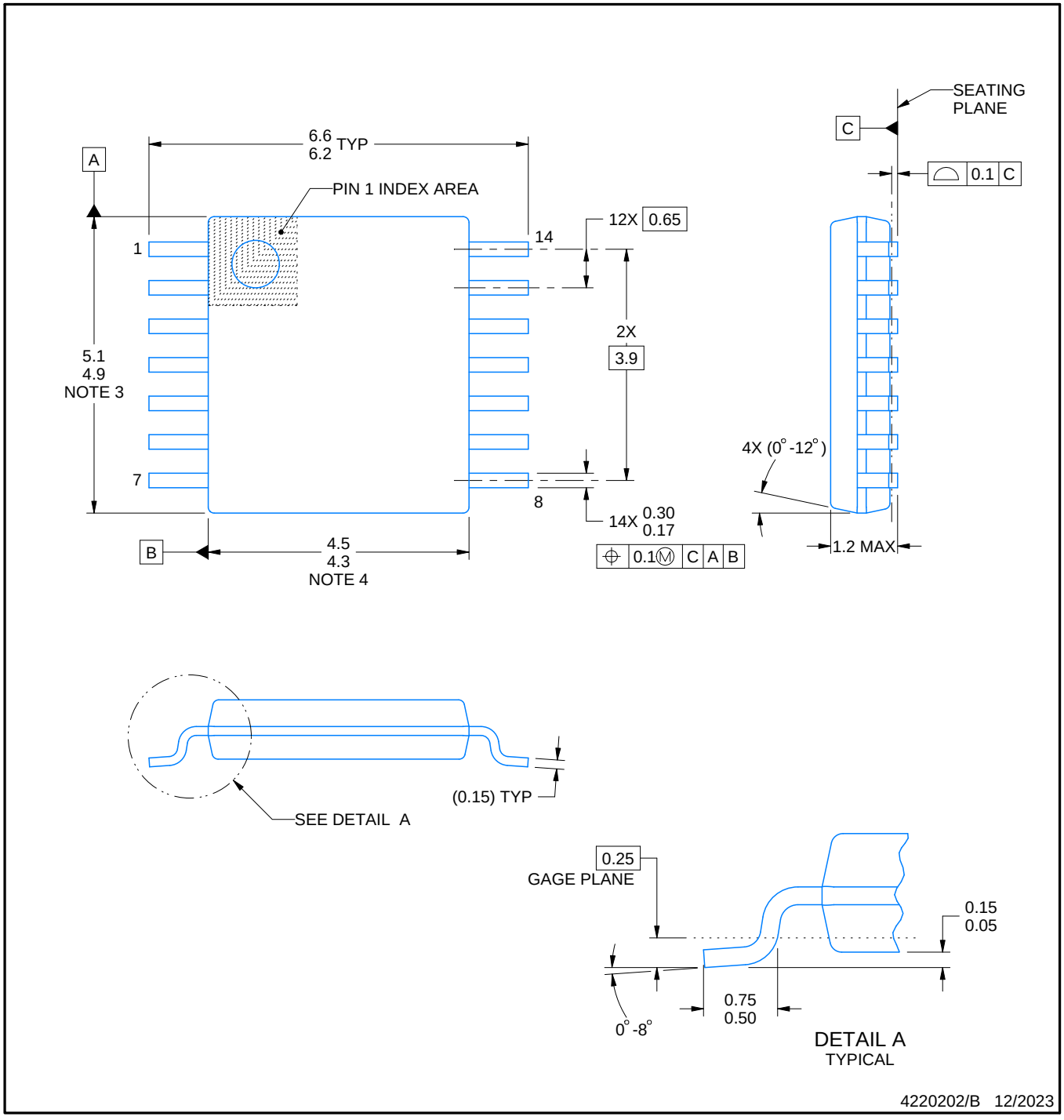
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

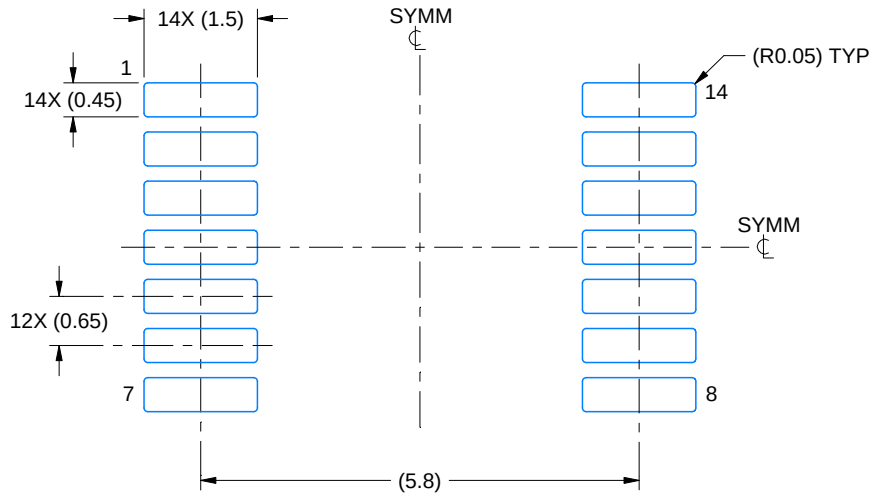
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

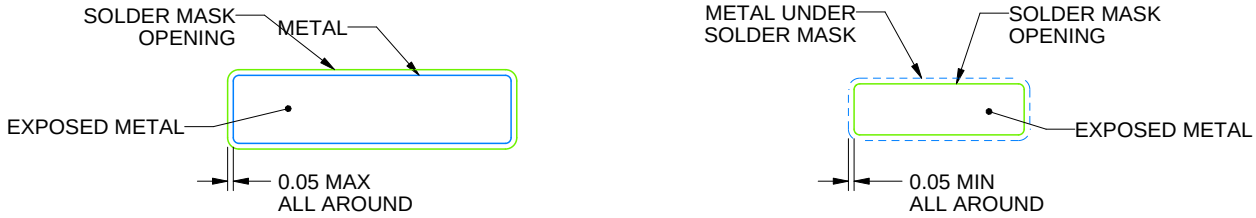


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

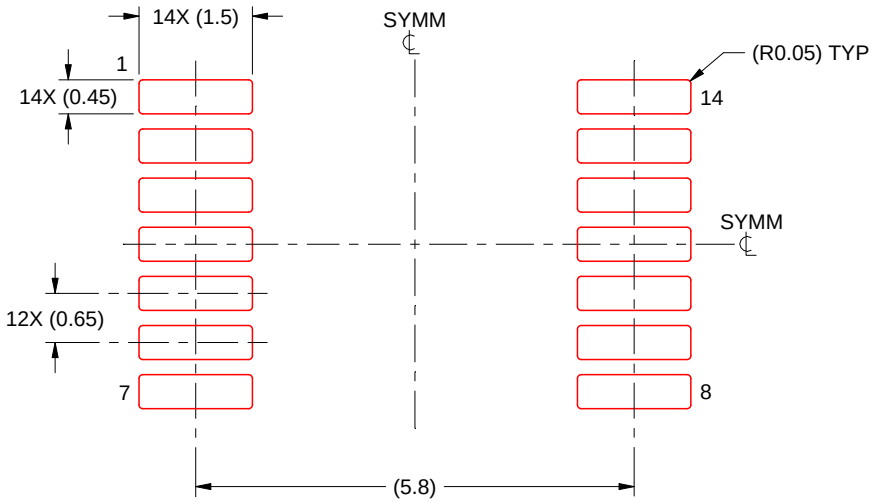


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265