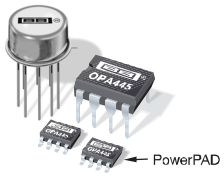


SBOS156B − MARCH 1987 − REVISED APRIL 2008

High Voltage FET-Input OPERATIONAL AMPLIFIER

FEATURES

- **WIDE-POWER SUPPLY RANGE: ±10V to ±45V**
- **HIGH SLEW RATE: 15V/μs**
- **LOW INPUT BIAS CURRENT: 10pA**
- **STANDARD-PINOUT TO-99, DIP, SO-8 PowerPAD™, AND SO-8 SURFACE-MOUNT PACKAGES**

APPLICATIONS

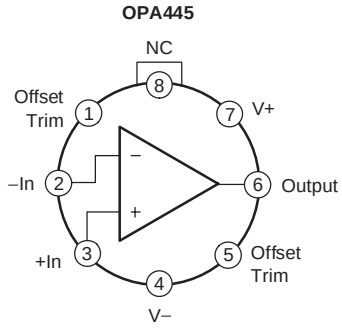
- **TEST EQUIPMENT**
- **HIGH-VOLTAGE REGULATORS**
- **POWER AMPLIFIERS**
- **DATA ACQUISITION**
- **SIGNAL CONDITIONING**
- **AUDIO**
- **PIEZO DRIVERS**

DESCRIPTION

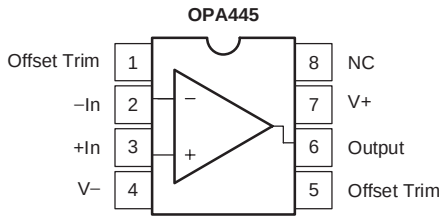
The OPA445 is a monolithic operational amplifier capable of operation from power supplies up to ±45V and output currents of 15mA. It is useful in a wide variety of applications requiring high output voltage or large common-mode voltage swings.

The OPA445's high slew rate provides wide power-bandwidth response, which is often required for high-voltage applications. FET input circuitry allows the use of high-impedance feedback networks, thus minimizing their output loading effects. Laser trimming of the input circuitry yields low input offset voltage and drift.

The OPA445 is available in standard pinout TO-99, DIP-8, and SO-8 surface-mount packages as well as an SO-8 PowerPAD package for reducing junction temperature. It is fully specified from −25°C to +85°C and operates from −55°C to +125°C. A SPICE macromodel is available for design analysis (from www.ti.com).



Case is connected to V−
TO−99



DIP−8, SO−8, SO−8 PowerPAD

NC = No internal connection;
leave NC floating or connect to GND, V+, or V−.

ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	±50V
Differential Input Voltage	±80V
Input Voltage Range	$\|\pm V_S\| - 3V$
Storage Temperature Range: M	−65°C to +150°C
P, U, DDA	−55°C to +125°C
Operating Temperature Range	−55°C to +125°C
Output Short-Circuit to Ground (T_J < +125°C)	Continuous
Junction Temperature: M	+175°C
Junction Temperature: P, U, DDA	+150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA445AP	DIP-8	P	OPA445AP
OPA445AU	SO-8 Surface-Mount	D	OPA445AU
OPA445ADDA	SO-8 PowerPAD	DDA	OPA445
OPA445BM	TO-99 8-Pin	LMC	OPA445BM

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

Boldface limits apply over the specified temperature range, **T_A = −25°C to +85°C. V_S = ±40V.**

At T_A = +25°C, V_S = ±40V, and R_L = 5kΩ, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA445BM			OPA445AP, AU, ADDA			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE									
Input Offset Voltage	V_{OS}	V_{CM} = 0, I_O = 0		±1	±3		±1.5	±5	mV
vs Temperature	**V_{OS}/dT**	**T_A = −25°C to +85°C**		**±10**			*		**µV/°C**
vs Power Supply	PSRR	V_S = ±10V to ±45V		4	100		*	*	µV/V
INPUT BIAS CURRENT(1)									
Input Bias Current	I_B	V_{CM} = 0V		±10	±50		*	±100	pA
Over Specified Temperature Range					**±10**			**±20**	**nA**
Input Offset Current	I_{OS}	V_{CM} = 0V		±4	±20		*	±40	pA
Over Specified Temperature Range					**±5**			**±10**	**nA**
NOISE									
Input Voltage Noise Density, f = 1kHz	e_n			15			*		nV/√Hz
Current Noise Density, f = 1kHz	i_n			6			*		fA/√Hz
INPUT VOLTAGE RANGE									
Common-Mode Voltage Range	V_{CM}	V_S = ±40V	(V−) + 5		(V+) − 5	*		*	V
Common-Mode Rejection	CMRR	V_{CM} = −35V to +35V	80	95		*	*		dB
Over Specified Temperature Range			**80**			*			**dB**
INPUT IMPEDANCE									
Differential				10^{13} || 1		*			Ω || pF
Common-Mode				10^{14} || 3		*			Ω || pF
OPEN-LOOP GAIN, DC									
Open-Loop Voltage Gain	A_{OL}	V_O = −35V to +35V	100	110		*	*		dB
Over Specified Temperature Range			**97**			*			**dB**
FREQUENCY RESPONSE									
Gain Bandwidth Product	GBW			2			*		MHz
Slew Rate	SR	V_O = 70V_{PP}	5	15		*	*		V/µs
Full Power Bandwidth		V_O = 70V_{PP}	23	70		*	*		kHz
Rise Time		V_O = ±200mV		100			*		ns
Overshoot		G = +1, Z_L = 5kΩ || 50pF		35			*		%
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, V_O = 3.5Vrms, G = 1		0.0002			*		%
		f = 1kHz, V_O = 10Vrms, G = 1		0.00008			*		%
OUTPUT									
Voltage Output	V_O		(V−) + 5		(V+) − 5	*		*	V
Over Specified Temperature Range			**(V−) + 5**		**(V+) − 5**	*		*	V
Current Output	I_O	V_O = ±28V	±15			*			mA
Output Resistance, Open Loop	R_O	dc		220			*		Ω
Short Circuit Current	I_{SC}			±26			*		mA
Capacitive Load Drive	C_{LOAD}		See Typical Characteristic(2)				*		
POWER SUPPLY									
Specified Operating Range	V_S			±40			*		V
Operating Voltage Range			±10		±45	*		*	V
Quiescent Current	I_Q	I_O = 0		±4.2	±4.7		*	*	mA
TEMPERATURE RANGE									
Specification Range			−25		+85	*		*	°C
Operating Range			−55		+125	*		*	°C
Storage Range			−65		+125	−55		+125	°C
Thermal Resistance, Junction-to-Ambient	θ_{JA}								
TO-99				200					°C/W
DIP-8							100		°C/W
SO-8 Surface-Mount							150		°C/W
SO-8 PowerPAD(3)							52		°C/W
Thermal Resistance, Junction-to-Case	θ_{JC}								
SO-8 PowerPAD(3)							10		°C/W

NOTE: * Specifications same as OPA445BM.

(1) High-speed test at T_J = +25°C.

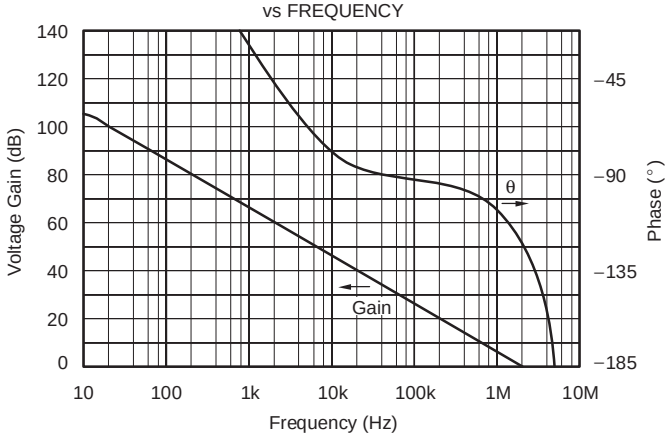
(2) See *Small-Signal Overshoot vs Load Capacitance* in the Typical Characteristics section.

(3) Test board 1in x 0.5in heat-spreader, 1oz copper.

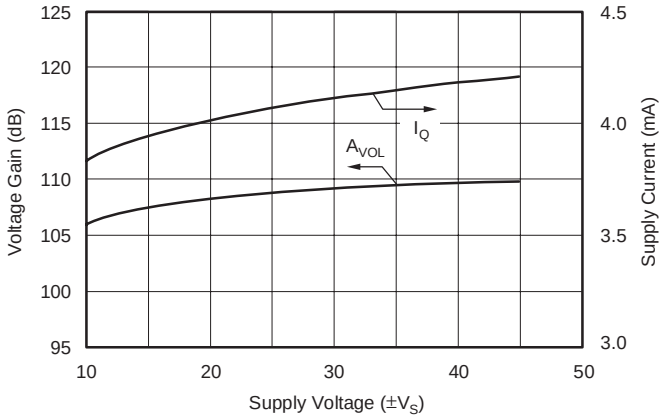
TYPICAL CHARACTERISTICS

At T_A = +25°C and V_S = ±40V, unless otherwise noted.

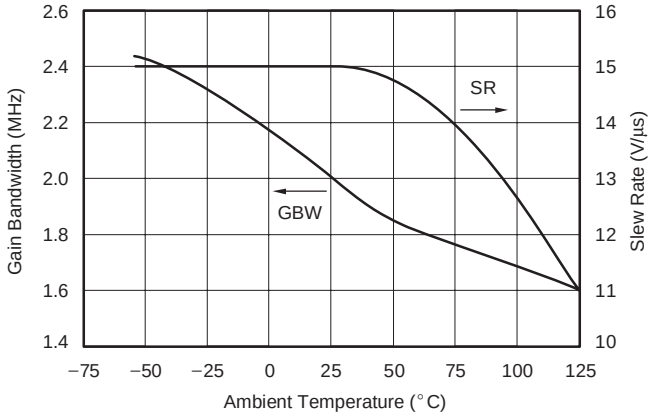
OPEN−LOOP GAIN AND PHASE vs FREQUENCY



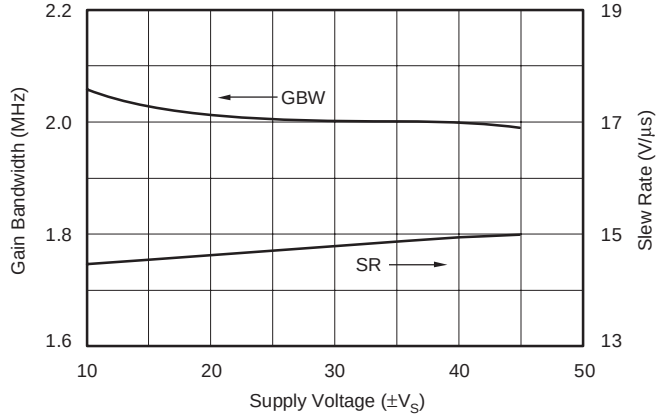
OPEN−LOOP GAIN AND SUPPLY CURRENT vs SUPPLY VOLTAGE



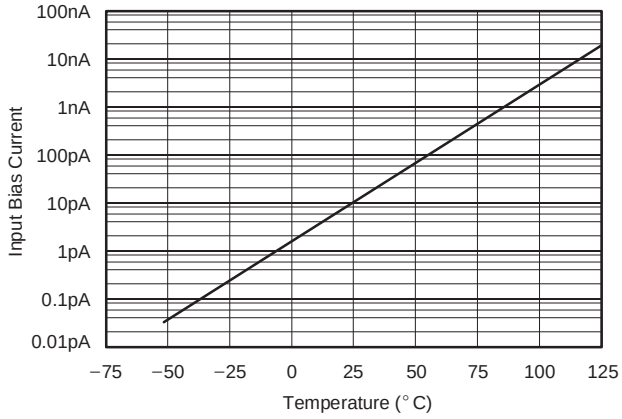
GAIN BANDWIDTH AND SLEW RATE vs TEMPERATURE



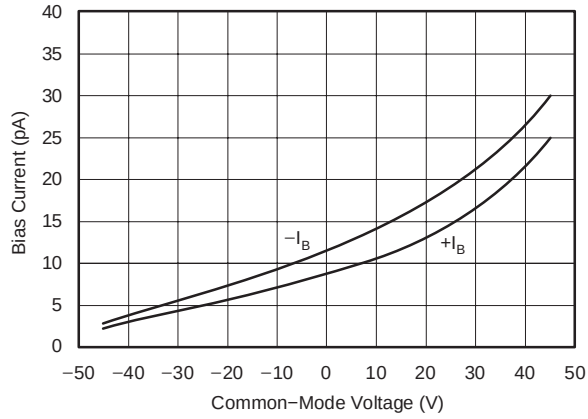
GAIN BANDWIDTH AND SLEW RATE vs SUPPLY VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE



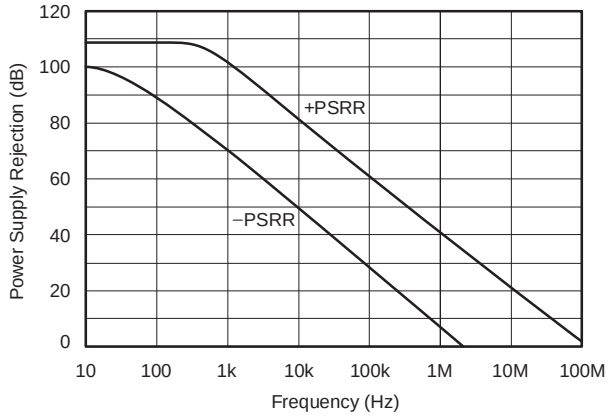
INPUT BIAS CURRENT vs COMMON−MODE VOLTAGE



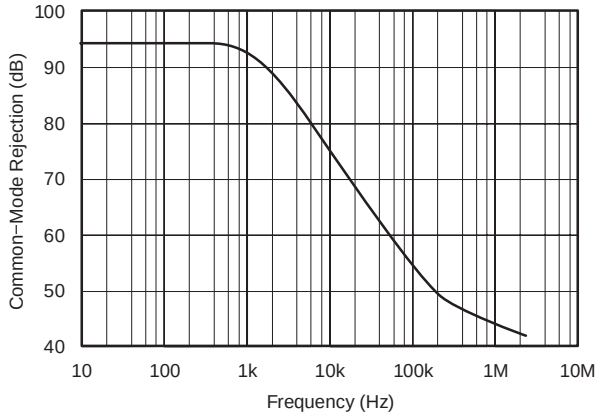
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_S = ±40V, unless otherwise noted.

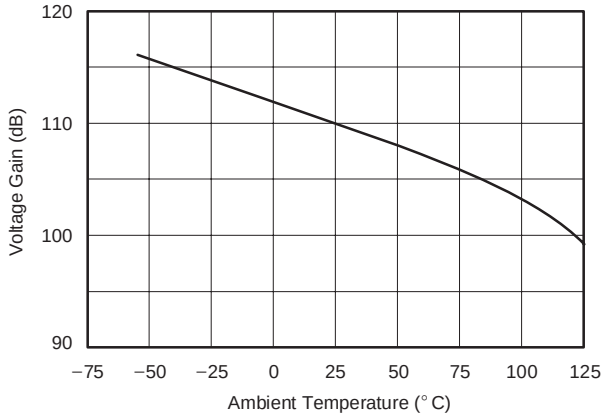
POWER SUPPLY REJECTION
vs FREQUENCY



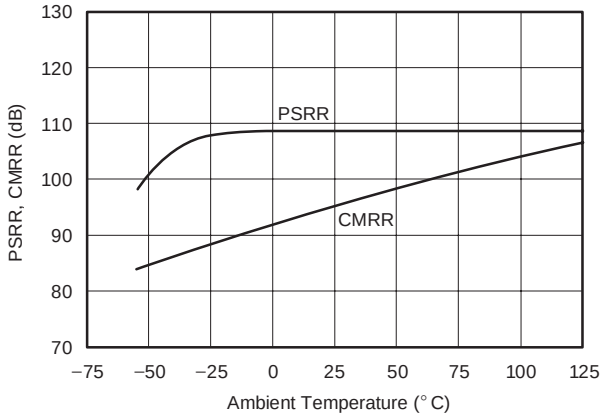
COMMON−MODE REJECTION
vs FREQUENCY



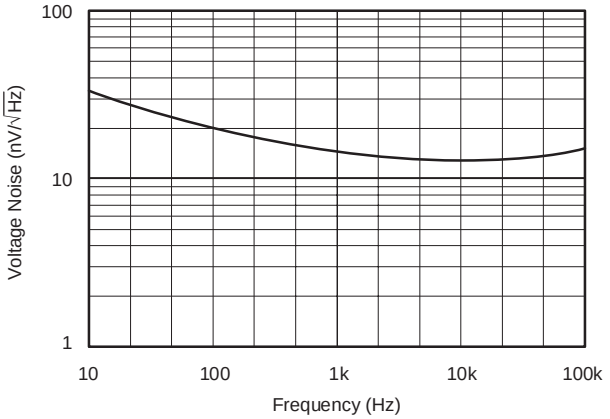
OPEN−LOOP GAIN
vs TEMPERATURE



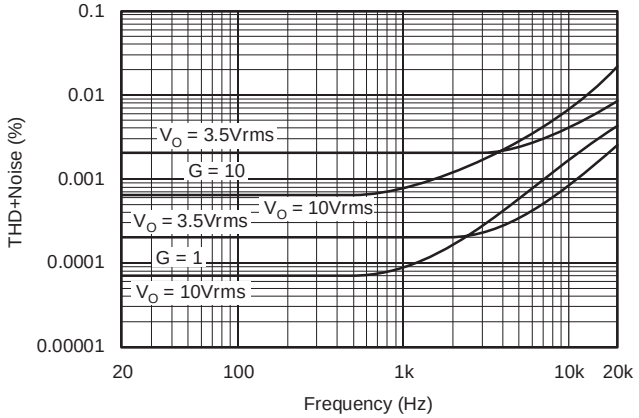
POWER SUPPLY REJECTION AND
COMMON−MODE REJECTION vs TEMPERATURE



INPUT VOLTAGE
NOISE SPECTRAL DENSITY



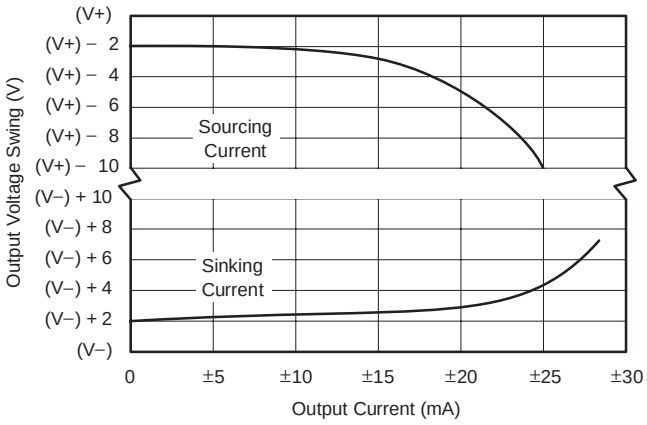
TOTAL HARMONIC DISTORTION + NOISE
vs FREQUENCY



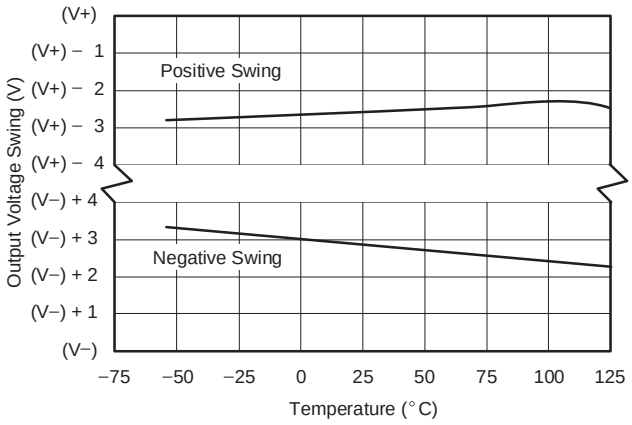
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_S = ±40V, unless otherwise noted.

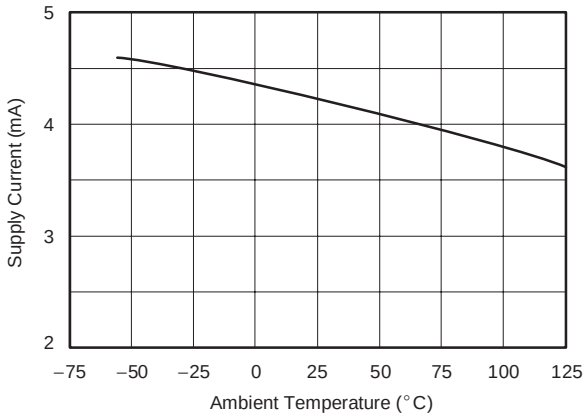
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



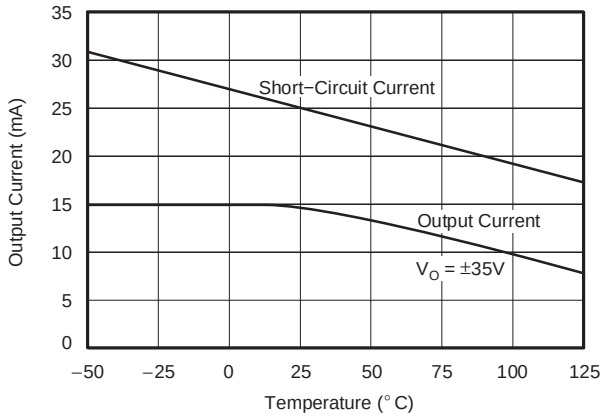
OUTPUT VOLTAGE SWING vs TEMPERATURE



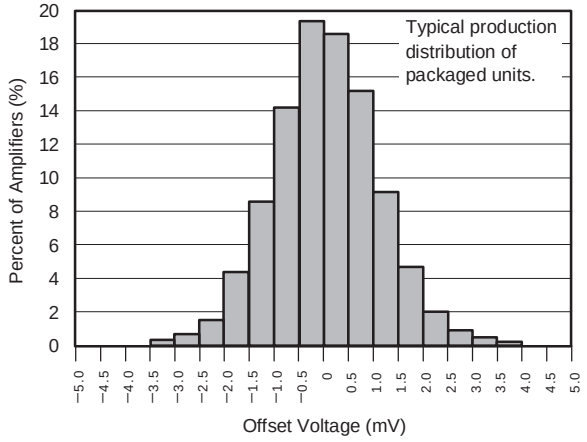
SUPPLY CURRENT vs TEMPERATURE



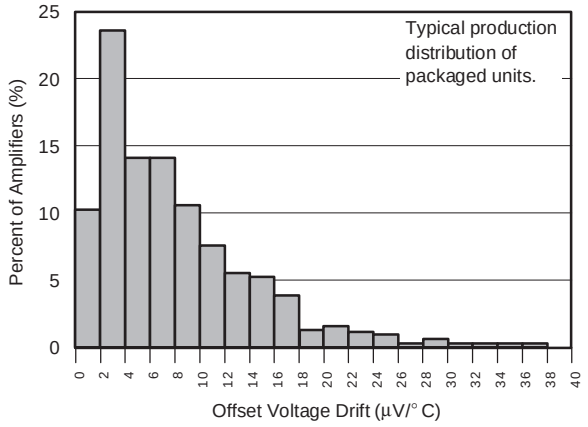
OUTPUT CURRENT vs TEMPERATURE



OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



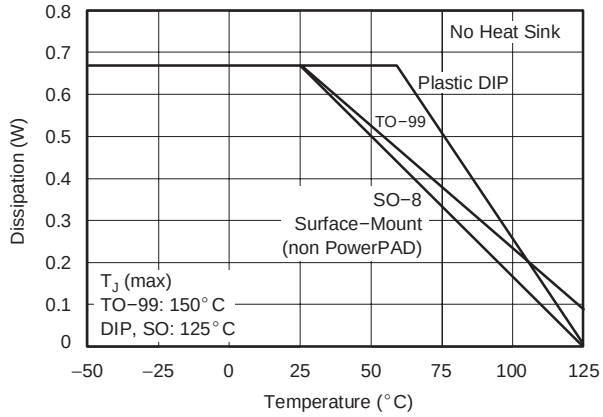
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



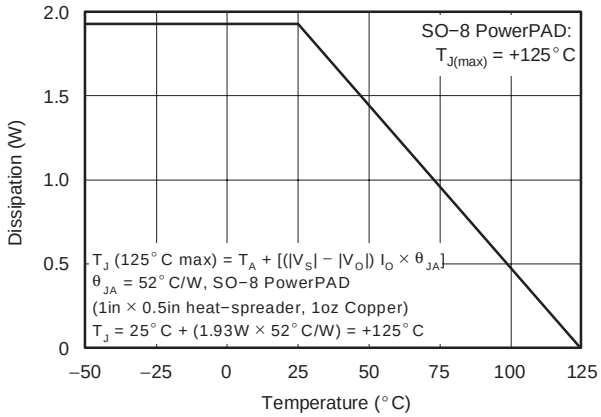
TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and V_S = ±40V, unless otherwise noted.

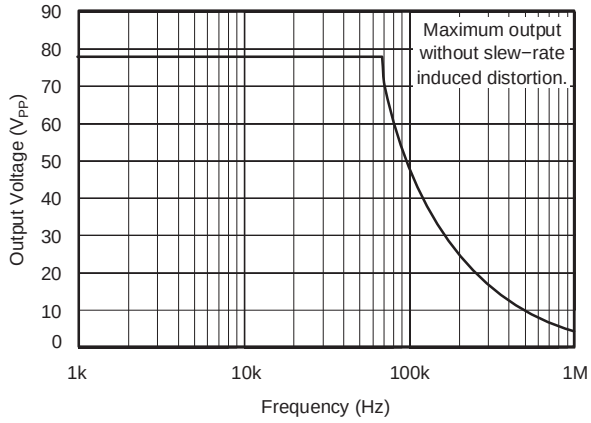
MAXIMUM POWER DISSIPATION vs TEMPERATURE



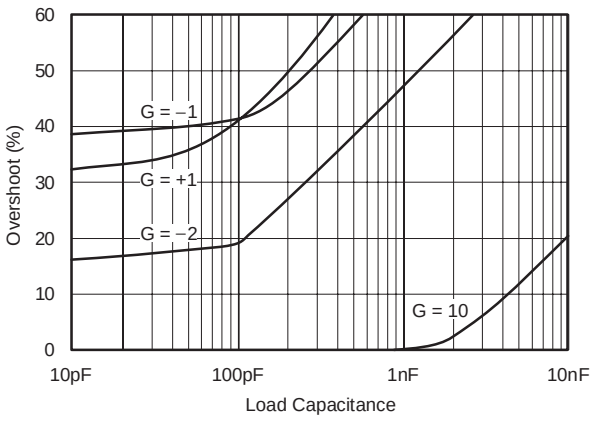
MAXIMUM POWER DISSIPATION vs TEMPERATURE



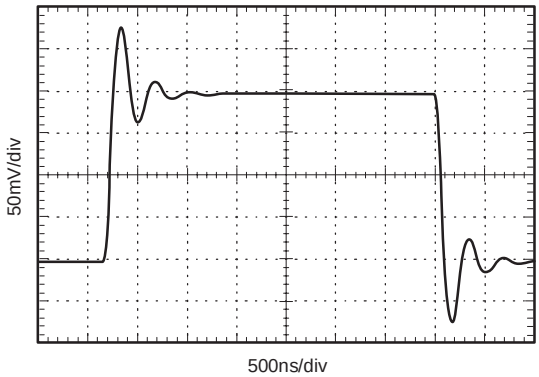
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY



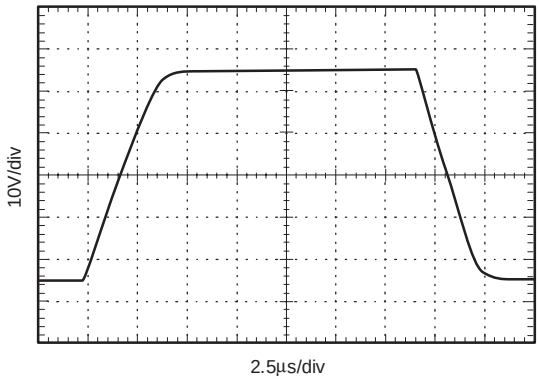
SMALL−SIGNAL OVERSHOOT vs LOAD CAPACITANCE



SMALL−SIGNAL STEP RESPONSE
G = 1, C_L = 100pF



LARGE−SIGNAL STEP RESPONSE
G = 1, C_L = 100pF



APPLICATIONS

Figure 1 shows the OPA445 connected as a basic noninverting amplifier. The OPA445 can be used in virtually any op amp configuration.

Power-supply terminals should be bypassed with 0.1µF capacitors, or greater, near the power supply pins. Be sure that the capacitors are appropriately rated for the power-supply voltage used.

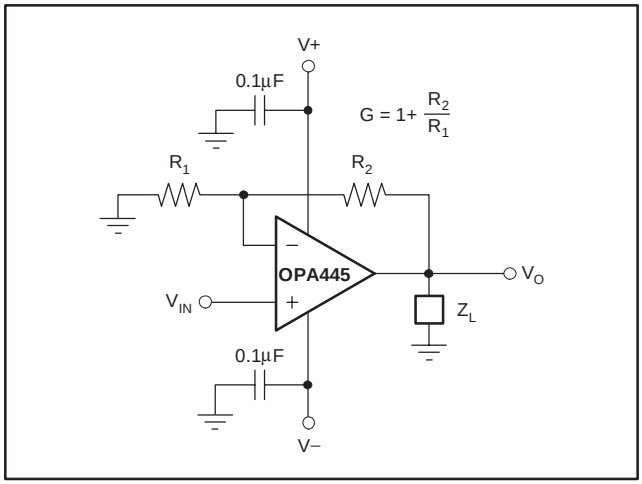


Figure 1. The OPA445 Configured as a Noninverting Amplifier

POWER SUPPLIES

The OPA445 may be operated from power supplies up to ±45V or a total of 90V with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the Typical Characteristics.

Some applications do not require equal positive and negative output voltage swing. Power-supply voltages do not need to be equal. The OPA445 can operate with as little as 20V between the supplies and with up to 90V between the supplies. For example, the positive supply could be set to 80V with the negative supply at −10V, or vice-versa.

INPUT PROTECTION

The inputs of conventional FET-input op amps should be protected against destructive currents that can flow when input FET gate-to-substrate isolation diodes are forward-biased. This can occur if the input voltage exceeds the power supplies or there is an input voltage with V_S = 0V. Protection is easily accomplished with a resistor in series with the input. Care should be taken because the resistance in series with the input capacitance may affect stability. Many input signals are inherently current-limited; therefore, a limiting resistor may not be required.

OFFSET VOLTAGE TRIM

The OPA445 provides offset voltage trim connections on pins 1 and 5. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 2. This adjustment should be used only to null the offset of the op amp, not to adjust system offset or offset produced by the signal source. Nulling system offset could degrade the offset voltage drift behavior of the op amp. While it is not possible to predict the exact change in drift, the effect is usually small.

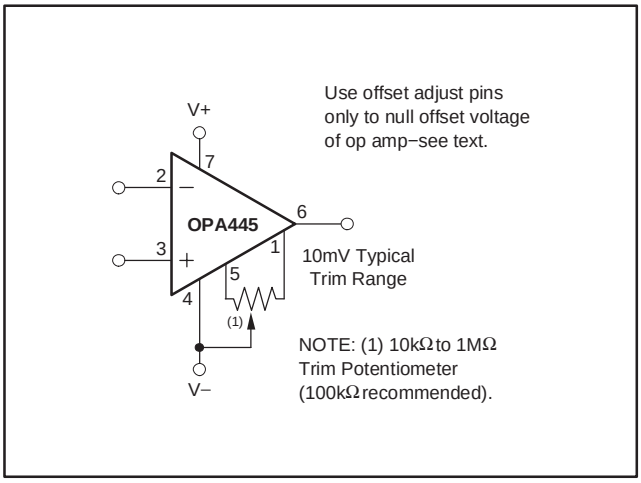
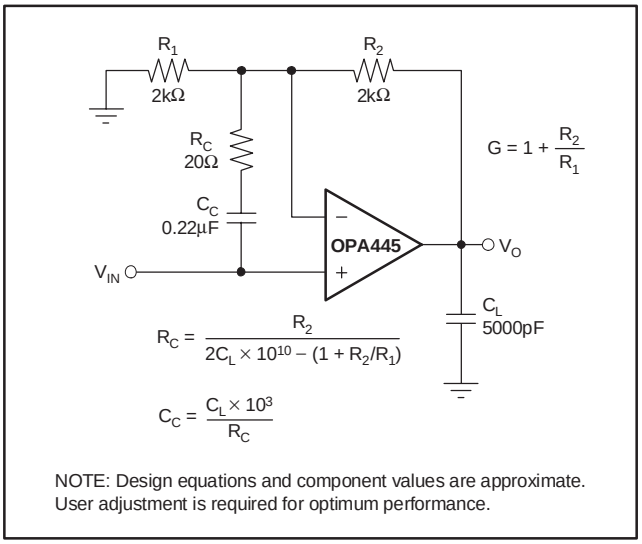


Figure 2. Offset Voltage Trim

CAPACITIVE LOADS

The dynamic characteristics of the OPA445 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and capacitive load will decrease the phase margin and may lead to gain peaking or oscillations. Figure 3 shows a circuit which preserves phase margin with capacitive load. The circuit does not suffer a voltage drop due to load current; however, input impedance is reduced at high frequencies. Consult Application Bulletin SBOA015, available for download at www.ti.com, for details of analysis techniques and application circuits.

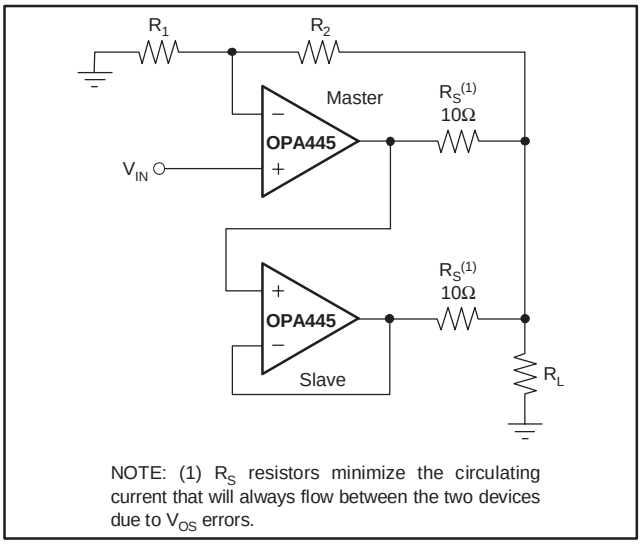


NOTE: Design equations and component values are approximate. User adjustment is required for optimum performance.

Figure 3. Driving Large Capacitive Loads

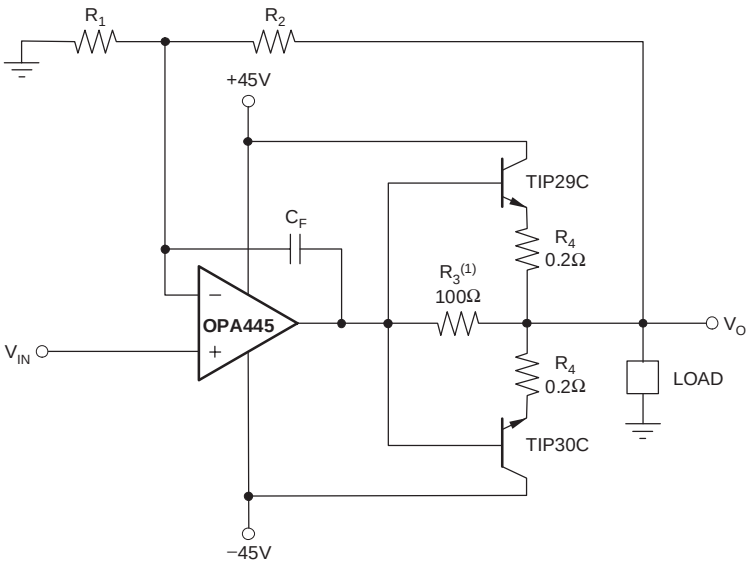
INCREASING OUTPUT CURRENT

In those applications where the 15mA of output current is not sufficient to drive the required load, output current can be increased by connecting two or more OPA445s in parallel as shown in Figure 4. Amplifier A1 is the *master* amplifier and may be configured in virtually any op amp circuit. Amplifier A2, the *slave*, is configured as a unity gain buffer. Alternatively, external output transistors can be used to boost output current. The circuit in Figure 5 is capable of supplying output currents up to 1A.



NOTE: (1) R_S resistors minimize the circulating current that will always flow between the two devices due to V_{OS} errors.

Figure 4. Parallel Amplifiers Increase Output Current Capability



NOTE: (1) Provides current limit for OPA445 and allows the amplifier to drive the load when the output is between +0.7V and −0.7V.

Figure 5. External Output Transistors Boost Output Current Up to 1 Amp

SAFE OPERATING AREA

Stress on the output transistors is determined both by the output current and by the output voltage across the conducting output transistors, $V_S - V_O$. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, $V_S - V_O$. The Safe Operating Area (SOA curve, Figure 6 through Figure 10) illustrates the permissible range of voltage and current. The curves shown represent devices soldered to a printed circuit board (PCB) with no heat sink. Increasing printed circuit trace area or the use of a heat sink (TO-99 package) can significantly reduce thermal resistance (θ), resulting in increased output current for a given output voltage (see Figure 11, Figure 12, and the *Heat Sink* section).

The safe output current decreases as $V_S - V_O$ increases. Output short-circuits are a very demanding case for SOA. A short-circuit to ground forces the full power supply voltage (V+ or V−) across the conducting transistor and produces a typical output current of 25mA. With ±40V power supplies, this creates an internal dissipation of 1W. This exceeds the maximum rating and is not recommended. If operation in this region is unavoidable, a heat sink is required. For further insight on SOA, consult Application Bulletin SBOA022 (available for download at www.ti.com).

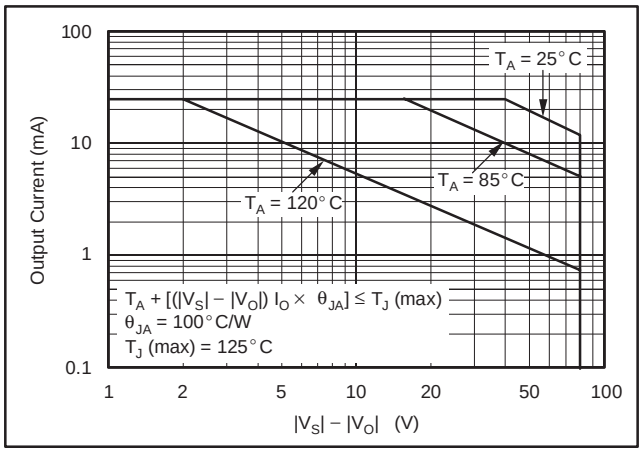


Figure 6. DIP-8 Safe Operating Area

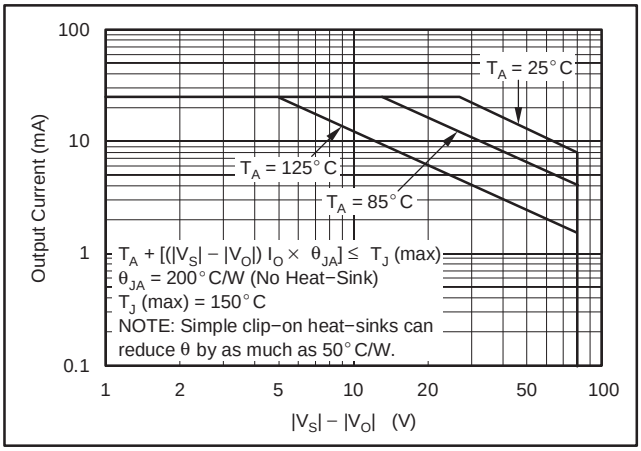


Figure 7. TO-99 Safe Operating Area

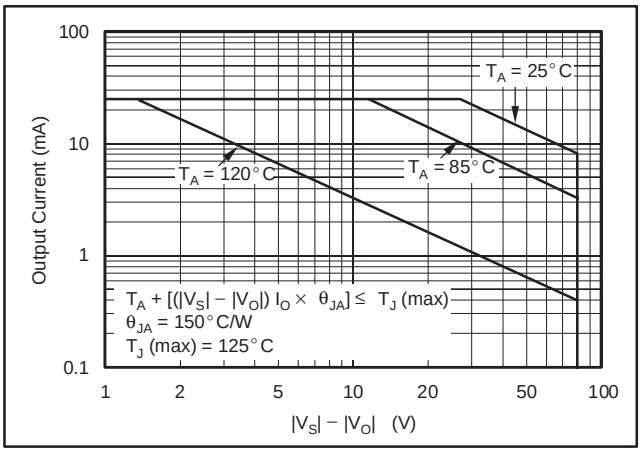


Figure 8. SO-8 (non PowerPAD) Safe Operating Area

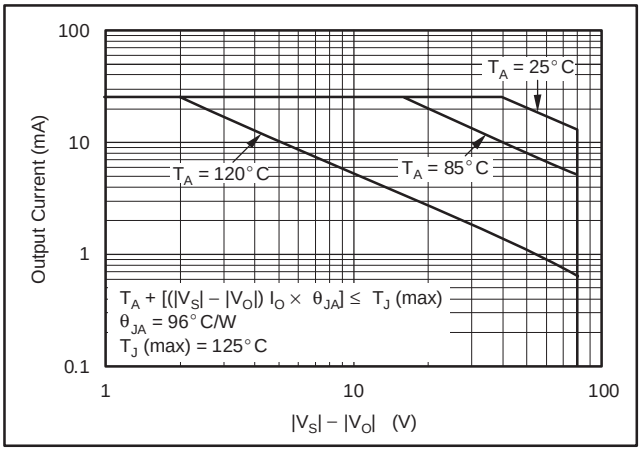


Figure 9. SO-8 PowerPAD Safe Operating Area (no heat-spreader, no airflow)

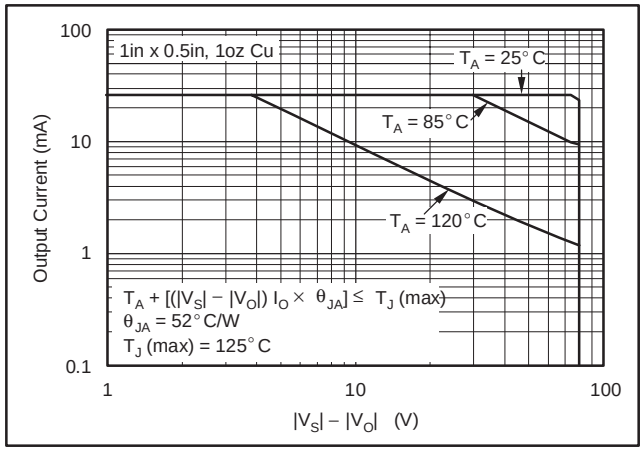


Figure 10. SO-8 PowerPAD Safe Operating Area (with heat-spreader, no airflow)

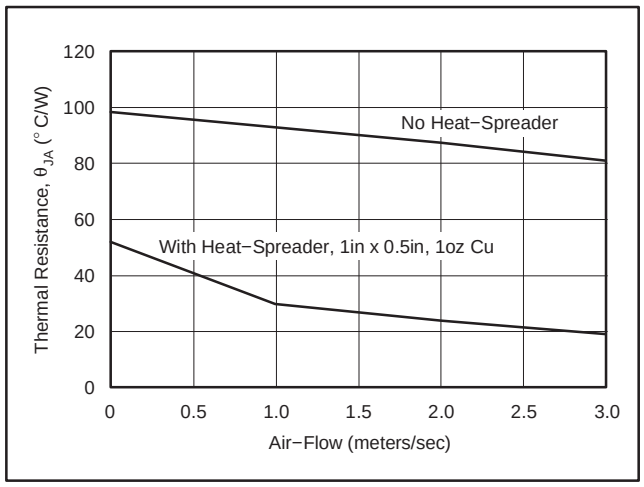


Figure 11. SO-8 PowerPAD Thermal Resistance (with and without heat-spreader)

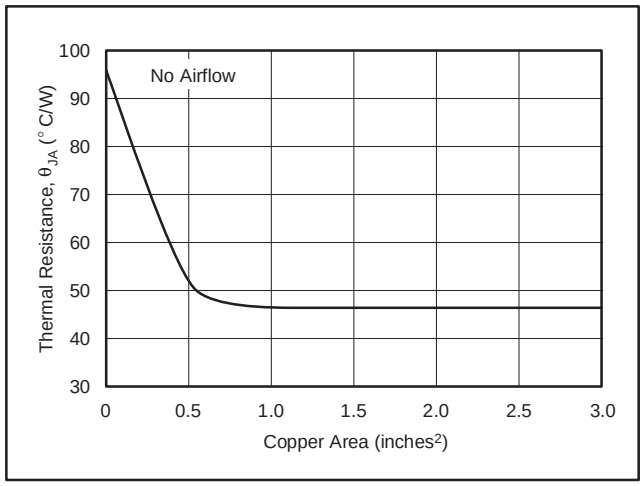


Figure 12. Thermal Resistance vs Circuit Board Copper Area

POWER DISSIPATION

Power dissipation depends on power supply, signal, and load conditions. For dc signals, power dissipation is equal to the product of the output current times the voltage across the conducting output transistor, $P_D = I_L (V_S - V_O)$. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a dc output voltage of one-half the power supply voltage. Dissipation with ac signals is lower. Application Bulletin SBOA022 explains how to calculate or measure dissipation with unusual loads or signals.

The OPA445 can supply output currents of 15mA and larger. This would present no problem for a standard op amp operating from ±15V supplies. With high supply voltages, however, internal power dissipation of the op amp can be quite large. Operation from a single power supply (or unbalanced power supplies) can produce even larger power dissipation since a large voltage is impressed across the conducting output transistor. Applications with large power dissipation may require a heat-sink.

HEAT SINKING

Power dissipated in the OPA445 will cause the junction temperature to rise. For reliable operation junction temperature should be limited to 125°C, maximum (150°C for TO-99 package). Some applications will require a heat-sink to assure that the maximum operating junction temperature is not exceeded. In addition, the junction temperature should be kept as low as possible for increased reliability. Junction temperature can be determined according to the following equation:

$$T_J = T_A + P_D \theta_{JA} \quad (1)$$

Package thermal resistance, θ_{JA}, is affected by mounting techniques and environments. Poor air circulation and use of sockets can significantly increase thermal resistance. Best thermal performance is achieved by soldering the op amp into a circuit board with wide printed circuit traces to allow greater conduction through the op amp leads. Simple clip-on heat sinks (such as a Thermalloy 2257) can reduce the thermal resistance of the TO-99 metal package by as much as 50°C/W. The SO-8 PowerPAD package will provide lower thermal resistance, especially with a simple heat-spreader—even lower with a heat-sink. For additional information on determining heat-sink requirements, consult Application Bulletin SBOA021.

PowerPAD THERMALLY-ENHANCED PACKAGE

In addition to the SO-8, DIP-8, and TO-99 packages, the OPA445 also comes in an SO-8 PowerPAD. The SO-8 PowerPAD is a standard-size SO-8 package where the exposed leadframe on the bottom of the package can be soldered directly to the PCB to create an extremely low thermal resistance. This architecture enhances the OPA445's power dissipation capability significantly and eliminates the use of bulky heatsinks and slugs traditionally used in thermal packages. This package can be easily mounted using standard PCB assembly techniques. NOTE: Since the SO-8 PowerPAD is pin-compatible with standard SO-8 packages, the OPA445 can directly replace operational amplifiers in existing sockets. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. Soldering the device to the PCB provides the necessary thermal and mechanical connection between the leadframe die pad and the PCB.

The PowerPAD package is designed so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC; see Figure 13. This design provides an extremely low thermal resistance (θ_{JC}) path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the PCB, using the PCB as a heatsink. In addition, plated-through holes (vias) provide a low thermal resistance heat flow path to the back side of the PCB.

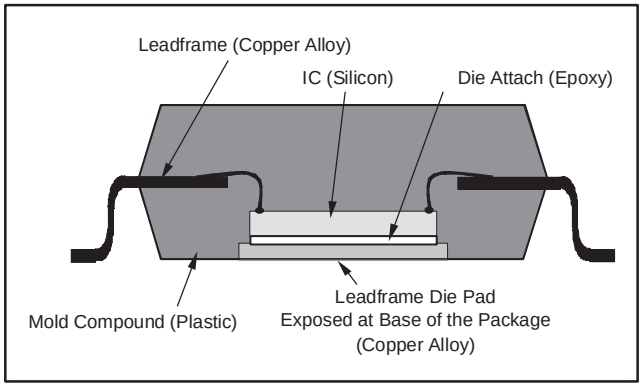


Figure 13. Section View of a PowerPAD Package

GENERAL PowerPAD LAYOUT GUIDELINES

The OPA445 is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package. This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the PCB is always required, even with applications that have low power dissipation. Follow these steps:

1. The PowerPAD must be connected to the most negative supply voltage on the device, V−.
2. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
3. Place recommended holes in the area of the thermal pad. Recommended thermal land size and thermal via patterns for the SO-8 DDA package is shown in Figure 14. These holes should be 13 mils in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow. The minimum recommended number of holes for the SO-8 PowerPAD package is five.
4. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA445 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
5. Connect all holes to the internal power plane of the correct voltage potential (V−).
6. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations, makeing the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPA445 PowerPAD package should make the connections to the internal plane with a complete connection around the entire circumference of the plated-through hole.
7. The top-side solder mask should leave the terminals of the package and the thermal pad area exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
8. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

9. With these preparatory steps in place, the PowerPAD IC is simply placed in position and run through the solder reflow operation as any standard surfacemount component. This preparation results in a properly installed part.

For detailed information on the PowerPAD package, including thermal modeling considerations and repair procedures, see technical brief SLMA002 *PowerPAD Thermally-Enhanced Package* available for download at www.ti.com.

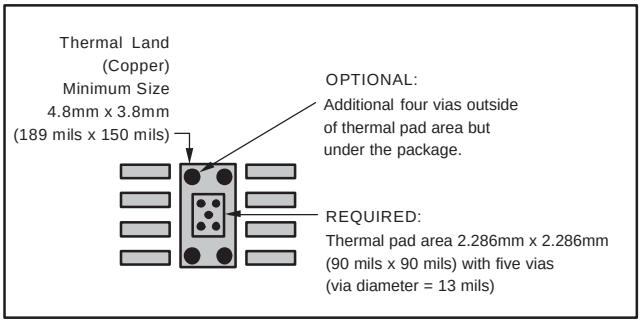


Figure 14. 8-Pin PowerPAD PCB Etch and Via Pattern

TYPICAL APPLICATIONS

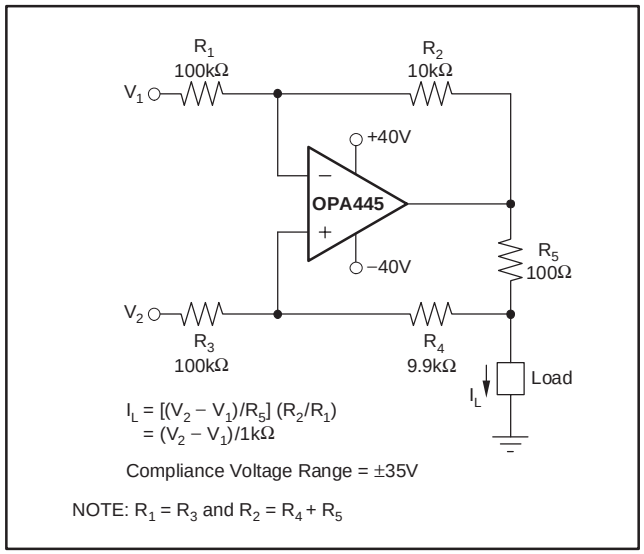


Figure 15. Voltage-to-Current Converter

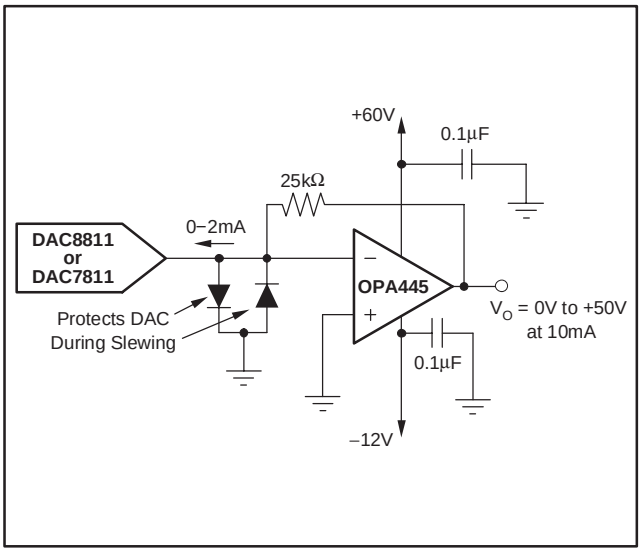


Figure 16. Programmable Voltage Source

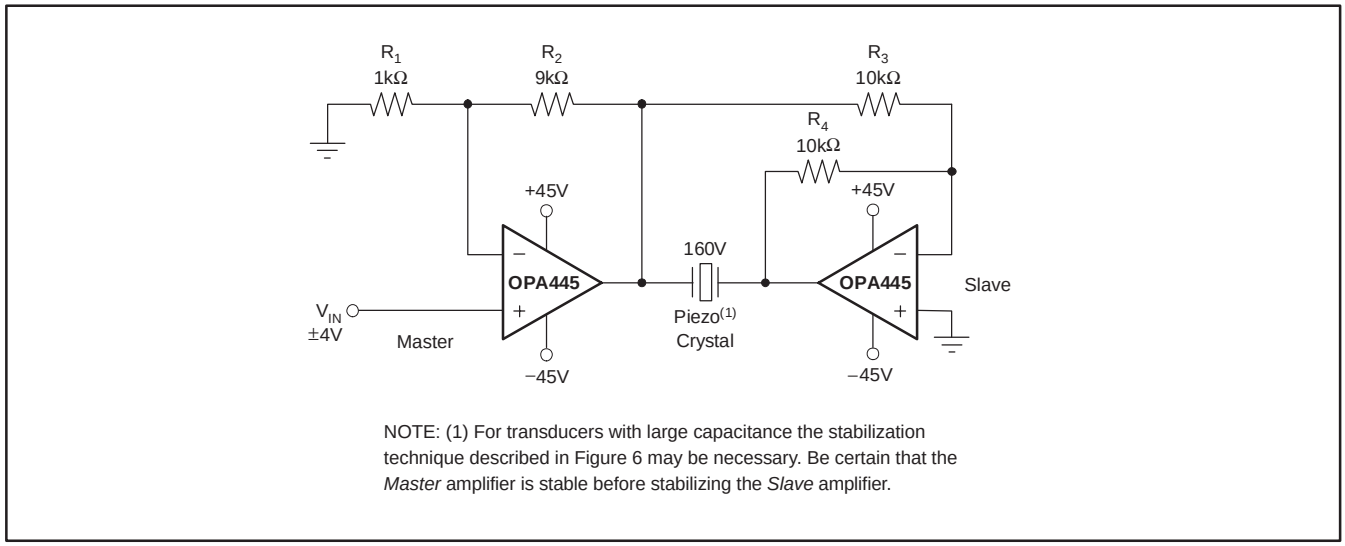


Figure 17. Bridge Circuit Doubles Voltage for Piezo Crystals

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA445ADDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	OPA445	Samples
OPA445ADDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-55 to 125	OPA445	Samples
OPA445AP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	OPA445AP	Samples
OPA445AU	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-50 to 125	OPA 445AU	Samples
OPA445AU/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	OPA 445AU	Samples
OPA445BM	ACTIVE	TO-99	LMC	8	20	RoHS & Green	AU	N / A for Pkg Type		OPA445BM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

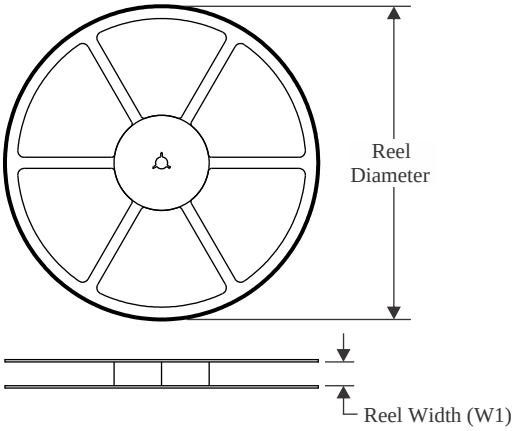
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

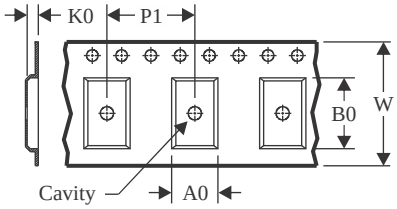
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

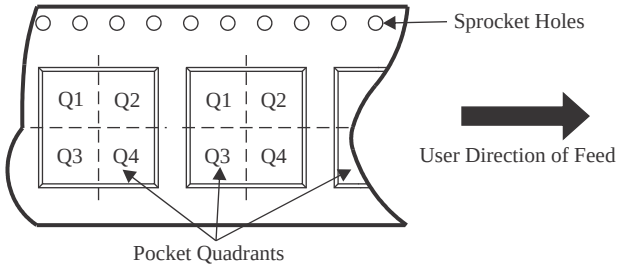


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

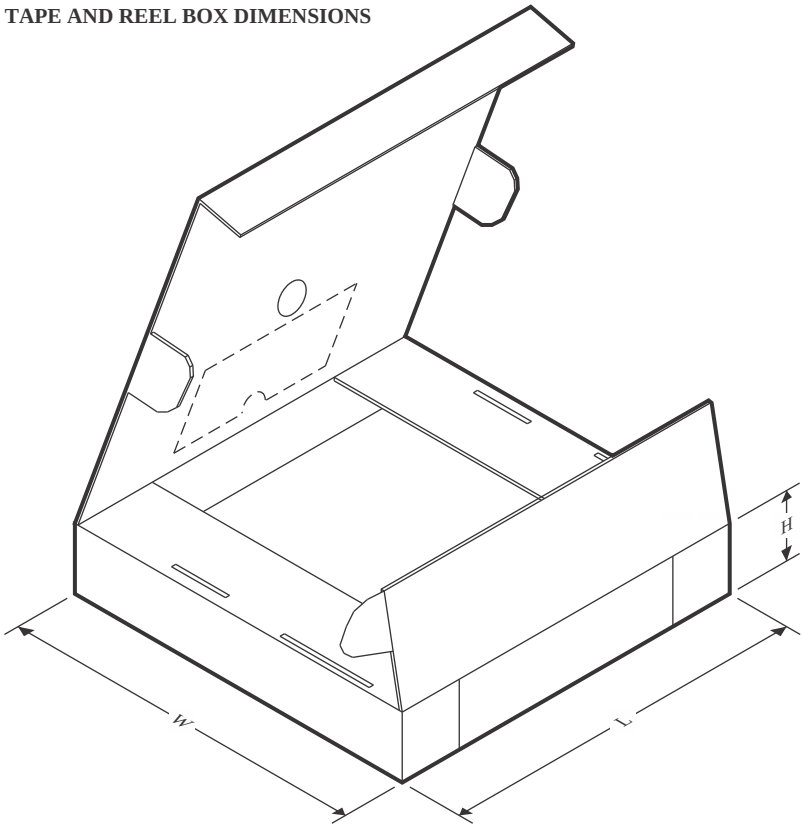
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA445ADDAR	SO PowerPAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA445AU/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

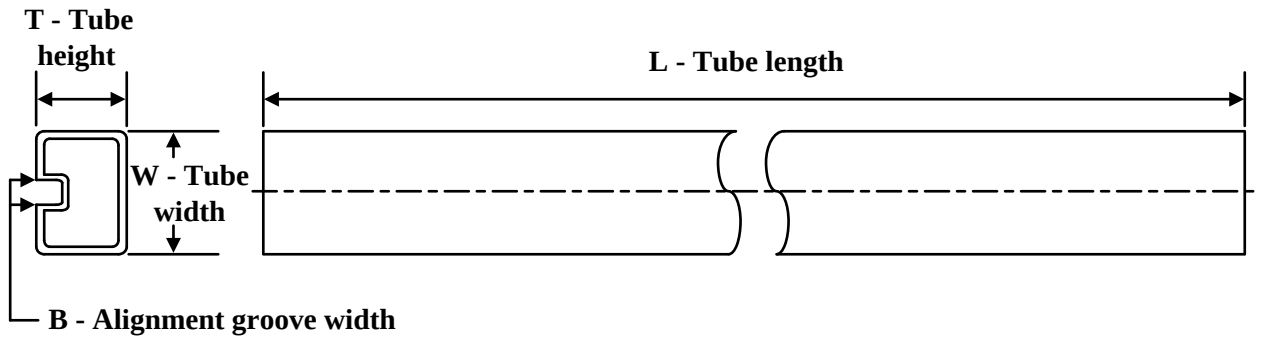
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA445ADDAR	SO PowerPAD	DDA	8	2500	356.0	356.0	35.0
OPA445AU/2K5	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

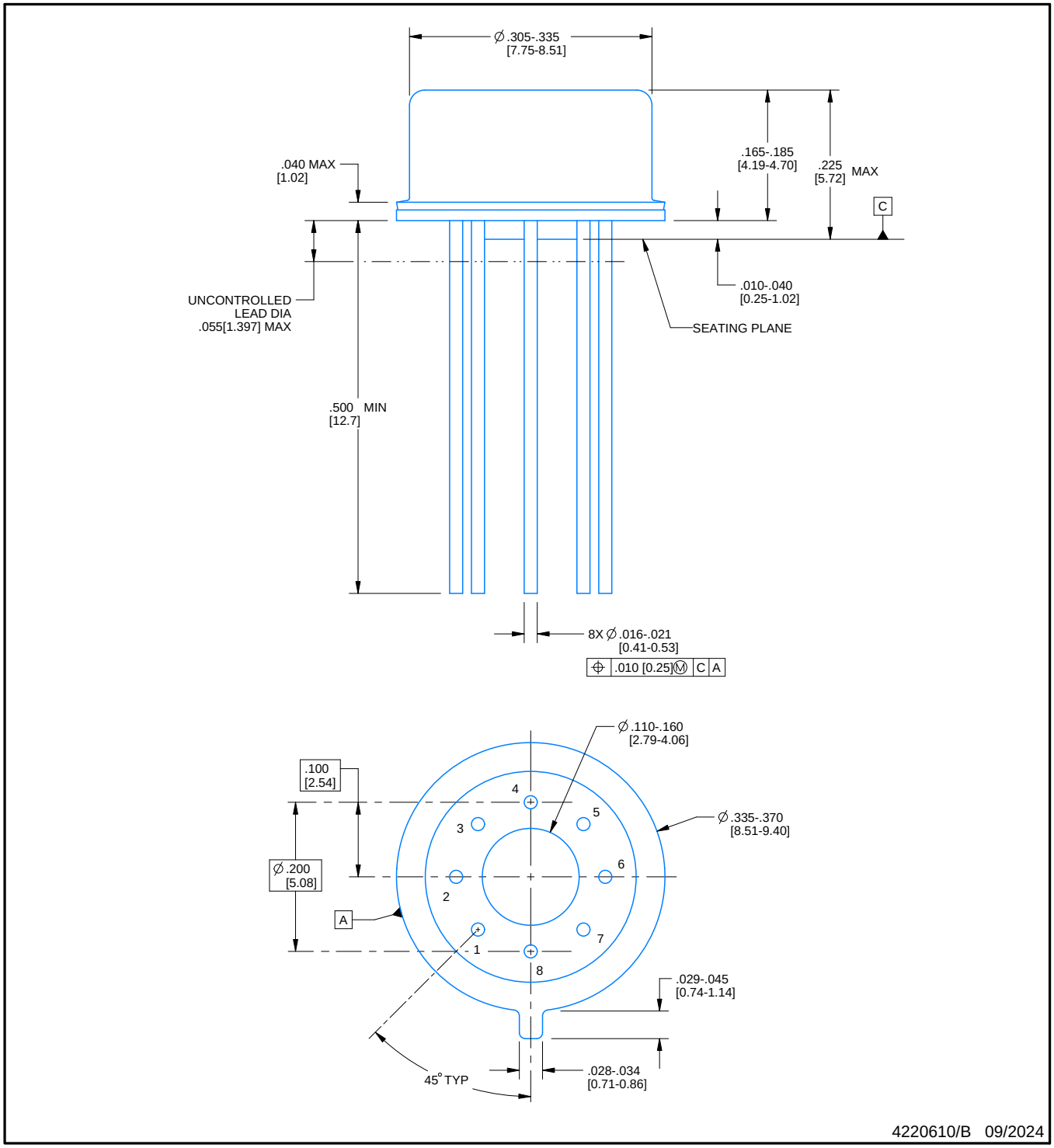
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA445ADDA	DDA	HSOIC	8	75	506.6	8	3940	4.32
OPA445AP	P	PDIP	8	50	506	13.97	11230	4.32
OPA445AU	D	SOIC	8	75	506.6	8	3940	4.32
OPA445BM	LMC	TO-CAN	8	20	532.13	21.59	889	NA

PACKAGE OUTLINE

LMC0008A

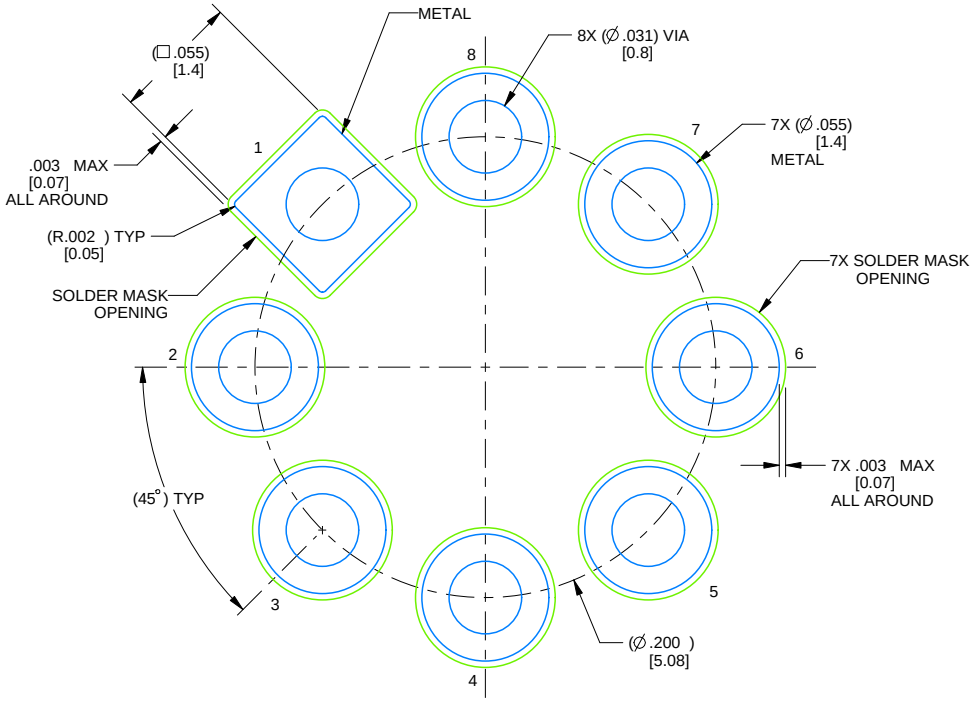
TO-CAN - 5.72 mm max height

TRANSISTOR OUTLINE



NOTES:

1. All linear dimensions are in inches [millimeters]. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pin numbers shown for reference only. Numbers may not be marked on package.
4. Reference JEDEC registration MO-002/TO-99.

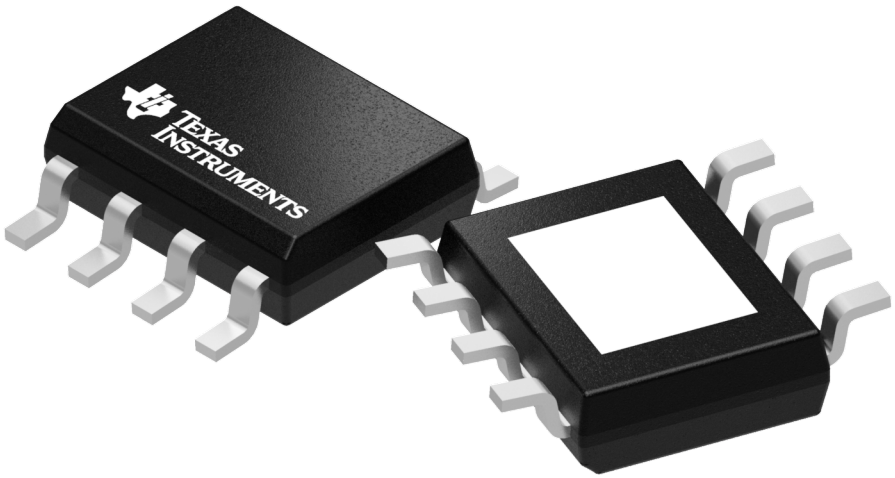


LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 12X

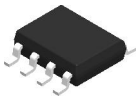
4220610/B 09/2024

DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

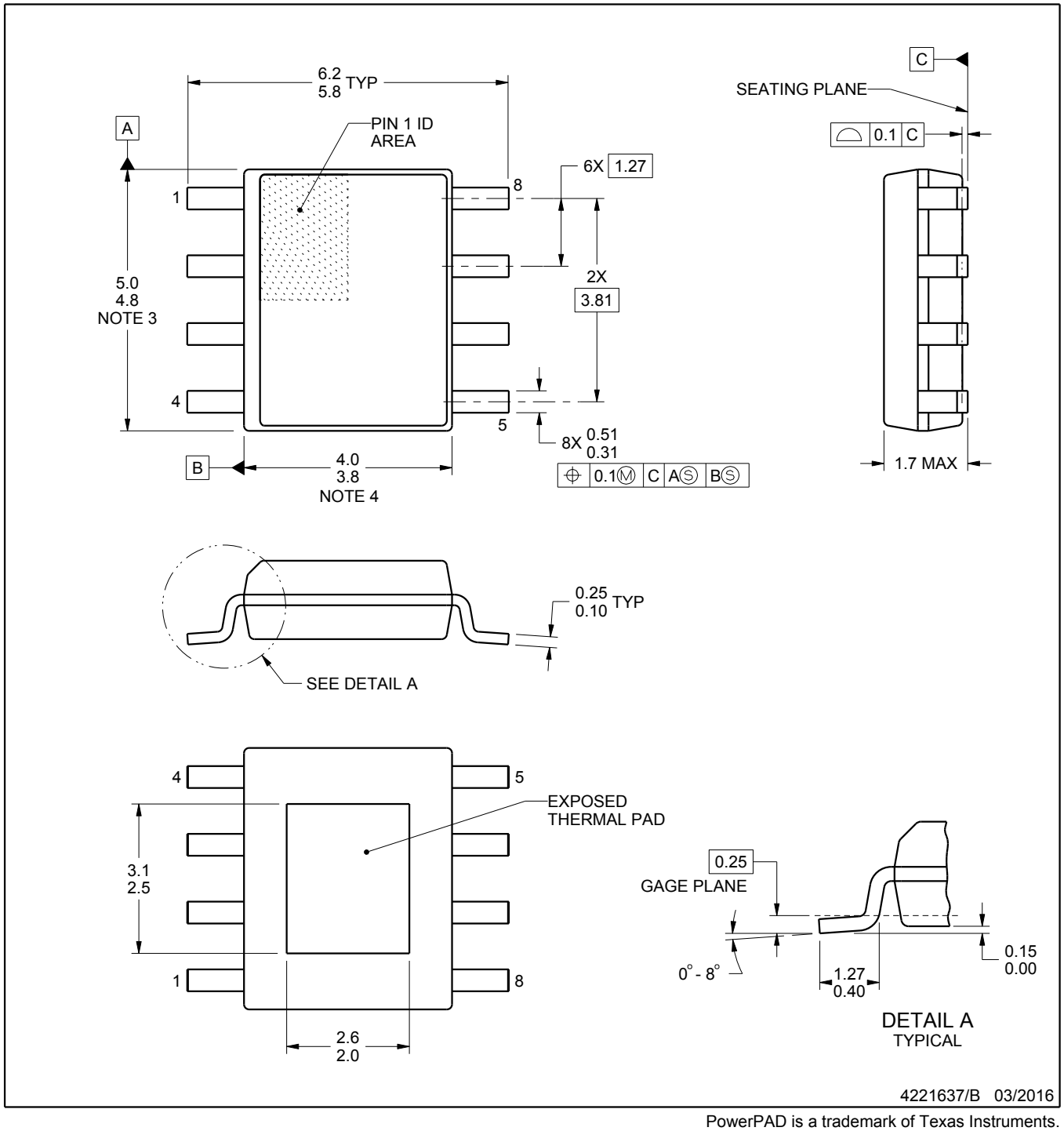


PACKAGE OUTLINE

DDA0008J

PowerPAD™ SOIC - 1.7 mm max height

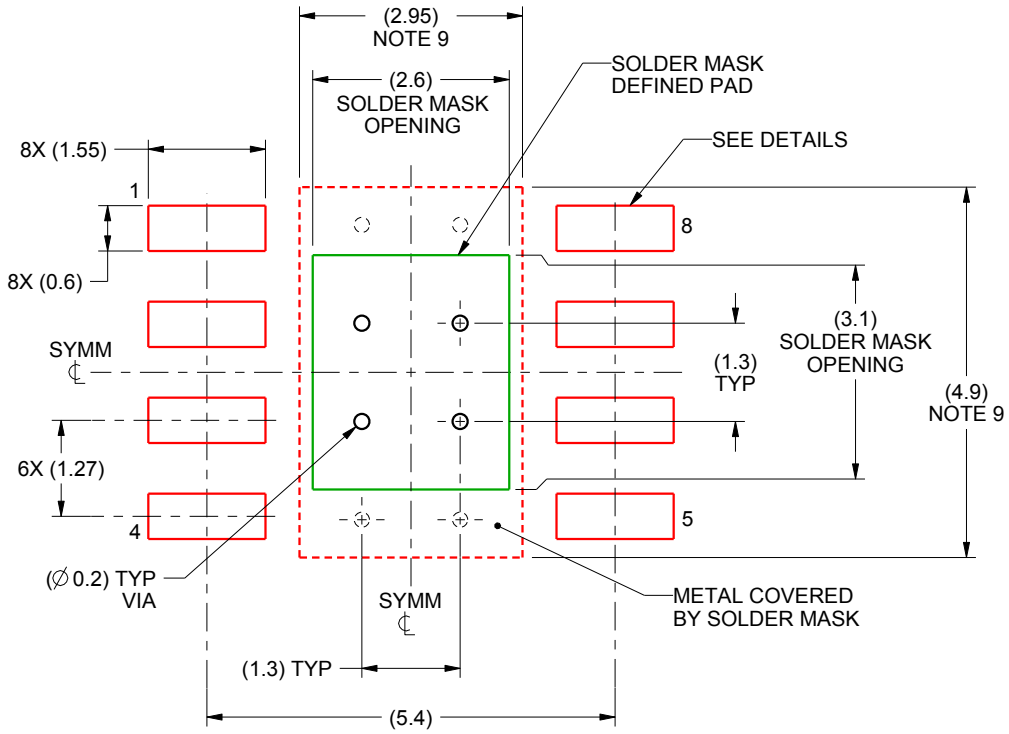
PLASTIC SMALL OUTLINE



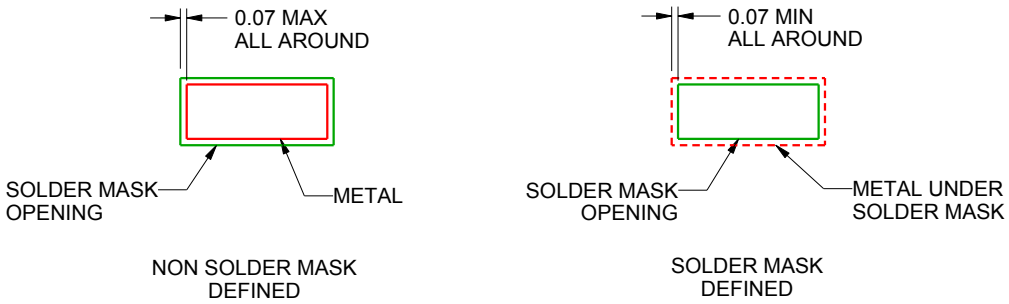
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

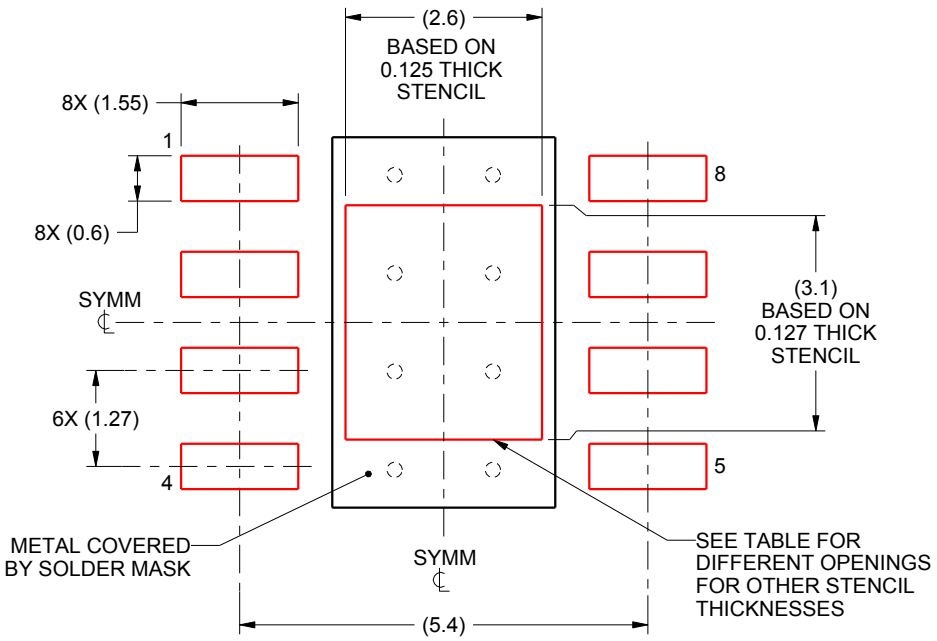


SOLDER MASK DETAILS

4221637/B 03/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



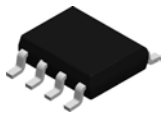
SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.47
0.125	2.6 X 3.1 (SHOWN)
0.150	2.37 X 2.83
0.175	2.20 X 2.62

4221637/B 03/2016

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

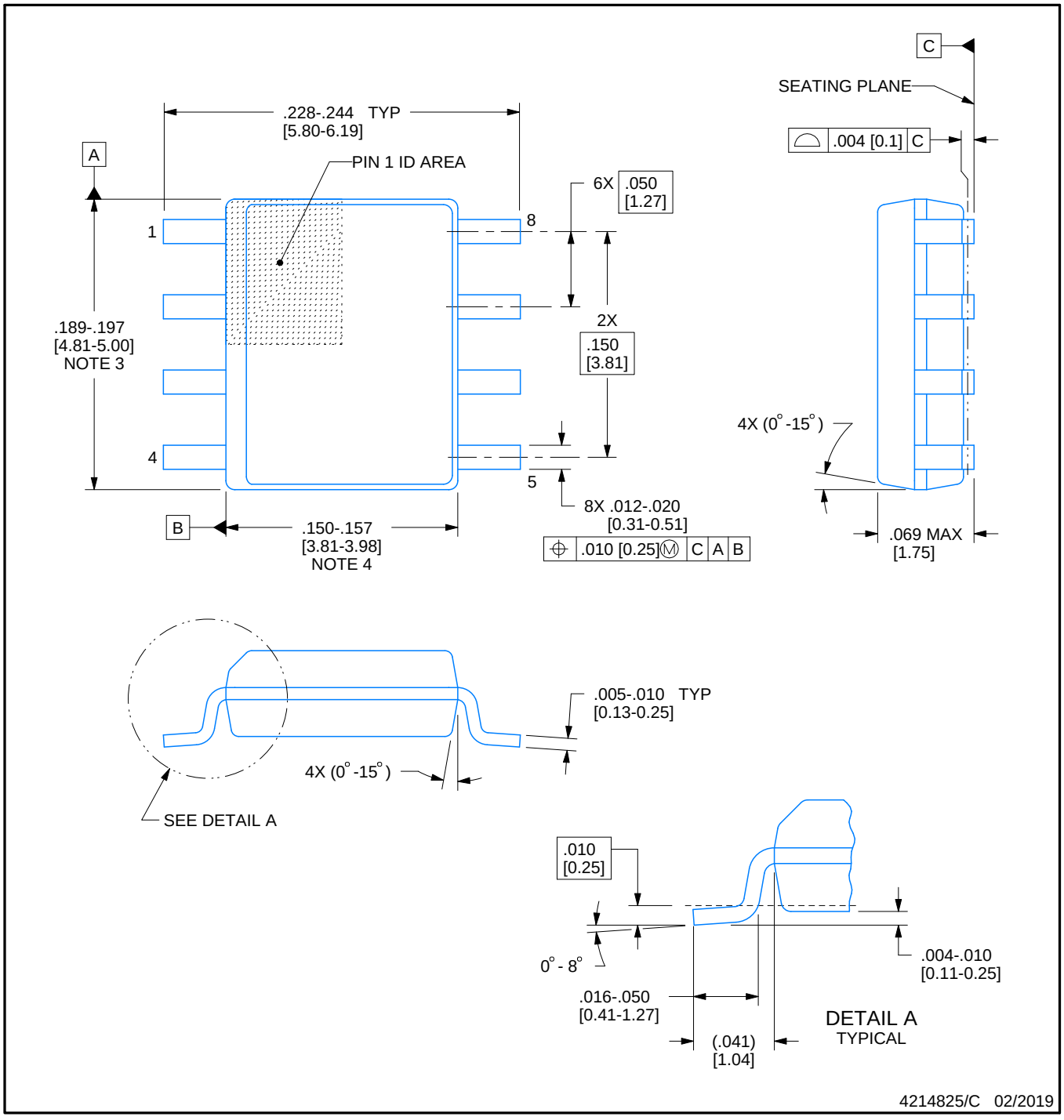


PACKAGE OUTLINE

D0008A

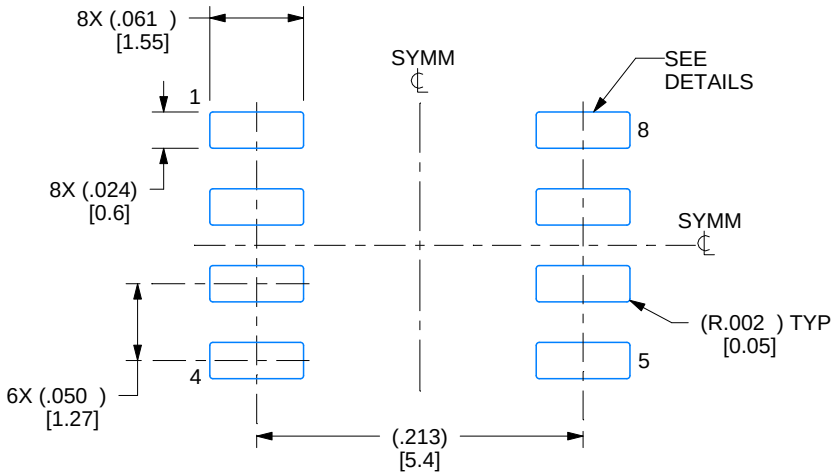
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

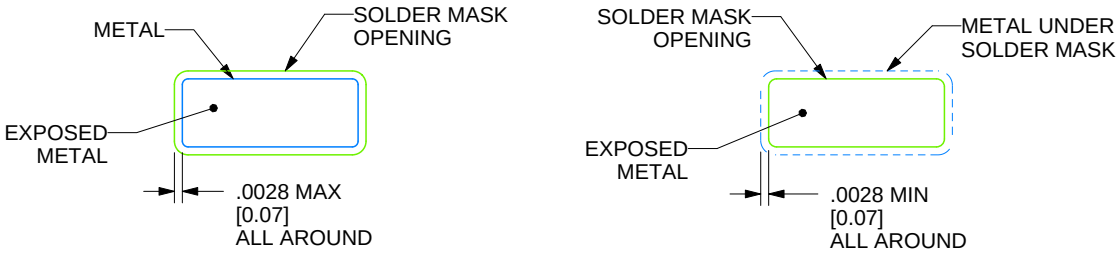


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

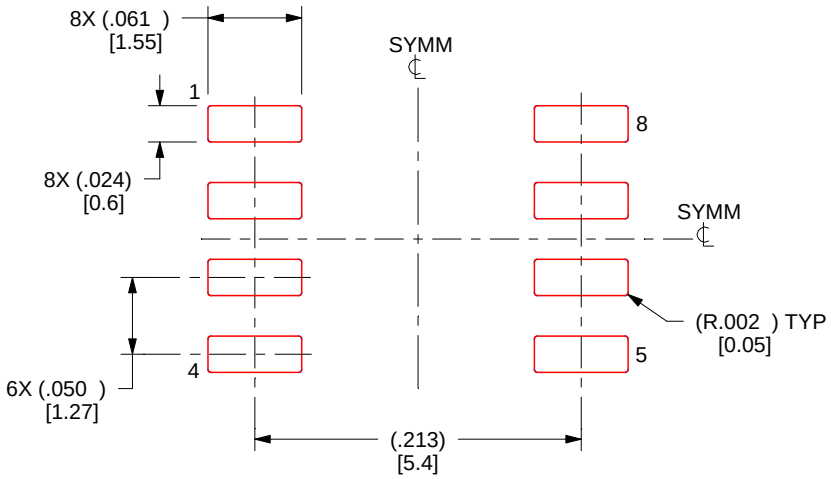
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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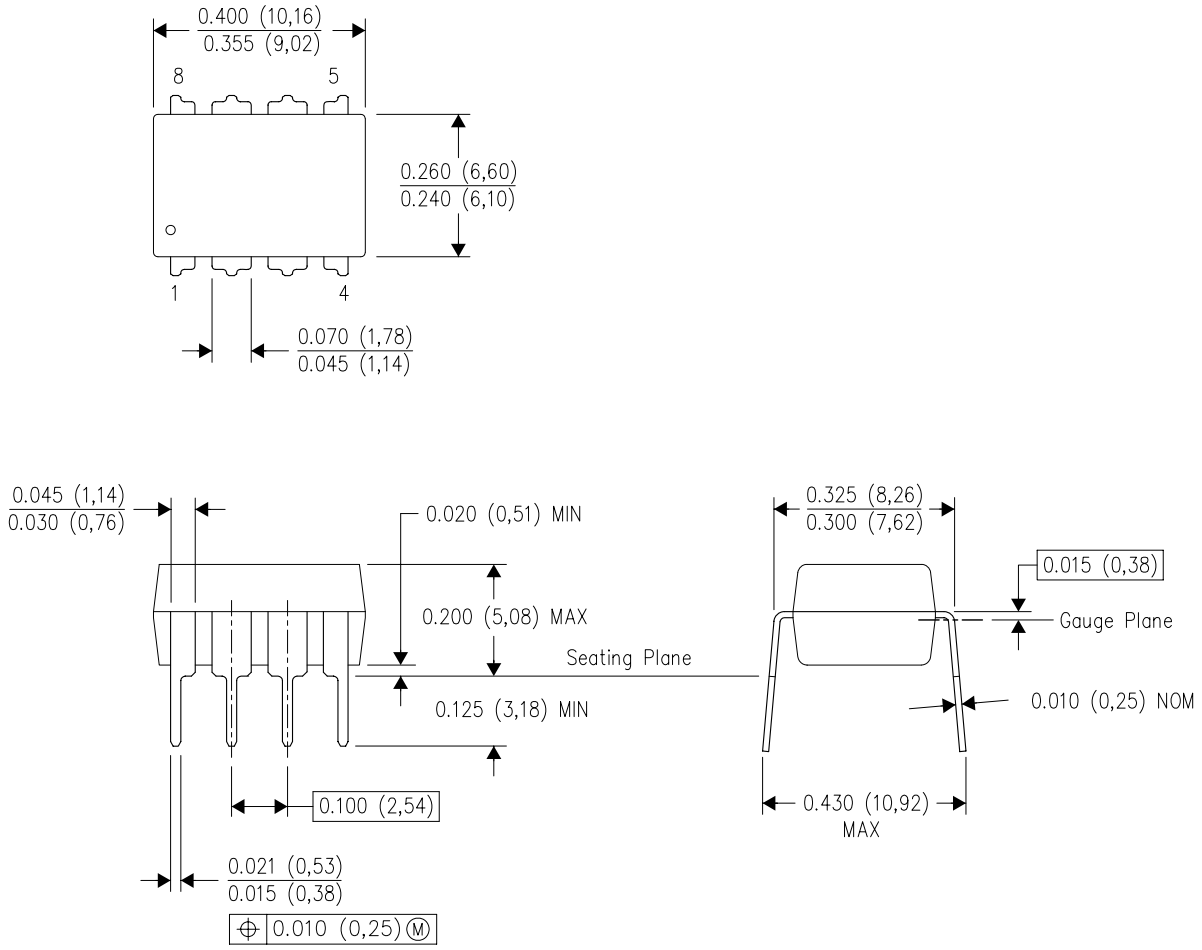
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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