Very Low-Power, Current Feedback OPERATIONAL AMPLIFIER With Disable

FEATURES

- REDUCED BANDWIDTH CHANGE VERSUS GAIN
- 150MHz BANDWIDTH G = +2
- > 90MHz BANDWIDTH TO GAIN > +10
- LOW DISTORTION: < –69dBc at 5MHz
- HIGH OUTPUT CURRENT: 110mA
- SINGLE +5V TO +12V SUPPLY OPERATION
- DUAL ±2.5V TO ±6V SUPPLY OPERATION
- LOW SUPPLY CURRENT: 0.94mA
- LOW SHUTDOWN CURRENT: 100µA

APPLICATIONS

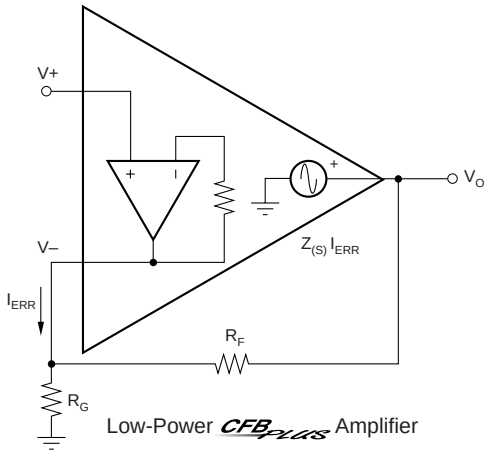
- LOW POWER BROADCAST VIDEO DRIVERS
- EQUALIZING FILTERS
- SAW FILTER HIGH GAIN POST AMPLIFIERS
- SHORT LOOP ADSL CO DRIVERS
- MULTICHANNEL SUMMING AMPLIFIERS
- PROFESSIONAL CAMERAS
- ADC INPUT DRIVERS

DESCRIPTION

The OPA683 provides a new level of performance in very low-power, wideband, current feedback amplifiers. This CFB$_{plus}$ amplifier is among the first to use an internally closed-loop input buffer stage that enhances performance significantly over earlier low-power CFB amplifiers. While retaining the benefits of very low power operation, this new architecture provides many of the advantages of a more ideal CFB amplifier. The closed-loop input stage buffer gives a very low and linearized impedance path at the inverting input to sense the feedback error current. This improved inverting input impedance gives exceptional bandwidth retention to much higher gains and improved harmonic distortion over earlier solutions limited by inverting input linearity. Beyond simple high gain applications, the OPA683 CFB$_{plus}$ amplifier can allow the gain setting element to be set with considerable freedom from amplifier bandwidth interaction. This allows frequency response peaking elements to be added, multiple input inverting summing circuits to have greater bandwidth, and low-power line drivers to meet the demanding requirements of studio cameras and broadcast video.

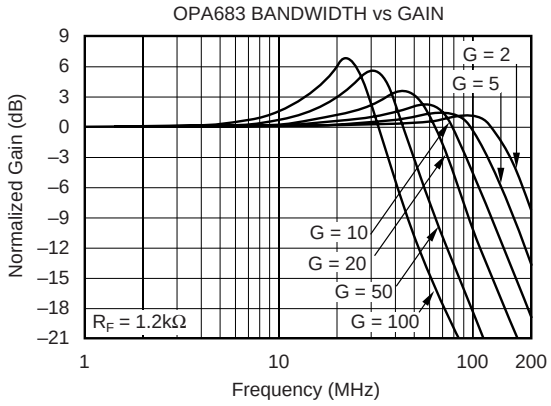
The output capability for the OPA683 also sets a new mark in performance for very low-power current feedback amplifiers. Delivering a full ±4V$_{PP}$ swing on ±5V supplies, the OPA683 also has the output current to support this swing into a 100Ω load. This minimal output headroom requirement is complemented by a similar 1.2V input stage headroom giving exceptional capability for single +5V operation.

The OPA683's low 0.94mA supply current is precisely trimmed at 25°C. This trim, along with low shift over temperature and supply voltage, gives a very robust design over a wide range of operating conditions. System power may be further reduced by using the optional disable control pin. Leaving this disable pin open, or holding it HIGH, gives normal operation. If pulled LOW, the OPA683 supply current drops to less than 100µA while the I/O pins go to a high impedance state.



Low-Power CFB$_{PLUS}$ Amplifier

U.S. Patent No. 6,724,260



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	$\pm 6.5V_{DC}$
Internal Power Dissipation	See Thermal Information
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: ID, IDBV	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+175°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

OPA683 RELATED PRODUCTS

SINGLES	DUALS	TRIPLES	QUADS	FEATURES
OPA684	OPA2683	OPA3684	OPA4684	Low-Power CFB_{plus}
OPA691	OPA2691	OPA3691	—	High Slew Rate CFB
OPA685	—	—	—	> 500MHz CFB

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

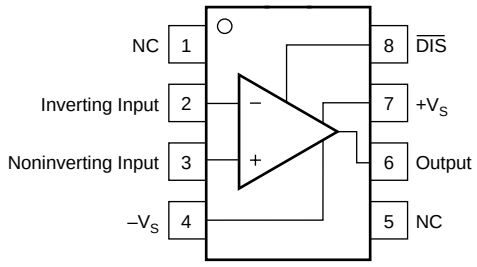
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA683	SO-8	D	–40°C to +85°C	OPA683D	OPA683ID	Rails,100
"	"	"	"	"	OPA683IDR	Tape and Reel, 2500
OPA683	SOT23-6	DBV	–40°C to +85°C	A83	OPA683IDBVT	Tape and Reel, 250
"	"	"	"	"	OPA683IDBVR	Tape and Reel, 3000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this document, or see the TI website at www.ti.com.

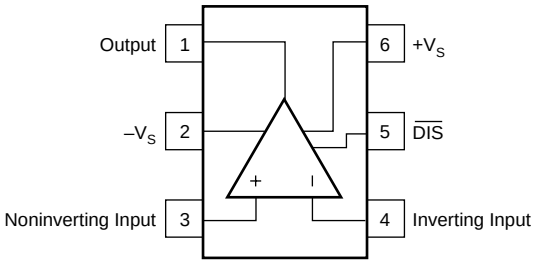
PIN CONFIGURATION

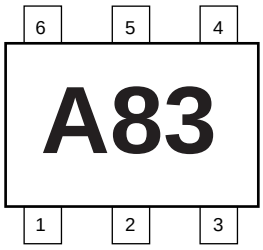
Top View **SO-8**



NC = No Connection

Top View **SOT23-6**





Pin Orientation/Package Marking

ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$

Boldface limits are tested at **+25°C.**

$R_F = 1.2k\Omega$, $R_L = 1k\Omega$, and G = +2 (see Figure 1 for AC performance only), unless otherwise noted.

PARAMETER	CONDITIONS	OPA683ID, IDBV						TEST LEVEL[3]
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[1]	0°C to 70°C[2]	–40°C to +85°C[2]	UNITS	MIN/ MAX	
AC PERFORMANCE (See Figure 1)								
Small-Signal Bandwidth ($V_O = 0.5V_{PP}$)	G = +1, $R_F = 1.2k\Omega$	200				MHz	typ	C
	G = +2, $R_F = 1.2k\Omega$	150	124	121	117	MHz	min	B
	G = +5, $R_F = 1.2k\Omega$	121				MHz	typ	C
	G = +10, $R_F = 1.2k\Omega$	94				MHz	typ	B
	G = +20, $R_F = 1.2k\Omega$	72				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, $V_O = 0.5V_{PP}$, $R_F = 1.2k\Omega$	37	15	14	14	MHz	min	B
Peaking at a Gain of +1	$R_F = 1.2k\Omega$, $V_O = 0.5V_{PP}$	1.8	6.5	7.7	8.0	dB	max	B
Large-Signal Bandwidth	G = +2, $V_O = 4V_{PP}$	63				MHz	typ	C
Slew Rate	G = –1, V_O = 4V Step (see Figure 2)	540	450	450	430	V/µs	min	B
	G = +2, V_O = 4V Step	400	345	338	336	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	4.6				ns	typ	C
	G = +2, V_O = 4VStep	7.8				ns	typ	C
Harmonic Distortion	G = +2, f = 5MHz, $V_O = 2V_{PP}$							
2nd-Harmonic	$R_L = 100\Omega$	–63	–54	–54	–54	dBc	max	B
	$R_L \geq 1k\Omega$	–65	–55	–55	–55	dBc	max	B
3rd-Harmonic	$R_L = 100\Omega$	–67	–62	–62	–62	dBc	max	B
	$R_L \geq 1k\Omega$	–74	–67	–66	–66	dBc	max	B
Input Voltage Noise	f > 1MHz	4.4	5.0	5.5	5.8	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	5.1	5.8	6.4	6.7	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	11.6	11.9	12.3	12.4	pA/√Hz	max	B
Differential Gain	G = +2, NTSC, $V_O = 1.4V_P$, $R_L = 150\Omega$	0.06				%	typ	C
Differential Phase	G = +2, NTSC, $V_O = 1.4V_P$, $R_L = 150\Omega$	0.03				deg	typ	C
DC PERFORMANCE[4]								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = 0V, $R_L = 1k\Omega$	**700**	300	270	250	kΩ	min	A
Input Offset Voltage	V_{CM} = 0V	**±1.5**	±3.5	±4.1	±4.3	mV	max	A
Average Offset Voltage Drift	V_{CM} = 0V			±12	±12	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = 0V	**±2.0**	±4.0	±4.6	±4.8	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = 0V			±15	±15	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = 0V	**±3.0**	±10	±11	±11.5	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = 0V			±20	±20	nA°/C	max	B
INPUT								
Common-Mode Input Range[5] (CMIR)		**±3.75**	±3.65	±3.65	±3.60	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = 0V	**60**	53	52	52	dB	min	A
Noninverting Input Impedance		50 || 2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open-Loop, DC	4.5				Ω	typ	C
OUTPUT								
Voltage Output Swing	1kΩ Load	**±4.1**	±4.0	±4.0	±3.9	V	min	A
Current Output, Sourcing	V_O = 0	**150**	130	125	120	mA	min	A
Current Output, Sinking	V_O = 0	**–110**	–100	–95	–90	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.007				Ω	typ	C
DISABLE (Disabled LOW)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0	–100	–150	–170	–180	µA	typ	C
Disable Time	V_{IN} = +1, See Figure 1	60				ms	typ	C
Enable Time	V_{IN} = +1, See Figure 1	40				ns	typ	C
Off Isolation	G = +2, 5MHz	70				dB	typ	C
Output Capacitance in Disable		1.7				pF	typ	C
Turn On Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0	±70				mV	typ	C
Turn Off Glitch	G = +2, $R_L = 150\Omega$, V_{IN} = 0	±20				mV	typ	C
Enable Voltage		**3.4**	3.5	3.6	3.7	V	min	A
Disable Voltage		**1.8**	1.7	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0V	**80**	120	130	135	µA	max	A
POWER SUPPLY								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage Range			±6	±6	±6	V	max	A
Minimum Operating Voltage Range		±1.4				V	min	C
Max Quiescent Current	$V_S = \pm 5V$	**0.94**	1.03	1.04	1.05	mA	max	A
Min Quiescent Current	$V_S = \pm 5V$	**0.94**	0.85	0.80	0.77	mA	min	A
Power-Supply Rejection Ratio (–PSRR)	Input Referred	**62**	55	54	54	dB	typ	A
TEMPERATURE RANGE								
Specification: D, DBV		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
DBV SOT-23-6		150				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for 25°C tested specifications. (2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +2°C at high temperature limit for over temperature tested specifications. (3) Test levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMR at ± CMIR limits.

ELECTRICAL CHARACTERISTICS: V_S = +5V

Boldface limits are tested at **+25°C.**

R_F = 1.4kΩ, R_L = 1kΩ, and G = +2 (see Figure 3 for AC performance only), unless otherwise noted.

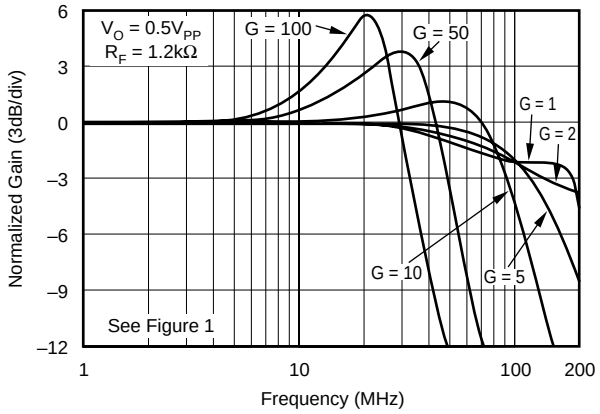
PARAMETER	CONDITIONS	OPA683ID, IDBV						
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C[1]	0°C to 70°C[2]	–40°C to +85°C[2]	UNITS	MIN/ MAX	TEST LEVEL[3]
AC PERFORMANCE (See Figure 3)								
Small-Signal Bandwidth (V_O = 0.2V_{PP})	G = +1, R_F = 1.4kΩ	145				MHz	typ	
	G = +2, R_F = 1.4kΩ	119	96	92	90	MHz	min	B
	G = +5, R_F = 1.4kΩ	95				MHz	typ	C
	G = +10, R_F = 1.4kΩ	87				MHz	typ	C
	G = +20, R_F = 1.4kΩ	60				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	G = +2, V_O < 0.5V_{PP}, R_F = 1.2kΩ	14	9	8	8	MHz	min	B
Peaking at a Gain of +1	R_F = 1.4kΩ, V_O < 0.5V_{PP}	1	6	8	8	dB	max	B
Large-Signal Bandwidth	G = +2, V_O = 2V_{PP}	70				MHz	typ	C
Slew Rate	G = +2, V_O = 2V Step	210	180	175	170	V/µs	min	B
Rise-and-Fall Time	G = +2, V_O = 0.5V Step	5.9				ns	typ	C
	G = +2, V_O = 2VStep	7.8				ns	typ	C
Harmonic Distortion	G = 2, f = 5MHz, V_O = 2V_{PP}							
2nd-Harmonic	R_L = 100Ω to V_S/2	–60	–54	–53	–53	dBc	max	B
	R_L ≥ 1kΩ to V_S/2	–66	–55	–55	–55	dBc	max	B
3rd-Harmonic	R_L = 100Ω to V_S/2	–59	–58	–58	–58	dBc	max	B
	R_L ≥ 1kΩ to V_S/2	–63	–57	–56	–56	dBc	max	B
Input Voltage Noise	f > 1MHz	4.4	5.0	5.5	5.8	nV/√Hz	max	B
Noninverting Input Current Noise	f > 1MHz	5.1	5.8	6.4	6.7	pA/√Hz	max	B
Inverting Input Current Noise	f > 1MHz	11.6	11.9	12.3	12.4	pA/√Hz	max	B
Differential Gain	G = +2, NTSC, V_O = 1.4V_P, R_L = 150Ω	0.24				%	typ	C
Differential Phase	G = +2, NTSC, V_O = 1.4V_P, R_L = 150Ω	0.19				deg	typ	C
DC PERFORMANCE[4]								
Open-Loop Transimpedance Gain (Z_{OL})	V_O = V_S/2, R_L = 1kΩ to V_S/2	**700**	300	270	250	kΩ	min	A
Input Offset Voltage	V_{CM} = V_S/2	**±1.0**	±3.0	±3.6	±3.8	mV	max	A
Average Offset Voltage Drift	V_{CM} = V_S/2			±12	±12	µV/°C	max	B
Noninverting Input Bias Current	V_{CM} = V_S/2	**±2**	±4	±4.6	±4.8	µA	max	A
Average Noninverting Input Bias Current Drift	V_{CM} = V_S/2			±12	±12	nA/°C	max	B
Inverting Input Bias Current	V_{CM} = V_S/2	**±3**	±8	±8.7	±8.9	µA	max	A
Average Inverting Input Bias Current Drift	V_{CM} = V_S/2			±15	±15	nA°/C	max	B
INPUT								
Least Positive Input Voltage[5]		**1.1**	1.25	1.29	1.34	V	max	A
Most Positive Input Voltage[5]		**3.9**	3.75	3.73	3.67	V	min	A
Common-Mode Rejection Ratio (CMRR)	V_{CM} = V_S/2	**58**	51	50	50	dB	min	A
Noninverting Input Impedance		50 || 2				kΩ || pF	typ	C
Inverting Input Resistance (R_I)	Open-Loop	4.8				Ω	typ	C
OUTPUT								
Most Positive Output Voltage	R_L = 1kΩ to V_S/2	**4.2**	4.1	4.1	4.0	V	min	A
Least Positive Output Voltage	R_L = 1kΩ to V_S/2	**0.8**	0.9	0.9	1.00		min	A
Current Output, Sourcing	V_O = V_S/2	**80**	65	63	58	mA	min	A
Current Output, Sinking	V_O = V_S/2	**70**	52	50	45	mA	min	A
Closed-Loop Output Impedance	G = +2, f = 100kHz	0.009				Ω	typ	C
DISABLE (Disabled LOW)								
Power-Down Supply Current (+V_S)	$V_{\overline{DIS}}$ = 0	100				µA	typ	C
Off Isolation	G = +2, 5MHz	70				dB	typ	C
Output Capacitance in Disable		1.7				pF	typ	C
Turn On Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2	±70				mV	typ	C
Turn Off Glitch	G = +2, R_L = 150Ω, V_{IN} = V_S/2	±20				mV	typ	C
Enable Voltage		**3.4**	3.5	3.6	3.7	V	min	A
Disable Voltage		**1.8**	1.7	1.6	1.5	V	max	A
Control Pin Input Bias Current ($\overline{DIS}$)	$V_{\overline{DIS}}$ = 0V	**80**	120	130	135	µA	max	A
POWER SUPPLY								
Specified Single-Supply Operating Voltage		5				V	typ	C
Max Single-Supply Operating Voltage			12	12	12	V	max	A
Min Single-Supply Operating Voltage		2.8				V	min	C
Max Quiescent Current	V_S = +5V	**0.82**	0.91	0.91	0.91	mA	max	A
Min Quiescent Current	V_S = +5V	**0.82**	0.71	0.69	0.67	mA	min	A
Power-Supply Rejection Ratio (+PSRR)	Input Referred	65				dB	typ	C
TEMPERATURE RANGE								
Specification: D, DBV		–40 to +85				°C	typ	C
Thermal Resistance, θ_{JA}	Junction-to-Ambient							
D SO-8		125				°C/W	typ	C
DBV SOT-23-6		150				°C/W	typ	C

NOTES: (1) Junction temperature = ambient for 25°C tested specifications. (2) Junction temperature = ambient at low temperature limit: junction temperature = ambient +2°C at high temperature limit for over temperature tested specifications. (3) Test levels: (A) 100% tested at 25°C. Over temperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information. (4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage. (5) Tested < 3dB below minimum specified CMR at ± CMIR limits.

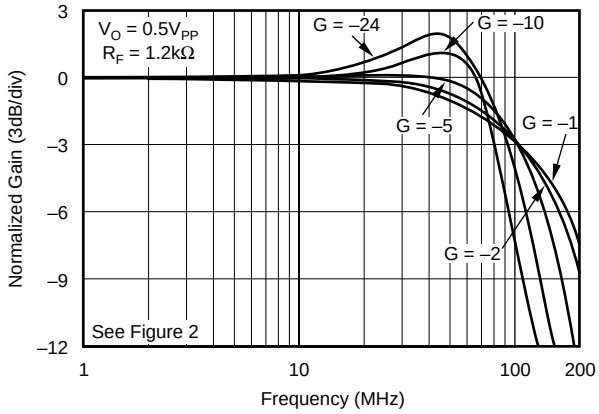
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$

$T_A = 25°C$, $R_F = 1.2k\Omega$, $R_L = 1k\Omega$, and G = +2 (see Figure 1 for AC performance only), unless otherwise noted.

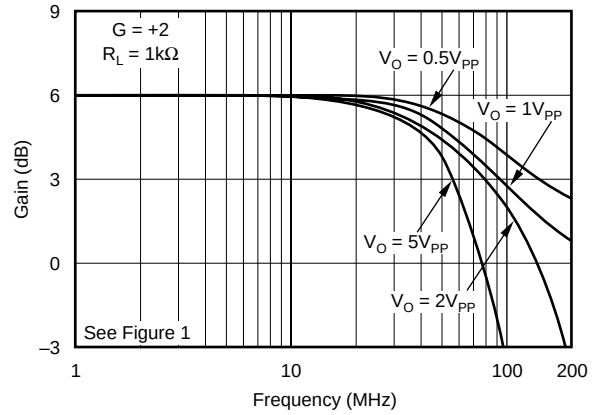
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



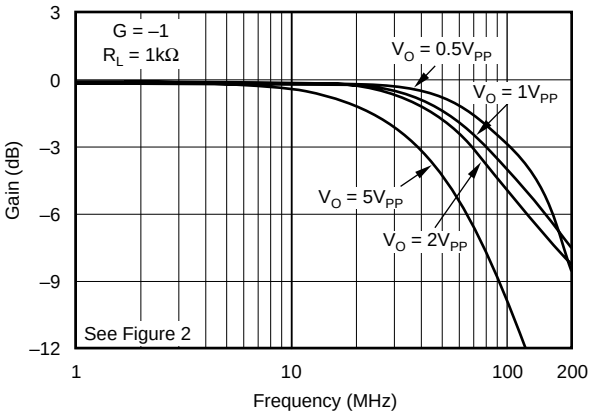
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



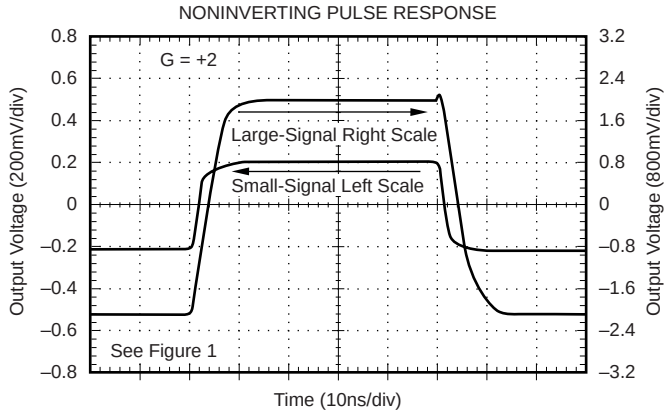
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



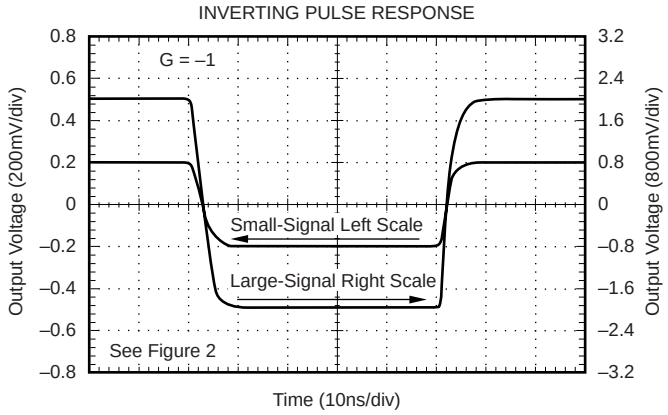
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



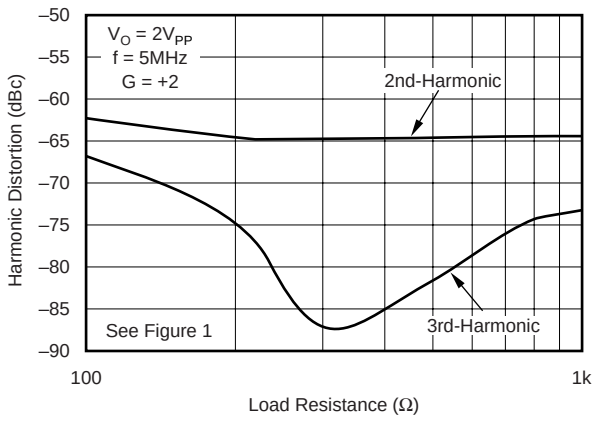
INVERTING PULSE RESPONSE



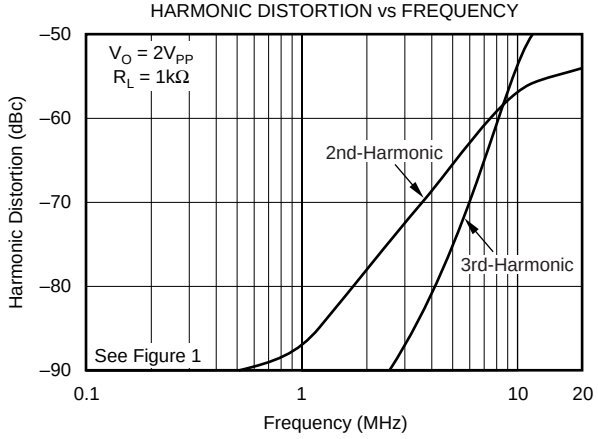
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

$T_A = 25°C$, $R_F = 1.2k\Omega$, $R_L = 1k\Omega$, and G = +2 (see Figure 1 for AC performance only), unless otherwise noted.

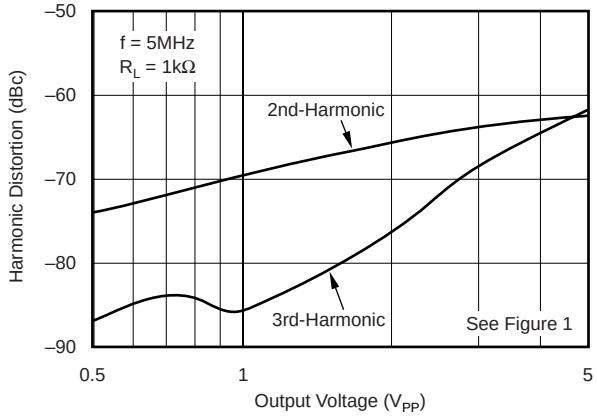
HARMONIC DISTORTION vs LOAD RESISTANCE



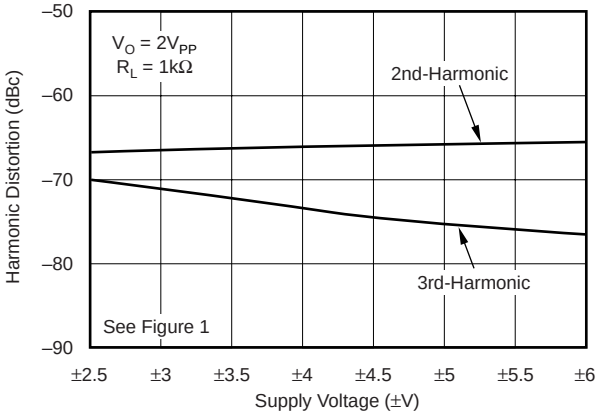
HARMONIC DISTORTION vs FREQUENCY



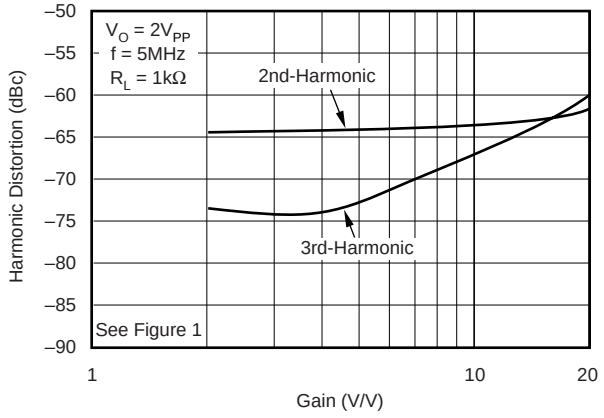
HARMONIC DISTORTION vs OUTPUT VOLTAGE



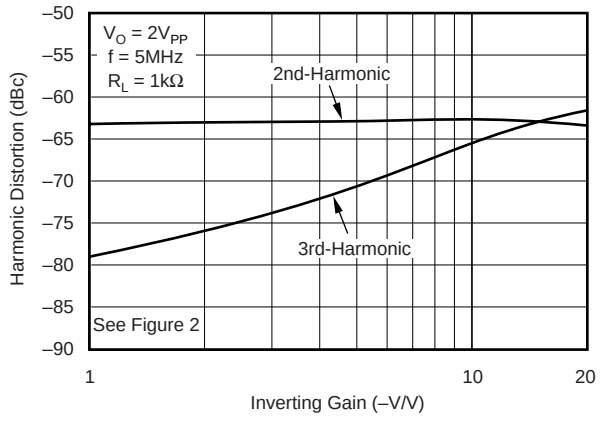
5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE



HARMONIC DISTORTION vs NONINVERTING GAIN



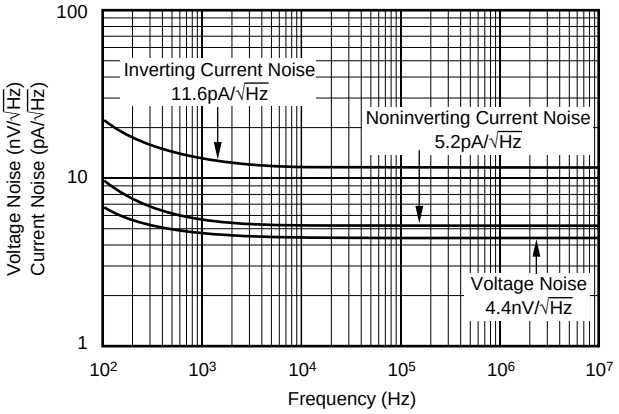
HARMONIC DISTORTION vs INVERTING GAIN



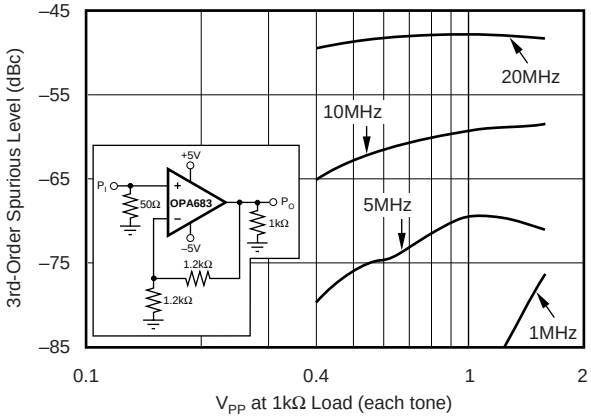
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

$T_A = 25°C$, $R_F = 1.2k\Omega$, $R_L = 1k\Omega$, and G = +2 (see Figure 1 for AC performance only), unless otherwise noted.

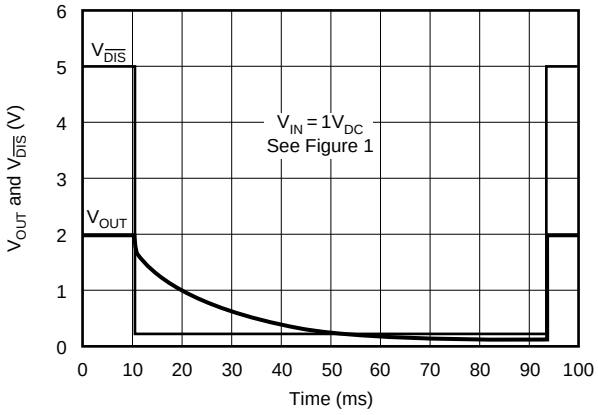
INPUT VOLTAGE AND CURRENT NOISE DENSITY



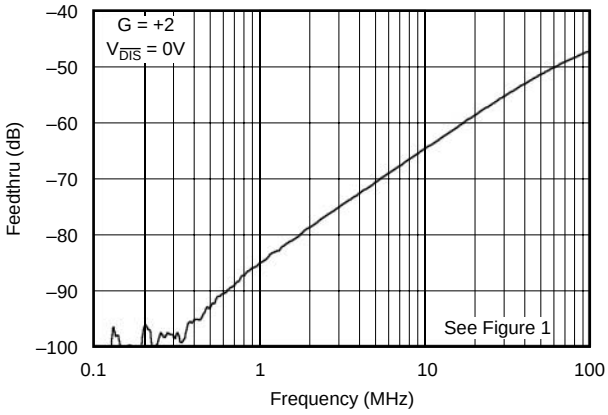
2-TONE, 3RD-ORDER
INTERMODULATION DISTORTION



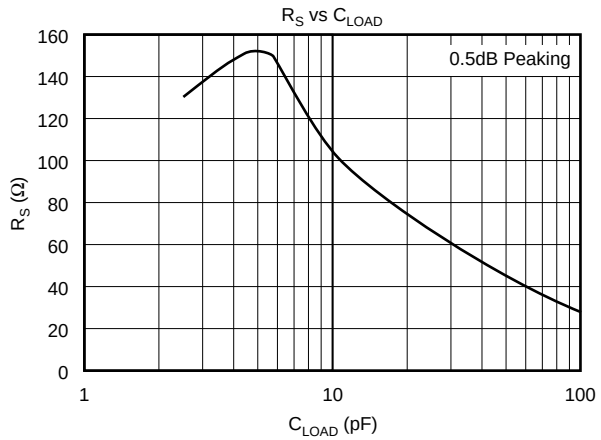
DISABLE TIME



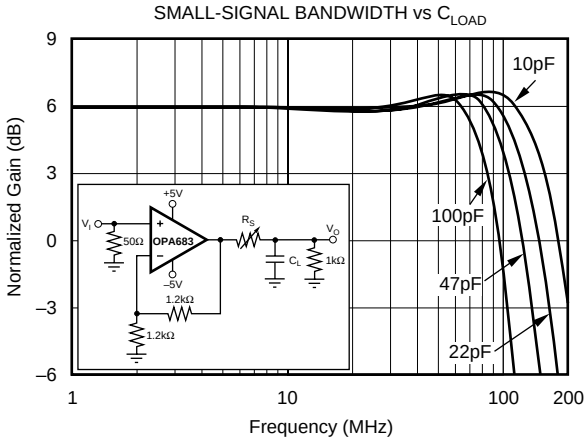
DISABLED FEEDTHRU



R_S vs C_{LOAD}



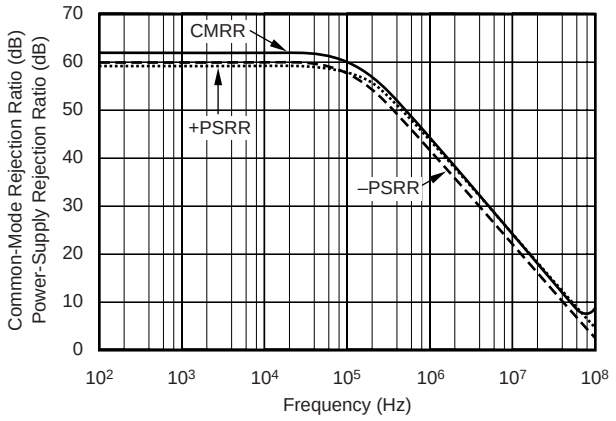
SMALL-SIGNAL BANDWIDTH vs C_{LOAD}



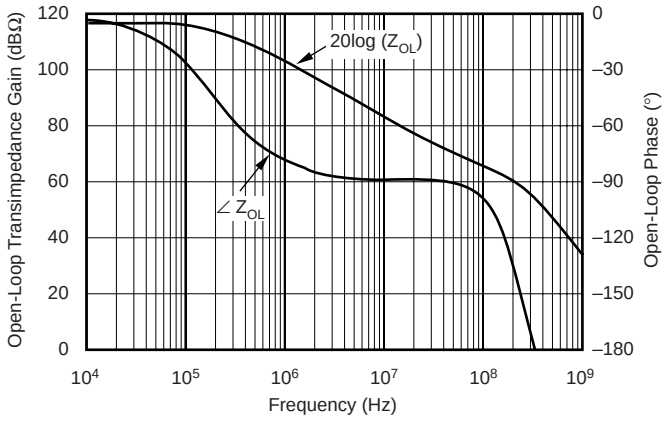
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

$T_A = 25°C$, $R_F = 1.2k\Omega$, $R_L = 1k\Omega$, and G = +2 (see Figure 1 for AC performance only), unless otherwise noted.

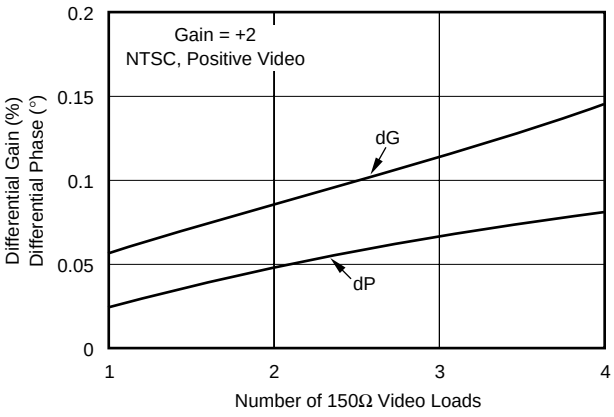
CMRR and PSRR vs FREQUENCY



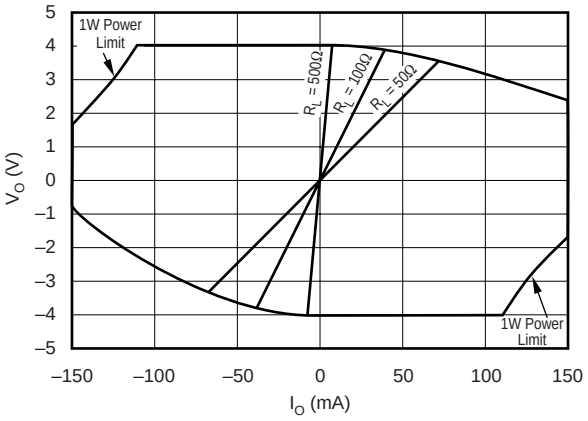
OPEN-LOOP TRANSIMPEDANCE GAIN AND PHASE



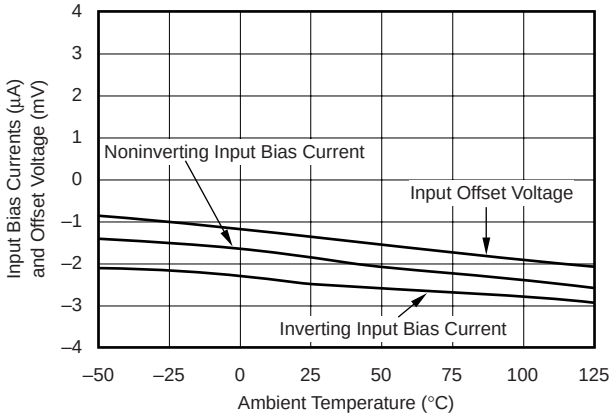
COMPOSITE VIDEO DIFFERENTIAL GAIN/PHASE



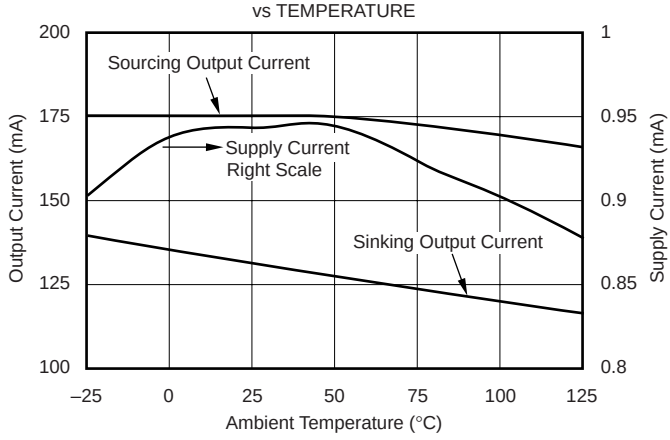
OUTPUT CURRENT AND VOLTAGE LIMITATIONS



TYPICAL DC DRIFT OVER TEMPERATURE



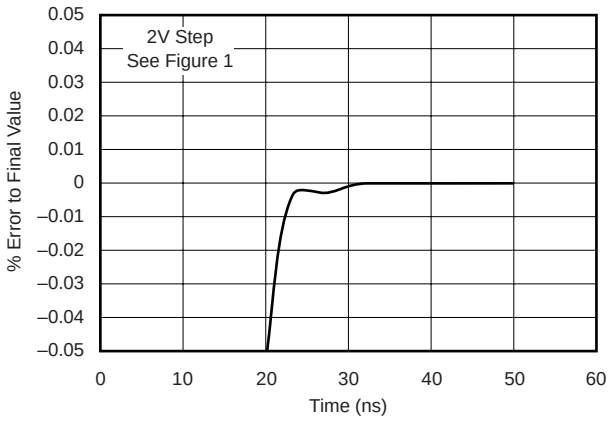
SUPPLY AND OUTPUT CURRENT vs TEMPERATURE



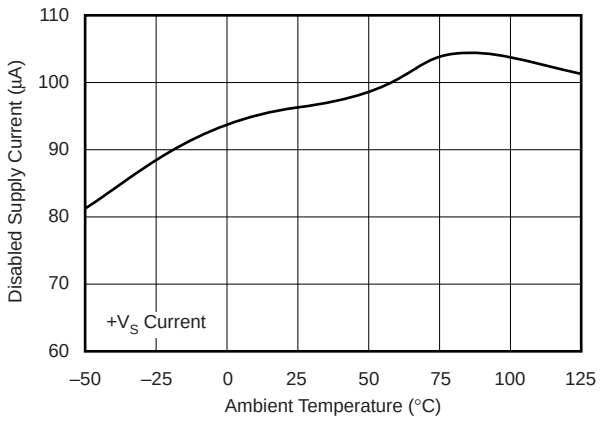
TYPICAL CHARACTERISTICS: $V_S = \pm 5V$ (Cont.)

$T_A = 25°C$, $R_F = 1.2k\Omega$, $R_L = 1k\Omega$, and G = +2 (see Figure 1 for AC performance only), unless otherwise noted.

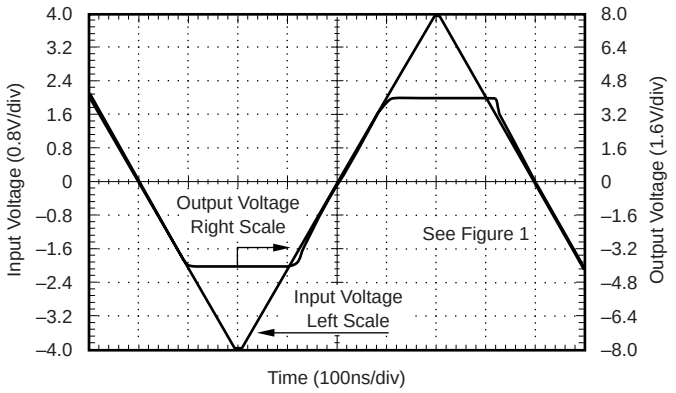
SETTLING TIME



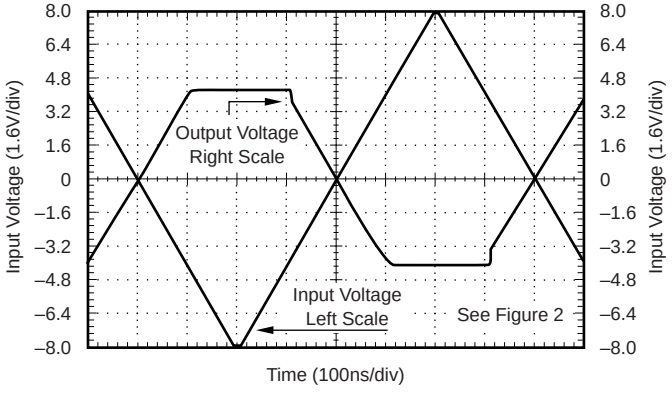
DISABLED SUPPLY CURRENT vs TEMPERATURE



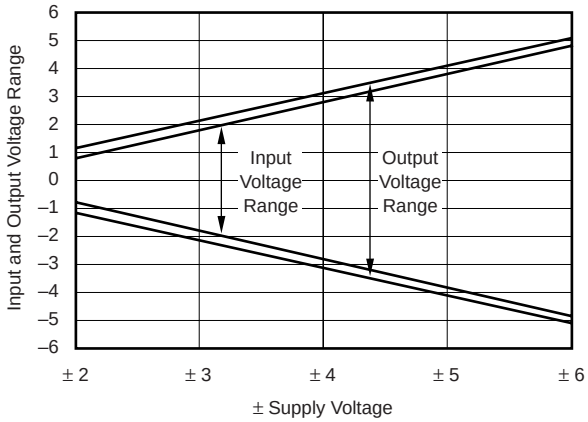
NONINVERTING OVERDRIVE RECOVERY



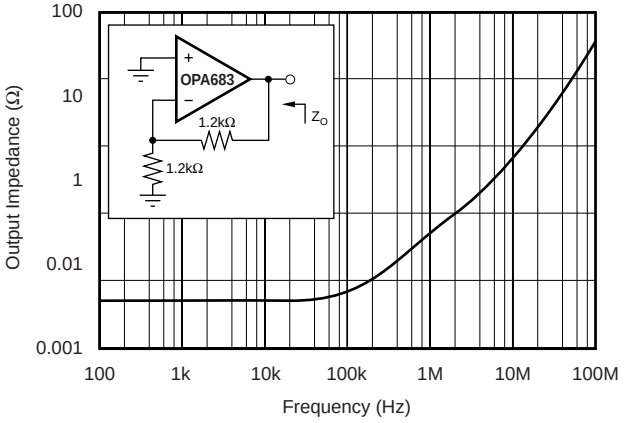
INVERTING OVERDRIVE RECOVERY



INPUT AND OUTPUT RANGE vs SUPPLY VOLTAGE



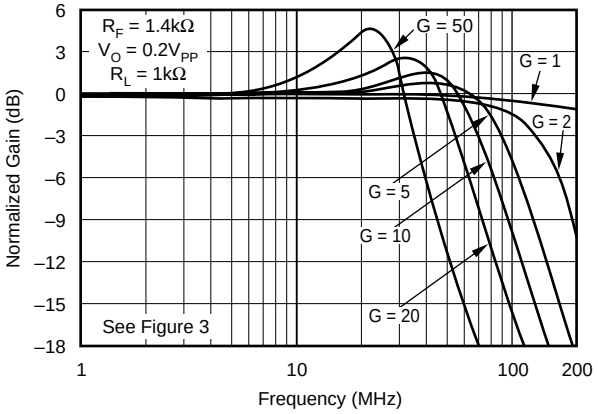
CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY



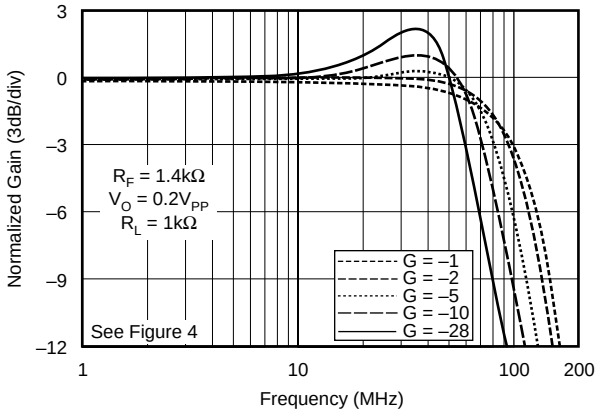
TYPICAL CHARACTERISTICS: V_S = +5V

T_A = 25°C, R_F = 1.4kΩ, R_L = 1kΩ, and G = +2 (see Figure 3 for AC performance only), unless otherwise noted.

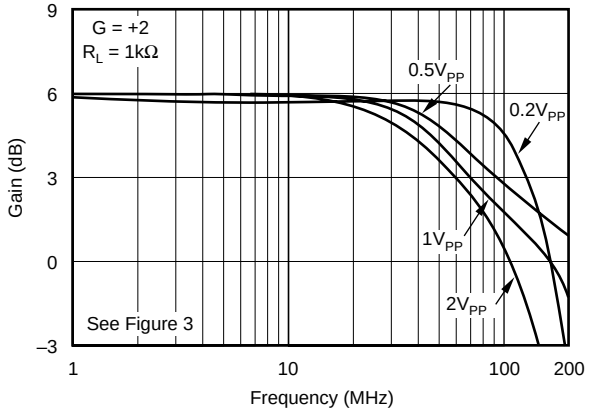
NONINVERTING SMALL-SIGNAL FREQUENCY RESPONSE



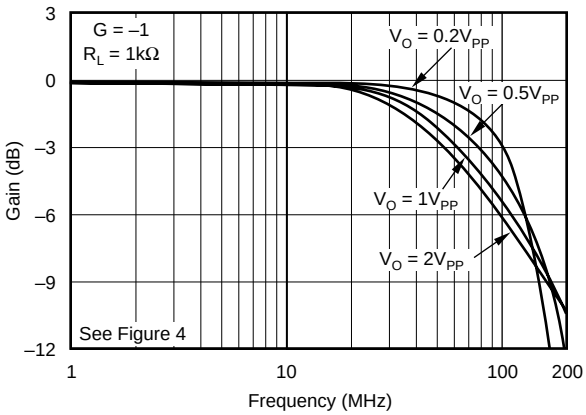
INVERTING SMALL-SIGNAL FREQUENCY RESPONSE



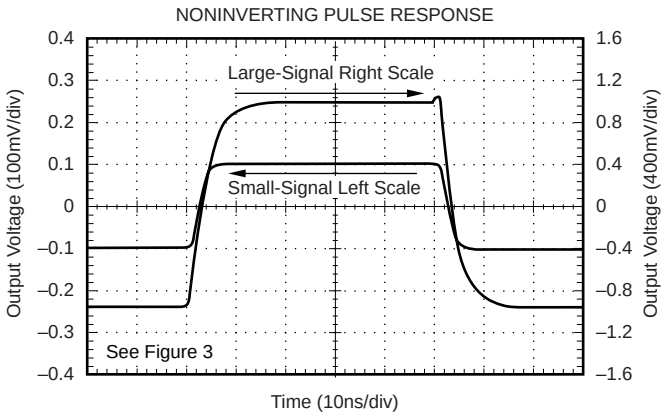
NONINVERTING LARGE-SIGNAL FREQUENCY RESPONSE



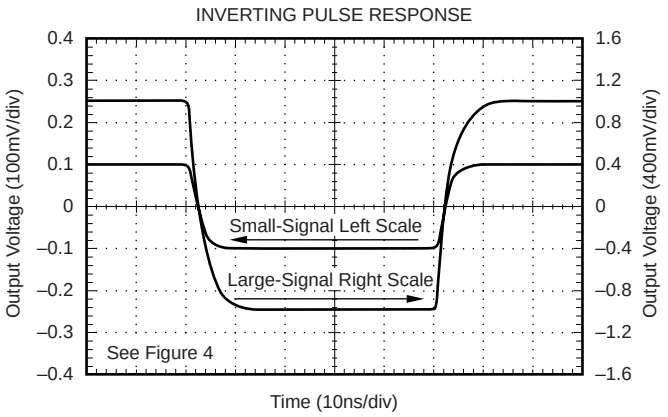
INVERTING LARGE-SIGNAL FREQUENCY RESPONSE



NONINVERTING PULSE RESPONSE



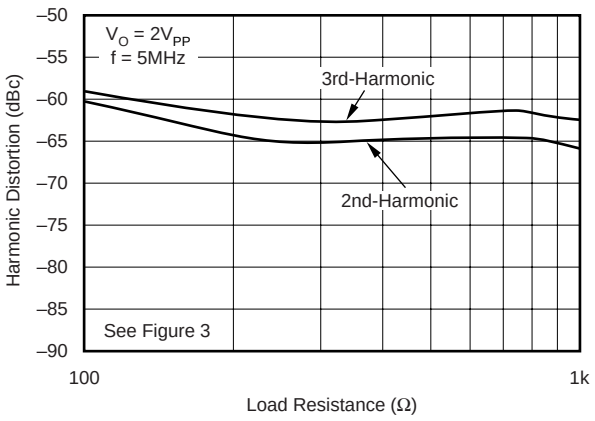
INVERTING PULSE RESPONSE



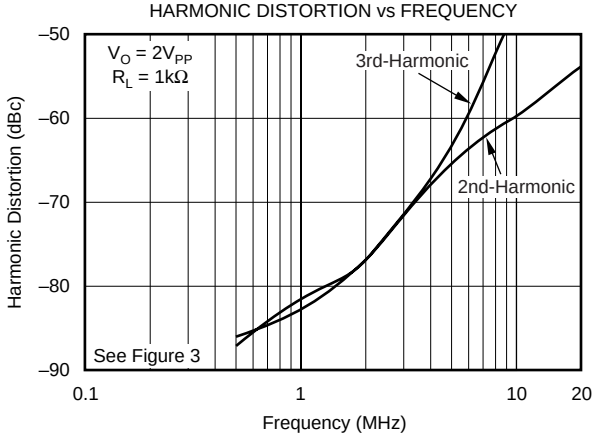
TYPICAL CHARACTERISTICS: V_S = +5V (Cont.)

T_A = 25°C, R_F = 1.4kΩ, R_L = 1kΩ, and G = +2 (see Figure 3 for AC performance only), unless otherwise noted.

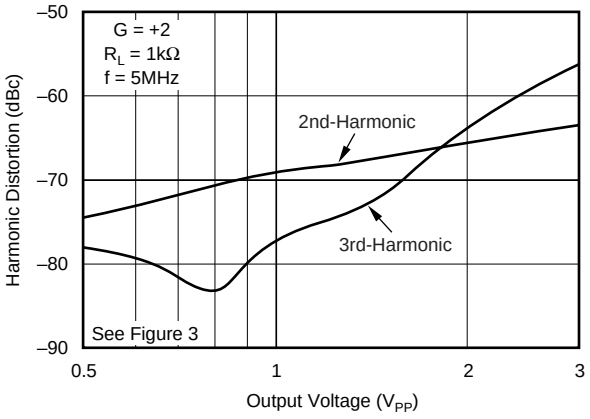
HARMONIC DISTORTION vs LOAD RESISTANCE



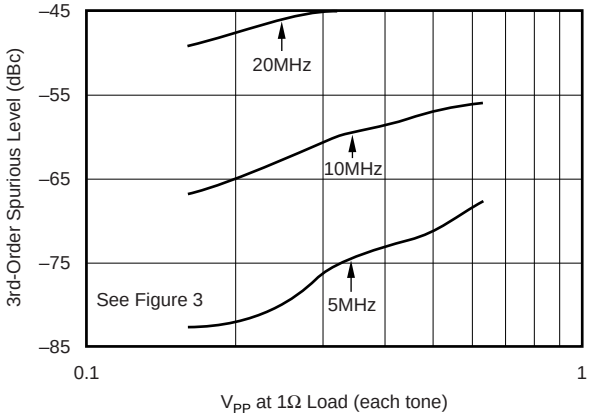
HARMONIC DISTORTION vs FREQUENCY



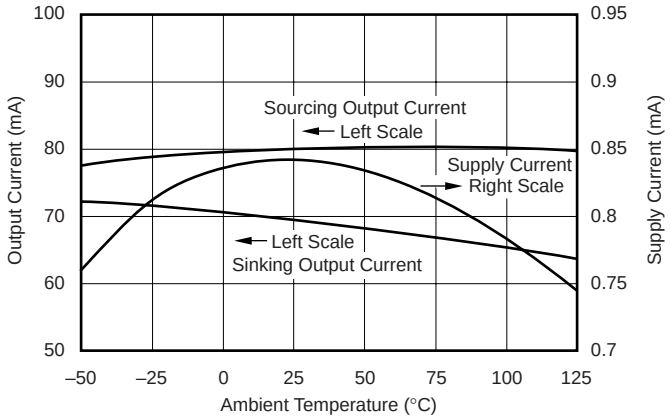
HARMONIC DISTORTION vs OUTPUT VOLTAGE



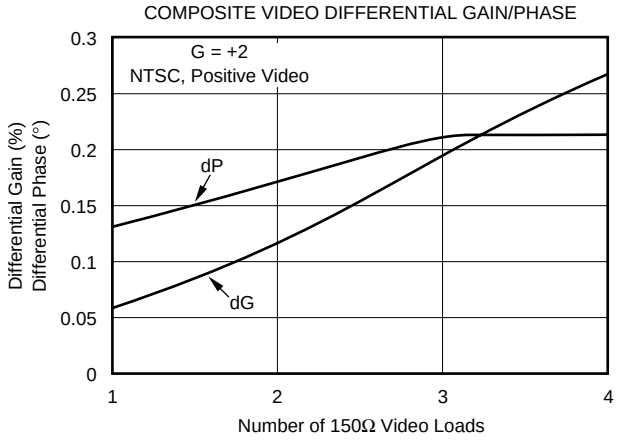
2-TONE, 3RD-ORDER
INTERMODULATION DISTORTION



SUPPLY AND OUTPUT CURRENT
vs TEMPERATURE



COMPOSITE VIDEO DIFFERENTIAL GAIN/PHASE



APPLICATIONS INFORMATION

VERY LOW POWER CURRENT-FEEDBACK OPERATION

The OPA683 gives a new level of performance in very low power current-feedback op amps. Using a new input stage buffer architecture, the OPA683 CFB_{plus} amplifier gives improved bandwidth to higher gains than previous < 1mA supply current amplifiers. This closed-loop internal buffer gives a very low and linearized impedance at the inverting node—isolating the amplifier's AC performance from gain element variations. This allows both the bandwidth and distortion to remain nearly constant over gain—moving closer to the ideal current-feedback performance of Gain Bandwidth independence. This low power amplifier also delivers exceptional output power—its ±4V swing on ±5V supplies with > 100mA output drive gives excellent performance into standard video loads or doubly-terminated 50Ω cables. Single +5V supply operation is also supported with similar bandwidths, but reduced output power capability. For improved harmonic distortion driving heavier loads, in a low power CFB_{plus} amplifier, consider the OPA684, while for even higher output power, consider the OPA691.

Figure 1 shows the DC-coupled, gain of +2, dual power-supply circuit used as the basis of the ±5V Electrical Characteristics and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground while the output load is a 1kΩ resistor. Voltage swings reported in the specifications are taken directly at the input and output pins while load powers (dBm) are interpreted as the voltage swing at the output converted to dBm as if the load were 50Ω. For the circuit of Figure 1, the total effective load will be 1kΩ || 2.4kΩ = 706Ω. Gain changes are most easily accomplished by simply resetting the R_G value—holding R_F constant at its recommended value of 1.2kΩ. The disable control line ($\overline{DIS}$) is typically left open to ensure normal amplifier operation. It may, however, be asserted LOW to reduce the amplifier quiescent to 100µA typically.

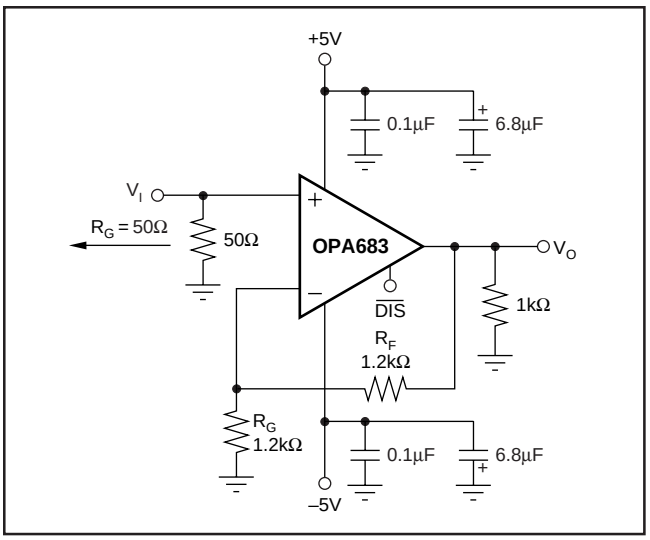


FIGURE 1. DC-Coupled, G = +2V/V, Bipolar Supply, Specification and Test Circuit.

Figure 2 shows the DC-coupled, gain of –1V/V, dual power-supply circuit used as the basis of the Inverting Typical Characteristics. Inverting operation offers several performance benefits. Since there is no common-mode signal across the input stage, the slew rate for inverting operation is higher and the distortion performance is slightly improved. An additional input resistor, R_M, is included in Figure 2 to set the input impedance equal to the 50Ω. The parallel combination of R_M and R_G set the input impedance. As the desired gain increases for the inverting configuration, R_G is adjusted to achieved the desired gain and R_M is also adjusted to hold a 50Ω input match. A point will be reached where R_G will equal 50Ω, R_M is then removed and the input match is set by R_G only. With R_G fixed to achieve an input match to 50Ω, to increase gain, R_F is simply increased. This will, however, quickly reduce the achievable bandwidth as the feedback resistor increases from its recommended value of 1.2kΩ. If the source does not require an input match to 50Ω, either adjust R_M to the get the desired load or remove it and let the R_G resistor alone provide the input load.

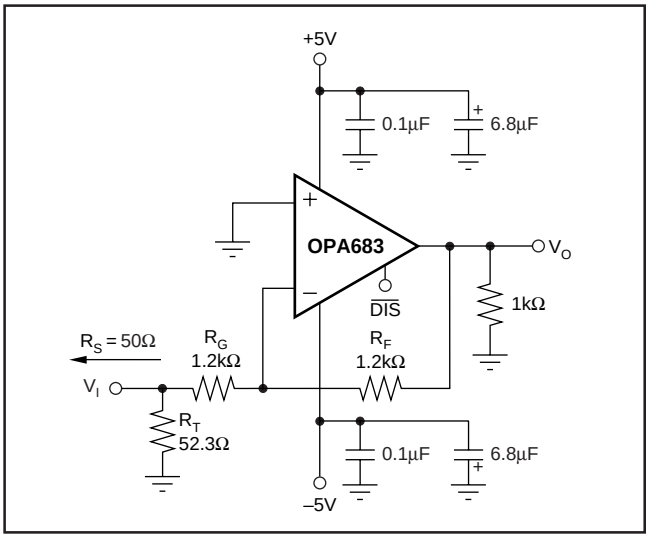


FIGURE 2. DC-Coupled, G = –1V/V, Bipolar Supply, Specification and Test Circuit.

These circuits are showing ±5V operation. The same circuit can be applied with bipolar supplies ranging from ±2.5V to ±6V. Internal supply independent biasing gives nearly the same performance for the OPA683 over this wide range of supplies. Generally, the optimum feedback resistor value (for nominally flat frequency response at G = +2) will increase in value as the total supply voltage across the OPA683 is reduced.

See Figure 3 for the AC-coupled, single +5V supply, gain of +2V/V circuit configuration used as a basis for the +5V only Electrical Characteristics and Typical Characteristics. The key requirement of broadband single-supply operation is to maintain input and output signal swings within the usable voltage ranges at both the input and the output. The circuit of Figure 3 establishes an input midpoint bias using a simple resistive divider from the +5V supply (two 12.5kΩ resistors) to the noninverting input. The input signal is then AC-coupled

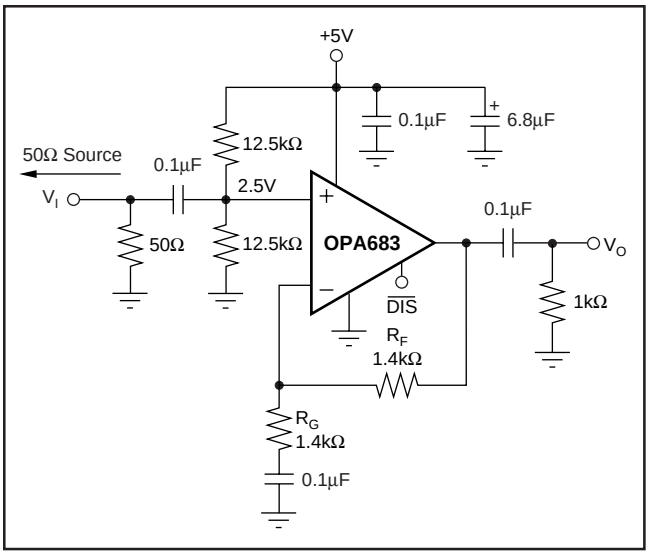


FIGURE 3. AC-Coupled, G = +2V/V, Single-Supply, Specification and Test Circuit.

into this midpoint voltage bias. The input voltage can swing to within 1.25V of either supply pin, giving a $2.5V_{PP}$ input signal range centered between the supply pins. The input impedance of Figure 3 is set to give a 50Ω input match. If the source does not require a 50Ω match, remove this and drive directly into the blocking capacitor. The source will then see the 6.25kΩ load of the biasing network. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of +1—which puts the noninverting input DC bias voltage (2.5V) on the output as well. The feedback resistor value has been adjusted from the bipolar supply condition to re-optimize for a flat frequency response in +5V only, gain of +2 operation. On a single +5V supply, the output voltage can swing to within 1.0V of either supply pin while delivering more than 50mA output current giving $3V_{PP}$ output swing into an AC-coupled 100Ω load if required (8dBm maximum at the matched load). The circuit of Figure 3 shows a blocking capacitor driving into a 1kΩ load resistor. Alternatively, the blocking capacitor could be removed if the load is tied to a supply midpoint or to ground if the DC current required by the load is acceptable.

Figure 4 shows the AC-coupled, single +5V supply, gain of –1V/V circuit configuration used as a basis for the +5V only Typical Characteristics. In this case, the midpoint DC bias on the noninverting input is also decoupled with an additional 0.1µF decoupling capacitor. This reduces the source impedance at higher frequencies for the noninverting input bias current noise. This 2.5V bias on the noninverting input pin appears on the inverting input pin and, since R_G is DC blocked by the input capacitor, will also appear at the output pin. One advantage to inverting operation is that since there is no signal swing across the input stage, higher slew rates and operation to even lower supply voltages is possible. To retain a $1V_{PP}$ output capability, operation down to a 3V supply is allowed. At a +3V supply, the input stage is saturated, but for the inverting configuration of a current-feedback amplifier, wideband operation is retained even under this condition.

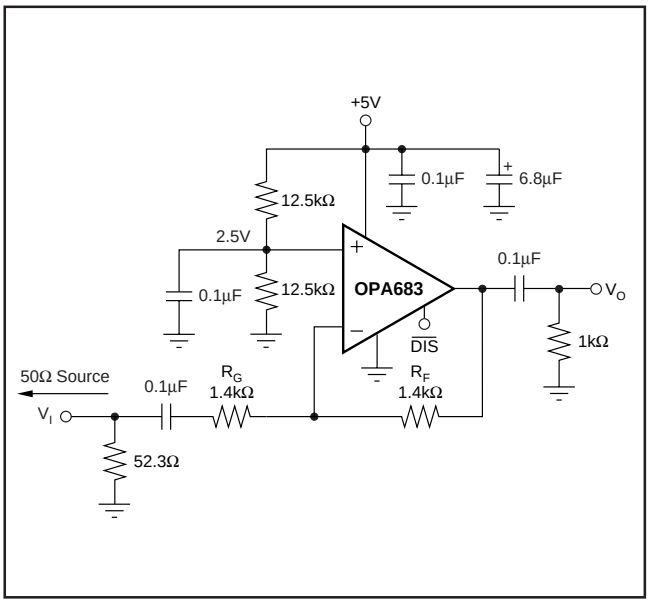


FIGURE 4. AC-Coupled, G = –1V/V, Single-Supply, Specification and Test Circuit.

The circuits of Figure 3 and 4 show single-supply operation at +5V. These same circuits may be used up to single supplies of +12V with minimal changes in the performance of the OPA683.

LOW POWER, VIDEO LINE DRIVER APPLICATIONS

For low power, video line driving, the OPA683 provides the output current and linearity to support multiple load composite video signals. Figure 5 shows a typical ±5V supply video line driver application. The improved 2nd-harmonic distortion of the CFB_{plus} architecture, along with the OPA683's high output current and voltage, gives exceptional differential gain and phase performance in a very low power solution. As the Typical Characteristics show, a single video load shows a dG/dP of 0.06%/0.03°. Multiple loads may also be driven with < 0.15%/0.1° dG/dP for up to 4 parallel video loads where the amplifier is driving an equivalent load of 37.5Ω.

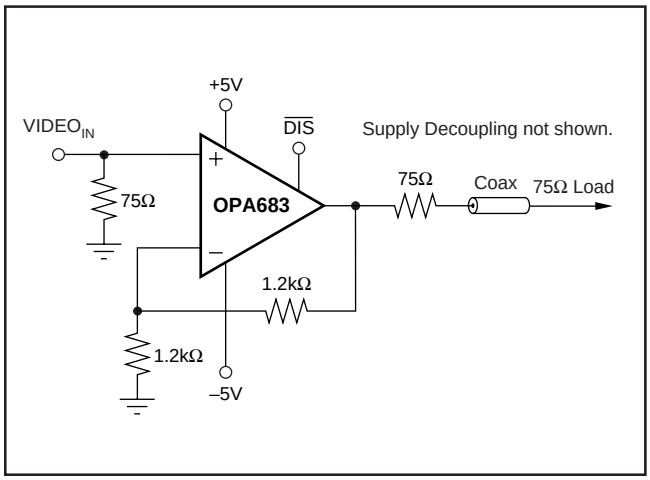


FIGURE 5. Gain of +2 Video Cable Driver.

VERY LOW POWER ACTIVE FILTER

The OPA683 provides an exceptionally capable gain block for implementing Sallen-Key type filters. Typically, the bandwidth interaction with gain setting for low power amplifiers, constrain these filters to using unity-gain amplifiers. Since the OPA683 CFB_{plus} design holds very high bandwidth to high gains, implementations that provide signal gain, as well as the desired filter shape, are easily implemented. Figure 6 shows an example of a 5MHz 2nd-order low-pass filter where the amplifier is providing a voltage gain of 4. This single-supply implementation (applicable to single +12V operation as well) consumes only 5.1mW quiescent power. The two 12.5kΩ resistors bias the input and output at the supply midpoint while the three 0.1µF capacitors block off the DC current paths to ground for this mid-scale operating point. The filter resistors and capacitors have been adjusted to provide a Butterworth (Q = 0.707) response with a $\omega_O = 2\pi \bullet 5MHz$. This gives a flat passband response with a –3dB cutoff at 5MHz. Figure 7 shows the small-signal frequency response for the circuit of Figure 6.

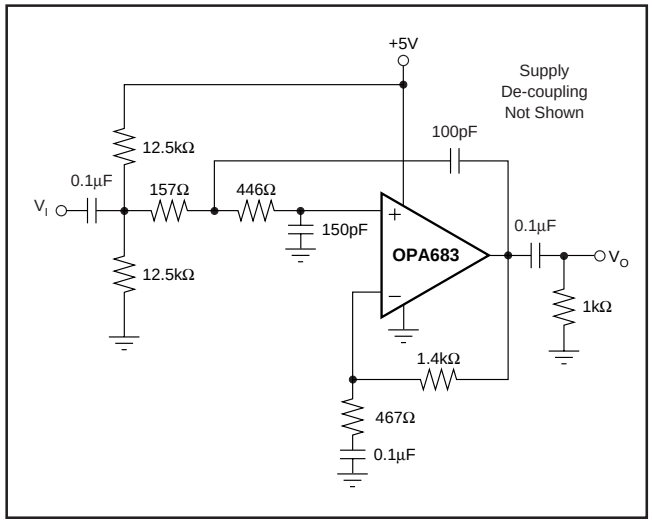


FIGURE 6. 5MHz, 2nd-Order Low Pass Filter.

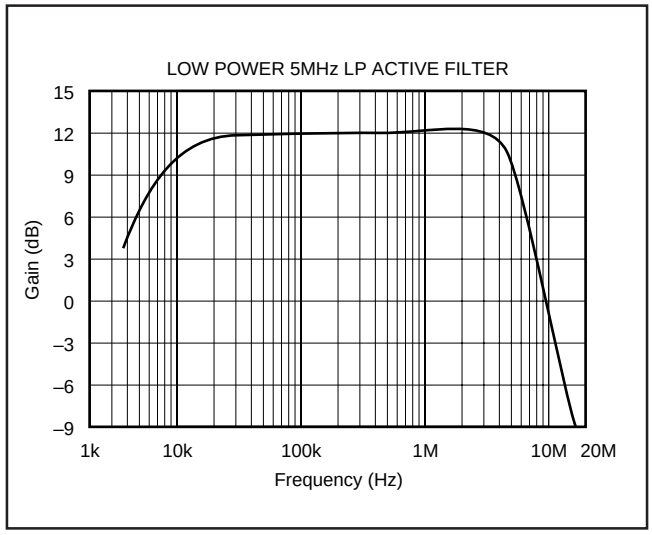


FIGURE 7. Low Power Active Filter Frequency Response.

HIGH GAIN HF AMPLIFIER

Where high gains at moderate frequencies are required in an HF receiver channel, the OPA683 can provide a very low power solution with moderate input noise figure. Figure 8 shows a technique that can improve the noise figure with no added power. An input transformer provides a noiseless voltage gain at the cost of higher source impedance for the amplifier's noninverting input current noise. The circuit of Figure 8, using a 1:4 turns ratio (1:16 impedance ratio) transformer, reduces the input noise figure from about 20dB for just the amplifier to 10.6dB in combination. The bandwidth for this circuit will be principally set by the transformer since the OPA683 will give > 80MHz for the gain of 20V/V shown in Figure 8. The overall circuit gives a gain to a matched 50Ω load of 32dB (40V/V) from the transformer input. This example circuit provides this gain using only 10mW of quiescent power with application from 500kHz to 30MHz.

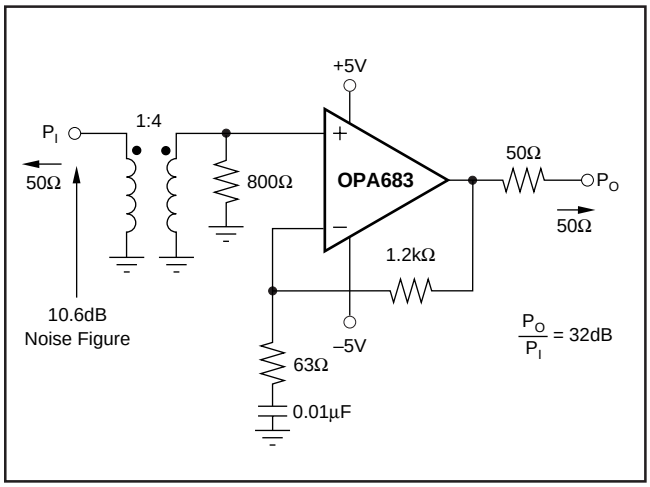


FIGURE 8. Low Power, High Gain HF Amplifier.

LOW POWER, ADC DRIVER

Where a low power, single-supply interface to a single-ended input +5V ADC is required, the circuit of Figure 9 can provide a very flexible, high performance solution. Running in an AC-coupled inverting mode allows the noninverting input to be used for the common-mode voltage from the ADS820 converter. This midpoint reference biases both the noninverting converter input and the amplifier noninverting input. With an AC-coupled gain path, this +2.5V DC bias has a gain of +1 to the output putting the output at the DC midpoint for the converter. The output then drives through an isolating resistor (60Ω) to the inverting input of the converter which is further decoupled by a 22pF external capacitance to add to its 5pF input capacitance. This coupling network provides a high cutoff low-pass while also giving a low source impedance at high frequencies for the converter. The gain for this circuit is set by adjusting R_G to the desired value. For a $2V_{PP}$ maximum output driving the light load of Figure 9, the OPA683 will provide < –80dBc THD through 1MHz as shown in the Typical Characteristics. One of the important advantages for this CFB_{plus} amplifier is that this distortion does not degrade significantly at higher gains.

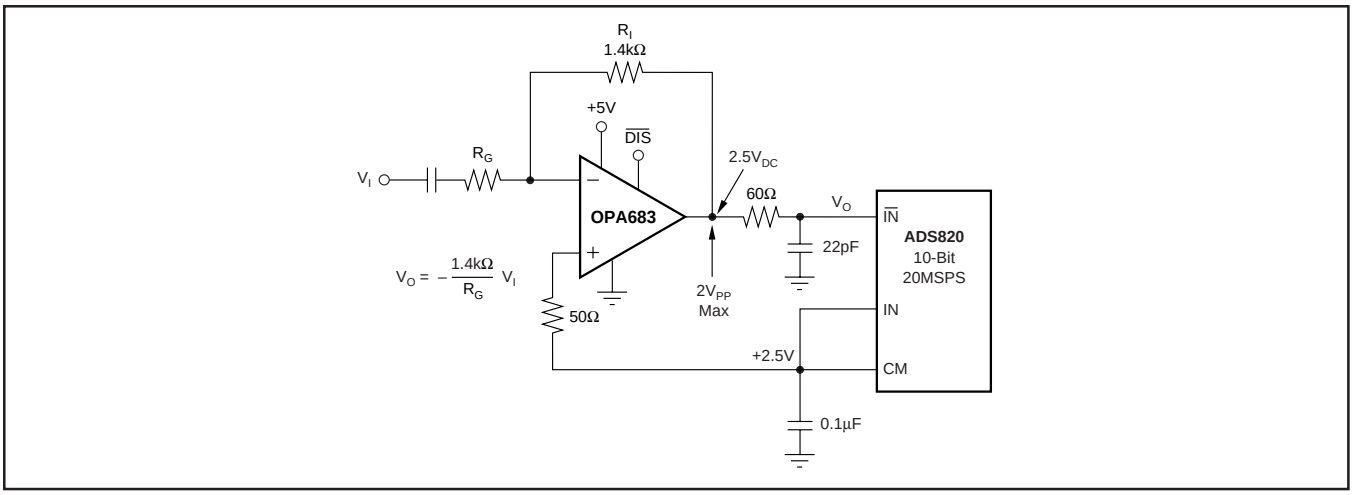


FIGURE 9. Low Power, Single-Supply, ADC Driver.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURES

Two printed circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA683 in its two package options. Both of these are offered free of charge as unpopulated PCBs, delivered with a user's guide. The summary information for these fixtures is shown in Table I.

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA683ID	SO-8	DEM-OPA-SO-1A	SBOU009
OPA683IDBQ	SOT23-6	DEM-OPA-SOT-1A	SBOU010

TABLE I. Demonstration Fixtures by Package.

The demonstration fixtures can be requested at the Texas Instruments web site (www.ti.com) through the OPA683 product folder.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH

Any current-feedback op amp like the OPA683 can hold high bandwidth over signal gain settings with the proper adjustment of the external resistor values. A low-power part like the OPA683 typically shows a larger change in bandwidth due to the significant contribution of the inverting input impedance to loop-gain changes as the signal gain is changed. Figure 10 shows a simplified analysis circuit for any current feedback amplifier.

The key elements of this current feedback op amp model are:

$\alpha \Rightarrow$ Buffer gain from the noninverting input to the inverting input

$R_I \Rightarrow$ Buffer output impedance

$i_{ERR} \Rightarrow$ Feedback error current signal

$Z(s) \Rightarrow$ Frequency dependent open loop transimpedance gain from i_{ERR} to V_O

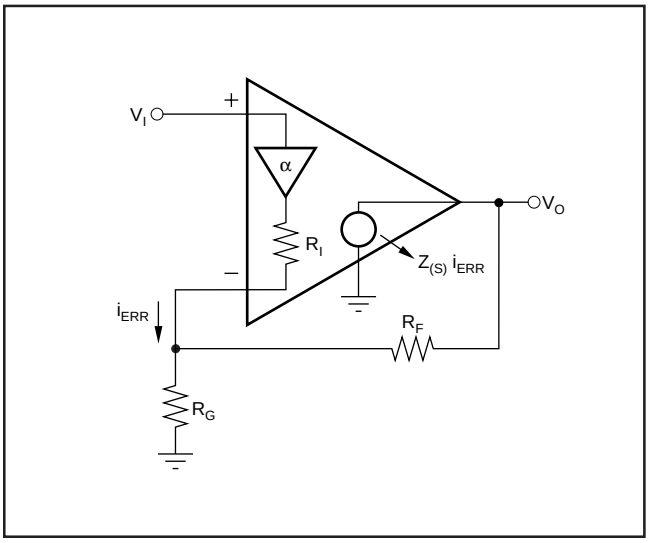


FIGURE 10. Current Feedback Transfer Function Analysis Circuit.

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It will, however set the CMRR for a single op amp differential amplifier configuration. For the buffer gain $\alpha < 1.0$, the CMRR = $-20 \cdot \log(1 - \alpha)$. The closed loop input stage buffer used in the OPA683 gives a buffer gain more closely approaching 1.00 and this shows up in a slightly higher CMRR than any previous current feedback op amp. The 60dB typical CMRR shown in the Electrical Characteristics implies a buffer gain of 0.9990.

R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. The OPA683 reduces this element to approximately 4.5Ω using the loop-gain of the input buffer stage. This significant reduction in buffer output impedance, on very low power, contributes significantly to extending the bandwidth at higher gains.

A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage feedback op amp) and passes this on to the output through an internal frequency dependent transimpedance gain. The Typical Characteristics show this open-loop transimpedance response. This is analogous to the open-loop voltage gain curve for a voltage feedback op amp. Developing the transfer function for the circuit of Figure 10 gives Equation 1:

(1)

$$\frac{V_O}{V_I} = \frac{\alpha\left(1+\frac{R_F}{R_G}\right)}{1+\frac{R_F + R_I\left(1+\frac{R_F}{R_G}\right)}{Z_{(S)}}} = \frac{\alpha NG}{1+\frac{R_F + R_I\, NG}{Z_{(S)}}}$$

$$\left[NG = \left(1+\frac{R_F}{R_G}\right)\right]$$

This is written in a loop-gain analysis format where the errors arising from a non-infinite open-loop gain are shown in the denominator. If Z(s) was infinite over all frequencies, the denominator of Equation 1 would reduce to 1 and the ideal desired signal gain shown in the numerator would be achieved. The fraction in the denominator of Equation 1 determines the frequency response. Equation 2 shows this as the loop-gain equation.

(2)

$$\frac{Z_{(S)}}{R_F + R_I\, NG} = \text{Loop Gain}$$

If 20 • log(R_F + NG • R_I) were drawn on top of the open-loop transimpedance plot, the difference between the two would be the loop gain at a given frequency. Eventually, Z(s) rolls off to equal the denominator of Equation 2 at which point the loop gain has reduced to 1 (and the curves have intersected). This point of equality is where the amplifier's closed-loop frequency response given by Equation 1 will start to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage feedback op amp. The difference here is that the total impedance in the denominator of Equation 2 may be controlled somewhat separately from the desired signal gain (or NG).

The OPA683 is internally compensated to give a maximally flat frequency response for R_F = 1.2kΩ at NG = 2 on ±5V supplies. That optimum value goes to 1.4kΩ on a single +5V supply. Normally, with a current feedback amplifier, it is possible to adjust the feedback resistor to hold this bandwidth up as the gain is increased. The CFB_{plus} architecture has reduced the contribution of the inverting input impedance to provide exceptional bandwidth to higher gains without adjusting the feedback resistor value. The Typical Characteristics show the small-signal bandwidth over gain with a fixed feedback resistor.

At very high gains, 2nd-order effects in the buffer output impedance cause the overall response to peak up. If desired, it is possible to retain a flatter frequency response at higher gains by adjusting the feedback resistor to higher values as the gain is increased. Figure 11 shows the empirically determined feedback resistor and resulting –3dB bandwidth from gains of +2 to +100 to hold a < 0.5dB peaked response. Here, since a slight peaking was allowed, a lower nominal R_F is suggested at a gain of +2 giving > 250MHz bandwidth. This exceeds that shown in the Electrical Characteristics due to the slightly lower feedback resistor allowing a modest peaking in the response. Figure 12 shows the measured frequency response curves with the adjusted feedback resistor value. While the bandwidth for this low-power part does reduce at higher gains, going over a 50:1 gain range gives only a factor of 10 bandwidth reduction. The 25MHz bandwidth at a gain of 100V/V is equivalent to a 2.5GHz gain bandwidth product voltage feedback amplifier capability. Even better bandwidth retention to higher gains can be delivered by the slightly higher quiescent power OPA684.

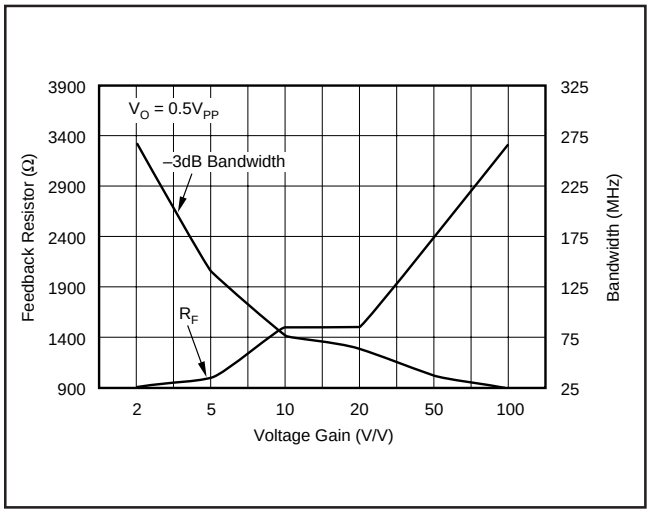


FIGURE 11. Bandwidth and R_F Optimized vs Gain.

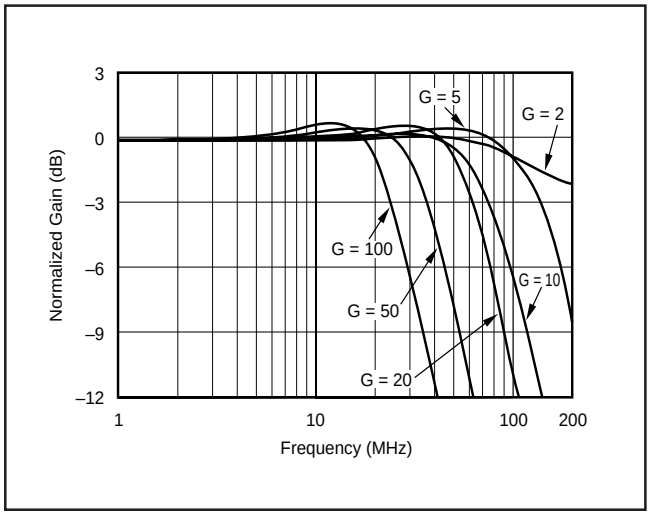


FIGURE 12. Small-Signal Frequency Response with Optimized R_F.

OUTPUT CURRENT AND VOLTAGE

The OPA683 provides output voltage and current capabilities that can support the needs of driving doubly-terminated 50Ω lines. Changing the 1kΩ load in Figure 1 to a 100Ω will give a total load that is the parallel combination of the 100Ω load and the 2.4kΩ total feedback network impedance. This 96Ω load will require no more than 36mA output current to support a ±3.5V output voltage swing. This is within the specified minimum output current of +58mA/–45mA over the full temperature range.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage • current, or V-I product, which is more relevant to circuit operation. Refer to the "Output Voltage and Current Limitations" plot in the Typical Characteristics. The X and Y axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA683's output drive capabilities. Superimposing resistor load lines onto the plot shows the available output voltage and current for specific loads.

The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup will the output current and voltage decrease to the numbers shown in the Electrical Specifications. As the output transistors deliver power, their junction temperatures will increase, decreasing their V_{BE}'s (increasing the available output voltage swing) and increasing their current gains (increasing the available output current). In steady state operation, the available output voltage and current will always be greater than that shown in the over-temperature specifications since the output stage junction temperatures will be higher than the minimum specified operating ambient.

To maintain maximum output stage linearity, no output short circuit protection is provided. This will not normally be a problem since most applications include a series matching resistor at the output that will limit the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin (8-pin packages) will, in most cases, destroy the amplifier. If additional short-circuit protection is required, consider a small series resistor in the power-supply leads. This will, under heavy output loads, reduce the available output voltage swing. A 5Ω series resistor in each power-supply lead will limit the internal power dissipation to less than 1W for an output short circuit while decreasing the available output voltage swing only 0.25V for up to 50mA desired load currents. Always place the 0.1µF power-supply decoupling capacitors after these supply current limiting resistors directly on the supply pins.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance which may be recommended to improve ADC linearity. A high-speed, high open-loop gain amplifier like the OPA683 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended "R_S vs Capacitive Load" and the resulting frequency response at the load. The 1kΩ resistor shown in parallel with the load capacitor is a measurement path and may be omitted. Parasitic capacitive loads greater than 3pF can begin to degrade the performance of the OPA683. Long PC board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA683 output pin (see Board Layout Guidelines).

DISTORTION PERFORMANCE

The OPA683 provides low distortion in a very low power amplifier. The CFB_{plus} architecture also gives two significant areas of distortion improvement. First, in operating regions where the 2nd-harmonic distortion due to output stage nonlinearities is very low (frequencies < 1MHz, low output swings into light loads) the linearization at the inverting node provided by the CFB_{plus} design gives 2nd-harmonic distortions that extend into the –90dBc region. Previous current feedback amplifiers have been limited to approximately –85dBc due to the nonlinearities at the inverting input. The second area of distortion improvement comes in a distortion performance that is more gain independent than prior solutions. To the extent that the distortion at a particular output power is output stage dependent, 2nd-harmonic particularly, and to a lesser extend 3rd-harmonic distortion, is constant as the gain is increased. This is due to the constant loop gain versus signal gain provided by the CFB_{plus} design. As shown in the Typical Characteristics, while the 2nd-harmonic is constant with gain, the 3rd-harmonic degrades at higher gains.

Relative to alternative amplifiers with < 1mA supply current, the OPA683 holds much lower distortion at higher frequencies (> 5MHz) and to higher gains. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd-harmonic will dominate the distortion with a lower 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion slightly for the OPA683. Remember that the total load in-

cludes the feedback network—in the noninverting configuration (see Figure 1) this is the sum of $R_F + R_G$, while in the inverting configuration it is just R_F. Also, providing an additional supply decoupling capacitor (0.1µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. A low-power part like the OPA683 includes quiescent boost circuits to provide the full-power bandwidth shown. These act to increase the bias in a very linear fashion only when high slew rate or output power are required. The Typical Characteristics show the 2nd-harmonic increasing slightly from $500mV_{PP}$ to $5V_{PP}$ outputs while the 3rd-harmonics also increase with output power.

The OPA683 has an extremely low 3rd-order harmonic distortion—particularly for light loads and at lower frequencies. This also gives low 2-tone, 3rd-order intermodulation distortion as shown in the Typical Characteristics. Since the OPA683 includes internal power boost circuits to retain good full-power performance at high frequencies and outputs, it does not show a classical 2-tone, 3rd-order intermodulation intercept characteristic. Instead, it holds relatively low and constant 3rd-order intermodulation spurious levels over power. The Typical Characteristics show this spurious level as a dBc below the carrier at fixed center frequencies swept over single-tone voltage swing at a 1kΩ load. Very light loads such as ADC inputs for will see < –85dBc 3rd-order spurious to 1MHz for full-scale inputs. For much lower 3rd-order intermodulation distortion through 200MHz, consider the OPA685.

NOISE PERFORMANCE

Wideband current-feedback op amps generally have a higher output noise than comparable voltage feedback op amps. The OPA683 offers an excellent balance between voltage and current noise terms to achieve low output noise in a low- power amplifier. The inverting current noise (11.6pA/$\sqrt{Hz}$) is lower than most other current feedback op amps while the input voltage noise (4.4nV/$\sqrt{Hz}$) is lower than any unity-gain stable, comparable slew rate, voltage feedback op amp. This low input voltage noise was achieved at the price of higher noninverting input current noise (5.1pA/$\sqrt{Hz}$). As long as the AC source impedance looking out of the noninverting node is less than 300Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 13 shows the op amp noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/$\sqrt{Hz}$ or pA/$\sqrt{Hz}$.

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 3 shows the general form for the output noise voltage using the terms shown in Figure 13.

(3)

$$E_O = \sqrt{\left(E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S\right)G_N^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FG_N}$$

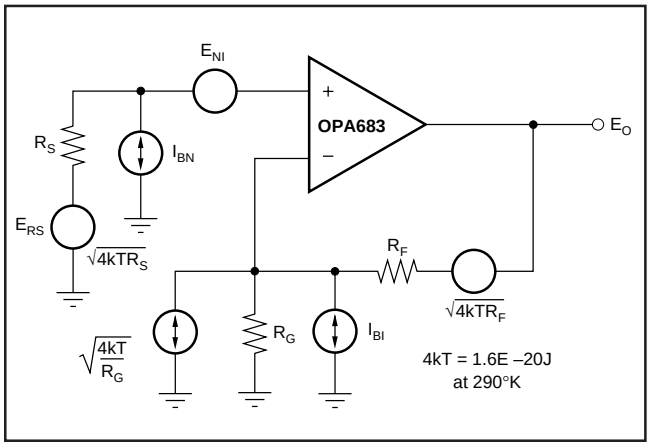


FIGURE 13. Op Amp Noise Analysis Model.

Dividing this expression by the noise gain (NG = $(1 + R_F/R_G)$) will give the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 4.

(4)

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{G_N}\right)^2 + \frac{4kTR_F}{G_N}}$$

Evaluating these two equations for the OPA683 circuit and component values (see Figure 1) will give a total output spot noise voltage of 17.6nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 8.8nV/$\sqrt{Hz}$. This total input referred spot noise voltage is higher than the 4.4nV/$\sqrt{Hz}$ specification for the op amp voltage noise alone. This reflects the noise added to the output by the inverting current noise times the feedback resistor. As the gain is increased, this fixed output noise power term contributes less to the total output noise and the total input referred voltage noise given by Equation 3 will approach just the 4.4nV/$\sqrt{Hz}$ of the op amp itself. For example, going to a gain of +20 in the circuit of Figure 1, adjusting only the gain resistor to 63.2Ω, will give a total input referred noise of 4.6nV/$\sqrt{Hz}$. A more complete description of op amp noise analysis can be found in the TI application note AB-103 (SBOA066). Refer to Texas Instruments' web site at www.ti.com.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp like the OPA683 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate DC accuracy. The Electrical Characteristics show an input offset voltage comparable to high slew rate voltage-feedback amplifiers. However, the two input bias currents are somewhat higher and are unmatched. Whereas bias current cancellation techniques are very effective with most voltage feedback op amps, they do not generally reduce the output DC offset for wideband current-feedback op amps. Since the two input bias currents are unrelated in both magnitude and polarity, matching the source impedance looking out of each input to reduce their error contribution to the output is ineffective. Evaluating the configuration of Figure 1, using worst case +25°C input offset voltage and

the two input bias currents, gives a worst case output offset range equal to:

$\pm(NG \bullet V_{OS(MAX)}) \pm (I_{BN} \bullet R_S/2 \bullet NG) \pm (I_{BI} \bullet R_F)$

where

NG = noninverting signal gain

$= \pm(2 \bullet 3.5mV) \pm (4\mu A \bullet 25\Omega \bullet 2) \pm (1.2k\Omega \bullet 10\mu A)$

$= \pm 7mV \pm 0.1mV \pm 12mV$

$= \pm 19.1mV$

While the last term, the inverting bias current error, is dominant in this low-gain circuit, the input offset voltage will become the dominant DC error term as the gain exceeds 4V/V. Where improved DC precision is required in a high-speed amplifier, consider the OPA642 single and OPA2822 dual voltage-feedback amplifiers.

DISABLE OPERATION

The OPA683 provides an optional disable feature that may be used to reduce system power when channel operation is not required. If the $V_{\overline{DIS}}$ control pin is left unconnected, the OPA683 will operate normally. To disable, the control pin must be asserted LOW. Figure 14 shows a simplified internal circuit for the disable control feature.

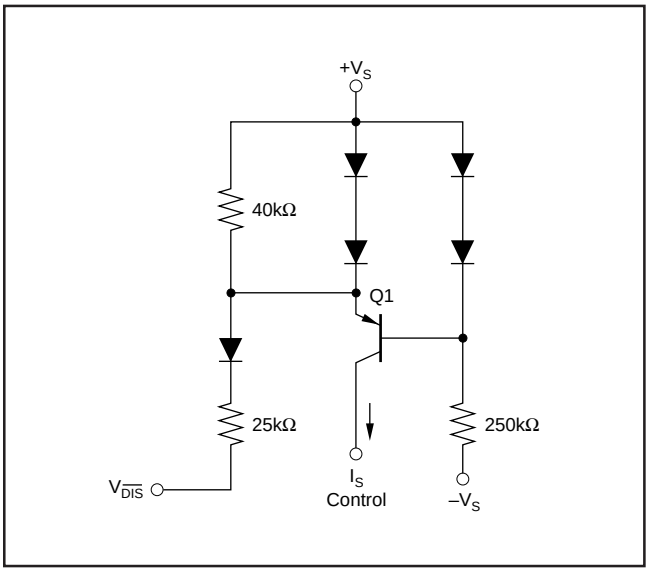


FIGURE 14. Simplified Disable Control Circuit.

In normal operation, base current to Q1 is provided through the 250kΩ resistor while the emitter current through the 40kΩ resistor sets up a voltage drop that is inadequate to turn on the two diodes in Q1's emitter. As $V_{\overline{DIS}}$ is pulled LOW, additional current is pulled through the 40kΩ resistor eventually turning on these two diodes (≈ 33μA). At this point, any further current pulled out of $V_{\overline{DIS}}$ goes through those diodes holding the emitter-base voltage of Q1 at approximately 0V. This shuts off the collector current out of Q1, turning the amplifier off. The supply current in the disable mode are only those required to operate the circuit of Figure 14.

When disabled, the output and input nodes go to a high impedance state. If the OPA683 is operating in a gain of +1 (with a 1.2kΩ feedback resistor still required for stability), this will show a very high impedance (1.7pF || 1MΩ) at the output and exceptional signal isolation. If operating at a gain greater than +1, the total feedback network resistance ($R_F + R_G$) will appear as the impedance looking back into the output, but the circuit will still show very high forward and reverse isolation. If configured as an inverting amplifier, the input and output will be connected through the feedback network resistance ($R_F + R_G$) giving relatively poor input to output isolation.

The OPA683 provides very high power gain on low quiescent current levels. When disabled, internal high impedance nodes discharge slowly which, with the exceptional power gain provided, give a self powering characteristic that leads to a slow turn off characteristic. Typical full turn off times to rated 100μA disabled supply current are 60ms. Turn on times are very fast—less than 40ns.

THERMAL ANALYSIS

The OPA683 will not require external heat-sinking for most applications. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \bullet \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \bullet R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As an absolute worst case example, compute the maximum T_J using an OPA683IDBV (SOT23-6 package) in the circuit of Figure 1 operating at the maximum specified ambient temperature of +85°C and driving a grounded 100Ω load.

$P_D = 10V \bullet 1.05mA + 5^2/(4 \bullet (100\Omega \parallel 2.4k\Omega)) = 76mW$

Maximum $T_J = +85°C + (0.076W \bullet 150°C/W) = 96°C$.

This maximum operating junction temperature is well below most system level targets. Most applications will be lower than this since an absolute worst case output stage power was assumed in this calculation.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high frequency amplifier like the OPA683 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional band-limiting.. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high frequency 0.1μF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high frequency performance of the OPA683. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition axially-leaded resistors can also provide good high frequency performance. Again, keep their leads and PC board trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Since the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value as described previously. Increasing its value will reduce the peaking at higher gains, while decreasing it will give a more peaked frequency response at lower gains. The 1.2kΩ feedback resistor used in the Electrical Characteristics at a gain of +2 on ±5V supplies is a good starting point for design. Note that a 1.2kΩ feedback resistor, rather than a direct short, is required for the unity-gain follower application. A current-feedback op amp requires a feedback resistor even in the unity-gain follower configuration to control stability.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of recommended R_S versus capacitive load. Low parasitic capacitive loads (< 5pF) may not need an R_S since the OPA683 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact a higher impedance environment will improve distortion as shown in the distortion versus load plots. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA683 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA683 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of "R_S vs Capacitive Load". This will not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is LOW, there will be some signal attenuation due to the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA683 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA683 onto the board.

INPUT AND ESD PROTECTION

The OPA683 is built using a very high speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table where an absolute maximum 13V across the supply pins is reported. All device pins have limited ESD protection using internal diodes to the power supplies as shown in Figure 15.

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (e.g. in systems with ±15V supply parts driving into the OPA683), current limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

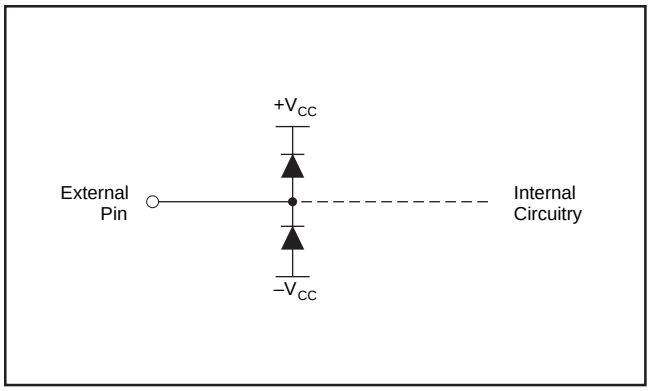


FIGURE 15. Internal ESD Protection.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
7/08	E	2	Abs Max Ratings	Changed Storage Temperature Range from –40°C to +125C to –65°C to +125C.
		3, 4	Electrical Characteristics, Power Supply	Added minimum supply voltage.
3/06	D	15	Design-In Tools	Board part number changed.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA683ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 683	Samples
OPA683IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A83	Samples
OPA683IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A83	Samples
OPA683IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 683	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

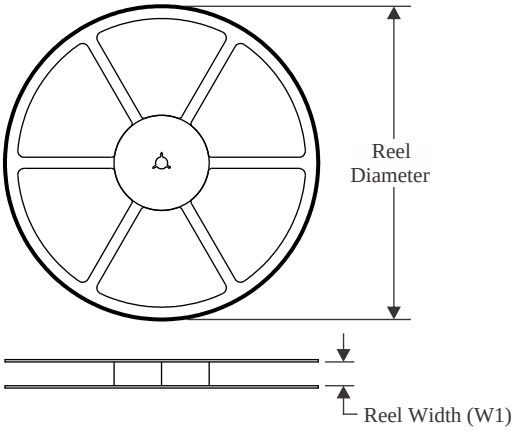
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

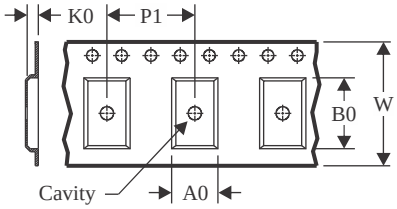
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

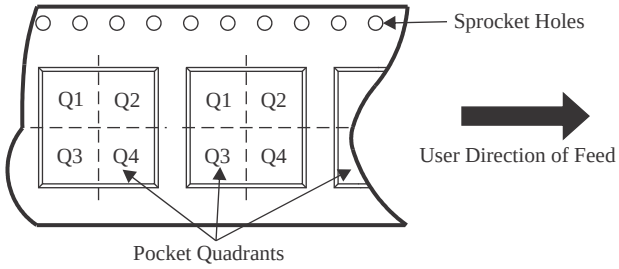


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

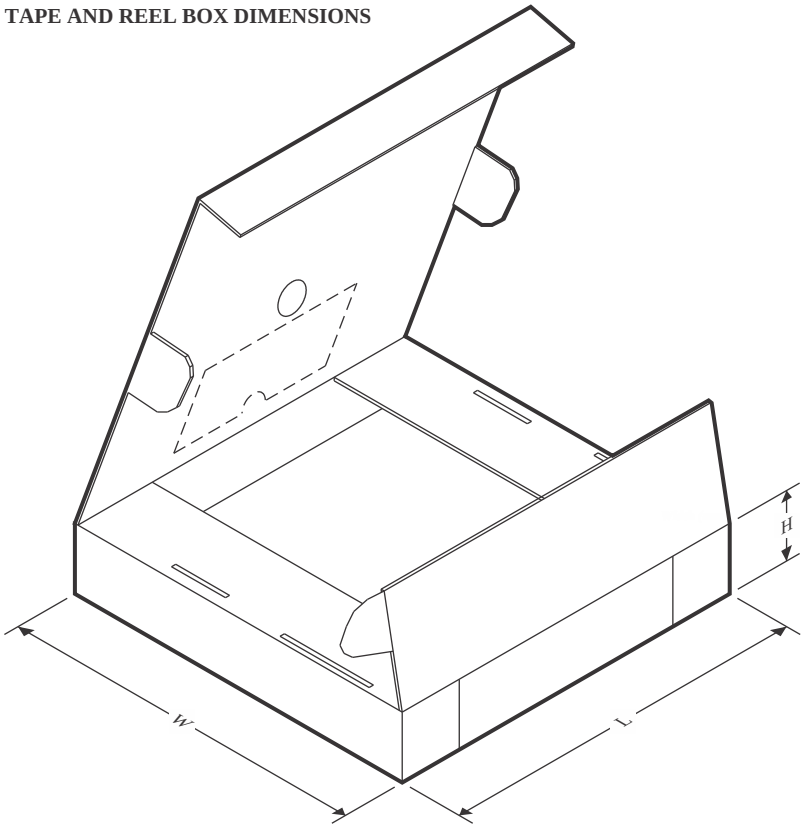
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA683IDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA683IDBVT	SOT-23	DBV	6	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA683IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

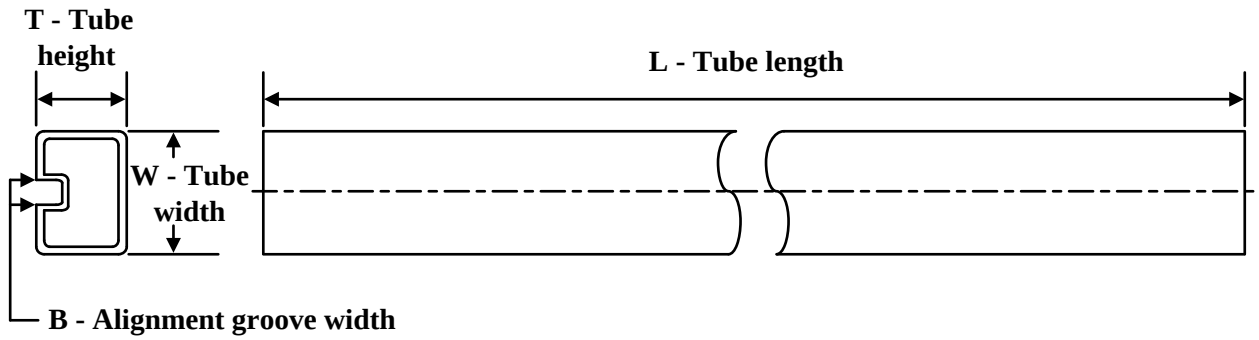
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

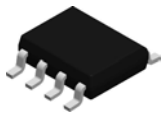
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA683IDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
OPA683IDBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
OPA683IDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA683ID	D	SOIC	8	75	506.6	8	3940	4.32

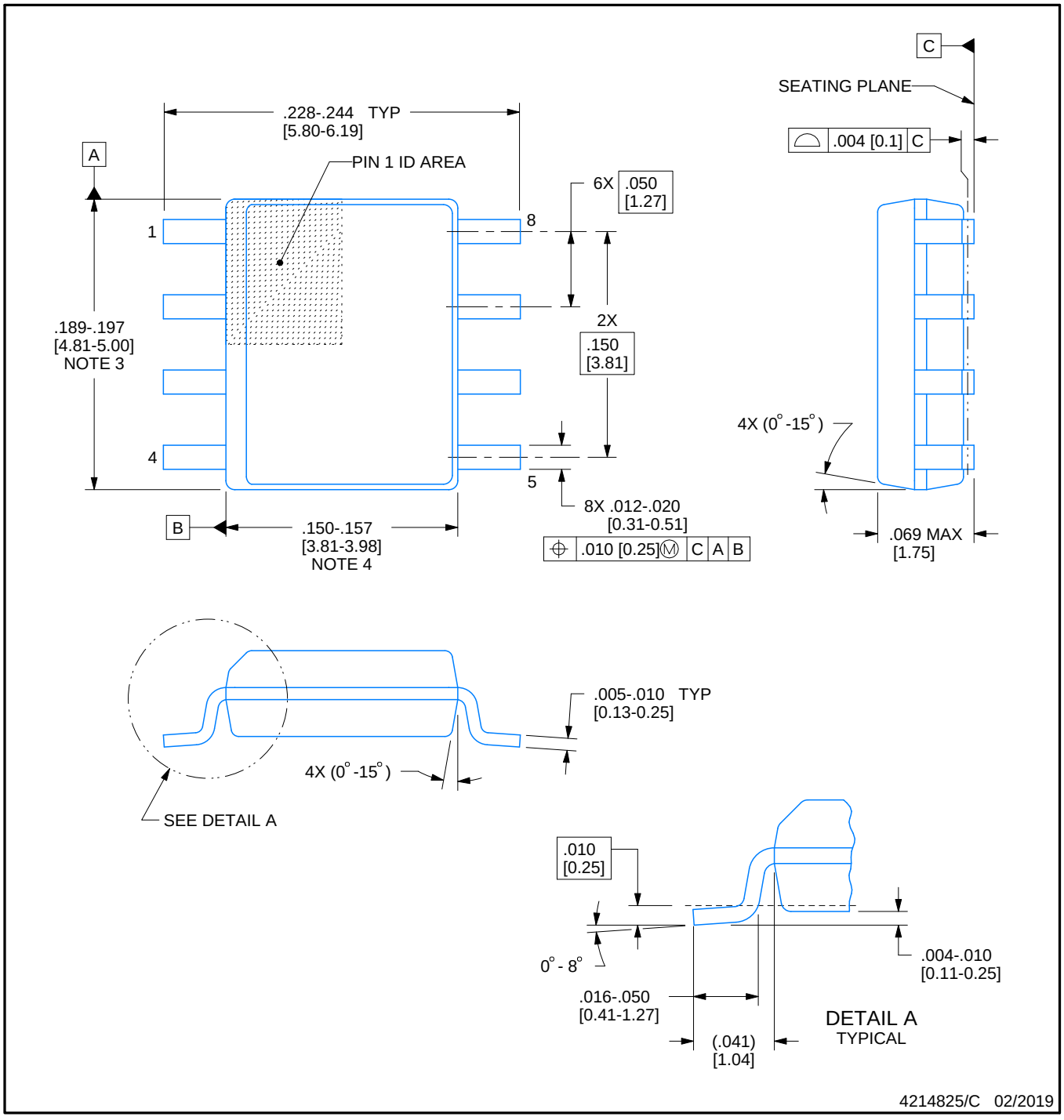


PACKAGE OUTLINE

D0008A

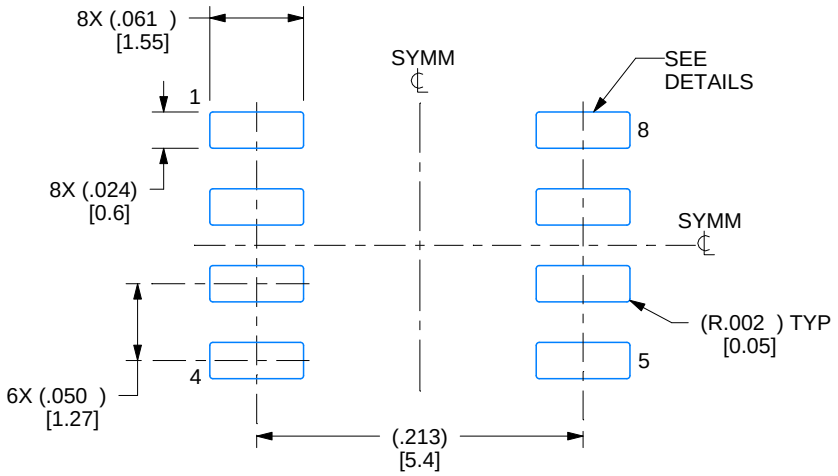
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

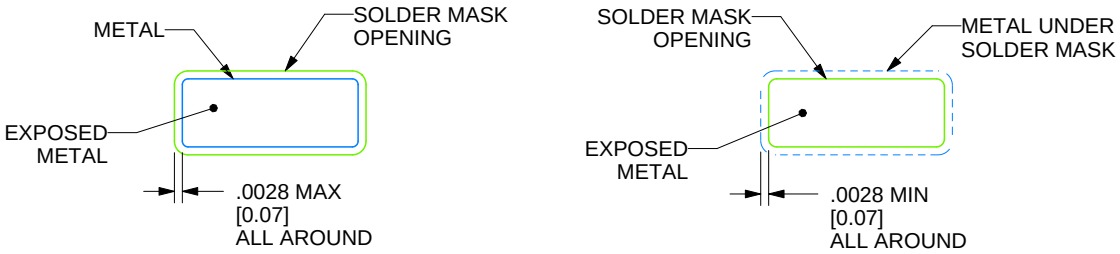


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

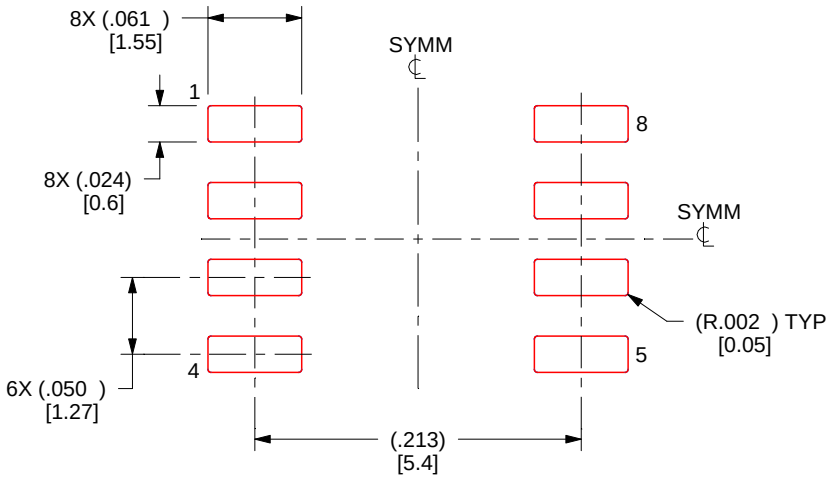
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

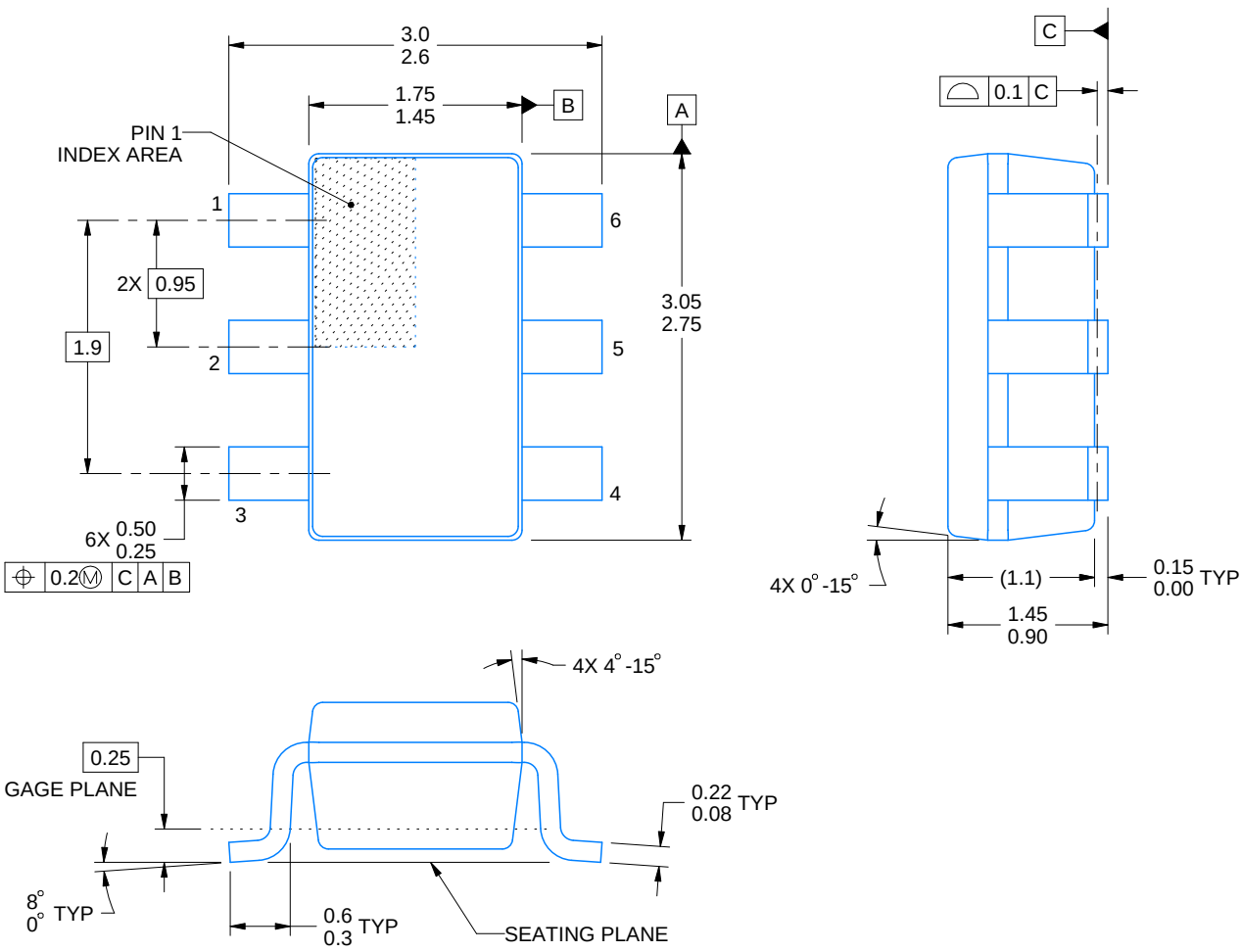
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

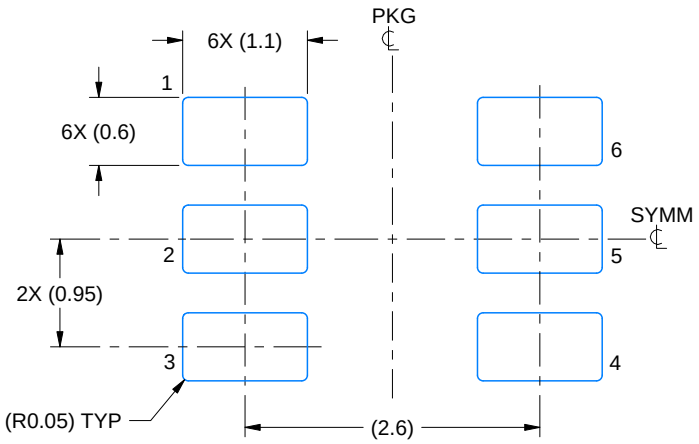
SMALL OUTLINE TRANSISTOR



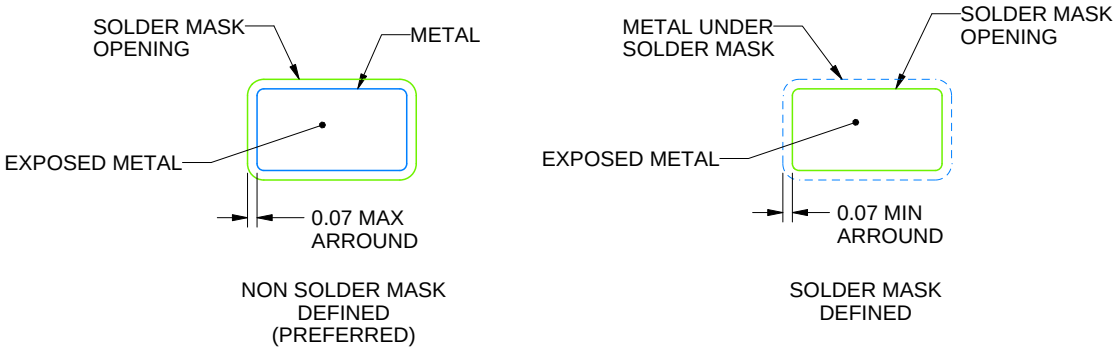
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

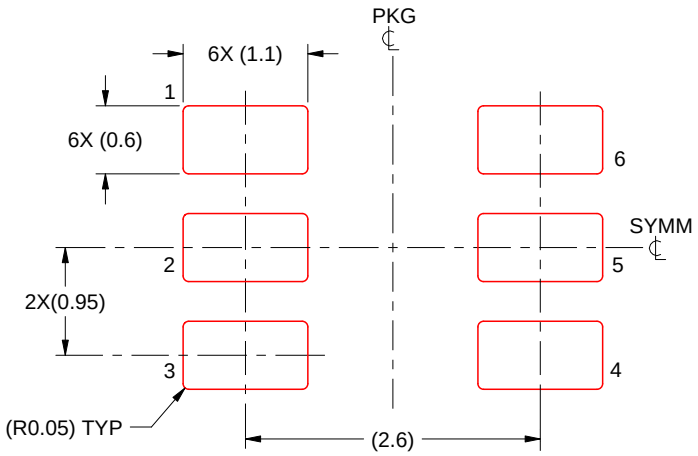


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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