3-A, 4.5-V to 14-V INPUT, NON-ISOLATED, WIDE-OUTPUT, ADJUSTABLE POWER MODULE WITH *TurboTrans*™

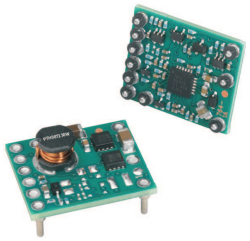
Check for Samples: PTH08T260W, PTH08T261W

FEATURES

- **Up to 3-A Output Current**
- **4.5-V to 14-V Input Voltage**
- **Wide-Output Voltage Adjust (0.69 V to 5.5 V)**
- **±1.5% Total Output Voltage Variation**
- **Efficiencies up to 95%**
- **Output Overcurrent Protection (Nonlatching, Auto-Reset)**
- **Operating Temperature: –40°C to 85°C**
- **Safety Agency Approvals**
  - **UL/IEC/CSA-C22.2 60950-1**
- **Prebias Startup**
- **On/Off Inhibit**
- **Differential Output Voltage Remote Sense**
- **Adjustable Undervoltage Lockout**
- **Auto-Track™ Sequencing**
- **Ceramic Capacitor Version (PTH08T261W)**
- **TurboTrans™ Technology**
- **Designed to meet Ultra-Fast Transient Requirements up to 300 A/µs**
- **SmartSync Technology**

APPLICATIONS

- **Complex Multi-Voltage Systems**
- **Microprocessors**
- **Bus Drivers**



DESCRIPTION

The PTH08T260/261W is the higher input voltage (4.5V to 14V) version of the PTH04T260/261W (2.2V to 5.5V), 3-A rated, non-isolated power module. This regulator represents the 2nd generation of the PTH series of power modules which include a reduced footprint and improved features. The PTH08T261W is optimized to be used in applications requiring all ceramic capacitors.

Operating from an input voltage range of 4.5V to 14V, the PTH08T260/261W requires a single resistor to set the output voltage to any value over the range, 0.69V to 5.5V. The wide input voltage range makes the PTH08T260/261W particularly suitable for advanced computing and server applications that use a loosely regulated 8-V to 12-V intermediate distribution bus. Additionally, the wide input voltage range increases design flexibility by supporting operation with tightly regulated 5-V, 8-V, or 12-V intermediate bus architectures.

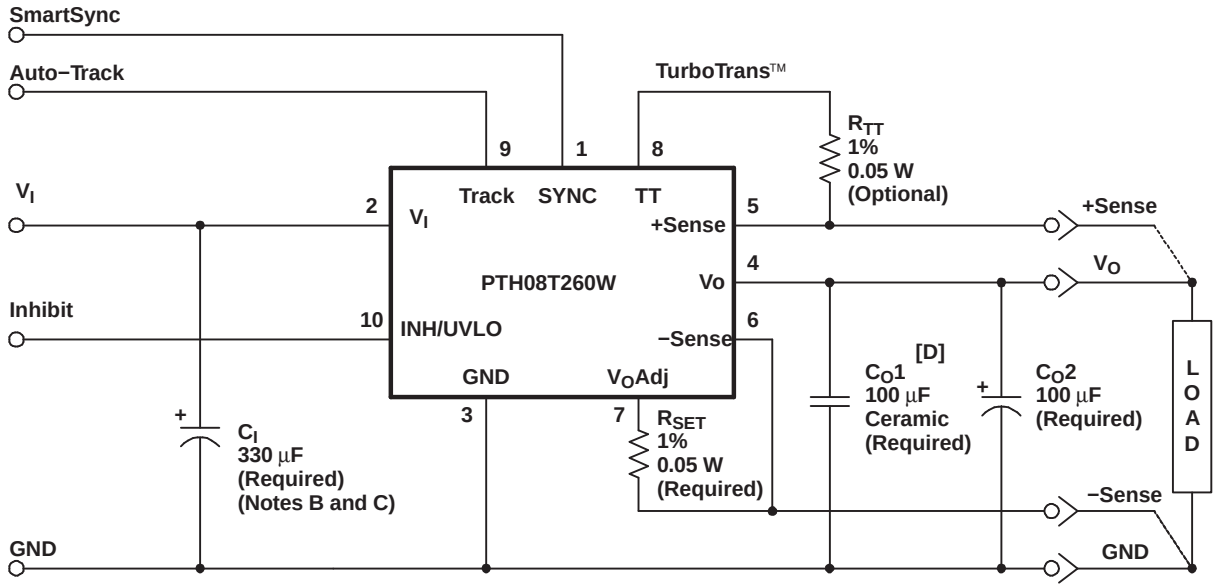
The module incorporates a comprehensive list of features. Output over-current and over-temperature shutdown protects against most load faults. A differential remote sense ensures tight load regulation. An adjustable under-voltage lockout allows the turn-on voltage threshold to be customized. Auto-Track™ sequencing is a popular feature that greatly simplifies the simultaneous power-up and power-down of multiple modules in a power system.

The PTH08T260/261W includes new patent pending technologies, **TurboTrans™** and **SmartSync**. The TurboTrans feature optimizes the transient response of the regulator while simultaneously reducing the quantity of external output capacitors required to meet a target voltage deviation specification. Additionally, for a target output capacitor bank, TurboTrans can be used to significantly improve the regulator's transient response by reducing the peak voltage deviation. SmartSync allows for switching frequency synchronization of multiple modules, thus simplifying EMI noise suppression tasks and reduces input capacitor RMS current requirements. Double-sided surface mount construction provides a low profile and compact footprint. Package options include both through-hole and surface mount configurations that are lead (Pb) - free and RoHS compatible.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PTH08T260W



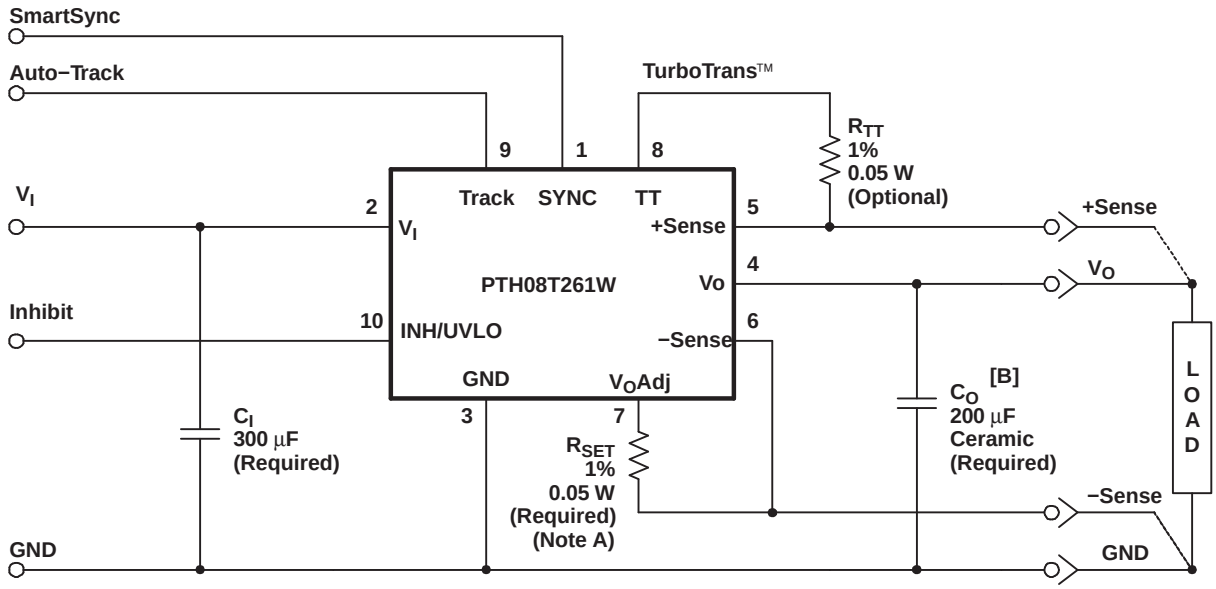
A. R_{SET} required to set the output voltage to a value higher than 0.69 V. See the *Electrical Characteristics* table.

B. An additional 22-µF ceramic input capacitor is recommended to reduce RMS ripple current.

C. For V_I greater than 8V, the minimum required C_I may be reduced to 220 µF plus a 22-µF ceramic capacitor.

D. 100 µF of output capacitance can be achieved by using two 47-µF ceramic capacitors .

PTH08T261W - Ceramic Capacitor Version



A. R_{SET} required to set the output voltage to a value higher than 0.69 V. See the *Electrical Characteristics* table.

B. 200 µF of output capacitance can be achieved by using two 100-µF ceramic capacitors or four 47-µF ceramic capacitors.

C. 300 µF of ceramic or 330 µF of electrolytic input capacitance is required for proper operation.

D. For V_I greater than 8 V, the minimum required C_I may be reduced to 200 µF ceramic or 220 µF electrolytic plus a 22-µF ceramic capacitor.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

DATASHEET TABLE OF CONTENTS

ENVIRONMENTAL AND ABSOLUTE MAXIMUM RATINGS

(Voltages are with respect to GND)

					UNIT
V_{Track}	Track pin voltage			–0.3 to V_I + 0.3	V
V_{SYNC}	SYNC pin voltage			–0.3 to 6.0	V
T_A	Operating temperature range	Over V_I range		–40 to 85	°C
T_{wave}	Wave soldering temperature	Surface temperature of module body or pins **(5 seconds maximum)**	AD suffix	260	°C
T_{reflow}	Solder reflow temperature	Surface temperature of module body or pins	AS suffix	235(1)	°C
			AZ suffix	260(1)	°C
T_{stg}	Storage temperature	Storage temperature of module removed from shipping package		–55 to 125	°C
T_{pkg}	Packaging temperature	Shipping Tray or Tape and Reel storage or bake temperature		45	°C
	Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 msec, 1/2 sine, mounted		500	G
	Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz	Suffix AD	20	G
			Suffix AS and AZ	15	G
	Weight			2.5	grams
	Flammability	Meets UL94V-O			

(1) During reflow of surface mount package version do not elevate peak temperature of the module, pins or internal components above the stated maximum.

ELECTRICAL CHARACTERISTICS

T_A =25°C, V_I = 5V, V_O = 3.3V, C_I = 330µF, C_O1 = 100µF ceramic, C_O2 = 100µF, I_O = $I_O$max (unless otherwise stated)

PARAMETER		TEST CONDITIONS			PTH08T260W			UNIT
					MIN	TYP	MAX	
I_O	Output current	Over V_O range	25°C, natural convection		0		3	A
V_I	Input voltage range	Over I_O range		0.69 ≤ V_O ≤ 1.2	4.5		14 (1)	V
				1.2 < V_O ≤ 3.6	4.5		14	
				3.6 < V_O ≤ 5.5	V_O +1 (2)		14	
V_O	Output adjust range	Over I_O range			0.69		5.5	V
	Set-point voltage tolerance						±1.0 (3)	%V_o
	Temperature variation	–40°C < T_A < 85°C				±0.25		%V_o
	Line regulaltion	Over V_I range				±3		mV
	Load regulation	Over I_O range				±2		mV
	Total output variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C					±1.5 (3)	%V_O
η	Efficiency	I_O = 3 A	R_{SET} = 169 Ω, V_I = 8.0 V, V_O = 5.0V			95%		
			R_{SET} = 1.21 kΩ, V_O = 3.3 V			92%		
			R_{SET} = 2.37 kΩ, V_O = 2.5 V			90%		
			R_{SET} = 4.75 kΩ, V_O = 1.8 V			88%		
			R_{SET} = 6.98 kΩ, V_O = 1.5 V			87%		
			R_{SET} = 12.1 kΩ, V_O = 1.2 V			85%		
			R_{SET} = 20.5 kΩ, V_O = 1.0 V			83%		
			R_{SET} = 681 kΩ, V_O = 0.7 V			79%		
	V_O Ripple (peak-to-peak)	20-MHz bandwidth				1 (1)		%V_O
I_{LIM}	Overcurrent threshold	Reset, followed by auto-recovery				5.5		A
	Transient response	2.5 A/µs load step 50% to 100% $I_O$max V_I = 12 V V_O = 3.3 V	w/o TurboTrans C_O1 = 100 µF, ceramic C_O2 = 100µF, Type B	Recovery Time		60		µSec
				V_O Overshoot		55		mV
			w/o TurboTrans (4) C_O1 = 100 µF, ceramic C_O2 = 660 µF, Type B	Recovery Time		70		µSec
				V_O Overshoot		37		mV
			with TurboTrans C_O1 = 100 µF, ceramic C_O2 = 660 µF, Type B R_{TT} = 3.4 kΩ	Recovery Time		110		µSec
				V_O Overshoot		20		mV
I_{IL}	Track input current (pin 9)	Pin to GND					-130 (5)	µA
dV_{track}/dt	Track slew rate capability	C_O ≤ C_O (max)					1	V/ms
$UVLO_{ADJ}$	Adjustable Under-voltage lockout (pin 10)	V_I increasing, R_{UVLO} = OPEN				4.3	4.45	V
		V_I decreasing, R_{UVLO} = OPEN			3.7	4.2		
		Hysteresis, R_{UVLO} ≤ 52.3 kΩ				0.5		
	Inhibit control (pin 10)	Input high voltage (V_{IH})					Open (6)	V
		Input low voltage (V_{IL})			-0.2		0.6	
		Input low current (I_{IL}), Pin 10 to GND				235		µA
I_{in}	Input standby current	Inhibit (pin 10) to GND, Track (pin 9) open				5		mA
f_s	Switching frequency	Over V_I and I_O ranges, SmartSync (pin 1) to GND				300		kHz

(1) For output voltages ≤ 1.2 V, at nominal operating frequency, the output ripple may increase (typically 2×) when operating at input voltages greater than (V_O × 11). When using the SmartSync feature to adjust the switching frequency, see the SmartSync Considerations section of the datasheet for further guidance.
(2) The minimum input voltage is 4.5V or (V_O+1)V, whichever is greater. Additional input capacitance may be required when V_I < (V_O+2)V.
(3) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/°C or better temperature stability.
(4) Without *TurboTrans*, the minimum ESR limit of 7 mΩ must not be violated.
(5) A low-leakage (<100 nA), open-drain device, such as MOSFET or voltage supervisor IC, is recommended to control pin 9. The open-circuit voltage is less than 6.5 Vdc.
(6) This control pin has an internal pull-up. Do not place an external pull-up on this pin. If it is left open-circuit, the module operates when input power is applied. A small, low-leakage (<100 nA) MOSFET is recommended for control. For additional information, see the related application information section.

ELECTRICAL CHARACTERISTICS (continued)

T_A =25°C, V_I = 5V, V_O = 3.3V, C_I = 330µF, C_O1 = 100µF ceramic, C_O2 = 100µF, I_O = $I_O$max (unless otherwise stated)

PARAMETER		TEST CONDITIONS			PTH08T260W			
					MIN	TYP	MAX	UNIT
f_{SYNC}	Synchronization (SYNC) frequency	SmartSync Control			240		400	kHz
V_{SYNCH}	SYNC High-Level Input Voltage				2		5.5	V
V_{SYNCL}	SYNC Low-Level Input Voltage						0.8	V
t_{SYNC}	SYNC Minimum Pulse Width				200			nSec
C_I	External input capacitance				330 (7)			µF
C_O	External output capacitance	without TurboTrans	Capacitance value	Nonceramic	100 (8)		5000 (9)	µF
				Ceramic	100 (8)		500	
			Equivalent series resistance (non-ceramic)		7			mΩ
		with Turbotrans	Capacitance value		see table (10)		10,000 (11)	µF
			Capacitance × ESR product (C_O × ESR)		1000		10,000	µF×mΩ
MTBF	Reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign			6.7			10^6 Hr

(7) A 330 µF electrolytic input capacitor is required for proper operation. The capacitor must be rated for a minimum of 450 mA rms of ripple current. An additional 22-µF ceramic input capacitor is recommended to reduce rms ripple current. When operating at V_I > 8V, the minimum required C_I may be reduced to a 220-µF electrolytic plus a 22-µF ceramic.

(8) 100 µF ceramic & 100 µF non-ceramic external output capacitance is required for basic operation. The 100 µF required ceramic output capacitance can be made up of 2 × 47 µF. The minimum output capacitance requirement increases when *TurboTrans*™ (TT) technology is used. See the Application Information for more guidance.

(9) This is the calculated maximum disregarding *TurboTrans*™ technology. When the *TurboTrans* feature is used, the minimum output capacitance must be increased. See the *TurboTrans* application notes for further guidance.

(10) When using *TurboTrans*™ technology, a minimum value of output capacitance is required for proper operation. Additionally, low ESR capacitors are required for proper operation. See the *TurboTrans* application notes for further guidance.

(11) This is the calaculated maximum when using the *TurboTrans* feature. Additionally, low ESR capacitors are required for proper operation. See the *TurboTrans* application notes for further guidance.

ELECTRICAL CHARACTERISTICS

T_A =25°C, V_I = 5 V, V_O = 3.3 V, C_I = 330 µF, C_O1 = 200 µF ceramic, and I_O = I_O max (unless otherwise stated)

PARAMETER		TEST CONDITIONS			PTH08T261W			UNIT
					MIN	TYP	MAX	
I_O	Output current	Over V_O range	25°C, natural convection		0		3	A
V_I	Input voltage range	Over I_O range		0.69 ≤ V_O ≤ 1.2	4.5		14 (1)	V
				1.2 < V_O ≤ 3.6	4.5		14	
				3.6 < V_O ≤ 5.5	V_O +1 (2)		14	
V_O	Output adjust range	Over I_O range			0.69		5.5	V
	Set-point voltage tolerance						±1.0 (3)	%V_o
	Temperature variation	–40°C < T_A < 85°C				±0.25		%V_o
	Line regulaltion	Over V_I range				±3		mV
	Load regulation	Over I_O range				±2		mV
	Total output variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C					±1.5 (3)	%V_O
η	Efficiency	I_O = 3 A	R_{SET} = 169 Ω, V_I = 8.0 V, V_O = 5.0V			95%		
			R_{SET} = 1.21 kΩ, V_O = 3.3 V			92%		
			R_{SET} = 2.37 kΩ, V_O = 2.5 V			90%		
			R_{SET} = 4.75 kΩ, V_O = 1.8 V			88%		
			R_{SET} = 6.98 kΩ, V_O = 1.5 V			87%		
			R_{SET} = 12.1 kΩ, V_O = 1.2 V			85%		
			R_{SET} = 20.5 kΩ, V_O = 1.0 V			83%		
			R_{SET} = 681 kΩ, V_O = 0.7 V			79%		
	V_O Ripple (peak-to-peak)	20-MHz bandwidth				1 (1)		%V_O
I_{LIM}	Overcurrent threshold	Reset, followed by auto-recovery				5.5		A
	Transient response	2.5 A/µs load step 50% to 100% $I_O$max V_I = 12 V V_O = 3.3 V	w/o TurboTrans C_O1 = 200 µF, ceramic	Recovery Time		50		µSec
				V_O Overshoot		43		mV
			w/o TurboTrans (4) C_O1 = 400 µF, ceramic	Recovery Time		70		µSec
				V_O Overshoot		38		mV
			with TurboTrans C_O1 = 400 µF, ceramic R_{TT} = 8.06 kΩ	Recovery Time		130		µSec
				V_O Overshoot		23		mV
I_{IL}	Track input current (pin 9)	Pin to GND					-130 (5)	µA
dV_{track}/dt	Track slew rate capability	C_O ≤ C_O (max)					1	V/ms
$UVLO_{ADJ}$	Adjustable Under-voltage lockout (pin 10)	V_I increasing, R_{UVLO} = OPEN				4.3	4.45	V
		V_I decreasing, R_{UVLO} = OPEN			3.7	4.2		
		Hysteresis, R_{UVLO} ≤ 52.3 kΩ				0.5		
	Inhibit control (pin 10)	Input high voltage (V_{IH})					Open (6)	V
		Input low voltage (V_{IL})			-0.2		0.6	
		Input low current (I_{IL}), Pin 10 to GND				235		µA
I_{in}	Input standby current	Inhibit (pin 10) to GND, Track (pin 9) open				5		mA
f_s	Switching frequency	Over V_I and I_O ranges, SmartSync (pin 1) to GND				300		kHz
f_{SYNC}	Synchronization (SYNC) frequency	SmartSync Control			240		400	kHz
V_{SYNCH}	SYNC High-Level Input Voltage				2		5.5	V
V_{SYNCL}	SYNC Low-Level Input Voltage						0.8	V
t_{SYNC}	SYNC Minimum Pulse Width				200			nSec

(1) For output voltages ≤ 1.2 V, at nominal operating frequency, the output ripple may increase (typically 2×) when operating at input voltages greater than (V_O × 11). When using the SmartSync feature to adjust the switching frequency, see the SmartSync Considerations section of the datasheet for further guidance.
(2) The minimum input voltage is 4.5V or (V_O+1)V, whichever is greater. Additional input capacitance may be required when V_I < (V_O+2)V.
(3) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1% with 100 ppm/°C or better temperature stability.
(4) Without *TurboTrans*, the minimum ESR limit of 7 mΩ must not be violated.
(5) A low-leakage (<100 nA), open-drain device, such as MOSFET or voltage supervisor IC, is recommended to control pin 9. The open-circuit voltage is less than 6.5 Vdc.
(6) This control pin has an internal pull-up. Do not place an external pull-up on this pin. If it is left open-circuit, the module operates when input power is applied. A small, low-leakage (<100 nA) MOSFET is recommended for control. For additional information, see the related application information section.

ELECTRICAL CHARACTERISTICS (continued)

T_A =25°C, V_I = 5 V, V_O = 3.3 V, C_I = 330 µF, C_O1 = 200 µF ceramic, and I_O = I_O max (unless otherwise stated)

PARAMETER		TEST CONDITIONS			PTH08T261W			
					MIN	TYP	MAX	UNIT
C_I	External input capacitance				300 (7)			µF
C_O	External output capacitance	without TurboTrans	Capacitance value	Ceramic	200 (8)		5000	µF
		with Turbotrans	Capacitance value	Ceramic	see table (9)		5000 (10)	µF
			Capacitance × ESR product (C_O × ESR)		100		1000	µF×mΩ
MTBF	Reliability	Per Telcordia SR-332, 50% stress, T_A = 40°C, ground benign			6.7			10^6 Hr

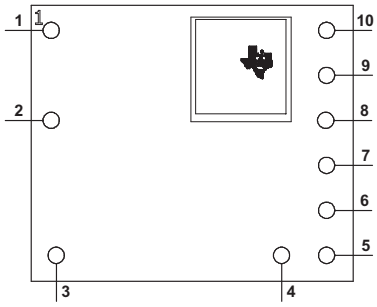
(7) 300 µF of ceramic or 330 µF of electrolytic input capacitance is required for proper operation. Electrolytic capacitance must be rated for a minimum of 450 mA rms of ripple current. An additional 22-µF ceramic input capacitor is recommended to reduce rms ripple current. When operating at V_I > 8V, the minimum required C_I may be reduced to 200 µF of ceramic or a 220-µF electrolytic plus a 22-µF ceramic.

(8) 200 µF ceramic external output capacitance is required for basic operation. The required ceramic output capacitance can be made up of 2 × 100 µF or 4 × 47 µF. The minimum output capacitance requirement increases when *TurboTrans*™ (TT) technology is used. See the Application Information for more guidance.

(9) When using *TurboTrans*™ technology, a minimum value of output capacitance is required for proper operation. Additionally, low ESR capacitors are required for proper operation. See the *TurboTrans* application notes for further guidance.

(10) This is the calaculated maximum when using the *TurboTrans* feature. Additionally, low ESR capacitors are required for proper operation. See the *TurboTrans* application notes for further guidance.

PTH08T260/261W
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
V_I	2	The positive input voltage power node to the module, which is referenced to common GND.
V_O	4	The regulated positive power output with respect to the GND.
GND	3	This is the common ground connection for the V_I and V_O power connections. It is also the 0 Vdc reference for the control inputs.
Inhibit and UVLO(1)	10	The Inhibit pin is an open-collector/drain, negative logic input that is referenced to GND. Applying a low level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module produces an output whenever a valid input source is applied. This pin is also used for input undervoltage lockout (UVLO) programming. Connecting a resistor from this pin to GND (pin 3) allows the ON threshold of the UVLO to be adjusted higher than the default value. For more information, see the Application Information section.
V_O Adjust	7	A 0.05 W 1% resistor must be directly connected between this pin and pin 6 (– Sense) to set the output voltage to a value higher than 0.69 V. The temperature stability of the resistor should be 100 ppm/°C (or better). The setpoint range for the output voltage is from 0.69 V to 5.5 V. If left open circuit, the output voltage will default to its lowest value. For further information, on output voltage adjustment see the related application note. The specification table gives the preferred resistor values for a number of standard output voltages.
+ Sense	5	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy, +Sense must be connected to V_O, close to the load.
– Sense	6	The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy, –Sense must be connected to GND (pin 3), very close to the module (within 10 cm).
Track	9	This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range the module's output voltage follows the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, this input should be connected to V_I. NOTE: Due to the undervoltage lockout feature, the output of the module cannot follow its own input voltage during power up. For more information, see the related application note.
TurboTrans™	8	This input pin adjusts the transient response of the regulator. To activate the TurboTrans feature, a 1%, 0.05 W resistor must be connected between this pin and pin 5 (+Sense) very close to the module. For a given value of output capacitance, a reduction in peak output voltage deviation is achieved by using this feature. If unused, this pin must be left open-circuit. The resistance requirement can be selected from the TurboTrans resistor table in the Application Information section. External capacitance must never be connected to this pin unless the TurboTrans resistor is a short, 0Ω.
SmartSync	1	This input pin sychronizes the switching frequency of the module to an external clock frequency. The SmartSync feature can be used to sychronize the switching fequency of multiple PTH08T260/261W modules, aiding EMI noise suppression efforts. If unused, this pin should be connected to GND (pin 3). For more information, please review the Application Information section.

(1) Denotes negative logic: Open = Normal operation, Ground = Function active

TYPICAL CHARACTERISTICS(1) (2)

CHARACTERISTIC DATA (V_{IN} = 12 V)

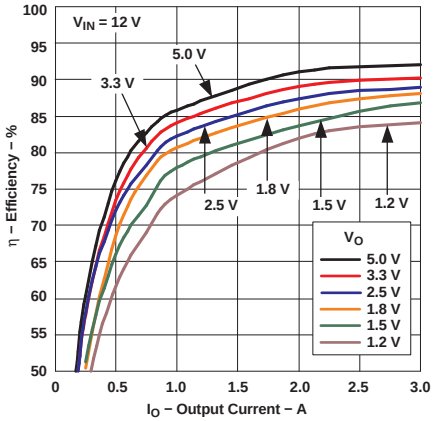


Figure 1. Efficiency vs. Output Current

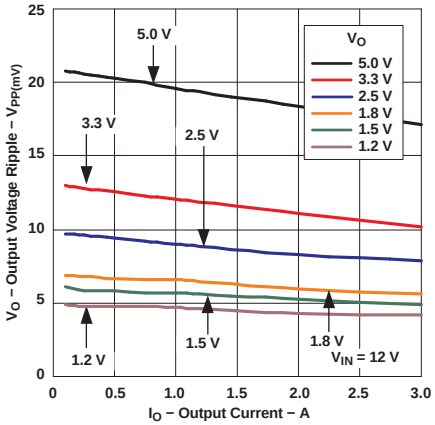


Figure 2. Output Ripple vs. Output Current

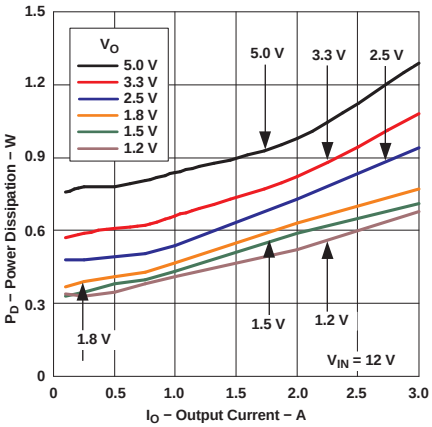


Figure 3. Power Dissipation vs. Output Current

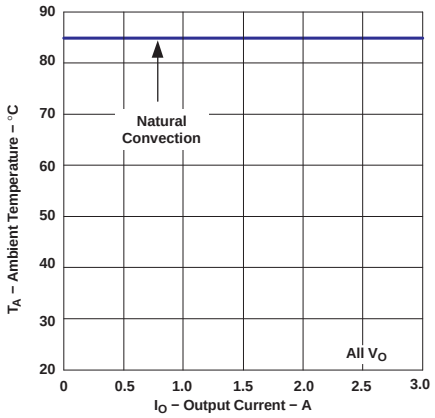


Figure 4. Ambient Temperature vs. Output Current

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 1, Figure 2, and Figure 3.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. Applies to Figure 4 .

TYPICAL CHARACTERISTICS(1) (2)

CHARACTERISTIC DATA (V_{IN} = 5 V)

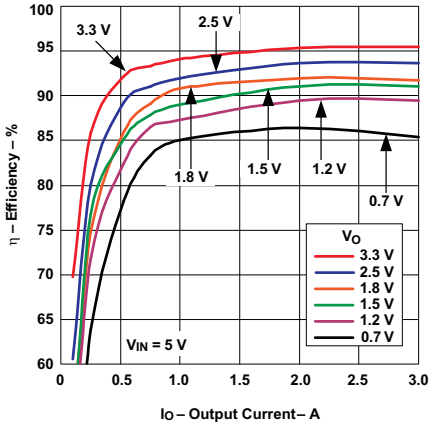


Figure 5. Efficiency vs. Output Current

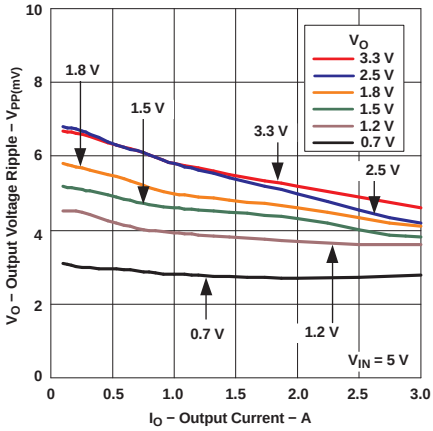


Figure 6. Output Ripple vs. Output Current

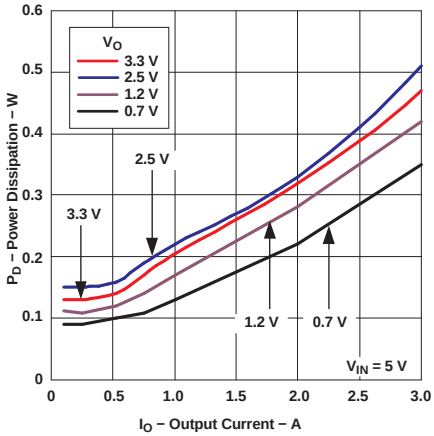


Figure 7. Power Dissipation vs. Output Current

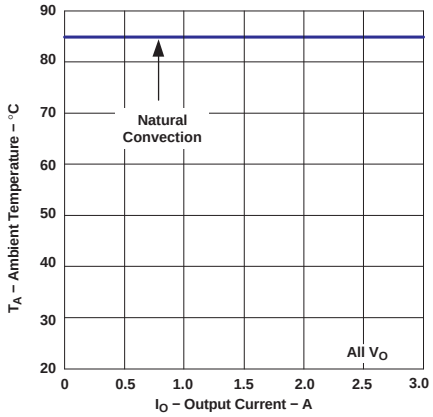


Figure 8. Ambient Temperature vs. Output Current

(1) The electrical characteristic data has been developed from actual products tested at 25°C. This data is considered typical for the converter. Applies to Figure 5, Figure 6, and Figure 7.

(2) The temperature derating curves represent the conditions at which internal components are at or below the manufacturer's maximum operating temperatures. Derating limits apply to modules soldered directly to a 100 mm x 100 mm double-sided PCB with 2 oz. copper. Applies to Figure 8.

APPLICATION INFORMATION

ADJUSTING THE OUTPUT VOLTAGE

The V_O Adjust control (pin 7) sets the output voltage of the PTH08T260/261W. The adjustment range is 0.69 V to 5.5 V. The adjustment method requires the addition of a single external resistor, R_{SET}, that must be connected directly between the V_O Adjust and the –Sense pins. Table 1 gives the standard value of the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

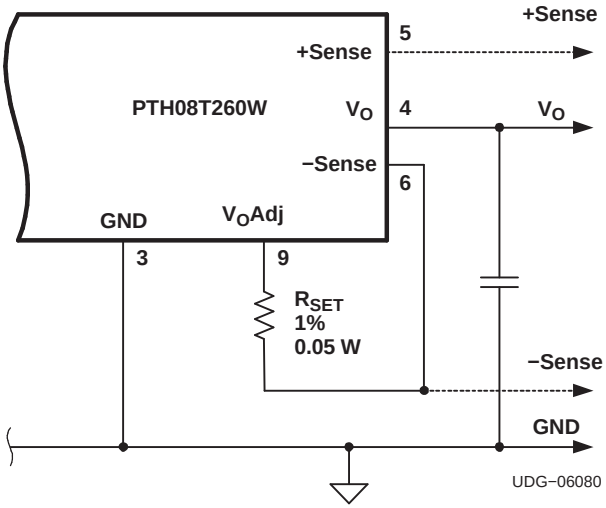
For other output voltages, the required resistor value can either be calculated using the following formula, or simply selected from the values given in Table 2. Figure 9 shows the placement of the required resistor.

$$R_{SET} = 10\ k\Omega \times \frac{0.69}{V_O - 0.69} - 1.43\ k\Omega \quad (1)$$

Table 1. Preferred Values of R_{SET} for Standard Output Voltages

V_O (Standard) (V)	R_{SET} (Standard Value) (kΩ)	V_O (Actual) (V)
5.0 (1)	0.169	5.01
3.3	1.2	3.30
2.5	2.37	2.51
1.8	4.7	1.81
1.5	6.98	1.51
1.2 (2)	12.1	1.20
1.0 (2)	20.5	1.01
0.7 (2)	681	0.70

(1) For V_O > 3.6 V, the minimum input voltage is (V_O + 2) V.
(2) For output voltages ≤ 1.2V, at nominal operating frequency, the output ripple may increase (typically 2×) when operating at input voltages greater than (V_O × 11). When using the SmartSync feature, review the SmartSync application section for further guidance.



(1) **R_{SET}:** Use a 0.05 W resistor with a tolerance of 1% and temperature stability of 100 ppm/°C (or better). Connect the resistor directly between pins 7 and 6, as close to the regulator as possible, using dedicated PCB traces.

(2) Never connect capacitors from V_O Adjust to either GND, V_O, or +Sense. Any capacitance added to the V_O Adjust pin affects the stability of the regulator.

Figure 9. V_O Adjust Resistor Placement

Table 2. Output Voltage Set-Point Resistor Values

V_O Required	R_{SET} (Ω)	V_O Required (V)	R_{SET} (Ω)
0.70	681 k	3.00	1.54 k
0.75	113 k	3.10	1.43 k
0.80	61.9 k	3.20	1.33 k
0.85	41.2 k	3.30	1.21 k
0.90	31.6 k	3.40	1.13 k
0.95	24.9 k	3.50	1.02 k
1.00	20.5 k	3.60	931
1.10	15.4 k	3.70	866
1.20	12.1 k	3.80	787
1.30	9.88 k	3.90	715
1.40	8.25 k	4.00	649
1.50	6.98 k	4.10	590
1.60	6.04 k	4.20	536
1.70	5.36 k	4.30	475
1.80	4.75 k	4.40	432
1.90	4.22 k	4.50	383
2.00	3.83 k	4.60	332
2.10	3.40 k	4.70	287
2.20	3.09 k	4.80	249
2.30	2.87 k	4.90	210
2.40	2.61 k	5.00	169
2.50	2.37 k	5.10	133
2.60	2.15 k	5.20	100
2.70	2.00 k	5.30	66.5
2.80	1.82 k	5.40	34.8
2.90	1.69 k	5.50	4.99

CAPACITOR RECOMMENDATIONS FOR THE PTH08T260/261W POWER MODULE

Capacitor Technologies

Electrolytic Capacitors

When using electrolytic capacitors, high quality, computer-grade electrolytic capacitors are recommended. Aluminum electrolytic capacitors provide adequate decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable when ambient temperatures are above -20°C. For operation below -20°C, tantalum, ceramic, or OS-CON type capacitors are required.

Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors is less effective. Multilayer ceramic capacitors have a low ESR and a resonant frequency higher than the bandwidth of the regulator. They can be used to reduce the reflected ripple current at the input as well as improve the transient response of the output.

Tantalum, Polymer-Tantalum Capacitors

Tantalum type capacitors may only used on the output bus, and are recommended for applications where the ambient operating temperature is less than 0°C. The AVX TPS series and Kemet capacitor series are suggested over many other tantalum types due to their lower ESR, higher rated surge, power dissipation, and ripple current capability. Tantalum capacitors that have no stated ESR or surge current rating are not recommended for power applications.

Input Capacitor (Required)

The PTH08T261W requires a minimum input capacitance of 300 µF of ceramic type.

The PTH08T260W requires a minimum input capacitance of 330 µF. The ripple current rating of the capacitor must be at least 350 mArms. An optional 22-µF X5R/X7R ceramic capacitor is recommended to reduce the RMS ripple current. When operating with an input voltage greater than 8 V, the minimum required input capacitance may be reduced to a 220-µF electrolytic plus a 22-µF ceramic.

Input Capacitor Information

The size and value of the input capacitor is determined by the converter's transient performance capability. This minimum value assumes that the converter is supplied with a responsive, low inductance input source. This source should have ample capacitive decoupling, and be distributed to the converter via PCB power and ground planes.

Ceramic capacitors should be located as close as possible to the module's input pins, within 0.5 inch (1,3 cm). Adding ceramic capacitance is necessary to reduce the high-frequency ripple voltage at the module's input. This will reduce the magnitude of the ripple current through the electroytic capacitor, as well as the amount of ripple current reflected back to the input source. Additional ceramic capacitors can be added to further reduce the RMS ripple current requirement for the electrolytic capacitor.

Increasing the minimum input capacitance to 680 µF is recommended for high-performance applications, or wherever the input source performance is degraded.

The main considerations when selecting input capacitors are the RMS ripple current rating, temperature stability, and less than 100 mΩ of equivalent series resistance (ESR).

Regular tantalum capacitors are not recommended for the input bus. These capacitors require a recommended minimum voltage rating of 2 × (maximum dc voltage + ac ripple). This is standard practice to ensure reliability. No tantalum capacitors were found with a sufficient voltage rating to meet this requirement.

When the operating temperature is below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, OS-CON, poly-aluminum, and polymer-tantalum types should be considered.

Output Capacitor (Required)

The PTH08T261W requires a minimum output capacitance of 200 µF of ceramic type.

The PTH08T260W requires a minimum output capacitance of 100 µF ceramic and 100 µF non-ceramic. Additional non-ceramic, low-ESR capacitance is recommended for improved performance. See the Electrical Characteristics table for maximum capacitor limits.

The required capacitance above the minimum will be determined by actual transient deviation requirements. See the TurboTrans Technology application section within this document for specific capacitance selection.

Output Capacitor Information

When selecting output capacitors, the main considerations are capacitor type, temperature stability, and ESR. When using the TurboTrans feature, the capacitance x ESR product should also be considered (see the following section).

Ceramic output capacitors added for high-frequency bypassing should be located as close as possible to the load to be effective. Ceramic capacitor values below 10 µF should not be included when calculating the total output capacitance value.

When the operating temperature is below 0°C, the ESR of aluminum electrolytic capacitors increases. For these applications, OS-CON, poly-aluminum, and polymer-tantalum types should be considered.

TurboTrans Output Capacitance

TurboTrans allows the designer to optimize the output capacitance according to the system transient design requirement. High quality, ultra-low ESR capacitors are required to maximize TurboTrans effectiveness. When using TurboTrans, the capacitor's capacitance (in µF) × ESR (in mΩ) product determines its capacitor type; Type A, B, or C. These three types are defined as follows:

Type A = (100 ≤ capacitance × ESR ≤ 1000) (e.g. ceramic)

Type B = (1000 < capacitance × ESR ≤ 5000) (e.g. polymer-tantalum)

Type C = (5000 < capacitance × ESR ≤ 10,000) (e.g. OS-CON)

When using more than one type of output capacitor, select the capacitor type that makes up the majority of your total output capacitance. When calculating the C × ESR product, use the maximum ESR value from the capacitor manufacturer's data sheet.

Working Examples:

A capacitor with a capacitance of 330 µF and an ESR of 5 mΩ, has a C × ESR product of 1650 µF x mΩ (330 × 5). This is a Type B capacitor. A capacitor with a capacitance of 1000 µF and an ESR of 8 mΩ, has a C × ESR product of 8000 µF x mΩ (1000 × 8). This is a Type C capacitor.

See the TurboTrans Technology application section within this document for specific capacitance selection.

Table 3 includes a preferred list of capacitors by type and vendor. See the Output Bus / TurboTrans column.

Non-TurboTrans Output Capacitance

If the TurboTrans feature is not used, minimum ESR and maximum capacitor limits must be followed. System stability may be effected and increased output capacitance may be required without TurboTrans.

When using the PTH08T260W without the TurboTrans feature, observe the minimum ESR of the entire output capacitor bank. The minimum ESR limit of the output capacitor bank is 7 mΩ. A list of preferred low-ESR type capacitors, are identified in Table 3. Large amounts of capacitance may reduce system stability when not using the TurboTrans feature.

When using the PTH08T261W without the TurboTrans feature, the maximum amount of capacitance is tbd µF of ceramic type. Large amounts of capacitance may reduce system stability.

Using the TurboTrans feature improves system stability, improves transient response, and reduces the amount of output capacitance required to meet system transient design requirements.

Designing for Fast Load Transients

The transient response of the dc/dc converter has been characterized using a load transient with a di/dt of 2.5 A/µs. The typical voltage deviation for this load transient is given in the Electrical Characteristics table using the minimum required value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc/dc converter once the speed of the transient exceeds its bandwidth capability.

If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional low ESR ceramic capacitor decoupling. Generally, with load steps greater than 100 A/µs, adding multiple 10 µF ceramic capacitors plus 10 × 1 µF, and numerous high frequency ceramics (≤ 0.1 µF) is all that is required to soften the transient higher frequency edges. The PCB location of these capacitors in relation to the load is critical. DSP, FPGA and ASIC vendors identify types, location and amount of capacitance required for optimum performance. Low impedance buses, unbroken PCB copper planes, and components located as close as possible to the high frequency devices are essential for optimizing transient performance.

Table 3. Input/Output Capacitors (1)

Capacitor Vendor, Type Series (Style)	Capacitor Characteristics					Quantity			Vendor Part No.
	Working Voltage	Value (µF)	Max. ESR at 100 kHz	Max Ripple Current at 85°C (Irms)	Physical Size (mm)	Input Bus	Output Bus (2)		
							No Turbo-Trans	Turbo-Trans Cap Type (3)	
Panasonic									
FC (Radial)	25 V	1000	43mΩ	1690mA	16 × 15	1	≥ 2	N/R (4)	EEUFC1E102S
FC (Radial)	25 V	820	38mΩ	1655mA	12 × 20	1	≥ 1	N/R (4)	EEUFC1E821S
FC (SMD)	35 V	470	43mΩ	1690mA	16 × 16,5	1	≥ 1	N/R (4)	EEVFC1V471N
FK (SMD)	35 V	1000	35mΩ	1800mA	16 ×16,5	1	≥ 2	N/R (4)	EEVFK1V102M
United Chemi-Con									
PTB, Poly-Tantalum(SMD)	6.3 V	330	25mΩ	2600mA	7,3×4,3×2.8	N/R (5)	1 ~ 4	C ≥ 2 (6)	6PTB337MD6TER (V_O≤ 5.1V) (7)
LXZ, Aluminum (Radial)	35 V	680	38mΩ	1660mA	12,5 × 20	1	1 ~ 3	N/R (4)	LXZ35VB681M12X20LL
PS, Poly-Alum (Radial)	16 V	330	14mΩ	5060mA	10 × 12,5	1	1 ~ 3	B ≥ 2 (6)	16PS330MJ12
PS, Poly-Alum (Radial)	6.3 V	390	12mΩ	5500mA	8 × 12,5	N/R (5)	1 ~ 2	B ≥ 1 (6)	6PS390MH11 (V_O≤ 5.1V) (7)
PXA, Poly-Alum (SMD)	16 V	330	14mΩ	5050mA	10 × 12,2	1	1 ~ 3	B ≥ 2 (6)	PXA16VC331MJ12TP
PXA, Poly-Alum (Radial)	10 V	330	14mΩ	4420mA	8 × 12,2	N/R (5)	1 ~ 2	B ≥ 1 (6)	PXA10VC331MH12
Nichicon, Aluminum									
PM (Radial)	25 V	1000	43mΩ	1520mA	18 × 15	1	≥ 2	N/R (4)	UPM1E102MHH6
HD (Radial)	35 V	470	23mΩ	1820mA	10 × 20	1	≥ 2	N/R (4)	UHD1V471HR
Panasonic, Poly-Aluminum	2.0 V	390	5mΩ	4000mA	7,3×4,3×4,2	N/R (5)	N/R (8)	B ≥ 2 (6)	EEFSE0J391R(V_O≤ 1.6V) (7)

(1) **Capacitor Supplier Verification**
Please verify availability of capacitors identified in this table. Capacitor suppliers may recommend alternative part numbers because of limited availability or obsolete products.
RoHS, Lead-free and Material Details
See the capacitor suppliers regarding material composition, RoHS status, lead-free status, and manufacturing process requirements. Component designators or part number deviations can occur when material composition or soldering requirements are updated.
(2) Additional output capacitance must include the required 200 µF of ceramic type.
(3) Required capacitors with TurboTrans. See the TurboTrans Application information for Capacitor Selection
Capacitor Types:
(a) Type A = (100 < capacitance × ESR ≤ 1000)
(b) Type B = (1,000 < capacitance × ESR ≤ 5,000)
(c) Type C = (5,000 < capacitance × ESR ≤ 10,000)
(4) Aluminum Electrolytic capacitor not recommended for the TurboTrans due to higher ESR × capacitance products. Aluminum and higher ESR capacitors can be used in conjunction with lower ESR capacitance.
(5) N/R – Not recommended. The voltage rating does not meet the minimum operating limits.
(6) Required capacitors with TurboTrans. See the TurboTrans Application information for Capacitor Selection
Capacitor Types:
(a) Type A = (100 < capacitance × ESR ≤ 1000)
(b) Type B = (1,000 < capacitance × ESR ≤ 5,000)
(c) Type C = (5,000 < capacitance × ESR ≤ 10,000)
(7) The voltage rating of this capacitor only allows it to be used for output voltage that is equal to or less than 80% of the working voltage.
(8) N/R – Not recommended. The ESR value of this capacitor is below the required minimum when not using TurboTrans.

Table 3. Input/Output Capacitors(1) (continued)

Capacitor Vendor, Type Series (Style)	Capacitor Characteristics					Quantity			Vendor Part No.
	Working Voltage	Value (µF)	Max. ESR at 100 kHz	Max Ripple Current at 85°C (Irms)	Physical Size (mm)	Input Bus	Output Bus (2)		
							No Turbo-Trans	Turbo-Trans Cap Type(3)	
Sanyo									
TPE, Poscap (SMD)	10 V	330	25mΩ	3300mA	7,3×4,3	N/R(9)	1 ~ 3	C ≥ 1(10)	10TPE330MF(11)
TPE, Poscap (SMD)	2.5 V	470	7mΩ	4400mA	7,3×4,3	N/R(9)	1 ~ 2	B ≥ 2(10)	2R5TPE470M7(V_O≤ 1.8V)(11)
TPD, Poscap (SMD)	2.5 V	1000	5mΩ	6100mA	7,3×4,3	N/R(9)	N/R(12)	B ≥ 1(10)	2R5TPD1000M5(V_O≤ 1.8V)(11)
SEP, OS-CON (Radial)	16 V	330	16mΩ	4700mA	10 × 13	1	1 ~ 2	B ≥ 1(10)	16SEP330M
SEPC, OS-CON (Radial)	16 V	470	10mΩ	6100mA	10 × 13	1	1 ~ 2	B ≥ 2(10)	16SEPC470M
SVP, OS-CON (SMD)	16 V	330	16mΩ	4700mA	10 × 12,6	1	1 ~ 2	B ≥ 1(10)	16SVP330M
AVX, Tantalum									
TPM Multianode	10 V	330	23mΩ	3000mA	7,3×4,3×4,1	N/R(9)	1 ~ 3	C ≥ 2(10)	TPME337M010R0035
TPS Series III (SMD)	10 V	330	40mΩ	1830mA	7,3×4,3×4,1	N/R(9)	1 ~ 6	N/R(13)	TPSE337M010R0040 (V_O≤ 5V)(14)
TPS Series III (SMD)	4 V	1000	25mΩ	2400mA	7,3×6,1×3.5	N/R(9)	1 ~ 5	N/R(13)	TPSV108K004R0035 (V_O≤ 2.1V)(14)
Kemet, Poly-Tantalum									
T520 (SMD)	10 V	330	25mΩ	2600mA	7,3×4,3×4,1	N/R(9)	1 ~ 3	C ≥ 2(10)	T520X337M010ASE025(11)
T530 (SMD)	6.3 V	330	15mΩ	3800mA	7,3×4,3×4,1	N/R(9)	2 ~ 3	B ≥ 2(10)	T530X337M010ASE015(11)
T530 (SMD)	4 V	680	5mΩ	7300mA	7,3×4,3×4,1	N/R(9)	N/R(12)	B ≥ 1(10)	T530X687M004ASE005 (V_O≤ 3.5V)(11)
T530 (SMD)	2.5 V	1000	5mΩ	7300mA	7,3×4,3×4,1	N/R(9)	N/R(12)	B ≥ 1(10)	T530X108M2R5ASE005 (V_O≤ 2.0V)(11)
Vishay-Sprague									
597D, Tantalum (SMD)	10 V	330	35mΩ	2500mA	7,3×5,7×4,1	N/R(9)	1 ~ 5	N/R(13)	597D337X010E2T
94SA, OS-CON (Radial)	16 V	470	20mΩ	6080mA	12 × 22	1	1 ~ 3	C ≥ 2(10)	94SA477X0016GBP
94SVP OS-CON(SMD)	16 V	330	17mΩ	4500mA	10 × 12,7	2	2 ~ 3	C ≥ 1(10)	94SVP337X06F12
Kemet, Ceramic X5R	16 V	10	2mΩ	–	3225	1	≥ 1(15)	A(10)	C1210C106M4PAC
(SMD)	6.3 V	47	2mΩ			N/R(9)	≥ 1(15)	A(10)	C1210C476K9PAC
Murata, Ceramic X5R	6.3 V	100	2mΩ	–	3225	N/R(9)	≥ 1(15)	A(10)	GRM32ER60J107M
(SMD)	6.3 V	47				N/R(9)	≥ 1(15)	A(10)	GRM32ER60J476M
	25 V	22				1	≥ 1(15)	A(10)	GRM32ER61E226K
	16 V	10				1	≥ 1(15)	A(10)	GRM32DR61C106K
TDK, Ceramic X5R	6.3 V	100	2mΩ	–	3225	N/R(9)	≥ 1(15)	A(10)	C3225X5R0J107MT
(SMD)	6.3 V	47				N/R(9)	≥ 1(15)	A(10)	C3225X5R0J476MT
	16 V	10				1	≥ 1(15)	A(10)	C3225X5R1C106MT0
	16 V	22				1	≥ 1(15)	A(10)	C3225X5R1C226MT

(9) N/R – Not recommended. The voltage rating does not meet the minimum operating limits.
(10) Required capacitors with TurboTrans. See the TurboTrans Application information for Capacitor Selection
Capacitor Types:
(a) Type A = (100 < capacitance × ESR ≤ 1000)
(b) Type B = (1,000 < capacitance × ESR ≤ 5,000)
(c) Type C = (5,000 < capacitance × ESR ≤ 10,000)
(11) The voltage rating of this capacitor only allows it to be used for output voltage that is equal to or less than 80% of the working voltage.
(12) N/R – Not recommended. The ESR value of this capacitor is below the required minimum when not using TurboTrans.
(13) Aluminum Electrolytic capacitor not recommended for the TurboTrans due to higher ESR × capacitance products. Aluminum and higher ESR capacitors can be used in conjunction with lower ESR capacitance.
(14) The voltage rating of this capacitor only allows it to be used for output voltage that is equal to or less than 50% of the working voltage.
(15) Any combination of ceramic capacitor values is limited as listed in the Electrical Characteristics table.

TURBOTRANS

TurboTrans™ Technology

TurboTrans technology is a feature introduced in the T2 generation of the PTH/PTV family of power modules. TurboTrans optimizes the transient response of the regulator with added external capacitance using a single external resistor. Benefits of this technology include reduced output capacitance, minimized output voltage deviation following a load transient, and enhanced stability when using ultra-low ESR output capacitors. The amount of output capacitance required to meet a target output voltage deviation will be reduced with TurboTrans activated. Likewise, for a given amount of output capacitance, with TurboTrans engaged, the amplitude of the voltage deviation following a load transient will be reduced. Applications requiring tight transient voltage tolerances and minimized capacitor footprint area will benefit greatly from this technology.

TurboTrans™ Selection

Using TurboTrans requires connecting a resistor, R_{TT}, between the +Sense pin (pin 5) and the TurboTrans pin (pin 8). The value of the resistor directly corresponds to the amount of output capacitance required. All T2 products require a minimum value of output capacitance whether or not TurboTrans is used. For the PTH08T260W, the minimum required capacitance is 200 µF. When using TurboTrans, capacitors with a capacitance × ESR product below 10,000 µF×mΩ are required. (Multiply the capacitance (in µF) by the ESR (in mΩ) to determine the capacitance × ESR product.) See the Capacitor Selection section of the datasheet for a variety of capacitors that meet this criteria.

Figure 10 through Figure 15 show the amount of output capacitance required to meet a desired transient voltage deviation with and without TurboTrans for several capacitor types; Type A (e.g. ceramic), Type B (e.g. polymer-tantalum), and Type C (e.g. OS-CON). To calculate the proper value of R_{TT}, first determine your required transient voltage deviation limits and magnitude of your transient load step. Next, determine what type of output capacitors will be used. (If more than one type of output capacitor is used, select the capacitor type that makes up the majority of your total output capacitance). Knowing this information, use the chart in Figure 10 through Figure 15 that corresponds to the capacitor type selected. To use the chart, begin by dividing the maximum voltage deviation limit (in mV) by the magnitude of your load step (in Amps). This gives a mV/A value. Find this value on the Y-axis of the appropriate chart. Read across the graph to the *'With TurboTrans*' plot. From this point, read down to the X-axis which lists the minimum required capacitance, C_O, to meet that transient voltage deviation. The required R_{TT} resistor value can then be calculated using the equation or selected from the TurboTrans table. The TurboTrans tables include both the required output capacitance and the corresponding R_{TT} values to meet several values of transient voltage deviation for 25% (0.75 A), 50% (1.5 A), and 75% (2.25 A) output load steps.

The chart can also be used to determine the achievable transient voltage deviation for a given amount of output capacitance. Selecting the amount of output capacitance along the X-axis, reading up to the *'With TurboTrans'* curve, and then over to the Y-axis, gives the transient voltage deviation limit for that value of output capacitance. The required R_{TT} resistor value can be calculated using the equation or selected from the TurboTrans table.

As an example, let's look at a 12-V application requiring a 24 mV deviation during an 1.5 A, 50% load transient. A majority of 330 µF, 10 mΩ ouput capacitors are used. Use the 12 V, Type B capacitor chart, Figure 12. Dividing 24 mV by 1.5 A gives 16 mV/A transient voltage deviation per amp of transient load step. Select 16 mV/A on the Y-axis and read across to the *'With TurboTrans*' plot. Following this point down to the X-axis gives us a minimum required output capacitance of approximately 600 µF. The required R_{TT} resistor value for 600 µF can then be calculated or selected from Table 5. The required R_{TT} resistor is 8.06 kΩ.

To see the benefit of TurboTrans, follow the 16 mV/A marking across to the *'Without TurboTrans*' plot. Following that point down shows that you would need 3000 µF of output capacitance to meet the same transient deviation limit. This is the benefit of TurboTrans. A typical TurboTrans schematic is shown in Figure 16.

PTH08T261W Type A Capacitors

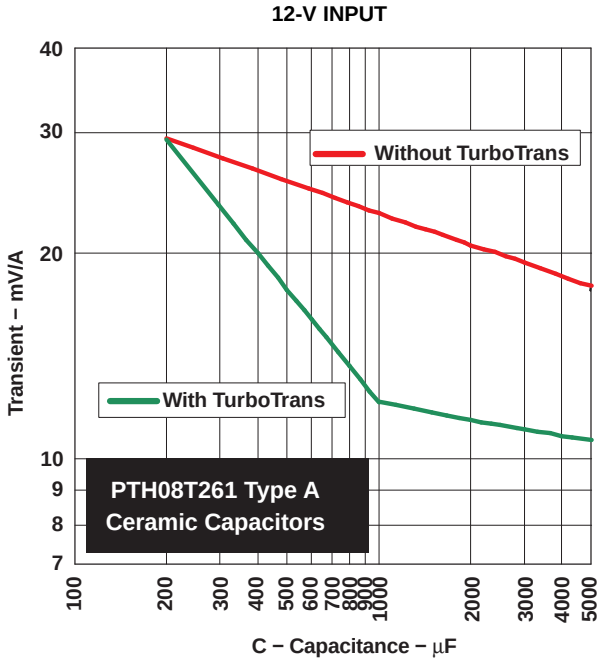


Figure 10. Capacitor Type A, 100 ≤ C(µF) x ESR(mΩ) ≤ 1000 (e.g. Ceramic)

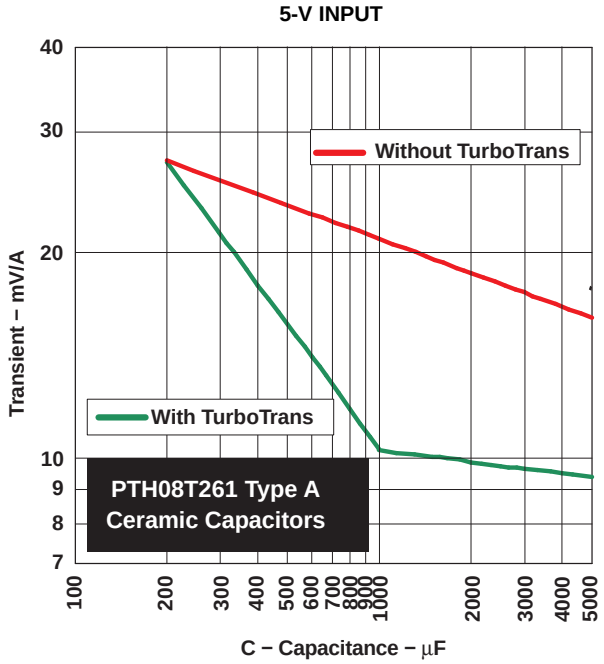


Figure 11. Capacitor Type A, 100 ≤ C(µF) x ESR(mΩ) ≤ 1000 (e.g. Ceramic)

Table 4. Type A TurboTrans C_O Values and Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			12 V Input		5 V Input	
25% load step (0.75 A)	50% load step (1.5 A)	75% load step (2.25 A)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)
25	50	75	200	open	200	open
20	40	60	240	150	210	634
18	35	55	300	56.2	260	97.6
15	30	45	400	23.7	340	37.4
13	25	40	560	9.76	460	16.5
10	20	30	840	2.0	660	5.9
8	15	25	5000	N/A	950	0.536

R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming equation:

$$R_{TT} = 40 \times \frac{1 - (C_O / 1000)}{\left[5 \times (C_O / 1000)\right] - 1} \ (k\Omega) \quad (2)$$

Where C_O is the total output capacitance in µF. C_O values greater than or equal to 1000 µF require R_{TT} to be a short, 0 Ω.

To ensure stability, a minimum amount of output capacitance is required for a given R_{TT} resistor value. The value of R_{TT} must be calculated using the minimum required output capacitance determined from the capacitor transient response charts above.

PTH08T260W Type B Capacitors

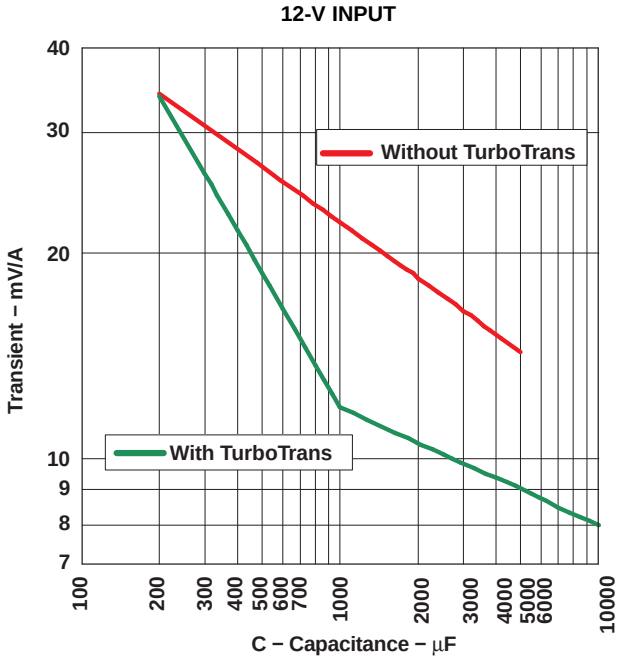


Figure 12. Capacitor Type B, 1000 < C(µF) x ESR(mΩ) ≤ 5000 (e.g. Polymer-Tantalum)

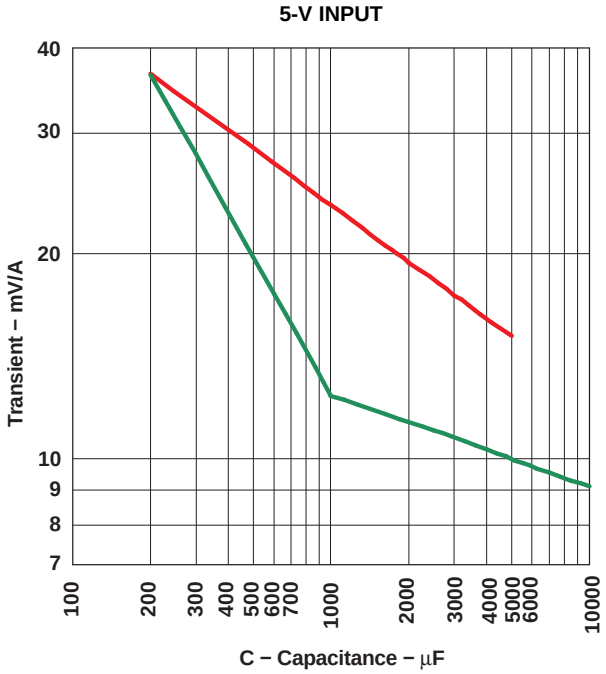


Figure 13. Capacitor Type B, 1000 < C(µF) x ESR(mΩ) ≤ 5000 (e.g. Polymer-Tantalum)

Table 5. Type B TurboTrans C_O Values and Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			12 V Input		5 V Input	
25% load step (0.75 A)	50% load step (1.5 A)	75% load step (2.25 A)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)
30	55	85	200	open	200	open
25	50	75	210	634	230	205
20	40	60	300	56.2	320	45.3
18	35	55	370	29.4	400	23.7
15	30	45	460	16.5	500	13.3
13	25	40	610	7.68	650	6.19
10	20	30	850	1.87	900	1.15
8	15	25	2700	short	5000	short

R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming equation:

$$R_{TT} = 40 \times \frac{1 - (C_O / 1000)}{\left[5 \times (C_O / 1000)\right] - 1} \ (k\Omega) \quad (3)$$

Where C_O is the total output capacitance in µF. C_O values greater than or equal to 1000 µF require R_{TT} to be a short, 0 Ω.

To ensure stability, a minimum amount of output capacitance is required for a given R_{TT} resistor value. The value of R_{TT} must be calculated using the minimum required output capacitance determined from the capacitor transient response charts above.

PTH08T260W Type C Capacitors

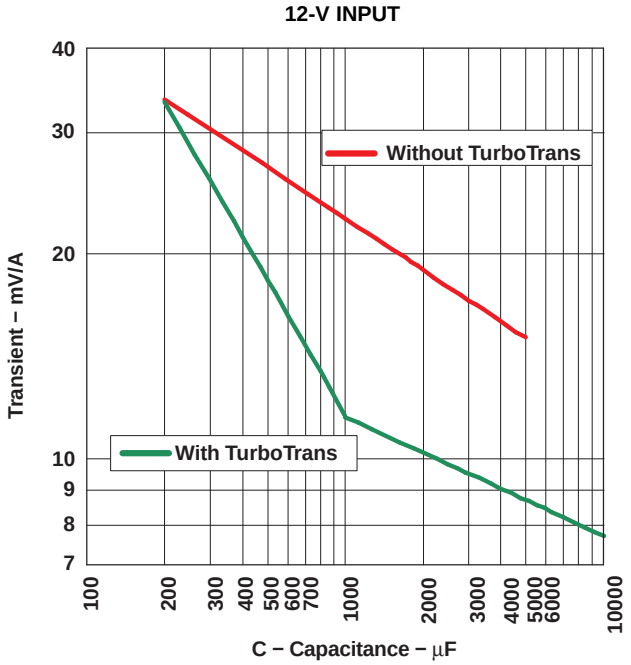


Figure 14. Capacitor Type C, 5000 < C(µF) x ESR(mΩ) ≤ 10,000 (e.g. OS-CON)

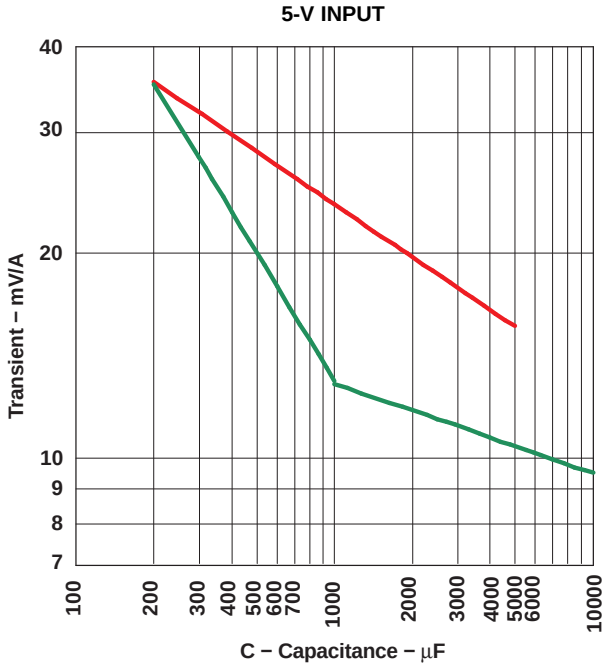


Figure 15. Capacitor Type C, 5000 < C(µF) x ESR(mΩ) ≤ 10,000 (e.g. OS-CON)

Table 6. Type C TurboTrans C_O Values and Required R_{TT} Selection Table

Transient Voltage Deviation (mV)			12 V Input		5 V Input	
25% load step (1.5 A)	50% load step (3 A)	75% load step (4.5 A)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)	C_O Minimum Required Output Capacitance (µF)	R_{TT} Required TurboTrans Resistor (kΩ)
30	55	85	200	open	200	open
25	50	75	200	open	220	309
20	40	60	240	150	270	82.5
18	35	55	290	63.4	330	41.2
15	30	45	440	18.7	520	12.1
13	25	40	580	8.87	690	5.11
10	20	30	820	2.32	980	0.205
8	15	25	2300	short	6800	short

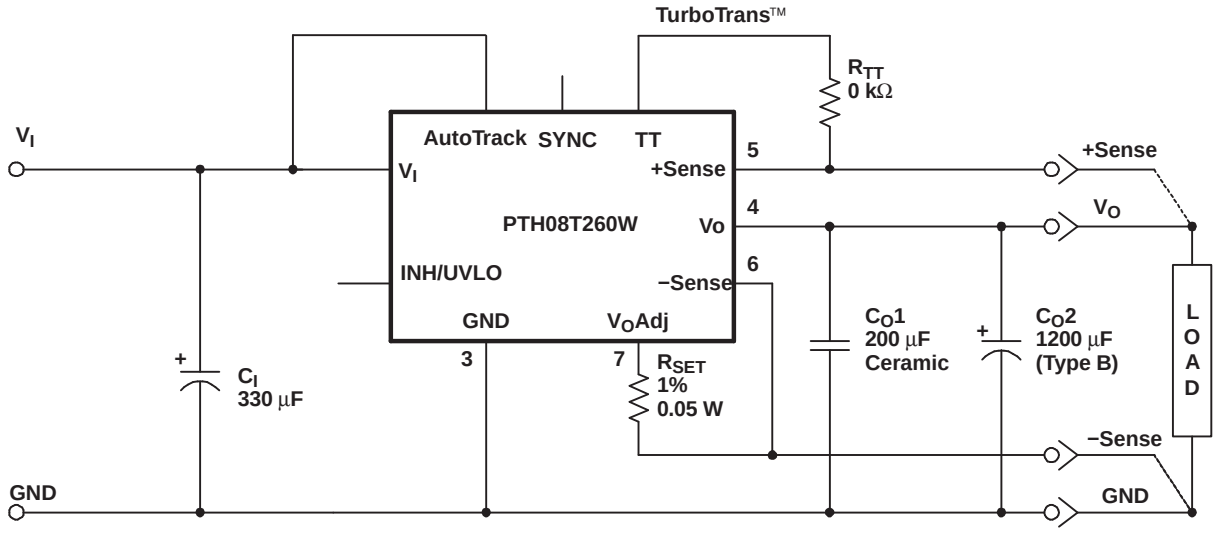
R_{TT} Resistor Selection

The TurboTrans resistor value, R_{TT} can be determined from the TurboTrans programming equation:

$$R_{TT} = 40 \times \frac{1 - (C_O / 1000)}{\left[5 \times (C_O / 1000)\right] - 1} \ (k\Omega) \quad (4)$$

Where C_O is the total output capacitance in µF. C_O values greater than or equal to 1000 µF require R_{TT} to be a short, 0 Ω.

To ensure stability, a minimum amount of output capacitance is required for a given R_{TT} resistor value. The value of R_{TT} must be calculated using the minimum required output capacitance determined from the capacitor transient response charts above.



A. The value of R_{TT} must be calculated using the total value of output capacitance.

Figure 16. Typical TurboTrans Schematic

UNDERVOLTAGE LOCKOUT (UVLO)

The PTH08T260/261W power modules incorporate an input undervoltage lockout (UVLO). The UVLO feature prevents the operation of the module until there is sufficient input voltage to produce a valid output voltage. This enables the module to provide a clean, monotonic powerup for the load circuit, and also limits the magnitude of current drawn from the regulator's input source during the power-up sequence.

The UVLO characteristic is defined by the *ON* threshold (V_{THD}) voltage. Below the *ON* threshold, the Inhibit control is overridden, and the module does not produce an output. The hysteresis voltage, which is the difference between the *ON* and *OFF* threshold voltages, is set at 500 mV. The hysteresis prevents start-up oscillations, which can occur if the input voltage droops slightly when the module begins drawing current from the input source.

The UVLO feature of the PTH08T260/261W module allows for limited adjustment of the *ON* threshold voltage. The adjustment is made via the *Inhibit/UVLO* control pin (pin 10) using a single resistor (see Figure 17). When pin 10 is left open circuit, the *ON* threshold voltage is internally set to its default value, which is 4.3 V. The *ON* threshold might need to be raised if the module is powered from a tightly regulated 12-V bus. Adjusting the threshold prevents the module from operating if the input bus fails to completely rise to its specified regulation voltage.

Threshold Adjust

Equation 5 determines the value of R_{UVLO} required to adjust V_{THD} to a new value. The default value is 4.3 V, and it may be adjusted, but only to a higher value.

$$R_{UVLO} = \frac{70.74 - V_{THD}}{V_{THD} - 4.26} \text{ k}\Omega \quad (5)$$

Calculated Values

Table 7 shows a chart of standard resistor values for R_{UVLO} for different values of the *ON* threshold (V_{THD}) voltage.

Table 7. Standard R_{UVLO} values for Various V_{THD} values

V_{THD} (V)	5.0	5.5	6.0	6.5	7.0	7.5	8.0	8.5	9.0	9.5	10.0	10.5	11.0
R_{UVLO} (kΩ)	88.7	52.3	37.4	28.7	23.2	19.6	16.9	14.7	13.0	11.8	10.5	9.76	8.87

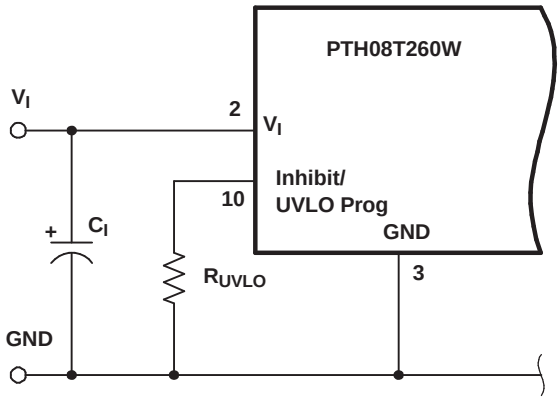


Figure 17. UVLO Implementation

Soft-Start Power Up

The Auto-Track feature allows the power-up of multiple PTH/PTV modules to be directly controlled from the Track pin. However in a stand-alone configuration, or when the Auto-Track feature is not being used, the Track pin should be directly connected to the input voltage, V_I (see Figure 18).

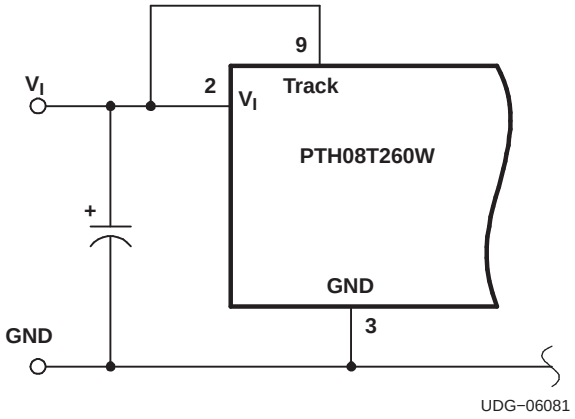


Figure 18. Defeating the Auto-Track Function

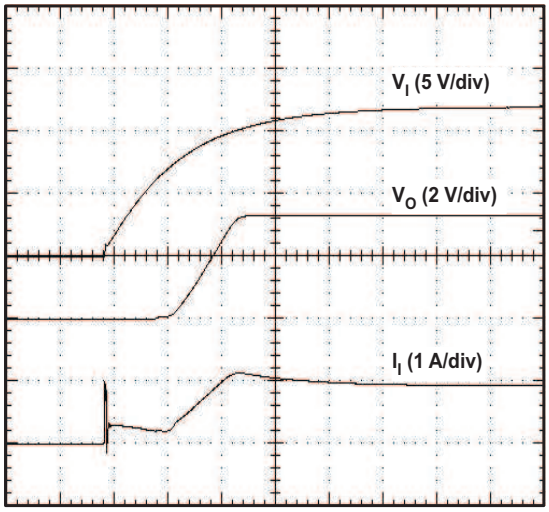


Figure 19. Power-Up Waveform

When the Track pin is connected to the input voltage the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate. From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 2 ms–10 ms) before allowing the output voltage to rise. The output then progressively rises to the module's setpoint voltage. Figure 19 shows the soft-start power-up characteristic of the PTH08T260W operating from a 12-V input bus and configured for a 3.3-V output. The waveforms were measured with a 3-A constant current load and the Auto-Track feature disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power-up is complete within 20 ms.

Overcurrent Protection

For protection against load faults, all modules incorporate output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold causes the regulated output to shut down. Following shutdown, a module periodically attempts to recover by initiating a soft-start power-up. This is described as a *hiccup* mode of operation, whereby the module continues in a cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

Overtemperature Protection (OTP)

A thermal shutdown mechanism protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold, the module's Inhibit control is internally pulled low. This turns the output off. The output voltage drops as the external output capacitors are discharged by the load circuit. The recovery is automatic, and begins with a soft-start power up. It occurs when the sensed temperature decreases by about 10°C below the trip point.

The overtemperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and reduces the long-term reliability of the module. Always operate the regulator within the specified safe operating area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

Output On/Off Inhibit

For applications requiring output voltage on/off control, the PTH08T260/261W incorporates an output Inhibit control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned off.

The power modules function normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_I with respect to GND.

Figure 20 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The Inhibit input has its own internal pull-up. An external pull-up should never be connected to the inhibit pin. The input is not compatible with TTL logic devices. An open-collector (or open-drain) discrete transistor is recommended for control.

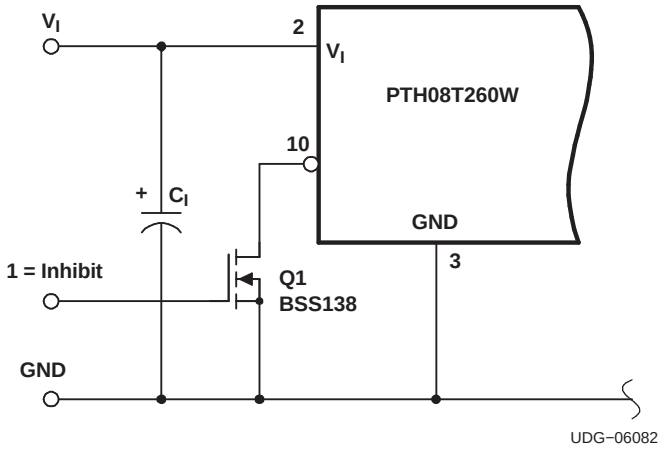


Figure 20. On/Off Inhibit Control Circuit

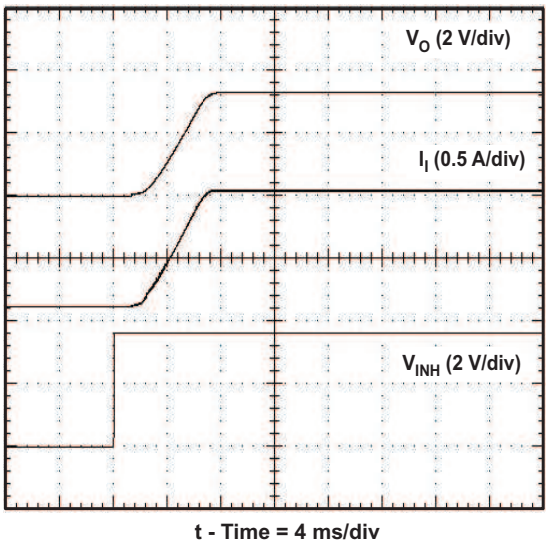


Figure 21. Power-Up Response from Inhibit Control

Turning Q1 on applies a low voltage to the Inhibit control pin and disables the output of the module. If Q1 is then turned off, the module executes a soft-start power-up sequence. A regulated output voltage is produced within 15 ms. Figure 21 shows the typical rise in both the output voltage and input current, following the turn-off of Q1. The turn off of Q1 corresponds to the rise in the waveform, V_{INH}. The waveforms were measured with a 3-A constant current load.

Remote Sense

Differential remote sense improves the load regulation performance of the module by allowing it to compensate for any IR voltage drop between its output and the load in either the positive or return path. An IR drop is caused by the output current flowing through the small amount of pin and trace resistance. Connecting the +Sense (pin 5) and –Sense (pin 6) pins to the respective positive and ground reference of the load terminals improves the load regulation of the output voltage at the connection points.

With the sense pins connected at the load, the difference between the voltage measured directly between the V_O and GND pins, and that measured at the Sense pins, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 300 mV.

If the remote sense feature is not used at the load, connect the +Sense pin to V_O (pin 4) and connect the –Sense pin to the module GND (pin 3).

The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

Smart Sync

Smart Sync is a feature that allows multiple power modules to be synchronized to a common frequency. Driving the Smart Sync pins with an external oscillator set to the desired frequency, synchronizes all connected modules to the selected frequency. The synchronization frequency can be higher or lower than the nominal switching frequency of the modules within the range of 240 kHz to 400 kHz (see Electrical Specifications table for frequency limits). Synchronizing modules powered from the same bus, eliminates beat frequencies reflected back to the input supply, and also reduces EMI filtering requirements. These are the benefits of Smart Sync. Power modules can also be synchronized out of phase to minimize source current loading and minimize input capacitance requirements. Figure 22 shows a standard circuit with two modules syncronized 180° out of phase using a D flip-flop.

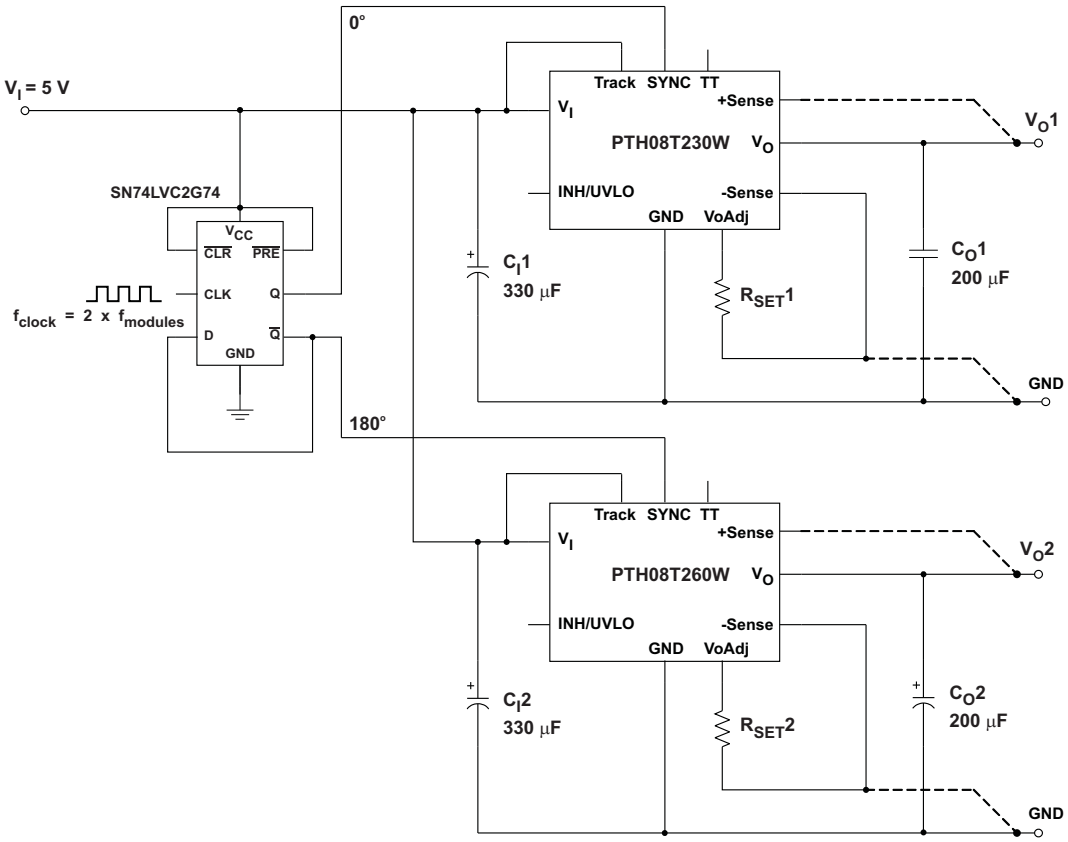


Figure 22. Typical SmartSync Circuit

Smart Sync Considerations

Operating the PTH08T260W with a low duty cycle may increase the output voltage ripple due to pulse skipping of the PWM controller. When operating at the nominal switching frequency, input voltages greater than (V_O × 11) may cause the output voltage ripple to increase (typically 2×).

Synchronizing to a higher frequency and operating with a low duty cycle may impact output voltage ripple. When operating at 300 kHz, Figure 23 shows the operating region where the output voltage ripple meets the electrical specifications and the operating region where the output voltage ripple may increase. Figure 24 shows the operating regions for several switching frequencies. For example, a module operating at 400 kHz and an output voltage of 1.2 V, the maximum input voltage that meets the output voltage ripple specification is 10 V. Exceeding 10 V may cause in an increase in output voltage ripple. As shown in Figure 24, operating below 6 V allows operation down to the minimum output voltage over the entire synchronization frequency range without affecting the output voltage ripple. See the *Electrical Characteristics* table for the synchronization frequency range limits.

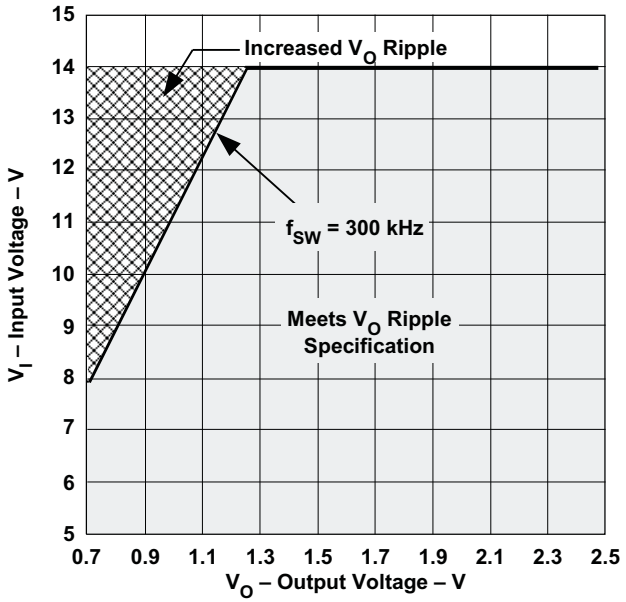


Figure 23. V_O Ripple Regions at 300 kHz (1) (2)

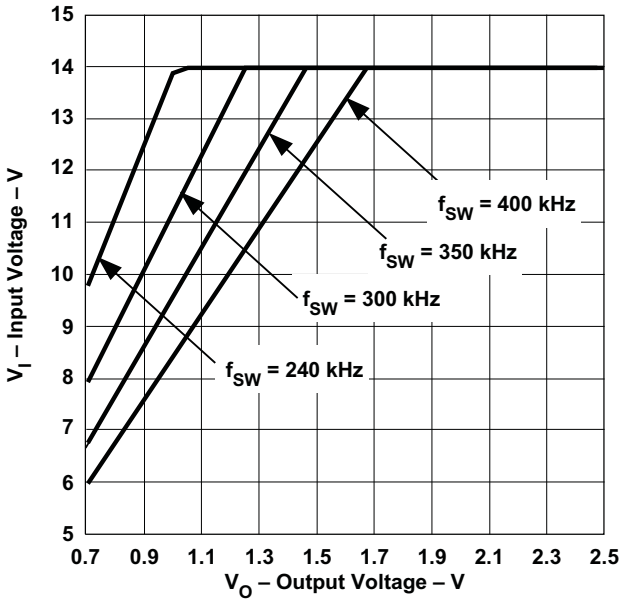


Figure 24. V_O Ripple Regions (1) (2)

(1) Operation above a given curve may cause the output voltage ripple to increase (typically 2 ×).
(2) When operating at the nominal switching frequency refer to the 300 kHz plot.

Auto-Track™ Function

The Auto-Track function is unique to the PTH/PTV family, and is available with all POLA products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications that use dual-voltage VLSI ICs such as the TMS320™ DSP family, microprocessors, and ASICs.

How Auto-Track™ Works

Auto-Track works by forcing the module output voltage to follow a voltage presented at the *Track* control pin (1). This control range is limited to between 0 V and the module set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module output remains at its set-point (2). As an example, if the *Track* pin of a 2.5-V regulator is at 1 V, the regulated output is 1 V. If the voltage at the *Track* pin rises to 3 V, the regulated output does not go higher than 2.5 V.

When under Auto-Track control, the regulated output from the module follows the voltage at its *Track* pin on a

volt-for-volt basis. By connecting the *Track* pin of a number of these modules together, the output voltages follow a common signal during power up and power down. The control signal can be an externally generated master ramp waveform, or the output voltage from another power supply circuit (3). For convenience, the *Track* input incorporates an internal RC-charge circuit. This operates off the module input voltage to produce a suitable rising waveform at power up.

Typical Auto-Track™ Application

The basic implementation of Auto-Track allows for simultaneous voltage sequencing of a number of Auto-Track compliant modules. Connecting the *Track* inputs of two or more modules forces their track input to follow the same collective RC-ramp waveform, and allows their power-up sequence to be coordinated from a common Track control signal. This can be an open-collector (or open-drain) device, such as a power-up reset voltage supervisor IC. See U3 in Figure 25.

To coordinate a power-up sequence, the Track control must first be pulled to ground potential. This should be done at or before input power is applied to the modules. The ground signal should be maintained for at least 20 ms after input power has been applied. This brief period gives the modules time to complete their internal soft-start initialization (4), enabling them to produce an output voltage. A low-cost supply voltage supervisor IC, that includes a built-in time delay, is an ideal component for automatically controlling the Track inputs at power up.

Figure 25 shows how the TL7712A supply voltage supervisor IC (U3) can be used to coordinate the sequenced power up of PTH08T260/261W modules. The output of the TL7712A supervisor becomes active above an input voltage of 3.6 V, enabling it to assert a ground signal to the common track control well before the input voltage has reached the module's undervoltage lockout threshold. The ground signal is maintained until approximately 28 ms after the input voltage has risen above U3's voltage threshold, which is 10.95 V. The 28-ms time period is controlled by the capacitor C3. The value of 2.2 µF provides sufficient time delay for the modules to complete their internal soft-start initialization. The output voltage of each module remains at zero until the track control voltage is allowed to rise. When U3 removes the ground signal, the track control voltage automatically rises. This causes the output voltage of each module to rise simultaneously with the other modules, until each reaches its respective set-point voltage.

Figure 26 shows the output voltage waveforms after input voltage is applied to the circuit. The waveforms, V_O1 and V_O2, represent the output voltages from the two power modules, U1 (3.3 V) and U2 (1.8 V), respectively. V_{TRK}, V_O1, and V_O2 are shown rising together to produce the desired simultaneous power-up characteristic.

The same circuit also provides a power-down sequence. When the input voltage falls below U3's voltage threshold, the ground signal is re-applied to the common track control. This pulls the track inputs to zero volts, forcing the output of each module to follow, as shown in Figure 27. Power down is normally complete before the input voltage has fallen below the modules' undervoltage lockout. This is an important constraint. Once the modules recognize that an input voltage is no longer present, their outputs can no longer follow the voltage applied at their track input. During a power-down sequence, the fall in the output voltage from the modules is limited by the Auto-Track slew rate capability.

Notes on Use of Auto-Track™

1. The *Track* pin voltage must be allowed to rise above the module set-point voltage before the module regulates at its adjusted set-point voltage.
2. The Auto-Track function tracks almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
3. The absolute maximum voltage that may be applied to the *Track* pin is the input voltage V_I.
4. The module cannot follow a voltage at its track control input until it has completed its soft-start initialization. This takes about 20 ms from the time that a valid voltage has been applied to its input. During this period, it is recommended that the *Track* pin be held at ground potential.
5. The Auto-Track function is disabled by connecting the *Track* pin to the input voltage (V_I). When Auto-Track is disabled, the output voltage rises at a quicker and more linear rate after input power has been applied.

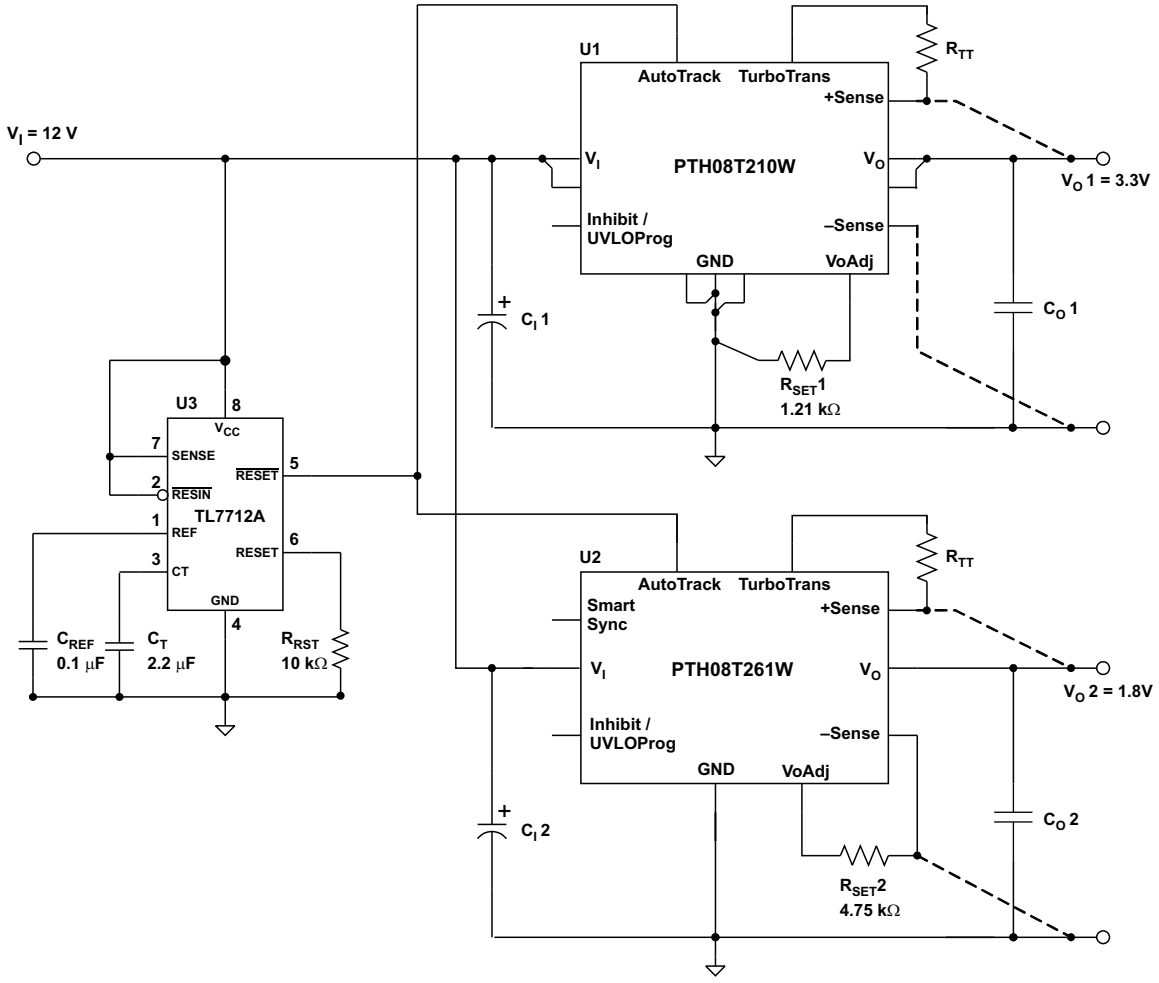


Figure 25. Sequenced Power Up and Power Down Using Auto-Track

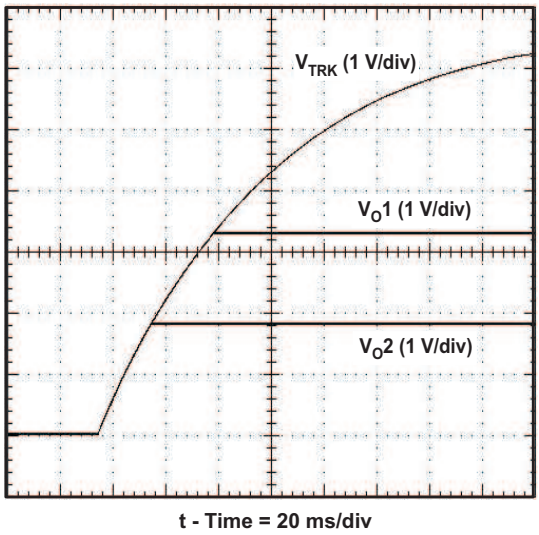


Figure 26. Simultaneous Power Up With Auto-Track Control

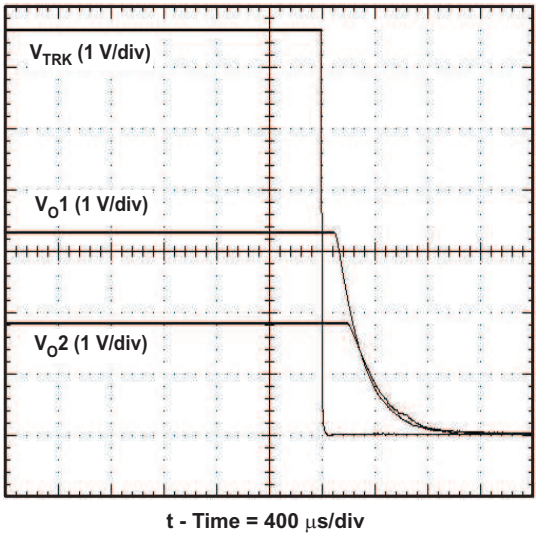


Figure 27. Simultaneous Power Down With Auto-Track Control

Prebias Startup Capability

A prebias startup condition occurs as a result of an external voltage being present at the output of a power module prior to its output becoming active. This often occurs in complex digital systems when current from another power source is backfed through a dual-supply logic component, such as an FPGA or ASIC. Another path might be via clamp diodes as part of a dual-supply power-up sequencing arrangement. A prebias can cause problems with power modules that incorporate synchronous rectifiers. This is because under most operating conditions, these types of modules can sink as well as source output current.

The PTH family of power modules incorporate synchronous rectifiers, but does not sink current during startup(1), or whenever the Inhibit pin is held low. However, to ensure satisfactory operation of this function, certain conditions must be maintained(2). Figure 29 shows an application demonstrating the prebias startup capability. The startup waveforms are shown in Figure 28. Note that the output current (I_O) is negligible until the output voltage rises above the voltage backfed through the intrinsic diodes.

The prebias start-up feature is not compatible with Auto-Track. When the module is under Auto-Track control, it sinks current if the output voltage is below that of a back-feeding source. To ensure a pre-bias hold-off one of two approaches must be followed when input power is applied to the module. The Auto-Track function must either be disabled(3), or the module's output held off (for at least 50 ms) using the Inhibit pin. Either approach ensures that the Track pin voltage is above the set-point voltage at start up.

1. Startup includes the short delay (approximately 10 ms) prior to the output voltage rising, followed by the rise of the output voltage under the module's internal soft-start control. Startup is complete when the output voltage has risen to either the set-point voltage or the voltage at the Track pin, whichever is lowest.
2. To ensure that the regulator does not sink current when power is first applied (even with a ground signal applied to the Inhibit control pin), the input voltage must always be greater than the output voltage *throughout* the power-up and power-down sequence.
3. The Auto-Track function can be disabled at power up by immediately applying a voltage to the module's Track pin that is greater than its set-point voltage. This can be easily accomplished by connecting the Track pin to V_I.

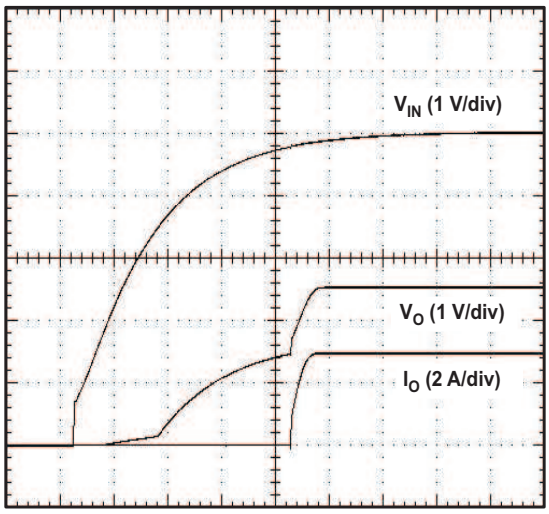


Figure 28. Prebias Startup Waveforms

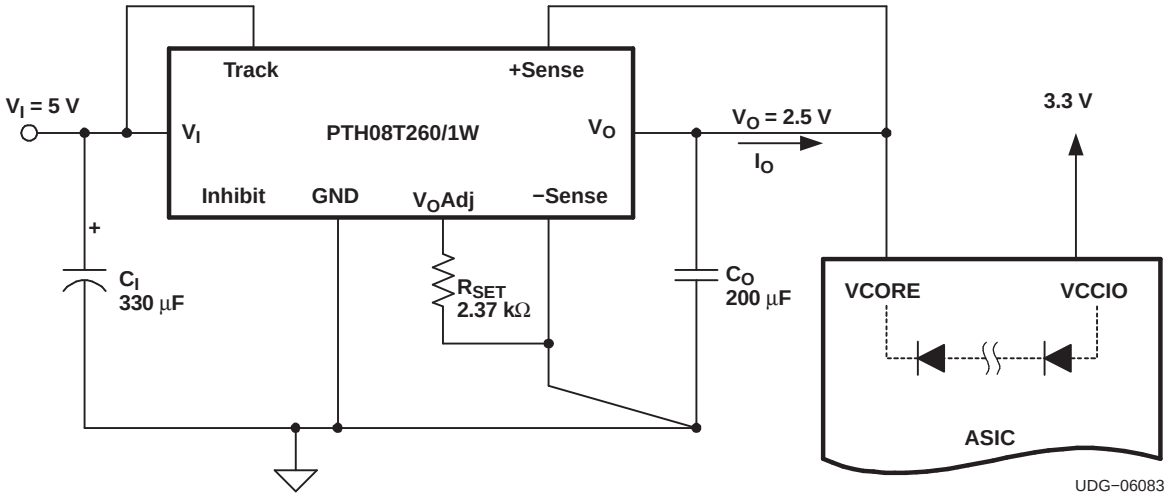
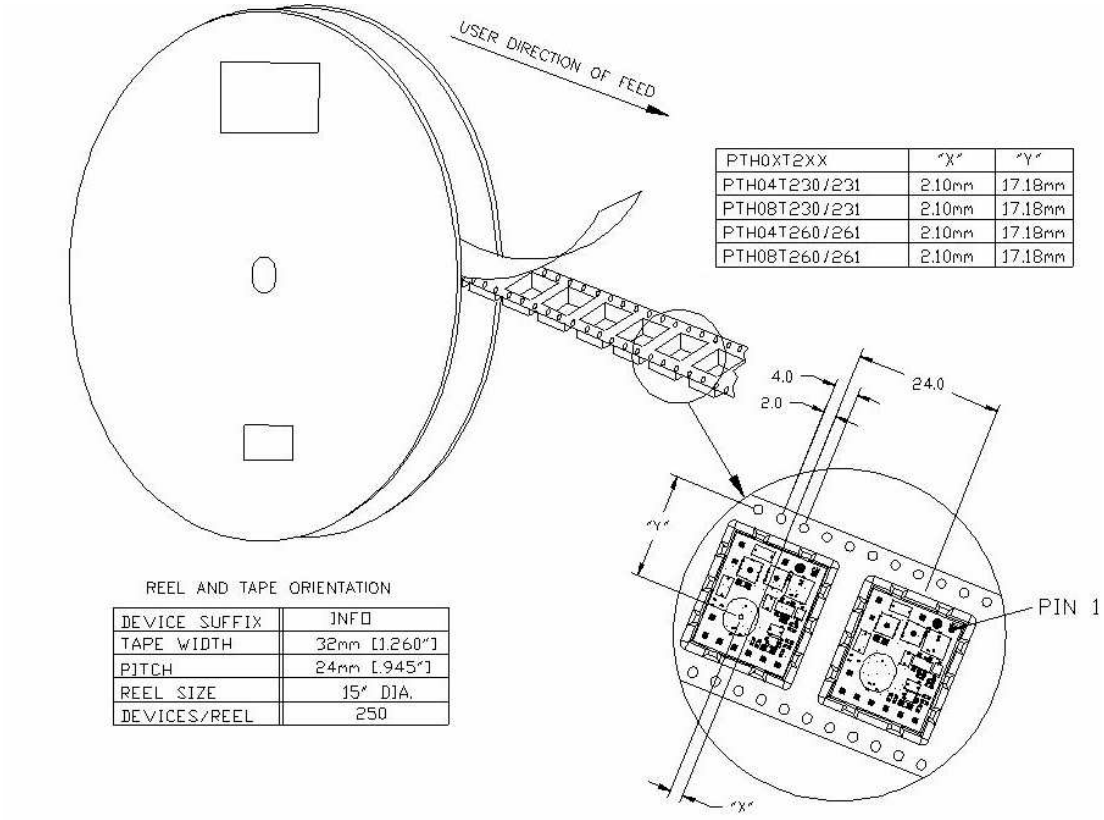


Figure 29. Application Circuit Demonstrating Prebias Startup

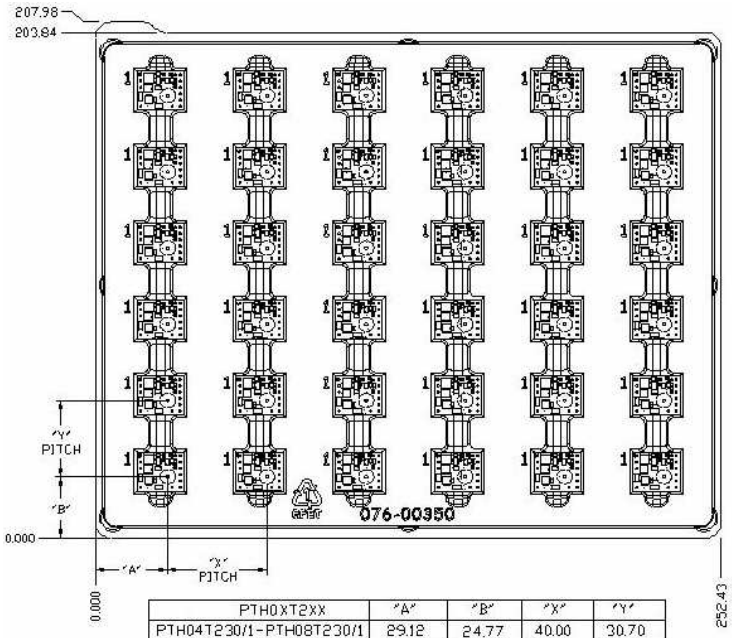
TRAY AND TAPE & REEL DRAWINGS

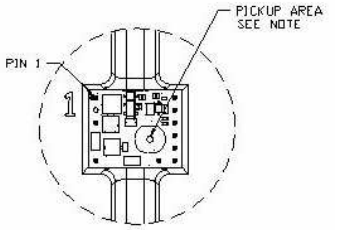


PTH0XT2XX	"X"	"Y"
PTH04T230/231	2.10mm	17.18mm
PTH08T230/231	2.10mm	17.18mm
PTH04T260/261	2.10mm	17.18mm
PTH08T260/261	2.10mm	17.18mm

REEL AND TAPE ORIENTATION

DEVICE SUFFIX	INFO
TAPE WIDTH	32mm [1.260"]
PITCH	24mm [.945"]
REEL SIZE	15" DIA.
DEVICES/REEL	250





NOTE: THE INDUCTOR IS USED TO PICK AND PLACE THE MODULE. IT'S LOCATION MAY VARY FROM PACKAGE STYLE. SEE PRODUCT TABLE

DEVICES/TRAY	42

PTH0XT2XX	"A"	"B"	"X"	"Y"
PTH04T230/1-PTH08T230/1	29.12	24.77	40.00	30.70
PTH04T260/1-PTH08T260/1	29.12	24.77	40.00	30.70
ALL DIMENSIONS ARE IN MILLIMETER.				

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTH08T260WAD	ACTIVE	Through-Hole Module	ECL	10	36	RoHS Exempt & Green	SN	N / A for Pkg Type	-40 to 85		Samples
PTH08T260WAS	ACTIVE	Surface Mount Module	ECM	10	36	Non-RoHS & Green	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH08T260WAST	ACTIVE	Surface Mount Module	ECM	10	250	Non-RoHS & Green	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH08T260WAZ	ACTIVE	Surface Mount Module	BCM	10	36	RoHS Exempt & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples
PTH08T260WAZT	ACTIVE	Surface Mount Module	BCM	10	250	RoHS Exempt & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples
PTH08T261WAD	ACTIVE	Through-Hole Module	ECL	10	36	RoHS Exempt & Green	SN	N / A for Pkg Type	-40 to 85		Samples
PTH08T261WAS	ACTIVE	Surface Mount Module	ECM	10	36	Non-RoHS & Green	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH08T261WAST	ACTIVE	Surface Mount Module	ECM	10	250	Non-RoHS & Green	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		Samples
PTH08T261WAZ	ACTIVE	Surface Mount Module	BCM	10	36	RoHS Exempt & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples
PTH08T261WAZT	ACTIVE	Surface Mount Module	BCM	10	250	RoHS Exempt & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

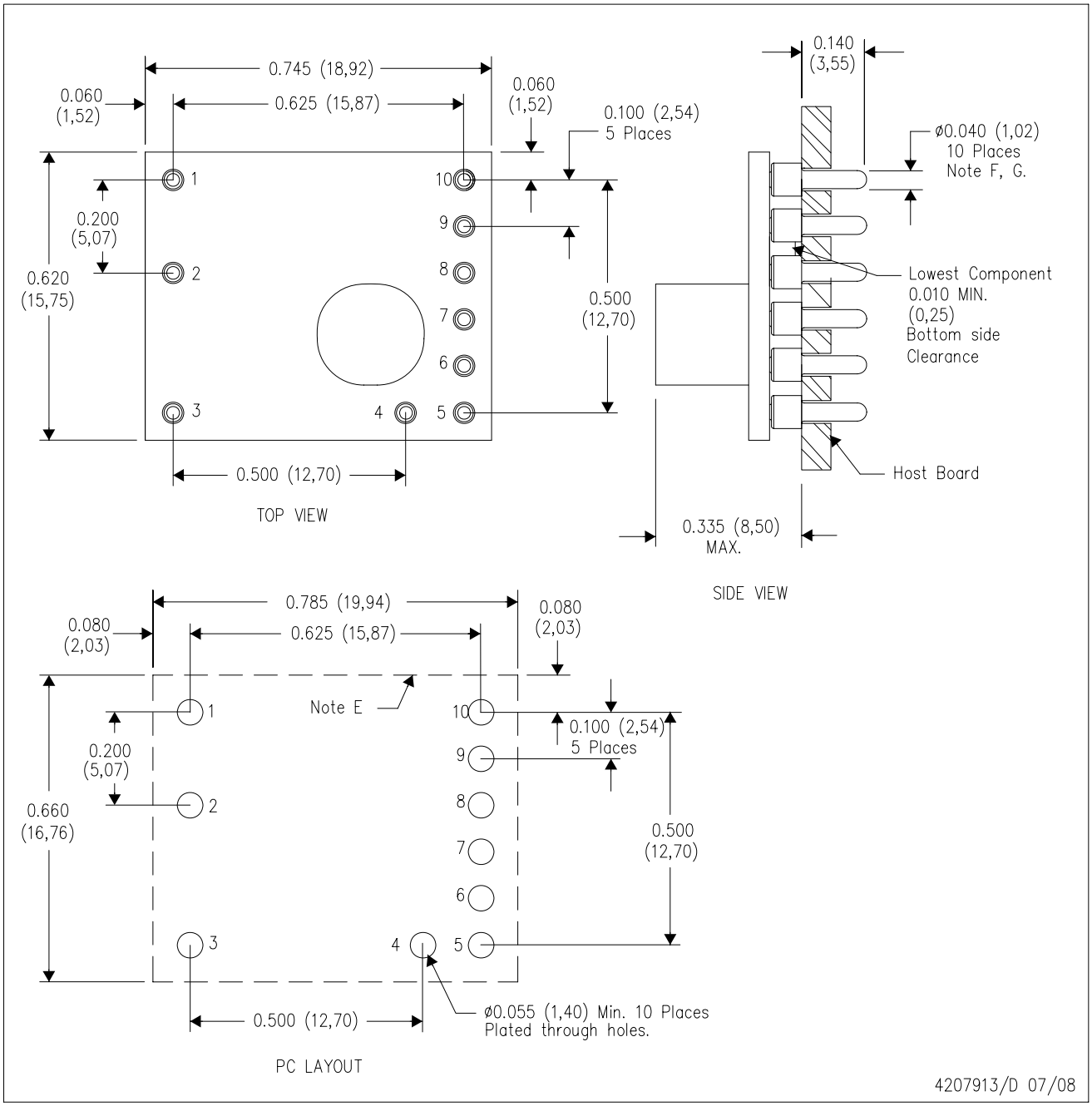
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

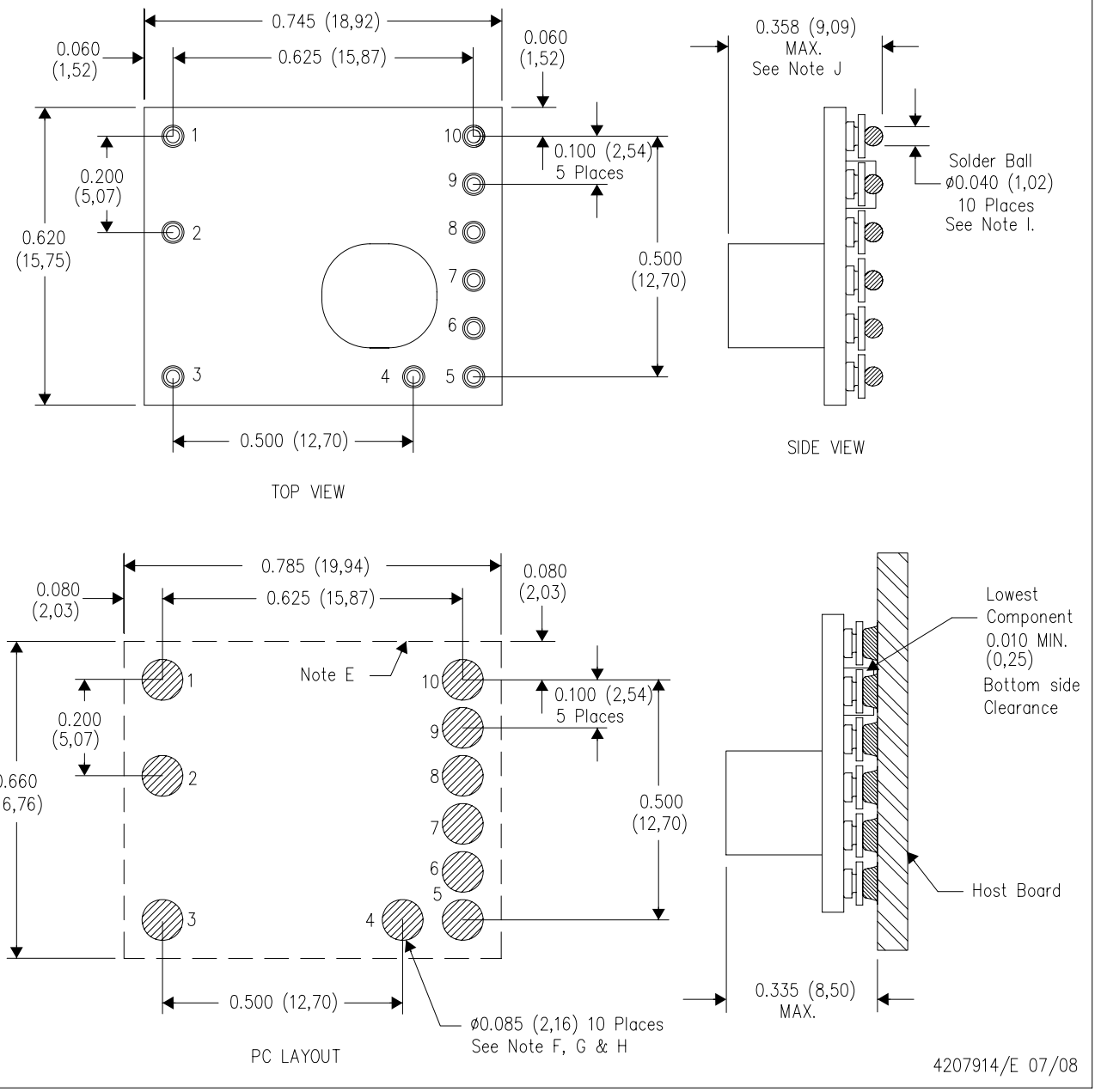
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

ECL (R–PDSS–T10) DOUBLE SIDED MODULE



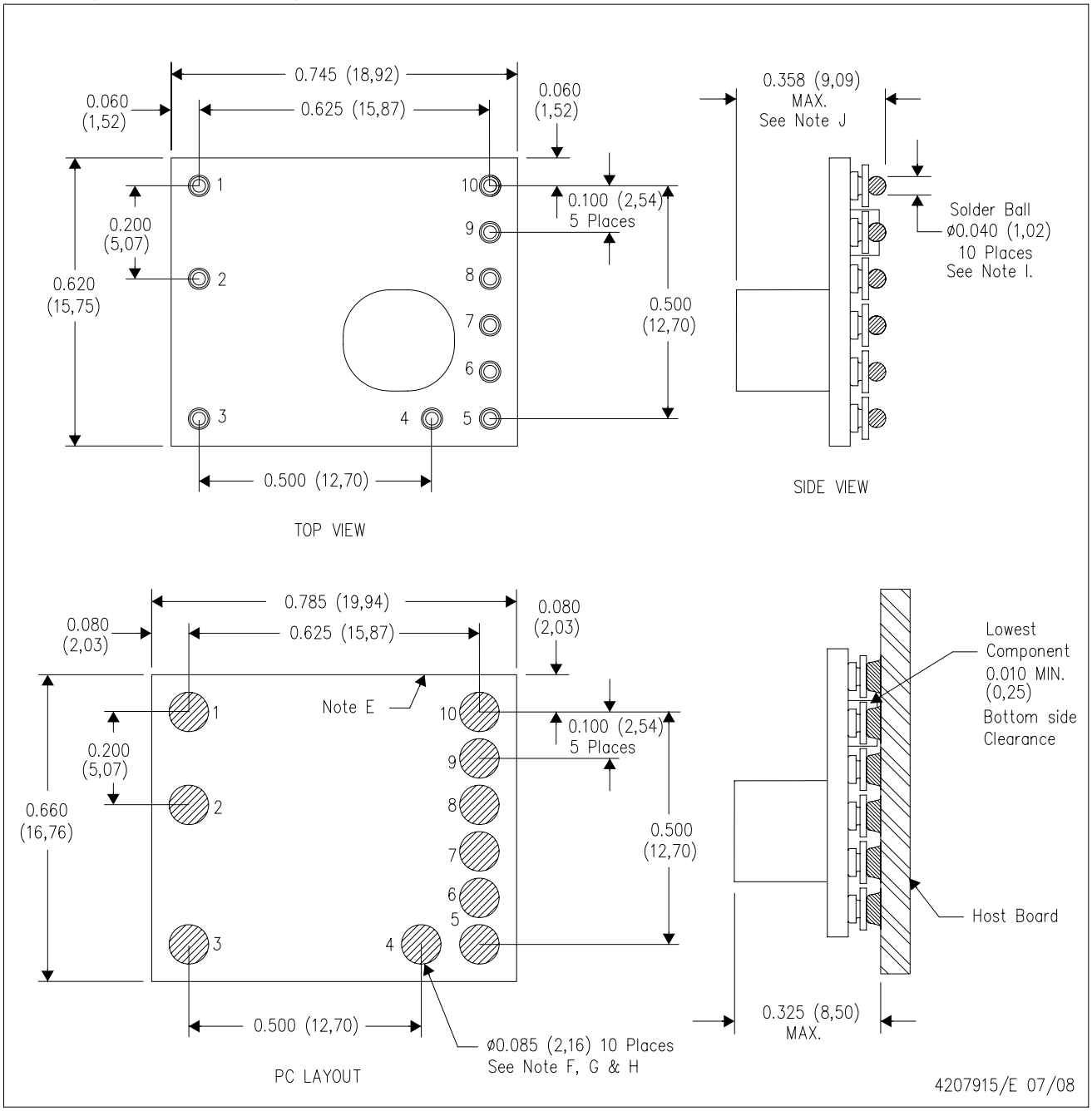
NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
G. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

ECM (R–PDSS–B10) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

BCM (R–PDSS–B10) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize two or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. This is a lead–free solder ball design.
Finish: Tin (100%) over Nickel plate
Solder ball: 96.5 Sn/3.0 Ag/0.5 Cu
J. Dimension prior to reflow solder.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265