SN54AC00-SP Radiation Hardened Quad 2 Input NAND Gate

1 Features

- 5962R87549:
  - Radiation hardness assurance (RHA) up to TID 100 krad (Si)
  - SEL immune to 86 MeV×cm^2/mg
- 5962-87549:
  - Total ionizing dose 50 krad (Si)
- 2 V to 6 V V_{CC} operation
- Inputs accept voltages to 6 V
- Maximum t_{pd} of 7 ns at 5 V

2 Applications

- Satellite payloads
- Satellite power on reset logic
- RHA known good Die (KGD) offering for space hybrids

Pin Functions (Each Gate)

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

Logic Diagram (Positive Logic)

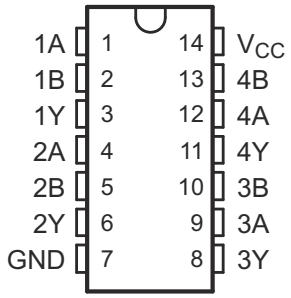
3 Description

The SN54AC00 device contains four independent 2-input NAND gates. Each gate performs the Boolean function of $Y = \overline{A \bullet B}$ or $Y = \overline{A} + \overline{B}$ in positive logic.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN54AC00-SP	CDIP (14)	5.97 mm × 9.21 mm
	CFP (14)	6.67 mm × 19.56 mm
	KGD (0)	Not applicable

(1) For all available packages, see the orderable addendum at the end of the data sheet.



J or W Package
(Top View)

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

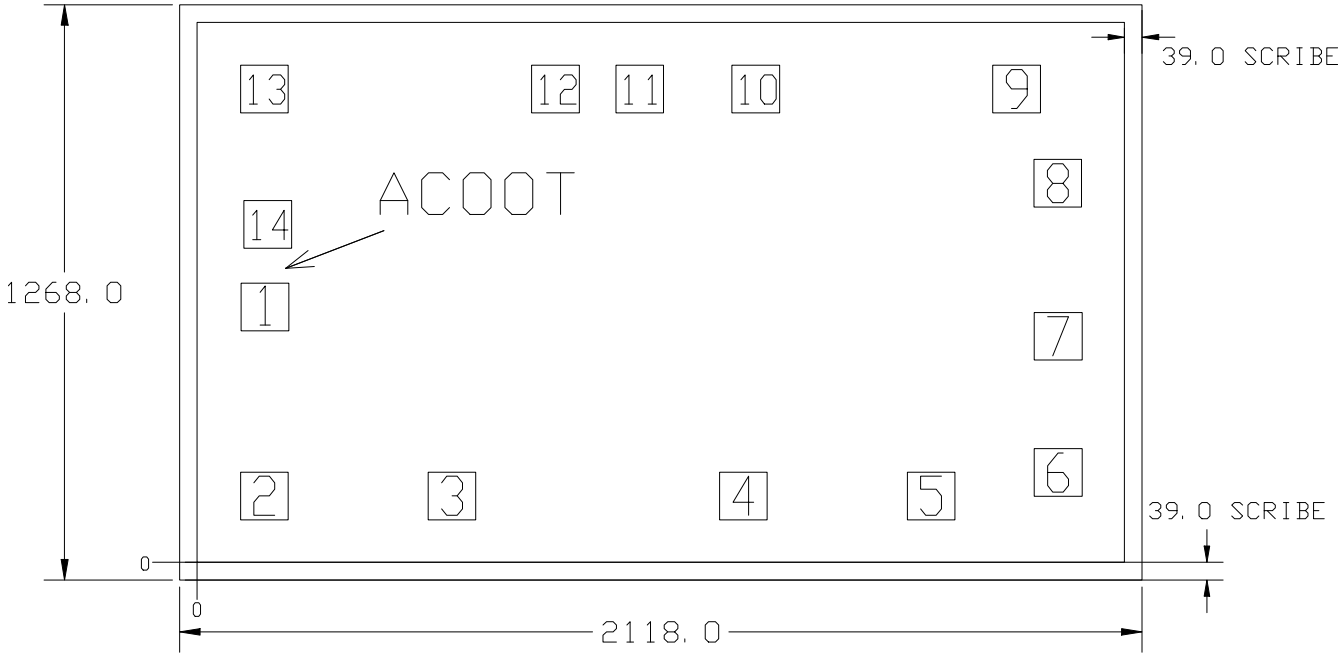
Changes from Revision B (October 2015) to Revision C (April 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Removed *SEU* from the *Features* section	1
• Changed *SEL* immune to 86 MeV×cm^2/mg	1

Changes from Revision A (December 2013) to Revision B (February 2015)	Page
• Added KGD package information	1
• Added *Device and Documentation Support* section and *Mechanical, Packaging, and Orderable Information* section	1
• Added *Bare Die Information*, image, and *Bond Pad Coordinates in Microns*	3
• Added parameter information for KGD to *Section 6.5* and *Section 6.6*	6

Changes from Revision * (October 2008) to Revision A (December 2013)	Page
• Changed *Features* bullets	1
• Deleted *Ordering Information* table	1

5 Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Floating	TiW/AlCu2	15800 nm



Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
1A	1	96.3	510.5	201.3	615.5
1B	2	95	94	200	199
1Y	3	508	94	613	199
2A	4	1149	94	1254	199
2B	5	1562	94	1667	199
2Y	6	1841.5	145.5	1946.5	250.5
GND	7	1841.5	445.5	1946.5	550.5
3Y	8	1841	783	1946	888
3A	9	1750.5	991	1855.5	1096
3B	10	1176.5	991	1281.5	1096
4Y	11	921	991	1026	1096
4A	12	736	991	841	1096
4B	13	95	991	200	1096
VCC	14	102.5	692	207.5	797

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage(2)		–0.5	V_{CC} + 0.5	V
V_O	Output voltage(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0 or V_I > V_{CC}		±20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±50	mA
	Continuous current through V_{CC} or GND			±200	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	6	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 5.5 V	3.85		
V_{IL}	Low-level input voltage	V_{CC} = 3 V		0.9	V
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 5.5 V		1.65	
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V		12	mA
		V_{CC} = 4.5 V		24	
		V_{CC} = 5.5 V		24	
I_{OL}	Low-level output current	V_{CC} = 3 V		12	mA
		V_{CC} = 4.5 V		24	
		V_{CC} = 5.5 V		24	
Δt/Δv	Input transition rise or fall rate			8	ns/V
T_A	Operating free-air temperature		–55	125	°C

6.3 Thermal Information

THERMAL METRIC(1) (2)		SN54AC00-SP		UNIT
		J	W	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.1	125.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.6	30.85	
$R_{\theta JB}$	Junction-to-board thermal resistance	47.9	43.4	
ψ_{JT}	Junction-to-top characterization parameter	N/A	N/A	
ψ_{JB}	Junction-to-board characterization parameter	N/A	N/A	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7 and Mil Std 883 method 1012.1 (see www.JEDEC.org).

6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 µA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = –12 mA	3 V	2.56			2.4		
	I_{OH} = –24 mA	4.5 V	3.86			3.7		
		5.5 V	4.86			4.7		
	I_{OH} = –50 mA(1)	5.5 V				3.85		
V_{OL}	I_{OL} = 50 µA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.5	
	I_{OL} = 24 mA	4.5 V			0.36		0.5	
		5.5 V			0.36		0.5	
	I_{OL} = 50 mA(1)	5.5 V					1.65	
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40	µA
C_i	V_I = V_{CC} or GND	5 V		2.6				pF

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.

6.5 Switching Characteristics, V_{CC} = 3.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ±0.3 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	2	7	9.5	1	11	ns
t_{PHL}			1.5	5.5	8	1	9	
t_{PLH} (KGD only)(1)	A or B	Y	1	7	9.5	1	11	ns
t_{PHL} (KGD only)(1)			1	5.5	9.5	1	11	

(1) Specification limits for KGD are based on SMD 5962-8754903

6.6 Switching Characteristics, V_{CC} = 5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ±0.5 V (unless otherwise noted) (see Figure 7-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A or B	Y	1.5	6	8	1	8.5	ns
t_{PHL}			1.5	4.5	6.5	1	7	
t_{PLH} (KGD only)(1)	A or B	Y	1.5	6	8	1	8.5	ns
t_{PHL} (KGD only)(1)			1.5	4.5	8	1	8.5	

(1) Specification limits for KGD are based on SMD 5962-8754903

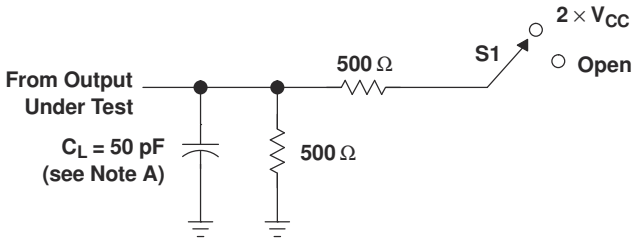
6.7 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

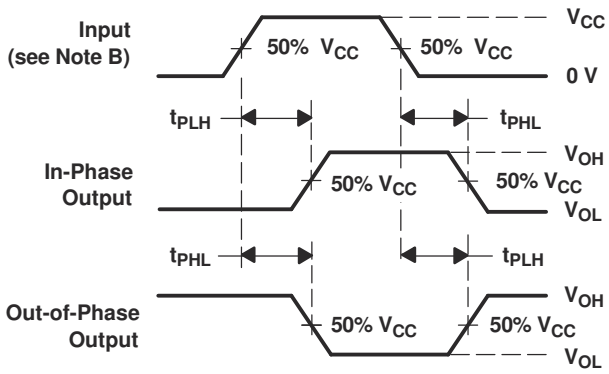
PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF, f = 1 MHz	40	pF

7 Parameter Measurement Information

TEST	S1
t_{PLH}/t_{PHL}	Open



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 7-1. Load Circuit and Voltage Waveforms

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8754903VCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8754903VC A SNV54AC00J	Samples
5962-8754903VDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8754903VD A SNV54AC00W	Samples
5962R8754903V9A	ACTIVE	XCEPT	KGD	0	95	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		Samples
5962R8754903VCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962R8754903VC A SNVR54AC00J	Samples
5962R8754903VDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962R8754903VD A SNVR54AC00W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

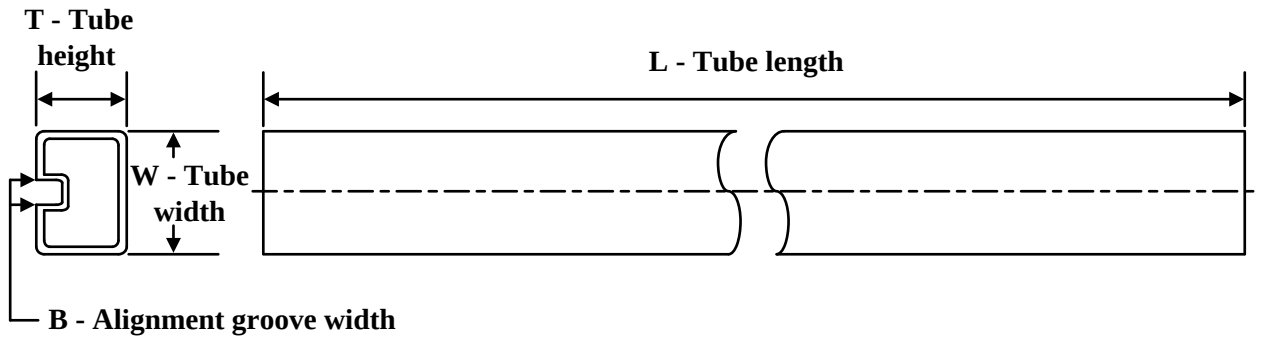
OTHER QUALIFIED VERSIONS OF SN54AC00-SP :

- Catalog : SN54AC00

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

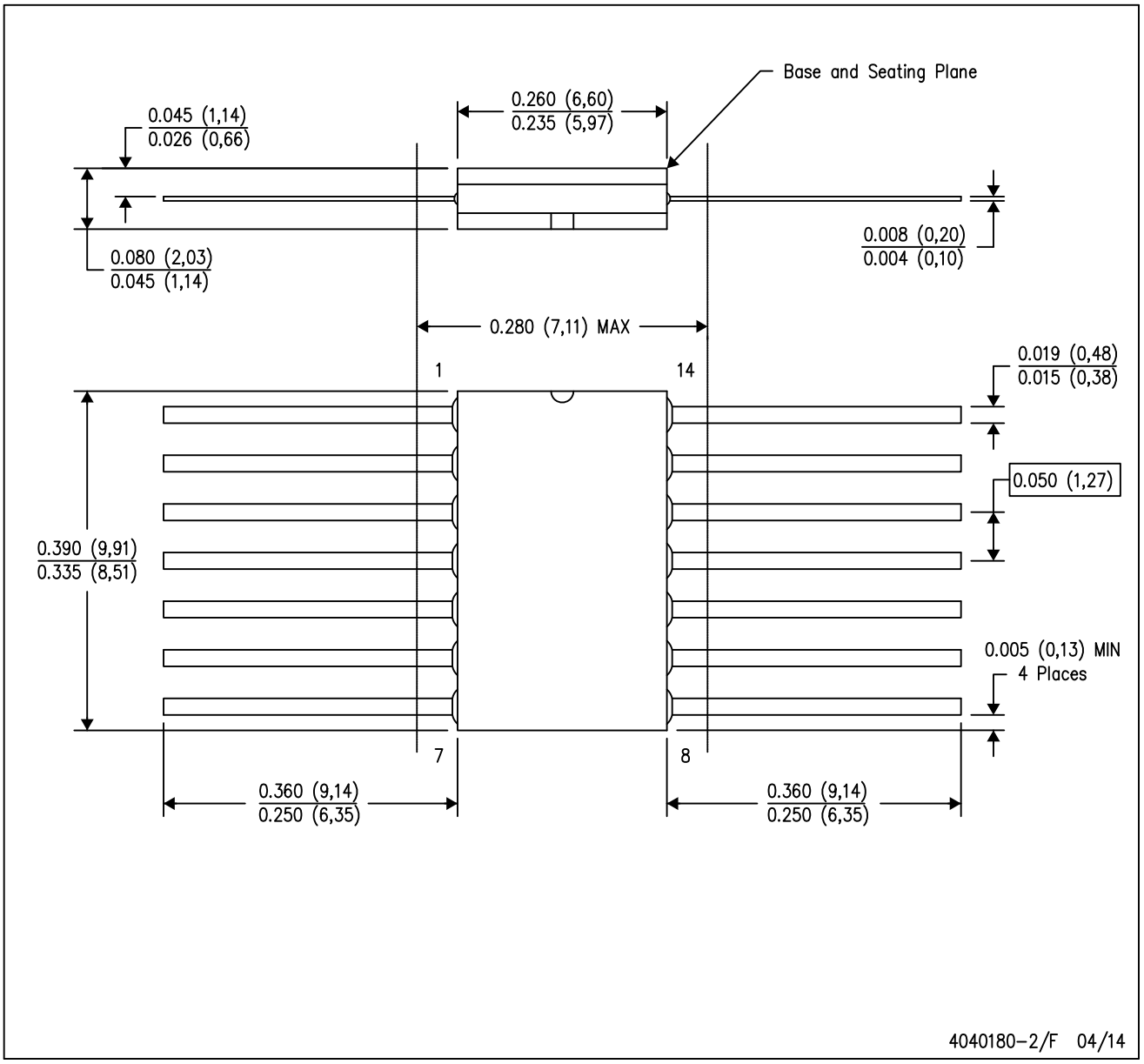
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-8754903VDA	W	CFP	14	25	506.98	26.16	6220	NA
5962R8754903VCA	J	CDIP	14	25	506.98	15.24	13440	NA
5962R8754903VDA	W	CFP	14	25	506.98	26.16	6220	NA

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

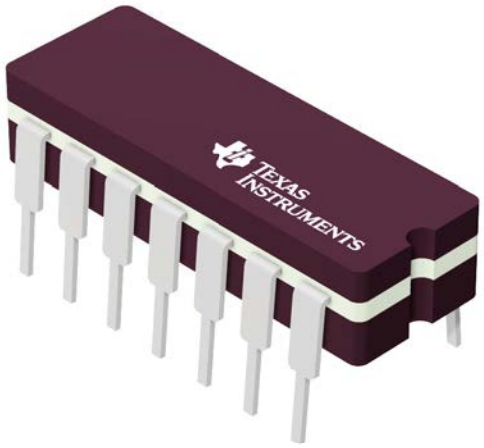


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

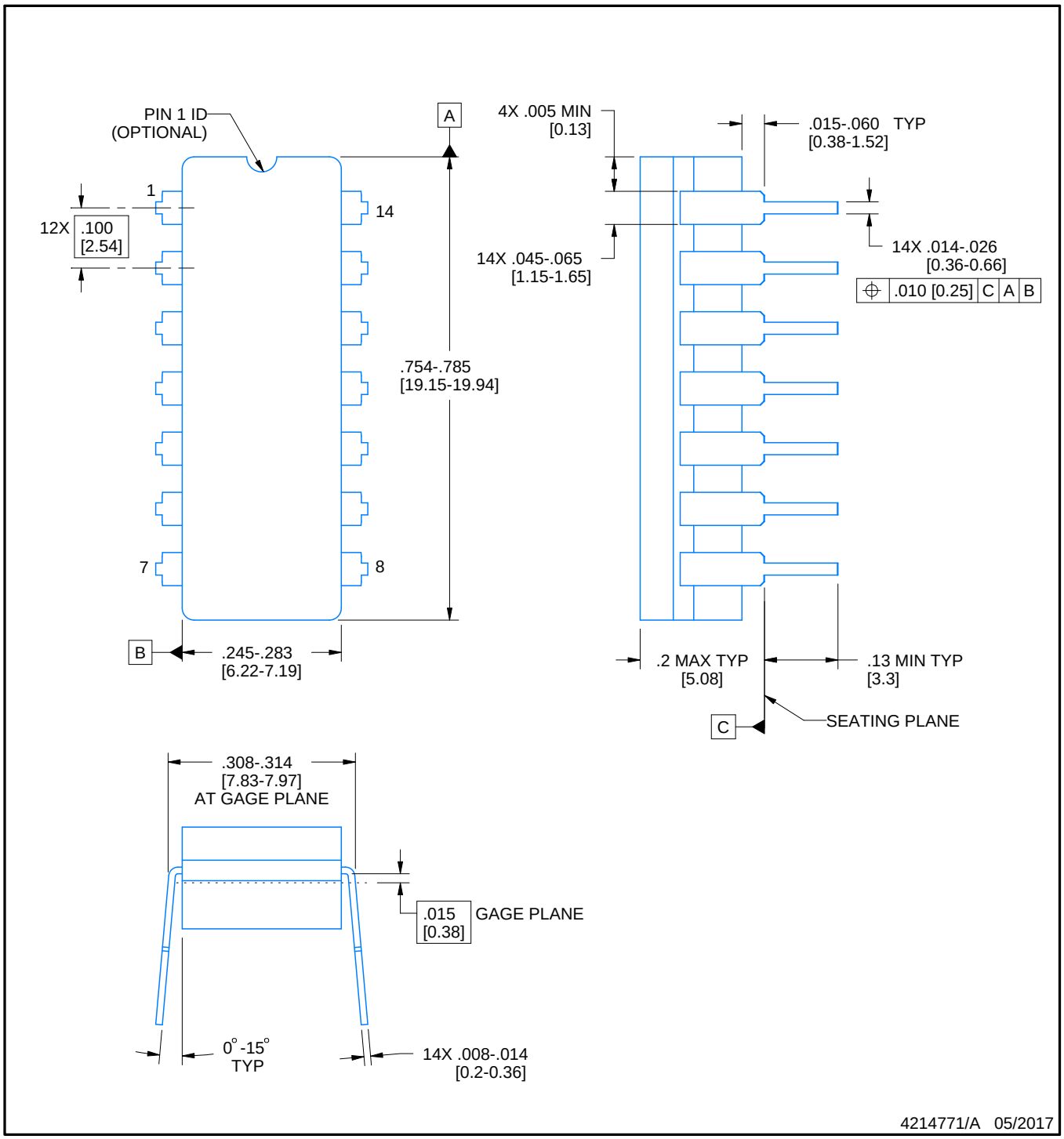
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

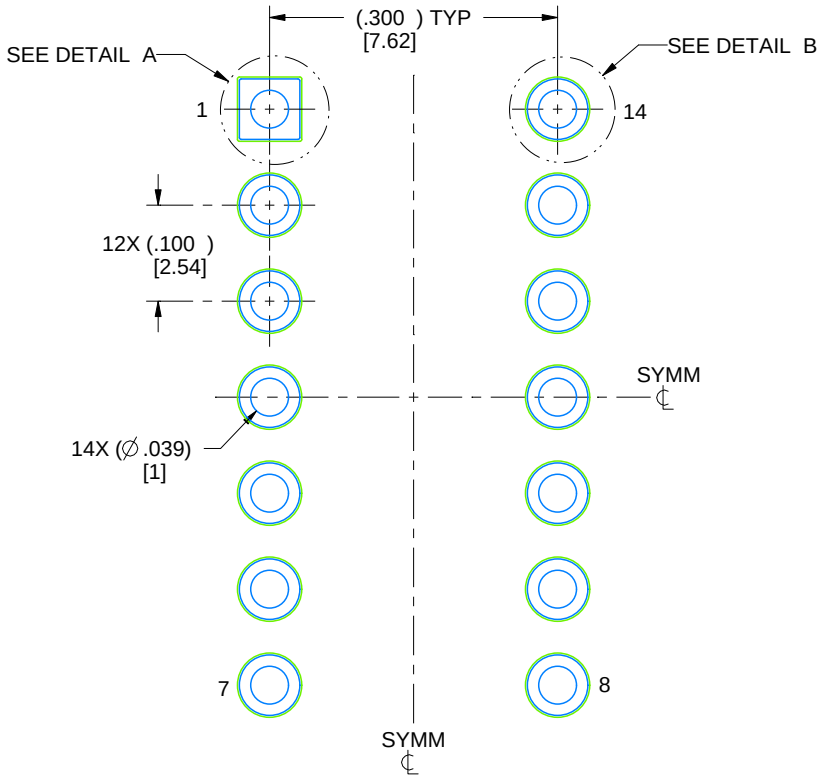
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

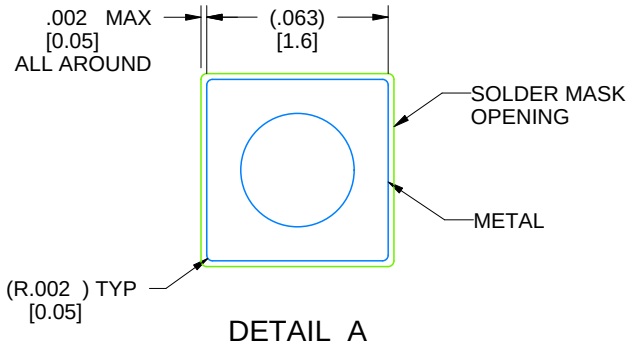
J0014A

CDIP - 5.08 mm max height

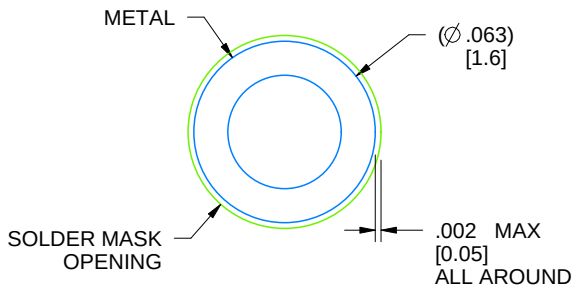
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

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