

SNx4AC374 Octal D-Type Edge-Triggered Flip-Flops with 3-State Outputs

1 Features

- Operation of 2V to 6V V_{CC}
- Inputs accept voltages to 6V
- Max t_{pd} of 9.5ns at 5V
- 3-state noninverting outputs drive bus lines directly
- Full parallel access for loading

2 Description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

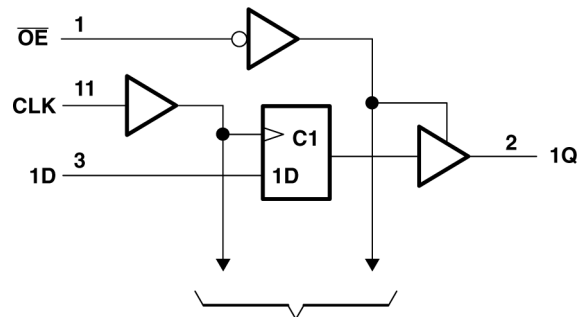
Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | PACKAGE SIZE ⁽²⁾ | BODY SIZE ⁽³⁾ |
|-------------|------------------------|-----------------------------|--------------------------|
| SNx4AC374 | DB (SSOP, 20) | 7.2mm x 7.8mm | 7.2mm x 5.30mm |
| | DW (SOIC, 20) | 12.80mm x 10.3mm | 12.80mm x 7.50mm |
| | N (PDIP, 20) | 24.33mm x 9.4mm | 24.33mm x 6.35mm |
| | NS (SOP, 20) | 12.6mm x 7.8mm | 12.6mm x 5.3mm |
| | PW (TSSOP, 20) | 6.50mm x 6.4mm | 6.50mm x 4.40mm |

(1) For more information, see [Section 10](#).

(2) The package size (length x width) is a nominal value and includes pins, where applicable.

(3) The body size (length x width) is a nominal value and does not include pins.



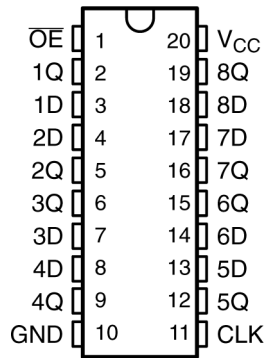
To Seven Other Channels
Logic Diagram (Positive Logic)



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3 Pin Configuration and Functions



**Figure 3-1. SN54AC374 J or W Package;
SN74AC374 DB, DW, N, NS, or PW Package (Top
View)**

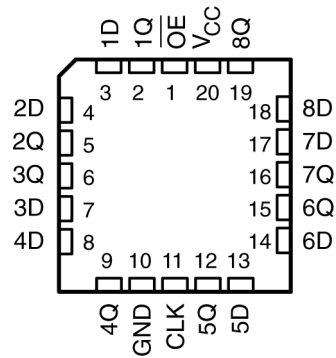


Figure 3-2. SN54AC374 FK Package (Top View)

Table 3-1. Pin Functions

| PIN | | TYPE | DESCRIPTION |
|-----------------|-----|------|-------------|
| NAME | NO. | | |
| OE | 1 | I | Enable pin |
| 1Q | 2 | O | Output 1 |
| 1D | 3 | I | Input 1 |
| 2D | 4 | I | Input 2 |
| 2Q | 5 | O | Output 2 |
| 3Q | 6 | O | Output 3 |
| 3D | 7 | I | Input 3 |
| 4D | 8 | I | Input 4 |
| 4Q | 9 | O | Output 4 |
| GND | 10 | – | Ground pin |
| CLK | 11 | I | Clock pin |
| 5Q | 12 | O | Output 5 |
| 5D | 13 | I | Input 5 |
| 6D | 14 | I | Input 6 |
| 6Q | 15 | O | Output 6 |
| 7Q | 16 | O | Output 7 |
| 7D | 17 | I | Input 7 |
| 8D | 18 | I | Input 8 |
| 8Q | 19 | O | Output 8 |
| V _{CC} | 20 | – | Power pin |

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)¹

| | | MIN | MAX | UNIT |
|---|---------------------------|---|-----------------------|---------|
| V _{CC} | Supply voltage range | -0.5 | 7 | V |
| V _I ² | Input voltage range | -0.5 | V _{CC} + 0.5 | V |
| V _O ² | Output voltage range | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | (V _I < 0 or V _I > V _{CC}) | | ±20 mA |
| I _{OK} | Output clamp current | (V _O < 0 or V _O > V _{CC}) | | ±20 mA |
| I _O | Continuous output current | (V _O = 0 to V _{CC}) | | ±50 mA |
| Continuous current through V _{CC} or GND | | | | ±200 mA |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

4.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)¹

| | | SN54AC374 | | SN74AC374 | | UNIT |
|-----------------|------------------------------------|-------------------------|-----------------|-----------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 2 | 6 | 2 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 3 V | 2.1 | 2.1 | | V |
| | | V _{CC} = 4.5 V | 3.15 | 3.15 | | |
| | | V _{CC} = 5.5 V | 3.85 | 3.85 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 3 V | 0.9 | | 0.9 | V |
| | | V _{CC} = 4.5 V | 1.35 | | 1.35 | |
| | | V _{CC} = 5.5 V | 1.65 | | 1.65 | |
| V _I | Input voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 3 V | -12 | | -12 | mA |
| | | V _{CC} = 4.5 V | -24 | | -24 | |
| | | V _{CC} = 5.5 V | -24 | | -24 | |
| I _{OL} | Low-level output current | V _{CC} = 3 V | 12 | | 12 | mA |
| | | V _{CC} = 4.5 V | 24 | | 24 | |
| | | V _{CC} = 5.5 V | 24 | | 24 | |
| Δt/Δv | Input transition rise or fall rate | 8 | | 8 | | ns/V |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

- (1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4.3 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN74AC374 | | | | | UNIT |
|---|-----------|-----------|----------|---------|------------|------|
| | DB (SSOP) | DW (SOIC) | N (PDIP) | NS (SO) | PW (TSSOP) | |
| | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| R _{θJA} Junction-to-ambient thermal resistance | 70 | 101.2 | 69 | 60 | 83 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

4.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54AC374 | | SN74AC374 | | UNIT |
|-----------------|---|-----------------|-----------------------|-----|-------|-----------|-----|-----------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50μA | 3 V | 2.9 | | | 2.9 | | 2.9 | V | |
| | | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | |
| | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | I _{OH} = -12 mA | 3 V | 2.56 | | | 2.4 | | 2.46 | | |
| | | 4.5 V | 3.86 | | | 3.7 | | 3.76 | | |
| | | 5.5 V | 4.86 | | | 4.7 | | 4.76 | | |
| V _{OL} | I _{OL} = 50μA | 3 V | | | 0.1 | | 0.1 | 0.1 | V | |
| | | 4.5 V | | | 0.1 | | 0.1 | 0.1 | | |
| | | 5.5 V | | | 0.1 | | 0.1 | 0.1 | | |
| | I _{OL} = 12 mA | 3 V | | | 0.36 | | 0.5 | 0.44 | | |
| | | 4.5 V | | | 0.36 | | 0.5 | 0.44 | | |
| | | 5.5 V | | | 0.36 | | 0.5 | 0.44 | | |
| I _I | V _I = V _{CC} or GND | 5.5 V | | | ±0.1 | | ±1 | ±1 | μA | |
| I _{OZ} | V _O = V _{CC} or GND | 5.5 V | | | ±0.25 | | ±5 | ±2.5 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 4 | | 80 | 40 | μA | |
| C _i | V _I = V _{CC} or GND | 5 V | | | 4.5 | | | | pF | |

4.5 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| | | T _A = 25°C | | SN54AC374 | | SN74AC374 | | UNIT |
|--------------------|---------------------------------|-----------------------|-----|-----------|-----|-----------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f _{clock} | Clock frequency | | 60 | | 60 | | 60 | MHz |
| t _w | Pulse duration, CLK high or low | 5.5 | | 6.5 | | 6 | | ns |
| t _{su} | Setup time, data before CLK↑ | 5.5 | | 6.5 | | 6 | | ns |
| t _h | Hold time, data after CLK↑ | 1 | | 1 | | 1 | | ns |

4.6 Timing Requirements, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| | | $T_A = 25^\circ\text{C}$ | | SN54AC374 | | SN74AC374 | | UNIT |
|--------------------|--|--------------------------|-----|-----------|-----|-----------|-----|------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | 100 | | 95 | | 100 | | MHz |
| t_w | Pulse duration, CLK high or low | 4 | | 5 | | 4.5 | | ns |
| t_{su} | Setup time, data before CLK \uparrow | 4 | | 5 | | 4.5 | | ns |
| t_h | Hold time, data after CLK \uparrow | 1.5 | | 1.5 | | 1.5 | | ns |

4.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | TO (INPUT) | TO (OUTPUT) | $T_A = 25^\circ\text{C}$ | | | SN54AC374 | | SN74AC374 | | UNIT |
|------------------|------------------------|-------------|--------------------------|------|------|-----------|------|-----------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 60 | 110 | | 60 | | 60 | MHz | |
| t_{PLH} | CLK | Q | 3 | 11 | 13.5 | 3 | 16.5 | 1.5 | 15.5 | ns |
| t_{PHL} | | | 2.5 | 10 | 12.5 | 3 | 15 | 2 | 14 | |
| t_{PZH} | $\overline{\text{OE}}$ | Q | 3 | 9.5 | 11.5 | 1 | 14 | 1.5 | 13 | ns |
| t_{PZL} | | | 3.5 | 9 | 11.5 | 1 | 14 | 1.5 | 13 | |
| t_{PHZ} | $\overline{\text{OE}}$ | Q | 3 | 10.5 | 12.5 | 1 | 16 | 2 | 14.5 | ns |
| t_{PLZ} | | | 2 | 8 | 11.5 | 1 | 13 | 1 | 12.5 | |

4.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

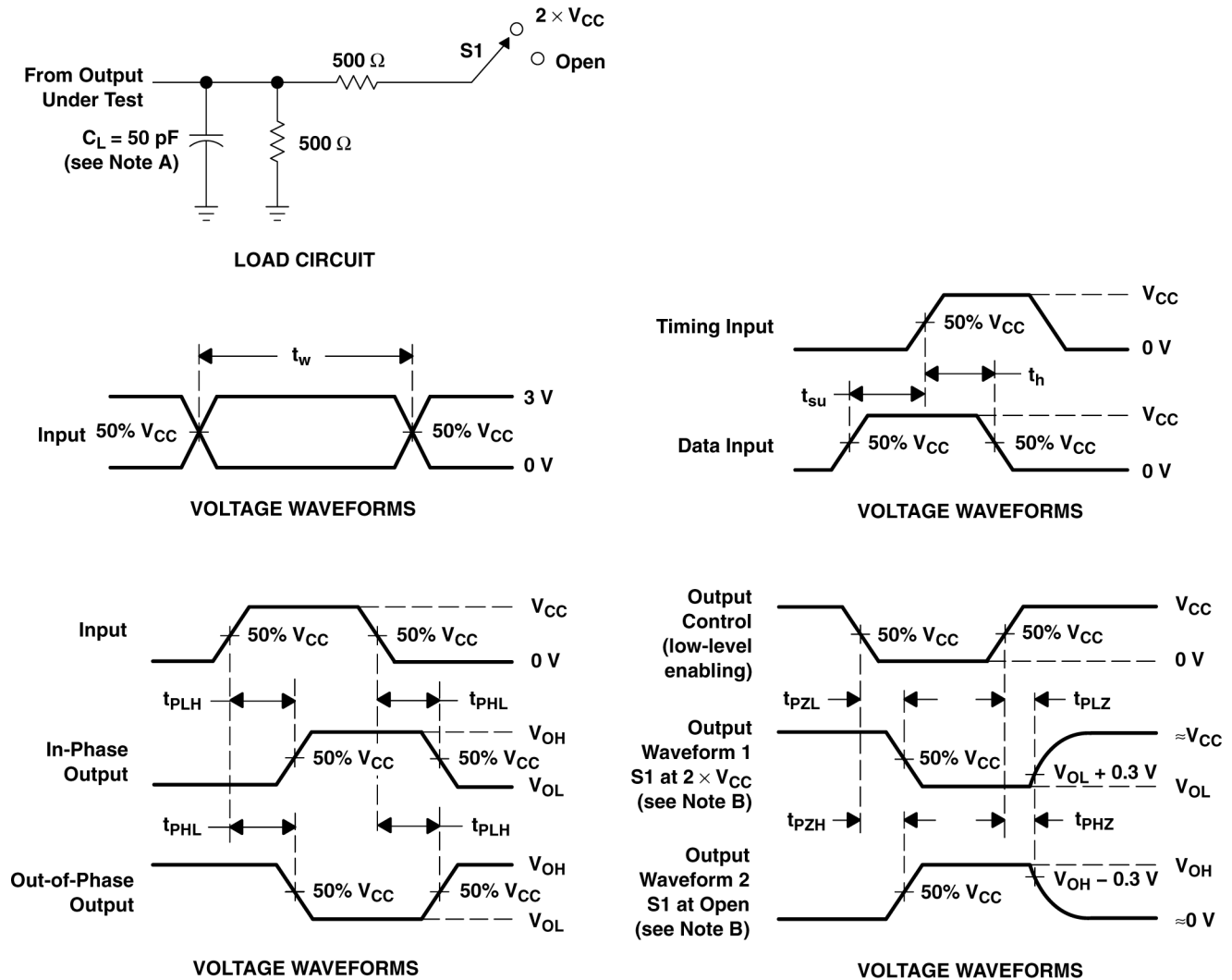
| PARAMETER | TO (INPUT) | TO (OUTPUT) | $T_A = 25^\circ\text{C}$ | | | SN54AC374 | | SN74AC374 | | UNIT |
|------------------|------------------------|-------------|--------------------------|-----|-----|-----------|------|-----------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| f_{max} | | | 100 | 155 | | 95 | | 100 | MHz | |
| t_{PLH} | CLK | Q | 2.5 | 8 | 9.5 | 3 | 12 | 1.5 | 10.5 | ns |
| t_{PHL} | | | 2 | 7 | 9 | 3 | 11 | 1.5 | 10 | |
| t_{PZH} | $\overline{\text{OE}}$ | Q | 2 | 7 | 8.5 | 1.5 | 10 | 1 | 9.5 | ns |
| t_{PZL} | | | 2 | 6.5 | 8.5 | 1.5 | 10.5 | 1 | 9.5 | |
| t_{PHZ} | $\overline{\text{OE}}$ | Q | 2 | 8 | 11 | 1.5 | 12.5 | 2 | 12.5 | ns |
| t_{PLZ} | | | 1.5 | 6.5 | 8.5 | 1.5 | 10.5 | 1 | 10 | |

4.9 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-----------------|--|-----|------|
| C_{pd} | Power dissipation capacitance $C_L = 50\text{ pF}$, $f = 1\text{ MHz}$ | 40 | pF |

5 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 5-1. Load Circuit and Voltage Waveforms

| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | Open |

6 Detailed Description

6.1 Overview

The eight flip-flops of the 'AC374 devices are D-type edge-triggered flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines in bus-organized systems without need for interface or pullup components.

\overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

For specified high-impedance state during power up or power down, \overline{OE} must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

6.2 Functional Block Diagram

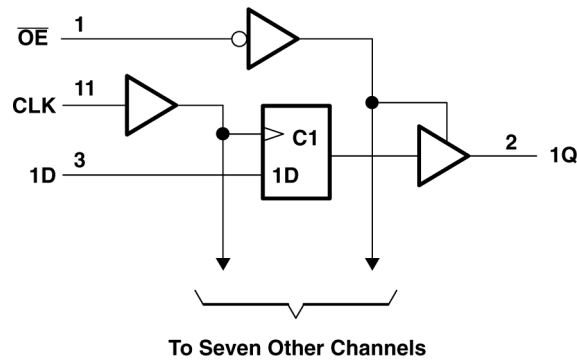


Figure 6-1. Logic Diagram (Positive Logic)

6.3 Device Functional Modes

Table 6-1. Function Table (Each Flip-flop)

| INPUTS | | | OUTPUT Q |
|--------|--------|---|----------|
| OE | CLK | D | |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q_0 |
| H | X | X | Z |

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in [Section 4.2](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1 μF and if there are multiple V_{CC} terminals, then TI recommends .01 μF or .022 μF for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

7.2.1.1 Layout Example

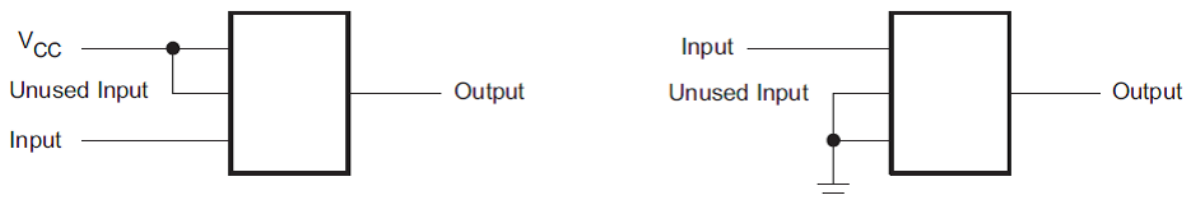


Figure 7-1. Layout Example

8 Device and Documentation Support

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54AC374 | Click here | Click here | Click here | Click here | Click here |
| SN74AC374 | Click here | Click here | Click here | Click here | Click here |

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

8.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (August 2023) to Revision G (February 2024) Page

- Updated RθJA value: DW = 58 to 101.2, all values in °C/W 5
- Added *Application and Implementation* section..... 9

Changes from Revision E (October 2003) to Revision F (August 2023) Page

- Added *Device Information* table, *Pin Functions* table, *Thermal Information* table, *Device Functional Modes, Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|------------------------------------|-------------------------|
| 5962-87694012A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-87694012A SNJ54AC 374FK | Samples |
| 5962-8769401RA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8769401RA SNJ54AC374J | Samples |
| 5962-8769401SA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8769401SA SNJ54AC374W | Samples |
| SN74AC374DBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC374 | Samples |
| SN74AC374DW | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | -40 to 85 | AC374 | |
| SN74AC374DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC374 | Samples |
| SN74AC374N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74AC374N | Samples |
| SN74AC374NSR | ACTIVE | SO | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC374 | Samples |
| SN74AC374PW | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI | -40 to 85 | AC374 | |
| SN74AC374PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC374 | Samples |
| SNJ54AC374FK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-87694012A SNJ54AC 374FK | Samples |
| SNJ54AC374J | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8769401RA SNJ54AC374J | Samples |
| SNJ54AC374W | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-8769401SA SNJ54AC374W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AC374, SN74AC374 :

● Catalog : [SN74AC374](#)

● Military : [SN54AC374](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AC374DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AC374DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AC374DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AC374NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AC374PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AC374DBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AC374DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AC374DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AC374NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AC374PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-87694012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-8769401SA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74AC374N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54AC374FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AC374W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

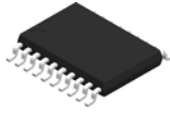
W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





4229370VA\

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 -  The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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