USB PORT TRANSIENT SUPPRESSORS

FEATURES

- **Qualified for Automotive Applications**
- **Design to Protect Submicron 3-V or 5-V Circuits from Noise Transients**
- **Port ESD Protection Capability Exceeds:**
  - **15-kV Human Body Model**
  - **2-kV Machine Model**
- **Available in a WCSP Chip-Scale Package**
- **Stand-Off Voltage . . . 6 V Min**
- **Low Current Leakage . . . 1 μA Max at 6 V**
- **Low Capacitance . . . 35 pF Typ**

APPLICATIONS

- **USB 1.1 Host, Hub, or Peripheral Ports**

DESCRIPTION

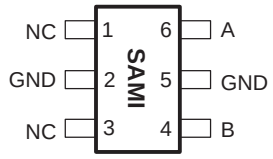
The SN65220 is a single transient voltage suppressor designed to provide electrical noise transient protection to universal serial bus (USB) 1.1 ports. Note that the input capacitance of the device makes it unsuitable for high-speed USB 2.0 applications.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the USB transceiver and/or the USB ASIC if they are of sufficient magnitude and duration.

USB ports are typically implemented in 3-V or 5-V digital CMOS with limited ESD protection. The SN65220 can significantly increase the port ESD protection level and reduce the risk of damage to the circuits of the USB port.

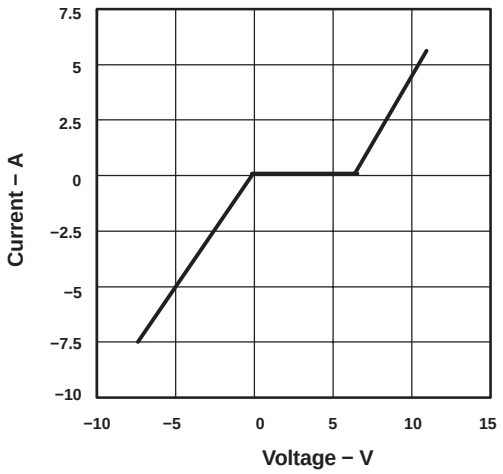
The IEC1000-4-2 ESD performance of the SN65220 is measured at the system level. Therefore, system design impacts the results of these tests. A high compliance level may be attained with proper board design and layout.

DBV
(TOP VIEW)†



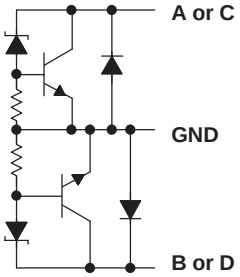
NC − No internal connection
†When read horizontally, pin 1 is the bottom left pin.

CURRENT vs VOLTAGE



NOTE A: Typical current versus voltage curve was derived using the IEC 1.2/50-μs surge waveform.

EQUIVALENT SCHEMATIC DIAGRAM



(One Suppressor Shown)

NOTE: All GND terminals should be connected to ground.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

IEC1000-4-2 COMPLIANCE LEVEL

IEC1000-4-2 COMPLIANCE LEVEL	MAXIMUM TEST VOLTAGE	
	CONTACT DISCHARGE (kV)	AIR DISCHARGE (kV)
1	2	2
2	4	4
3	6	8
4	8	15

PACKAGE/ORDERING INFORMATION†

PRODUCT	SUPRESSORS	T_A	PACKAGE‡	PACKAGE DESIGNATOR	MARKED AS	ORDER NUMBER
SN65220	1	−40°C to 85°C	SOT23−6	DBV	SAMI	SN65220IDBVRQ1 (Mini Reel)

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.

‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UNIT
Continuous power dissipation	See Dissipation Rating Table
Electrostatic discharge	15 kV(2), 2 kV(3)
Peak power dissipation, $P_{D(peak)}$	60 W
Peak forward surge current, I_{FSM}	3 A
Peak reverse surge current, I_{RSM}	−9 A
Storage temperature range, T_{stg}	−65°C to 150°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) Human Body Model − Tested in accordance with JEDEC Standard 22, Test Method A114−A.

(3) Charged Device Model − Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$‡	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBV	385 mW	3.1 mW/°C	246 mW	200 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

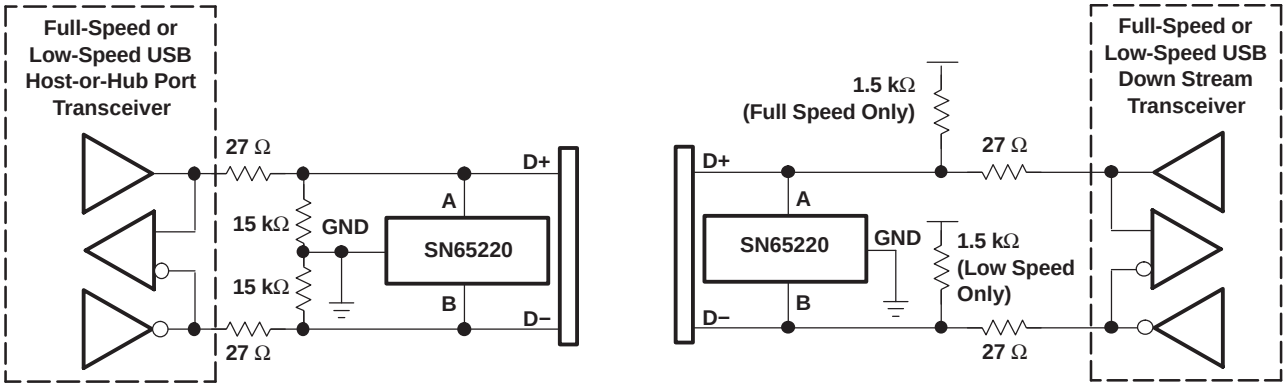
recommended operating conditions

	MIN	MAX	UNIT
Operating free-air temperature, T_A	−40	85	°C

electrical characteristics over recommended operating conditions (unless otherwise noted)

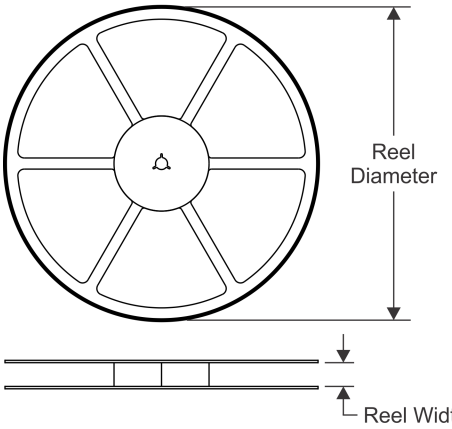
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{lkg}	Leakage current	V_I = 6 V at A, B, C, or D terminals			1	μA
$V_{(BR)}$	Breakdown voltage	V_I = 1 mA at A, B, C, or D terminals	6.5	7	8	V
C_{IN}	Input capacitance to ground	V_I = 0.4 sin (4E6πt) + 0.5 V		35		pF

APPLICATION INFORMATION

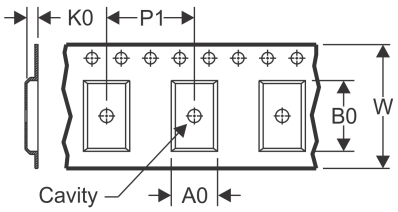


TAPE AND REEL INFORMATION

REEL DIMENSIONS

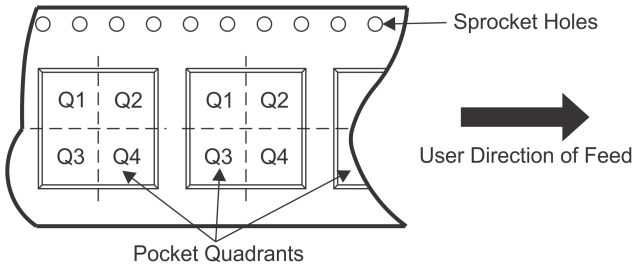


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

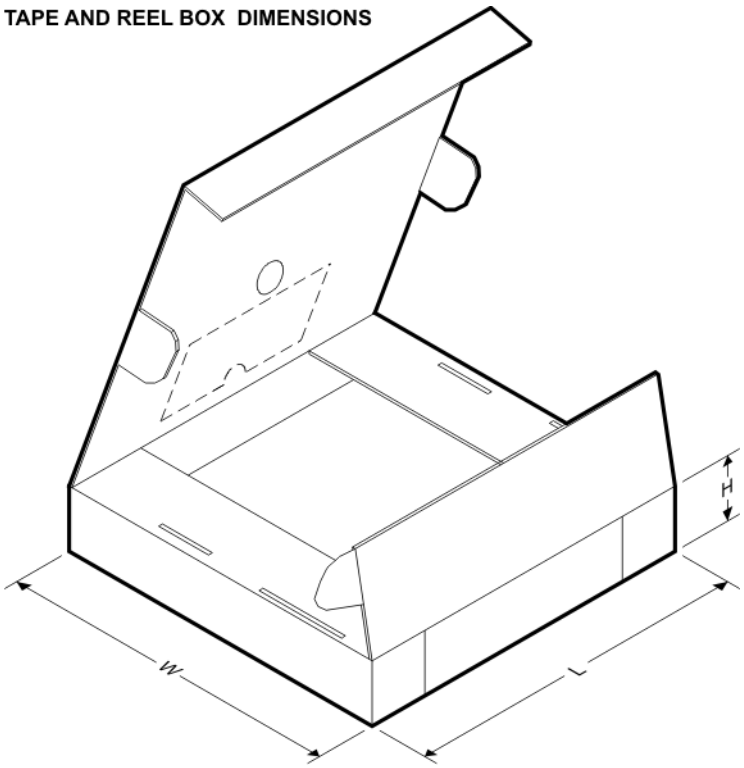
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65220IDBVRQ1	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

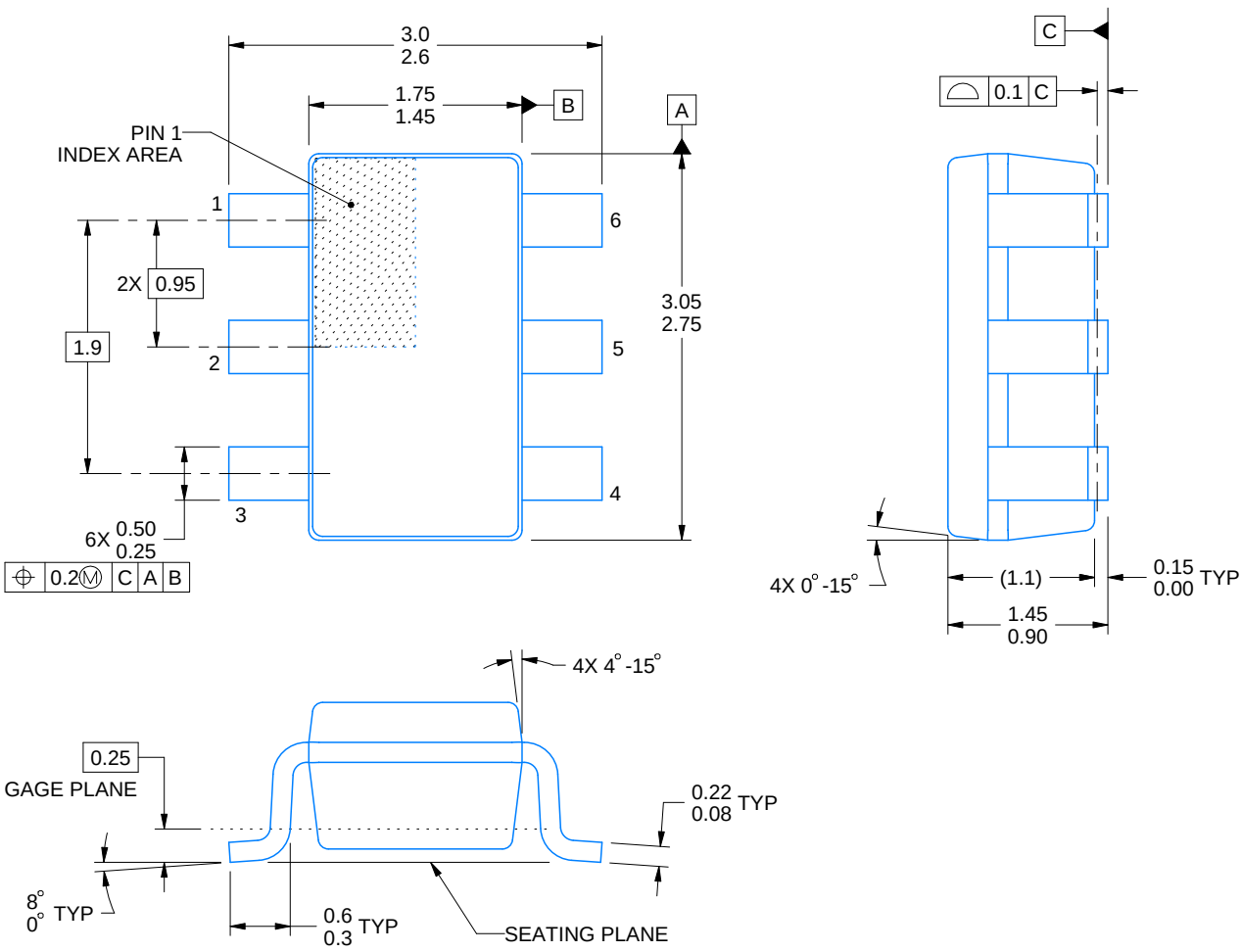
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65220IDBVRQ1	SOT-23	DBV	6	3000	182.0	182.0	20.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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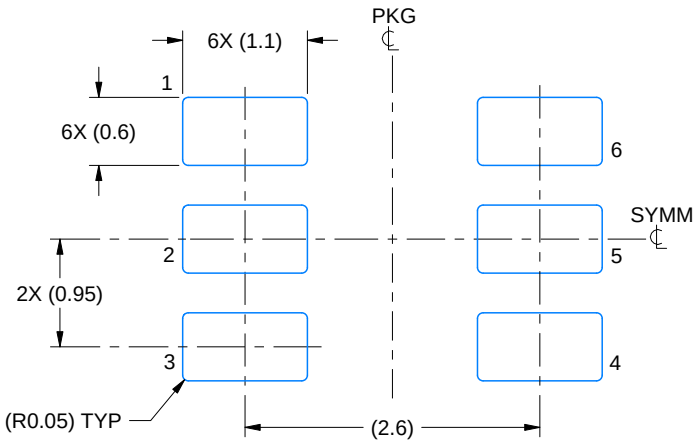
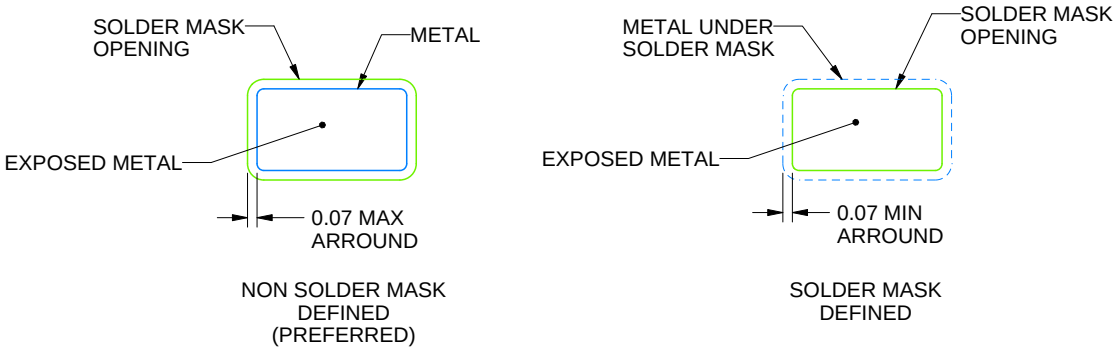
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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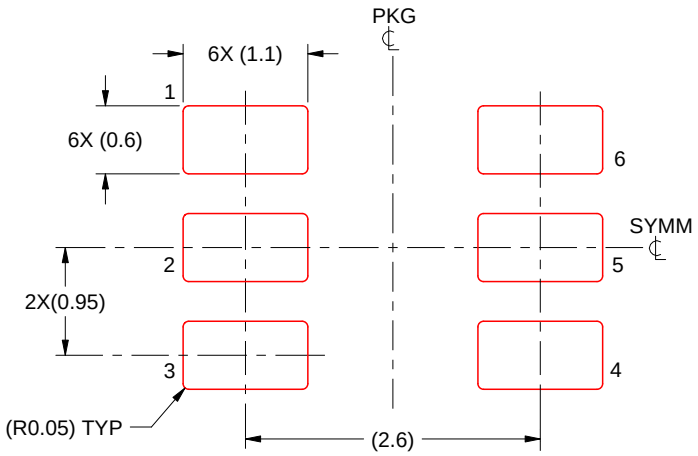
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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