# SN65LBC172, SN75LBC172 Quadruple Low-Power Differential Line Driver

## 1 Features

- Exceeds or meets EIA standard RS-485
- Designed for high-speed multipoint transmission on long bus lines in noisy environments
- Supports data rates up to and exceeding ten million transfers per second
- Provides a common-mode output voltage range of −7V to 12V
- Offers positive-and negative-current limiting
- Consumes low power to 1.5mA max (output disabled)
- Functions interchangeably with the SN75172

## 2 Applications

- Motor drives
- Factory automation and control

## 3 Description

The SN65LBC172 and SN75LBC172 are monolithic quadruple differential line drivers with three-state outputs. Both devices are designed to meet the requirements of EIA Standard RS-485. These devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common- mode output voltage ranges, current limiting, and thermal-shutdown circuitry which provides a party-line application in noisy environments. Both devices are designed using LinBiCMOS™, facilitating ultra-low power consumption and inherent robustness.

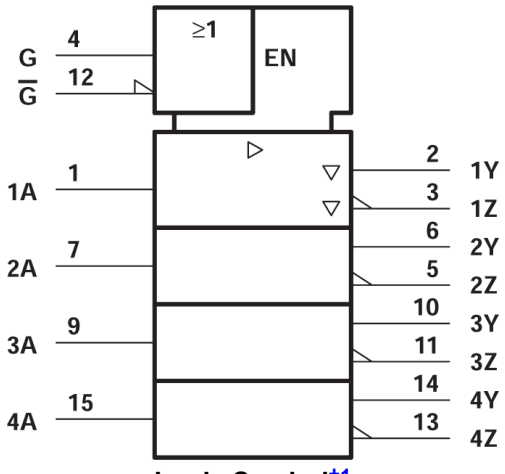
Both the SN65LBC172 and SN75LBC172 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. These devices offer optimum performance when used with the SN75LBC173 or SN75LBC175 quadruple line receivers. The SN65LBC172 and SN75LBC172 are available in the 16-pin DIP package (N) and the 20-pin wide-body small-outline inline-circuit (SOIC) package (DW).

The SN75LBC172 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC172 is characterized over the industrial temperature range of −40°C to 85°C.

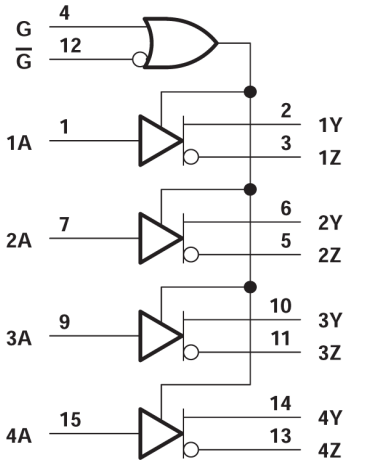
**Package Information**

| PART NUMBER | PACKAGE(1) | PACKAGE SIZE(2) |
|---|---|---|
| SN65LBC172<br>SN75LBC172 | DW (SOIC, 20) | 10.3mm × 10.3mm |
| | N (PDIP 16) | 19.3mm × 9.4mm |

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.




**Logic Symbol†1**




**Logic Diagram (Positive Logic)**

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
1 Pin numbers shown are for the N package.

# Table of Contents

## 4 Pin Configuration and Functions

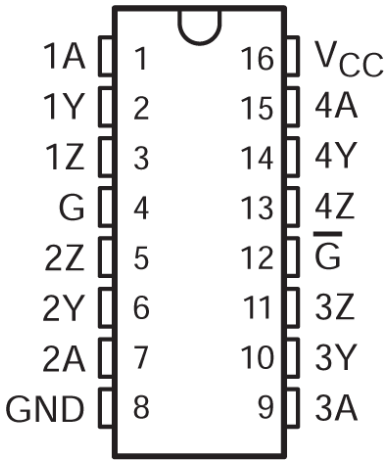



**Figure 4-1. N Package (Top View)**

**Table 4-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1A | 1 | I | Driver 1 input |
| 1Y | 2 | O | Driver 1 output |
| 1Z | 3 | O | Driver 1 inverted output |
| G | 4 | I | Active high enable all drivers |
| 2Z | 5 | O | Driver 2 inverted output |
| 2Y | 6 | O | Driver 2 output |
| 2A | 7 | I | Driver 2 input |
| GND | 8 | G | Ground pin |
| 3A | 9 | I | Driver 3 input |
| 3Y | 10 | O | Driver 3 output |
| 3Z | 11 | O | Driver 3 inverted output |
| $\overline{G}$ | 12 | I | Active low enable all drivers |
| 4Z | 13 | O | Driver 4 inverted output |
| 4Y | 14 | O | Driver 4 output |
| 4A | 15 | O | Driver 4 input |
| $V_{CC}$ | 16 | P | Power pin |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

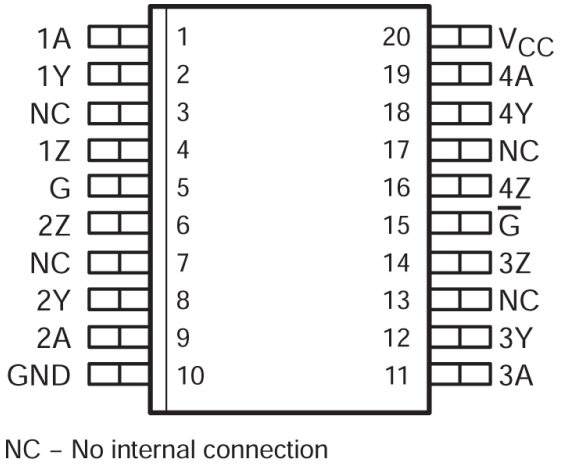



**Figure 4-2. DW Package (Top View)**

**Table 4-2. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| 1A | 1 | I | Driver 1 input |
| 1Y | 2 | O | Driver 1 output |
| NC | 3 | - | No Internal Connection |
| 1Z | 4 | O | Driver 1 inverted output |
| G | 5 | I | Active high enable all drivers |
| 2Z | 6 | O | Driver 2 inverted output |
| NC | 7 | - | No Internal Connection |
| 2Y | 8 | O | Driver 2 output |
| 2A | 9 | I | Driver 2 input |
| GND | 10 | G | Ground pin |
| 3A | 11 | I | Driver 3 input |
| 3Y | 12 | O | Driver 3 output |
| NC | 13 | - | No Internal Connection |
| 3Z | 14 | O | Driver 3 inverted output |
| $\overline{G}$ | 15 | I | Active low enable all drivers |
| 4Z | 16 | O | Driver 4 inverted output |
| NC | 17 | – | No Internal Connection |
| 4Y | 18 | O | Driver 4 output |
| 4A | 19 | I | Driver 4 input |
| $V_{CC}$ | 20 | P | Power pin |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range, (see (3)) | −0.3 | 7 | V |
| $V_O$ | Output voltage range | −10 | 15 | V |
| $V_I$ | Voltage range at A, $\overline{G}$, G | −0.3 | $V_{CC}$ + 0.5 | V |
| $P_D$ | Continuous power dissipation | Internally limited(2) | | |
| $T_{stg}$ | Storage temperature range | −65 | 150 | °C |
| $T_{LEAD}$ | Lead temperature 1,6mm (1/16 inch) from case for 10 seconds | | 260 | °C |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
(3) All voltage values are with respect to GND.

## 5.2 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, $V_{IH}$ | | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | | | | 0.8 | V |
| Voltage at any bus terminal (separately or common mode), $V_O$ | Y or Z | -7 | | 12 | V |
| High-level output current, $I_{OH}$ | Y or Z | | | −60 | mA |
| Low-level output current, $I_{OL}$ | Y or Z | | | 60 | mA |
| Continuous total power dissipation | | See Dissipation Rating Table | | | |
| Junction temperature, $T_J$ | | | | 140 | °C |
| Operating free-air temperature, $T_A$ | SN65LBC172 | −40 | | 85 | °C |
| | SN75LBC172 | 0 | | 70 | |

## 5.3 Dissipation Rating Table

| PACKAGE | THERMAL MODEL | $T_A$ < 25°C POWER RATING | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|---|
| DW | Low K(1) | 1094mW | 10.4mW/°C | 625mW | 469mW |
| | High K(2) | 1669mW | 15.9mW/°C | 954mW | 715mW |
| N | | 1150mW | 9.2mW/°C | 736mW | 598mW |

(1) In accordance with the low effective thermal conductivity metric definitions of EIA/JESD 51−3.
(2) In accordance with the high effective thermal conductivity metric definitions of EIA/JESD 51−7.

## 5.4 Thermal Information

| THERMAL METRIC[1] | | N (PDIP) | DW (SOIC) | UNIT |
|---|---|---|---|---|
| | | 16 PINS | 20 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 60.6 | 66.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 48.1 | 34.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 40.6 | 39.7 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 27.5 | 8.9 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 40.3 | 39 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP [1] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | $I_I$ = -18mA | | | | -1.5 | V |
| $\|V_{OD}\|$ | Differential output voltage[2] | $R_L$ = 54Ω See Figure 6-1 | SN65LBC172 | 1.1 | 1.8 | 5 | |
| | | | SN75LBC172 | 1.5 | 1.8 | 5 | V |
| | | $R_L$ = 60Ω, See Figure 6-2 | SN65LBC172 | 1.1 | 1.7 | 5 | |
| | | | SN75LBC172 | 1.5 | 1.7 | 5 | |
| $\Delta\|V_{OD}\|$ | Change in magnitude of common-mode output voltage[3] | $R_L$ = 54Ω, | See Figure 6-1 | | | ±0.2 | V |
| $V_{OC}$ | Common-mode output voltage | | | -1 | | 3 | V |
| $\Delta\|V_{OC}\|$ | Change in magnitude of common-mode output voltage[3] | | | | | ±0.2 | V |
| $I_O$ | Output current with power off | $V_{CC}$ = 0, | $V_O$ = - 7V to 12V | | | ± 100 | µA |
| $I_{OZ}$ | High-impedance-state output current | $V_O$ = - 7V to 12V | | | | ± 100 | µA |
| $I_{IH}$ | High-level input current | $V_I$ = 2.4V | | | | -100 | µA |
| $I_{IL}$ | Low-level input current | $V_I$ = 0.4V | | | | -100 | µA |
| $I_{OS}$ | Short-circuit output current | $V_O$ = -7V to 12V | | | | ±250 | mA |
| $I_{CC}$ | Supply current (all drivers) | No load | Outputs enabled | | | 7 | mA |
| | | | Outputs disabled | | | 1.5 | |

(1) All typical values are at $V_{CC}$ = 5V and $T_A$ = 25°C.
(2) The minimum $V_{OD}$ specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal-transmission distance.
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of $V_{OD}$ and $V_{OC}$, respectively, that occur when the input changes from a high level to a low level.

## 5.6 Switching Characteristics

$V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{d(OD)}$ | Differential output delay time | $R_L$ = 54Ω, | See Figure 6-3 | 2 | 11 | 20 | ns |
| $t_{t(OD)}$ | Differential output transition time | | | 9 | 15 | 25 | |
| $t_{PZH}$ | Output enable time to high level | $R_L$ = 110Ω, | See Figure 6-4 | | 20 | 30 | ns |
| $t_{PZL}$ | Output enable time to low level | $R_L$ = 110Ω, | See Figure 6-5 | | 21 | 30 | ns |
| $t_{PHZ}$ | Output disable time from high level | $R_L$ = 110Ω, | See Figure 6-4 | | 48 | 70 | ns |
| $t_{PLZ}$ | Output disable time from low level | $R_L$ = 110Ω, | See Figure 6-5 | | 21 | 30 | ns |

## 5.7 Typical Characteristics

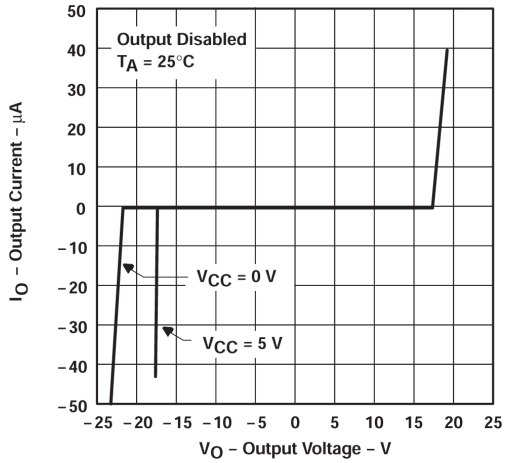



**Figure 5-1. Output Current vs Output Voltage**

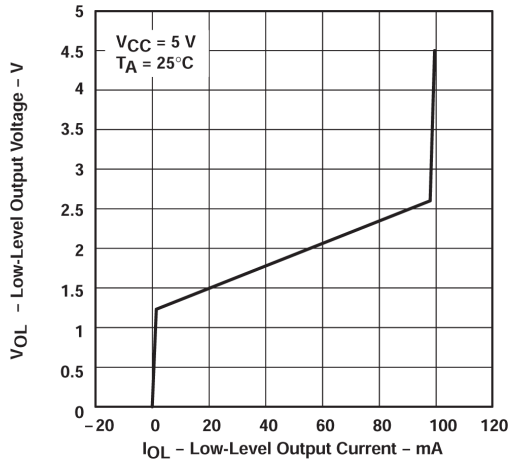



**Figure 5-2. Low-level Output Voltage vs Low-level Output Current**

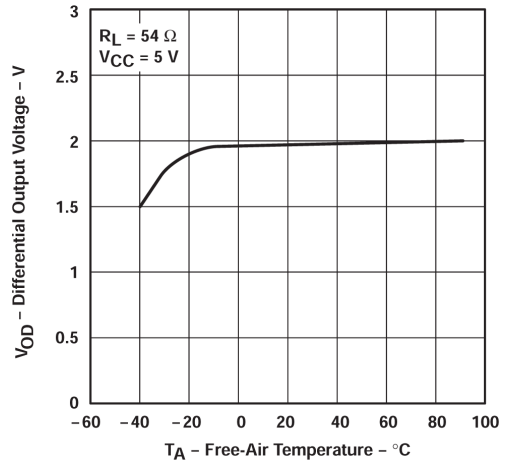



**Figure 5-3. Differential Output Voltage vs Free-air Temperature**

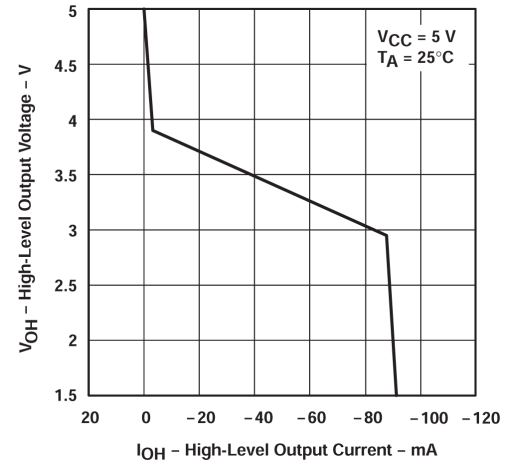



**Figure 5-4. High-level Output Voltage vs High-level Output Current**

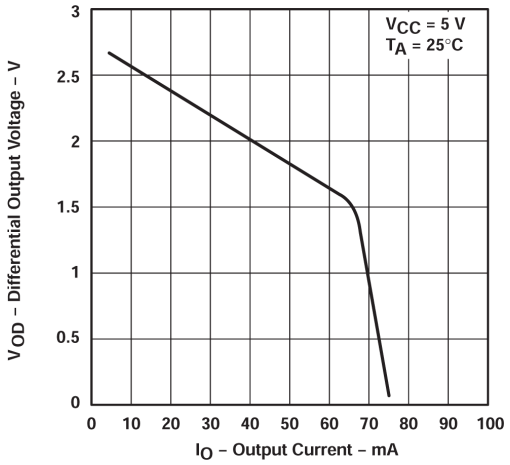



**Figure 5-5. Differential Output Voltage vs Output Current**

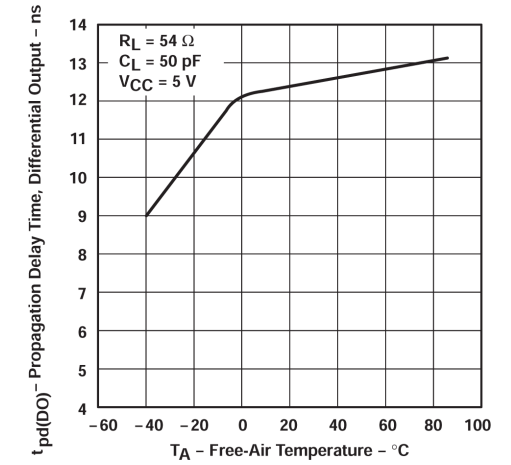



**Figure 5-6. Propagation Delay Time, Differential Output vs Free-air Temperature**

## 6 Parameter Measurement Information

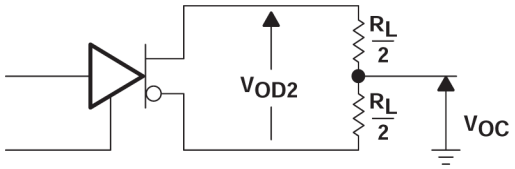
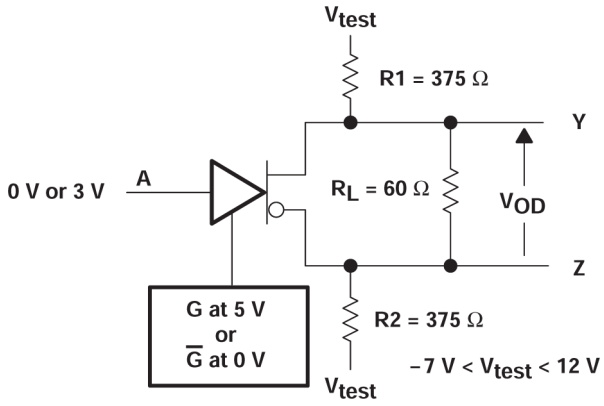


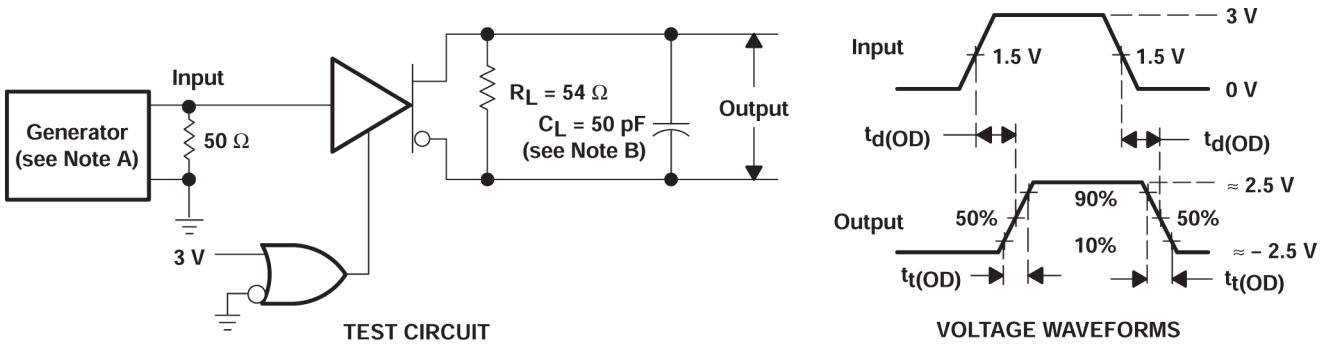

**Figure 6-1. Differential and Common-Mode Output Voltages**




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r$ ≤ 5 ns, $t_f$ ≤ 5 ns, $Z_O$ = 50 Ω.

B. $C_L$ includes probe and stray capacitance.

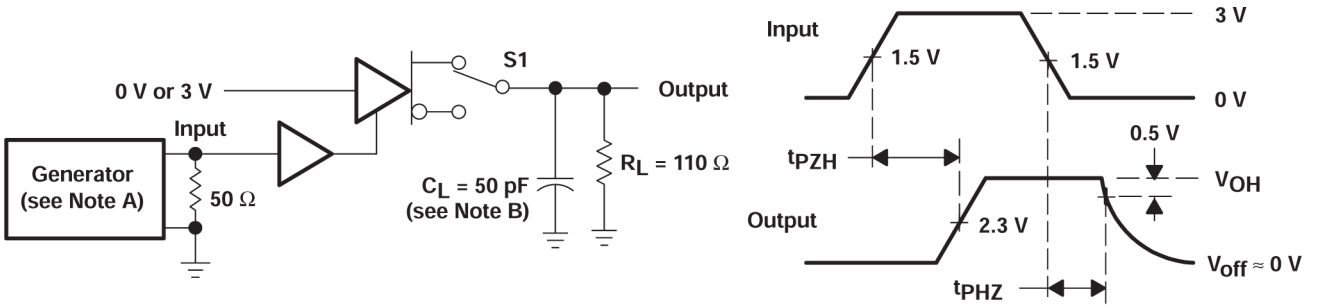
**Figure 6-2. Driver $V_{OD}$ Test Circuit**




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r$ ≤ 5 ns, $t_f$ ≤ 5 ns, $Z_O$ = 50 Ω.

B. $C_L$ includes probe and stray capacitance.

**Figure 6-3. Driver Differential-Output Test Circuit and Delay and Transition-Time Waveforms**

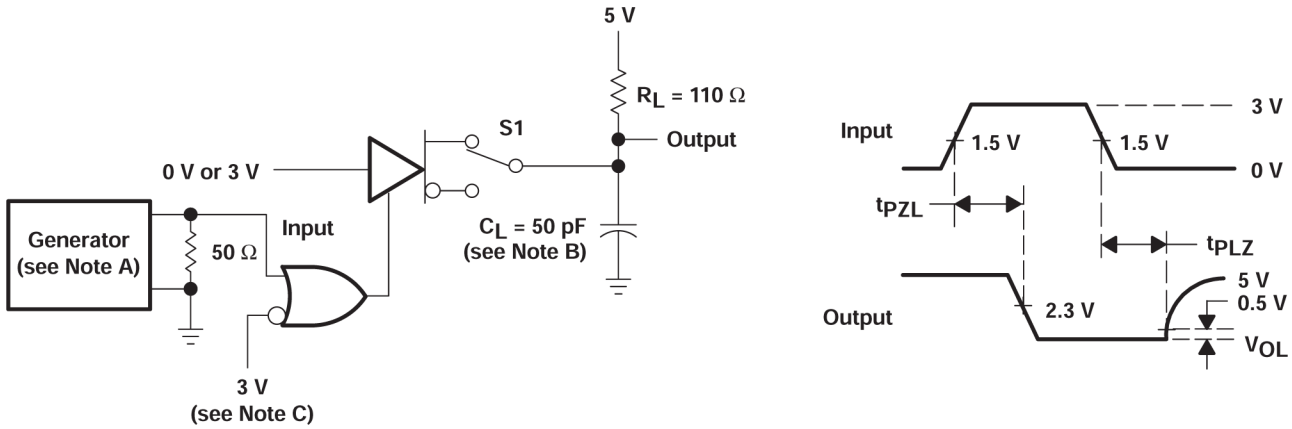



TEST CIRCUIT VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r$ ≤ 5 ns, $t_f$ ≤ 5 ns, $Z_O$ = 50 Ω.

B. $C_L$ includes probe and stray capacitance.

**Figure 6-4. $t_{PZH}$ and $t_{PHZ}$ Test Circuit and Voltage Waveforms**




TEST CIRCUIT VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r$ ≤ 5 ns, $t_f$ ≤ 5 ns, $Z_O$ = 50 Ω.

B. $C_L$ includes probe and stray capacitance

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

**Figure 6-5. $t_{PZL}$ and $t_{PLZ}$ Test Circuit and Waveforms**

# 7 Detailed Description

## 7.1 Thermal Characteristics of Ic Packages

$\Theta_{JA}$ (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

$\Theta_{JA}$ is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

$\Theta_{JA}$ can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. $\Theta_{JA}$ is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25mm long and 2 oz thick copper. The high-k board gives *best case* in−use condition and consists of two 1-oz buried power planes with a single trace layer 25mm long with 2-oz thick copper. A 4% to 50% difference in $\Theta_{JA}$ can be measured between these two test cards

$\Theta_{JC}$ (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

$\Theta_{JC}$ is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with $\Theta_{JB}$ in 1-dimensional thermal simulation of a package system.

$\Theta_{JB}$ (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold−plate structure. $\Theta_{JB}$ is only defined for the high-k test card.

$\Theta_{JB}$ provides an overall thermal resistance between the die and the PCB. Including a bit for the PCB thermal resistance (especially for BGAs with thermal balls), and can be used for simple 1-dimensional network analysis of package system (see Figure 7-1).

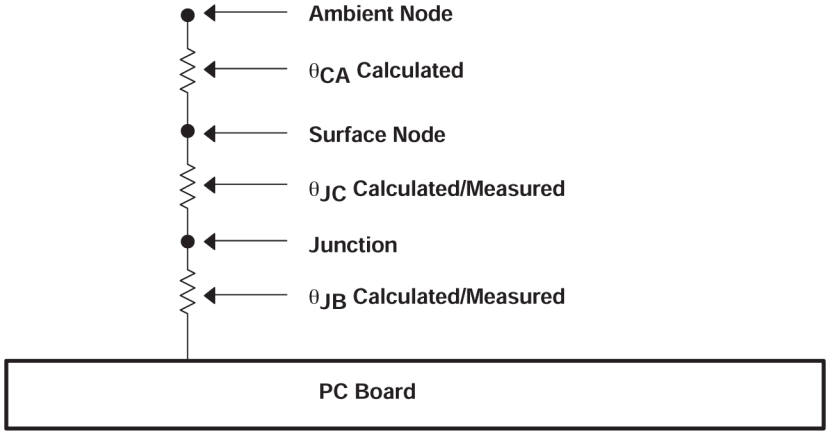



**Figure 7-1. Thermal Resistance**

## 7.2 Device Functional Modes

**Table 7-1. Function Table (Each Driver)**

| INPUT A | ENABLES(1) | | OUTPUTS | |
|---|---|---|---|---|
| | G | $\overline{G}$ | Y | Z |
| H | H | X | H | L |
| L | H | X | L | H |
| H | X | L | H | L |
| L | X | L | L | H |
| X | L | H | Z | Z |

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

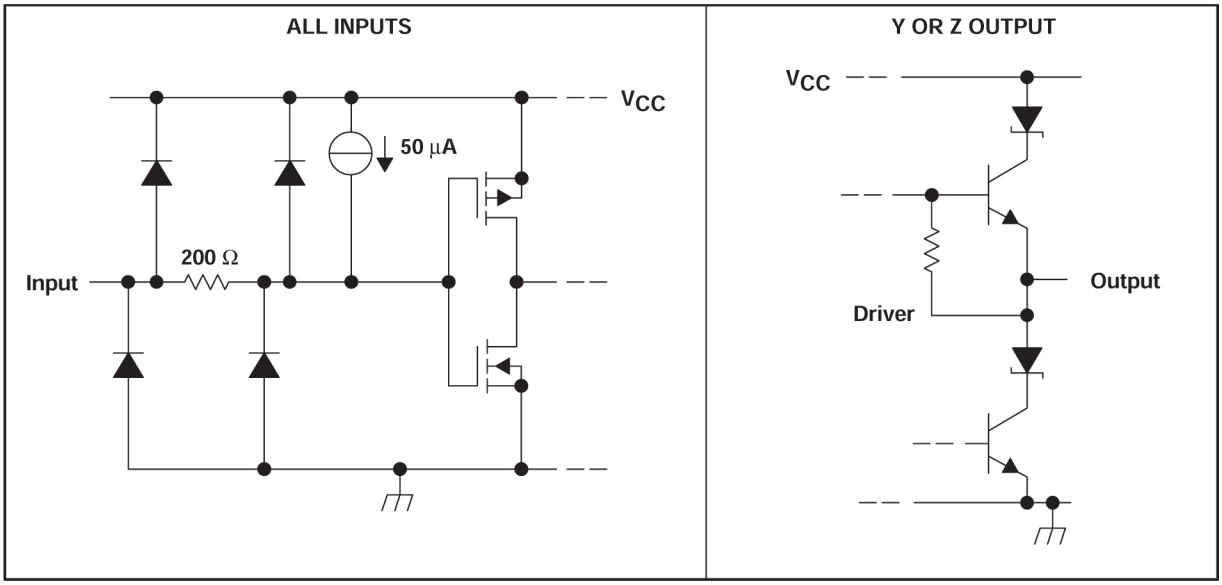



**Figure 7-2. Schematic Diagrams of Inputs and Outputs**

# 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.3 Trademarks

LinBiCMOS™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

## 8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.5 Glossary

| | |
|---|---|
| TI Glossary | This glossary lists and explains terms, acronyms, and definitions. |

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision E (April 2006) to Revision F (April 2024) | Page |
|---|---|
| • Changed the numbering format for tables, figures, and cross-references throughout the document | 1 |
| • Added the *Thermal Information* table | 6 |

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LBC172DW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SN65LBC172 | Samples |
| SN65LBC172N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN65LBC172N | Samples |
| SN75LBC172DW | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | 0 to 70 | SN75LBC172 | |
| SN75LBC172DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75LBC172 | Samples |
| SN75LBC172N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN75LBC172N | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN75LBC172 :**

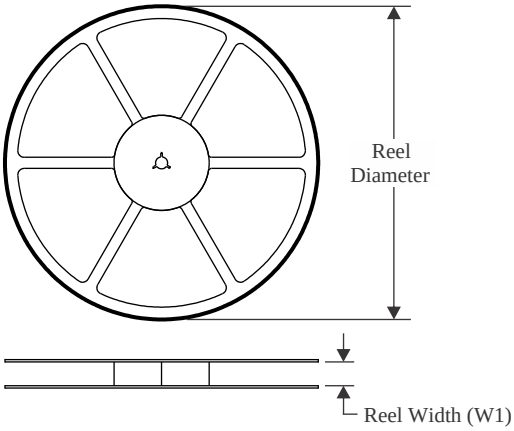
- Military : SN55LBC172

NOTE: Qualified Version Definitions:

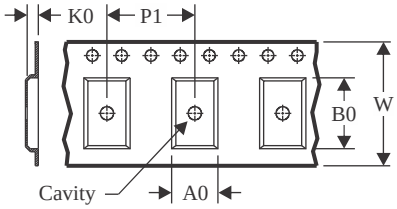
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

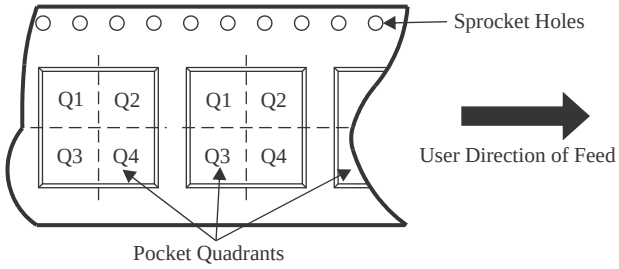



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

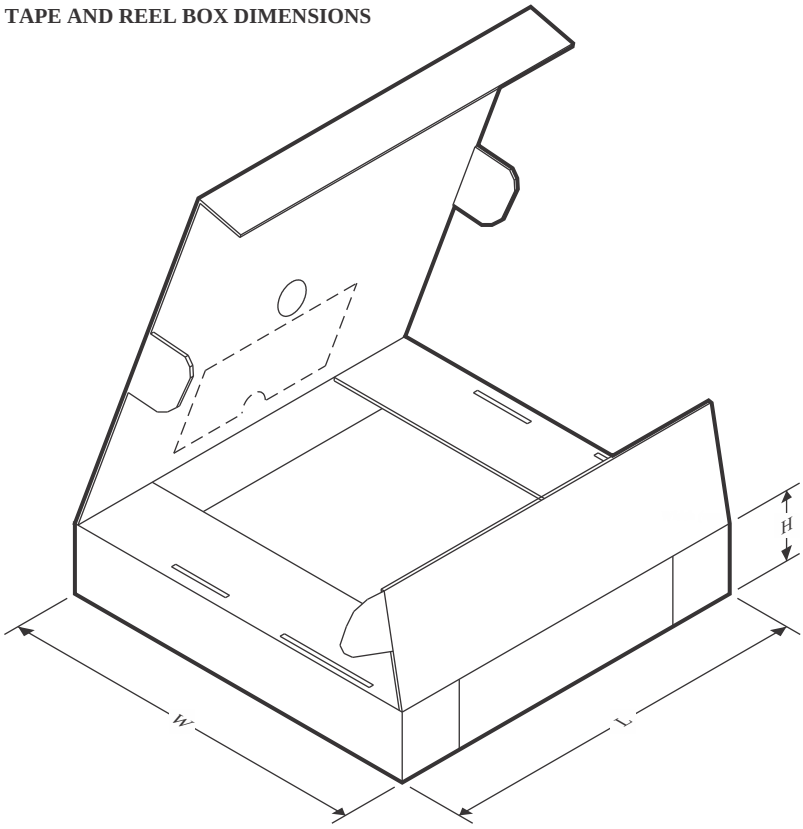
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN75LBC172DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN75LBC172DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

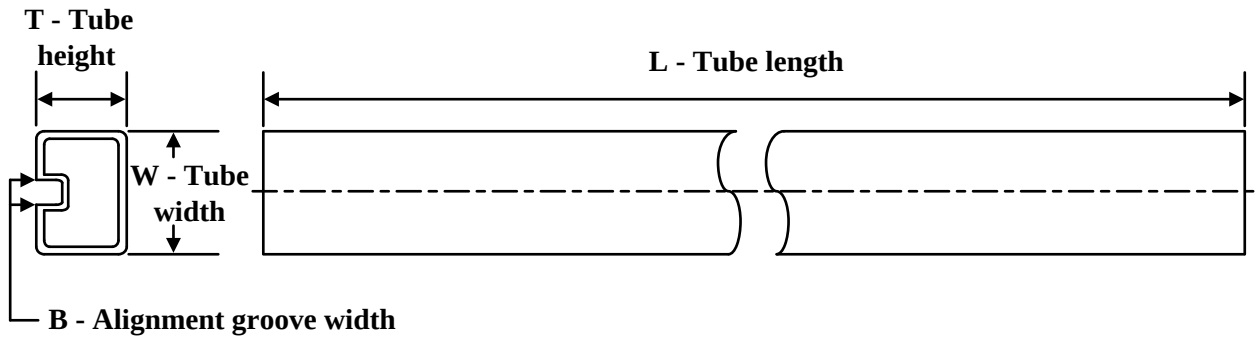
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN75LBC172DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN75LBC172DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |

## TUBE



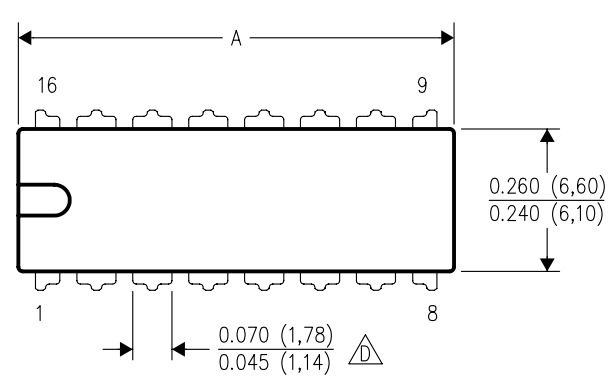

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN65LBC172DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN65LBC172DW | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN65LBC172N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN75LBC172N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

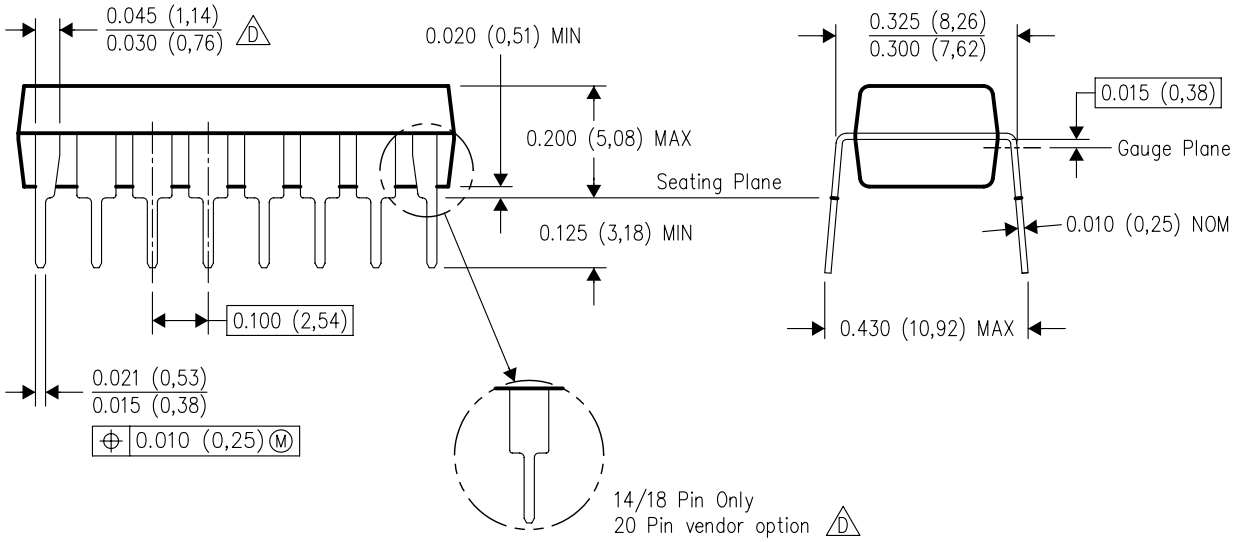
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

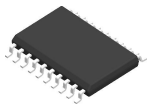



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

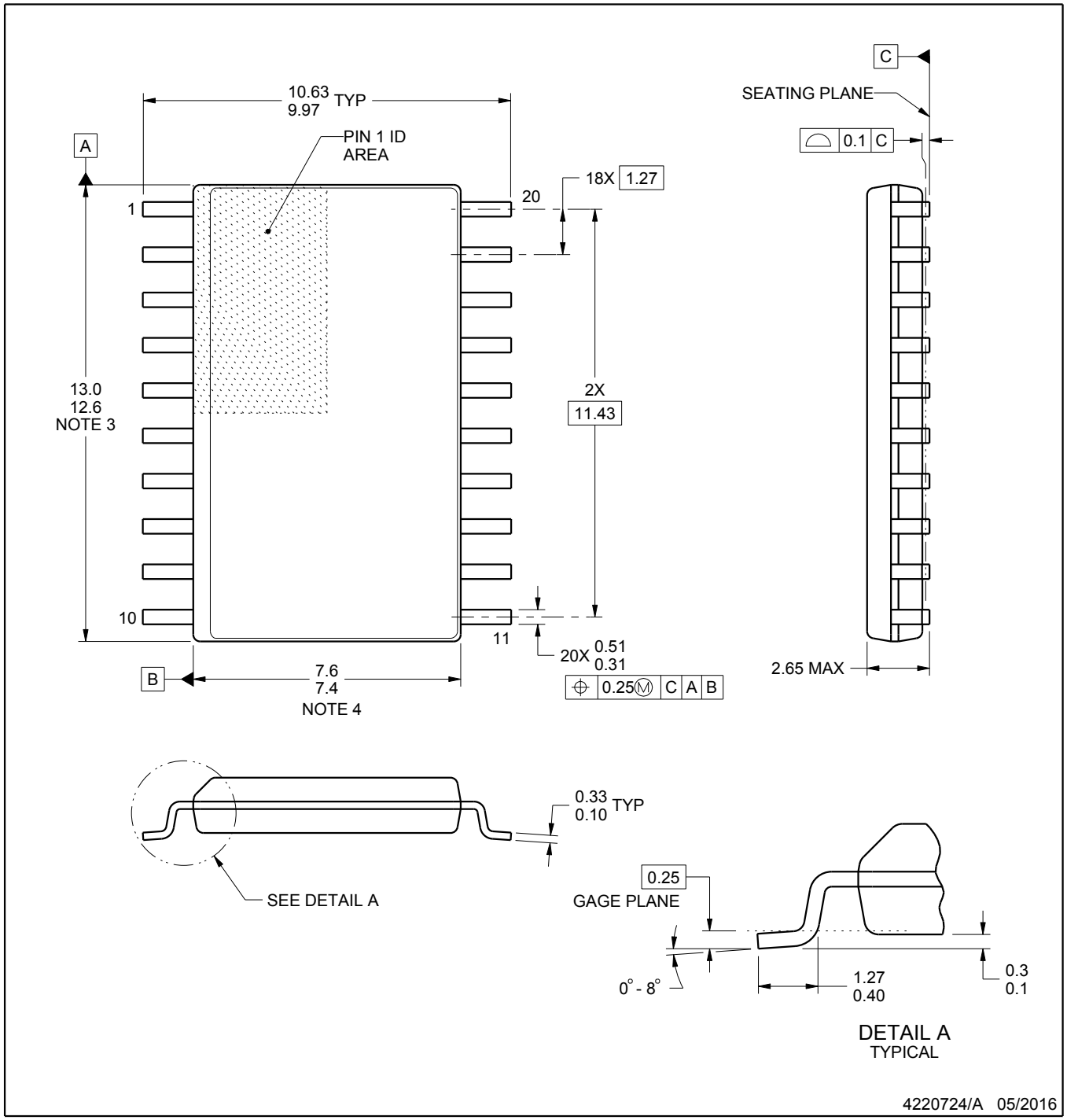


# PACKAGE OUTLINE

## DW0020A

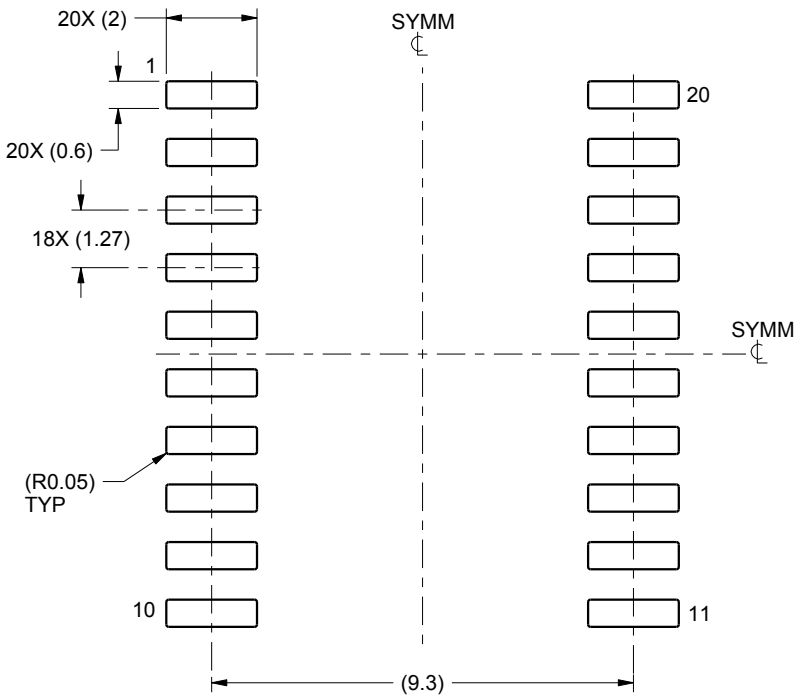
## SOIC - 2.65 mm max height

SOIC

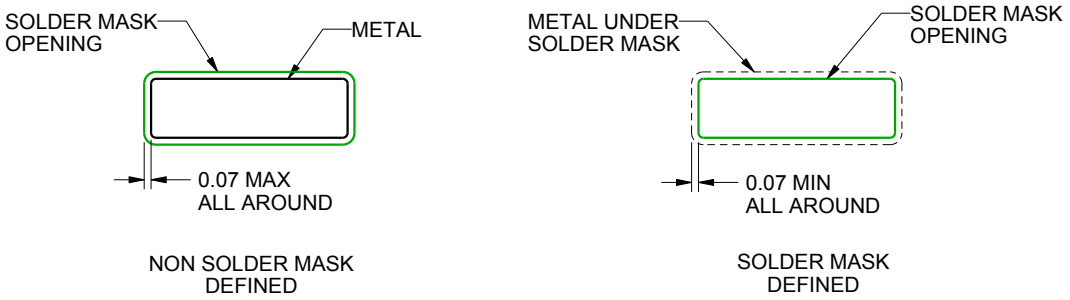



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

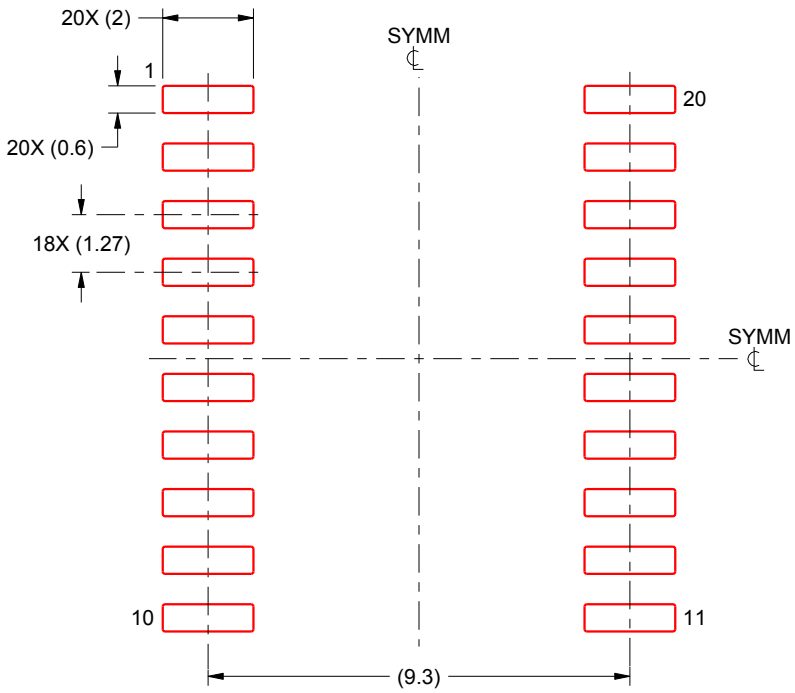



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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