

SN74AHC164-Q1 Automotive 8-Bit Parallel-Out Serial Shift Register

1 Features

- AEC-Q100 qualified for automotive applications:
 - Device temperature grade 1: -40°C to +125°C
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C4B
- Available in wettable flank QFN package
- Operating range 2V to 5.5V V_{CC}
- Low delay, 14ns max ($V_{CC} = 5V$, $C_L = 50pF$)
- Latch-up performance exceeds 250mA per JESD 17

2 Applications

- [Increase the number of outputs on a microcontroller](#)
- Store up to 8 bits of data temporarily

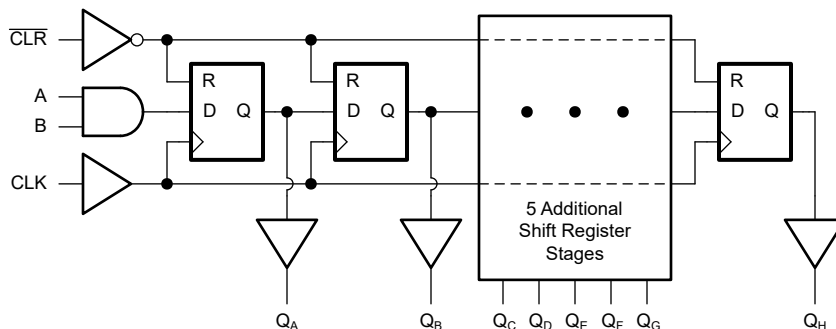
3 Description

The SN74AHC164-Q1 is an 8-bit shift register with AND-gated serial inputs and an asynchronous clear (\overline{CLR}) input. Outputs are directly connected to the internal shift register, resulting in immediate output changes as values are shifted into the register. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum set-up time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾	BODY SIZE (NOM) ⁽³⁾
SN74AHC164-Q1	BQA (WQFN, 14)	3mm × 2.5mm	3mm × 2.5mm
	PW (TSSOP, 14)	6.4mm × 5mm	5mm × 4.4mm

- (1) For more information, see [Section 11](#).
- (2) The package size (length × width) is a nominal value and includes pins, where applicable
- (3) The body size (length × width) is a nominal value and does not include pins.



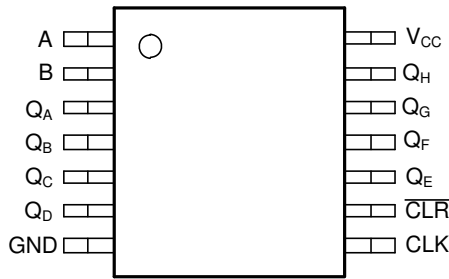
Logic Diagram (Positive Logic)



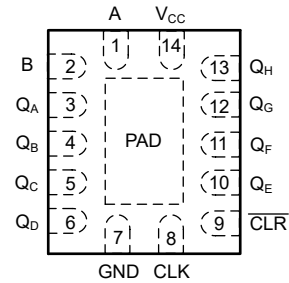
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4 Pin Configuration and Functions



**Figure 4-1. PW Package,
16-Pin TSSOP
(Top View)**



**Figure 4-2. BQA Package
16-Pin WQFN
(Top View)**

Table 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
A	1	I	Gated serial input A
B	2	I	Gated serial input B
Q _A	3	O	Parallel output A
Q _B	4	O	Parallel output B
Q _C	5	O	Parallel output C
Q _D	6	O	Parallel output D
GND	7	G	Ground
CLK	8	I	Clock input, rising edge triggered
CLR	9	I	Asynchronous register clear input, active low
Q _E	10	O	Parallel output E
Q _F	11	O	Parallel output F
Q _G	12	O	Parallel output G
Q _H	13	O	Parallel output H
V _{CC}	14	P	Positive supply
Thermal pad ⁽²⁾		—	The thermal pad can be connect to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, P = Power, G = Ground.

(2) BQA package only.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I	Input voltage range ⁽²⁾	-0.5	7	V
V _O	Output voltage range ⁽²⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < -0.5V	-20	mA
I _{OK}	Output clamp current	V _O < -0.5V or V _O > V _{CC} + 0.5V	±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±25	mA
	Continuous output current through V _{CC} or GND		±75	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 HBM ESD Classification Level 2 ⁽¹⁾	±2000
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
V _{CC}	Supply voltage		2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2V	1.5		V
		V _{CC} = 3V	2.1		
		V _{CC} = 5.5V	3.85		
V _{IL}	Low-Level input voltage	V _{CC} = 2V		0.5	V
		V _{CC} = 3V		0.9	
		V _{CC} = 5.5V		1.65	
V _I	Input Voltage		0	5.5	V
V _O	Output Voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2V		-50	μA
		V _{CC} = 3.3V ± 0.3V		-4	mA
		V _{CC} = 5V ± 0.5V		-8	mA
I _{OL}	Low-level output current	V _{CC} = 2V		50	μA
		V _{CC} = 3.3V ± 0.3V		4	mA
		V _{CC} = 5V ± 0.5V		8	mA
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3V ± 0.3V		100	ns/V
		V _{CC} = 5V ± 0.5V		20	ns/V

5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

Specification	Description	Condition	MIN	MAX	UNIT
T _A	Operating free-air temperature		-40	125	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		BQA (WQFN)	PW (TSSOP)	UNIT
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	93.4	138.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	96.4	67.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	62.8	94.8	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	12.5	10.6	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	62.5	93.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	39.7	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50μA	2V to 5.5V	V _{CC} -0.1	V _{CC}		V _{CC} -0.1	V _{CC}	V	
	I _{OH} = -4mA	3V	2.58			2.48			
	I _{OH} = -8mA	4.5V	3.94			3.8			
V _{OL}	I _{OL} = 50μA	2V to 5.5V			0.1			0.1	
	I _{OL} = 4mA	3V			0.36			0.44	
	I _{OL} = 8mA	4.5V			0.36			0.44	
I _I	V _I = 5.5V or GND and V _{CC} = 0V to 5.5V	0V to 5.5V			±0.1			±1	
I _{CC}	V _I = V _{CC} or GND, I _O = 0, and V _{CC} = 5.5V	5.5V			4			40	
C _I	V _I = V _{CC} or GND	5V		2	10			10	
C _{PD}	No load, F = 1MHz	5V		106				pF	

5.6 Timing Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V _{CC}	T _A = 25°C		-40°C to 85°C		-40°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t _{SU}	Setup time	CL _R high	3.3V ± 0.3V	2.5		2.5		2.5		ns
t _{SU}	Setup time	Data before CLK↑	3.3V ± 0.3V	5		6		6		ns
t _H	Hold time	Data after CLK↑	3.3V ± 0.3V	0		0		0		ns
t _W	Pulse duration	CLK high or low	3.3V ± 0.3V	5		5		5		ns
t _W	Pulse duration	CL _R low	3.3V ± 0.3V	5		5		5		ns
t _{SU}	Setup time	CL _R high	5V ± 0.5V	2.5		2.5		2.5		ns
t _{SU}	Setup time	Data before CLK↑	5V ± 0.5V	4.5		4.5		4.5		ns
t _H	Hold time	Data after CLK↑	5V ± 0.5V	0.5		0.5		0.5		ns

5.6 Timing Characteristics (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	CONDITION	V _{CC}	T _A = 25°C		-40°C to 85°C		-40°C to 125°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t _W	Pulse duration	CLK high or low	5V ± 0.5V	5		5		5		ns
t _W	Pulse duration	$\overline{\text{CLR}}$ low	5V ± 0.5V	5		5		5		ns

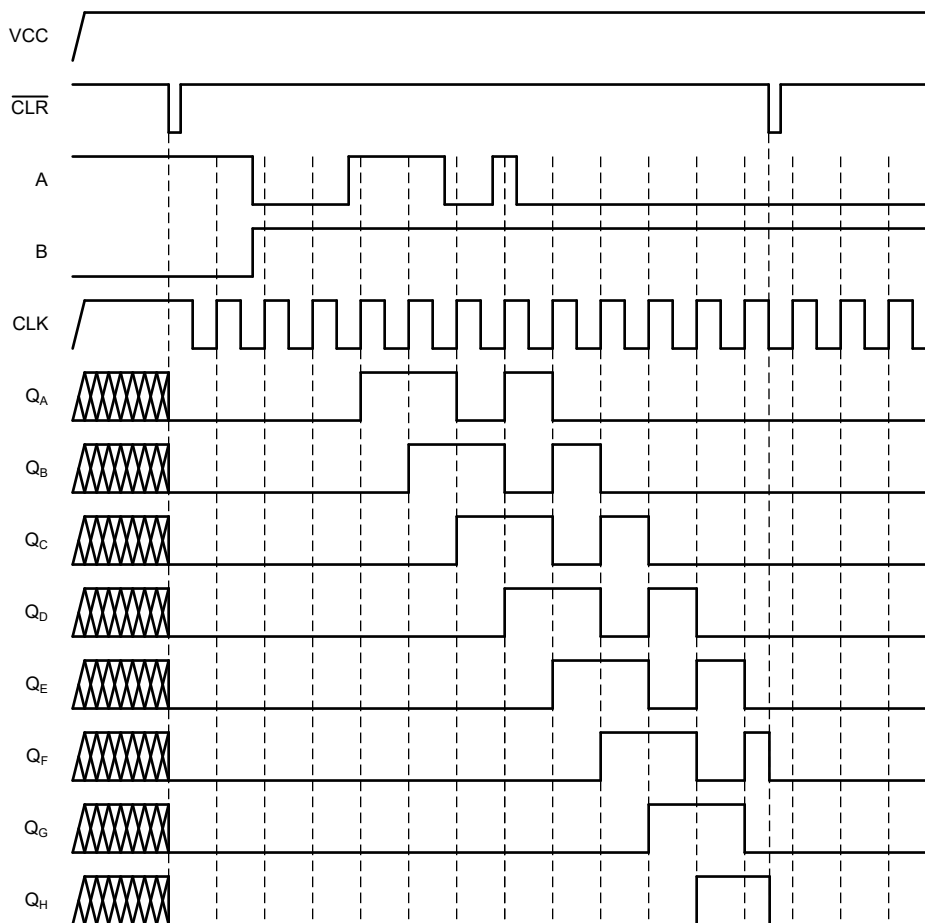


Figure 5-1. Timing Diagram

5.7 Switching Characteristics

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
					MIN	TYP	MA X	MIN	TYP	MA X	MIN	TYP	MA X	
F _{max}	-	-	C _L = 15pF	3.3V ± 0.3V	95	170		80	0	70			MHz	
				5V ± 0.5V	135	240		115		115			MHz	
			C _L = 50pF	3.3V ± 0.3V	55	130		50		50			MHz	
				5V ± 0.5V	120	180		95		95			MHz	
t _{PLH}	CLK	Q	C _L = 15pF	3.3V ± 0.3V	5.8	11	1	13	1	16	ns			
t _{PHL}	CLK	Q	C _L = 15pF	3.3V ± 0.3V	5.8	11	1	13	1	16	ns			
t _{PHL}	$\overline{\text{CLR}}$	Q	C _L = 15pF	3.3V ± 0.3V	4.5	11.4	1	13.5	1	16	ns			

5.7 Switching Characteristics (continued)

over operating free-air temperature range(unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{CC}	T _A = 25°C			-40°C to 85°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t _{PLH}	CLK	Q	C _L = 50pF	3.3V ± 0.3V	7.5	14.5		1	16.5	1	20.5		ns	
t _{PHL}	CLK	Q	C _L = 50pF	3.3V ± 0.3V	7.5	14.5		1	16.5	1	20.5		ns	
t _{PHL}	CLR	Q	C _L = 50pF	3.3V ± 0.3V	6	14.9		1	17	1	20.5		ns	
t _{PLH}	CLK	Q	C _L = 15pF	5V ± 0.5V	4.5	9		1	10.5	1	11.5		ns	
t _{PHL}	CLK	Q	C _L = 15pF	5V ± 0.5V	4.5	9		1	10.5	1	11.5		ns	
t _{PHL}	CLR	Q	C _L = 15pF	5V ± 0.5V	3	7.6		1	9	1	11		ns	
t _{PLH}	CLK	Q	C _L = 50pF	5V ± 0.5V	6.4	11		1	12.5	1	14		ns	
t _{PHL}	CLK	Q	C _L = 50pF	5V ± 0.5V	6.4	11		1	12.5	1	14		ns	
t _{PHL}	CLR	Q	C _L = 50pF	5V ± 0.5V	4.2	9.6		1	11	1	13.5		ns	

5.8 Noise Characteristics

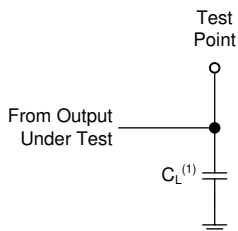
V_{CC} = 5V, C_L = 50pF, T_A = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
V _{OL(P)}	Quiet output, maximum dynamic V _{OL}		0.2	0.8	V
V _{OL(V)}	Quiet output, minimum dynamic V _{OL}	-0.9	-0.2		V
V _{OH(V)}	Quiet output, minimum dynamic V _{OH}	4.4	4.7		V
V _{IH(D)}	High-level dynamic input voltage	3.5			V
V _{IL(D)}	Low-level dynamic input voltage			1.5	V

6 Parameter Measurement Information

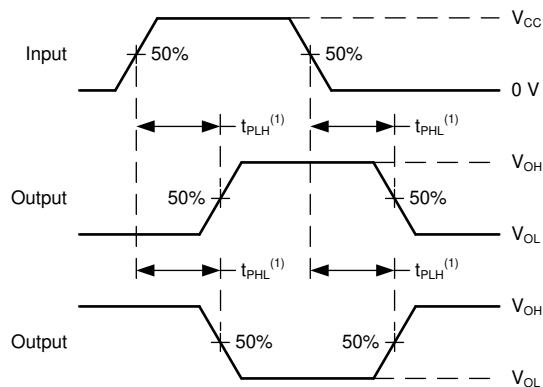
Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR \leq 1MHz, $Z_O = 50\Omega$, $t_t < 2.5$ ns.

The outputs are measured individually with one input transition per measurement.



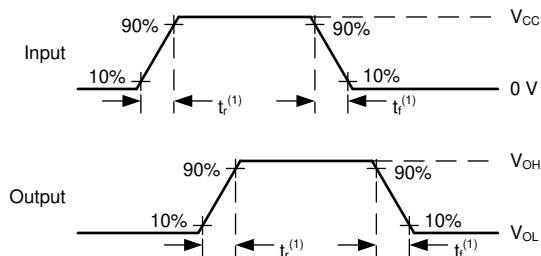
(1) C_L includes probe and test-fixture capacitance.

Figure 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{pLH} and t_{pHL} is the same as t_{pd} .

Figure 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

Figure 6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74AHC164-Q1 is an 8-bit shift register with 2 serial inputs (A and B) connected through an AND gate, as well as an asynchronous clear ($\overline{\text{CLR}}$). The device requires a high signal on both A and B to set the input data line high; a low signal on either input will set the input data line low. Data at A and B can be changed while CLK is high or low, provided that the minimum set-up time requirements are met.

The CLK pin of the SN74AHC164-Q1 is rising-edge triggered, activating on the transition from LOW to HIGH. Upon a positive-edge trigger, the device will store the result of the ($A \bullet B$) input data line in the first register and propagate each register's data to the next register. The data of the last register, Q_H , will be discarded at each clock trigger. If a low signal is applied to the $\overline{\text{CLR}}$ pin, then the SN74AHC164-Q1 will set all registers to a logical low value immediately.

7.2 Functional Block Diagram

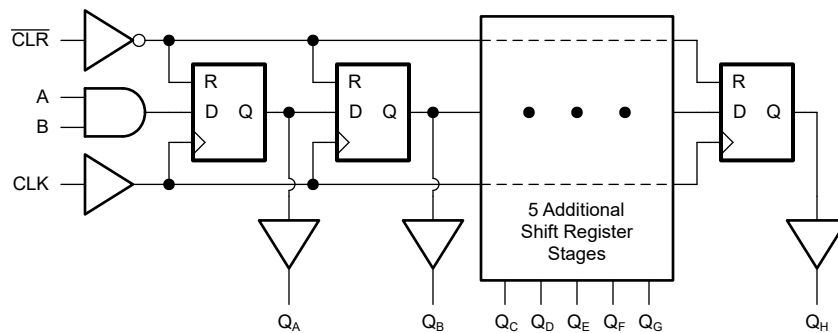


Figure 7-1. Logic Diagram (Positive Logic) for SN74AHC164-Q1

7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

7.3.2 Latching Logic

This device includes latching logic circuitry. Latching circuits commonly include D-type latches and D-type flip-flops, but include all logic circuits that act as volatile memory.

When the device is powered on, the state of each latch is unknown. There is no default state for each latch at start-up.

The output state of each latching logic circuit only remains stable as long as power is applied to the device within the supply voltage range specified in the *Recommended Operating Conditions* table.

7.3.3 Standard CMOS Inputs

This device includes standard CMOS inputs. Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

Standard CMOS inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in [Implications of Slow or Floating CMOS Inputs](#).

Do not leave standard CMOS inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; a 10k Ω resistor, however, is recommended and will typically meet all requirements.

7.3.4 Wettable Flanks

This device includes wettable flanks for at least one package. See the *Features* section on the front page of the data sheet for which packages include this feature.

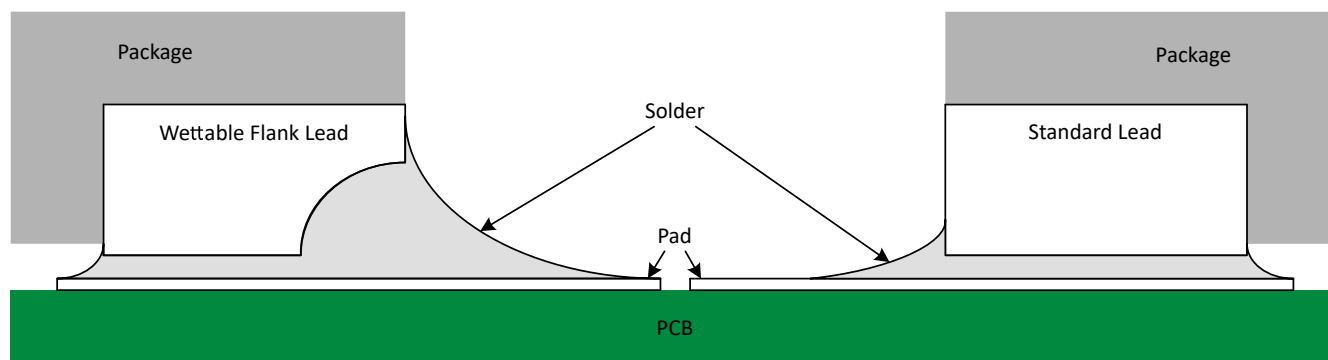


Figure 7-2. Simplified Cutaway View of Wettable-Flank QFN Package and Standard QFN Package After Soldering

Wettable flanks help improve side wetting after soldering, which makes QFN packages easier to inspect with automatic optical inspection (AOI). As shown in [Figure 7-2](#), a wettable flank can be dimpled or step-cut to provide additional surface area for solder adhesion which assists in reliably creating a side fillet. See the mechanical drawing for additional details.

7.3.5 Clamp Diode Structure

As [Figure 7-3](#) shows, the outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

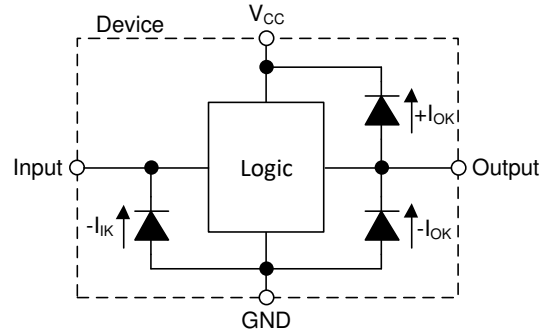


Figure 7-3. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

Table 7-1 lists the functional modes of the SN74AHC164-Q1 .

Table 7-1. Function Table

INPUTS ⁽¹⁾				FUNCTION
A	B	$\overline{\text{CLR}}$	CLK	
X	X	L	X	Shift register is cleared.
L	X	H	↑	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
X	L	H	↑	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	H	H	↑	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.

(1) H = High Voltage Level, L = Low Voltage Level, X = Do Not Care

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, the SN74AHC164-Q1 is used to control seven-segment displays. Unlike other I/O expanders, the SN74AHC164-Q1 does not need a communication interface for control. It can easily operate with simple GPIO pins. Additional control is provided with two serial inputs that feed into an AND gate.

At power-up, the initial state of the shift registers is unknown. To give them a defined state, the shift register needs to be cleared. An RC can be connected to the $\overline{\text{CLR}}$ pin as shown in Figure 8-1 to initialize the shift register to all zeros.

8.2 Typical Application

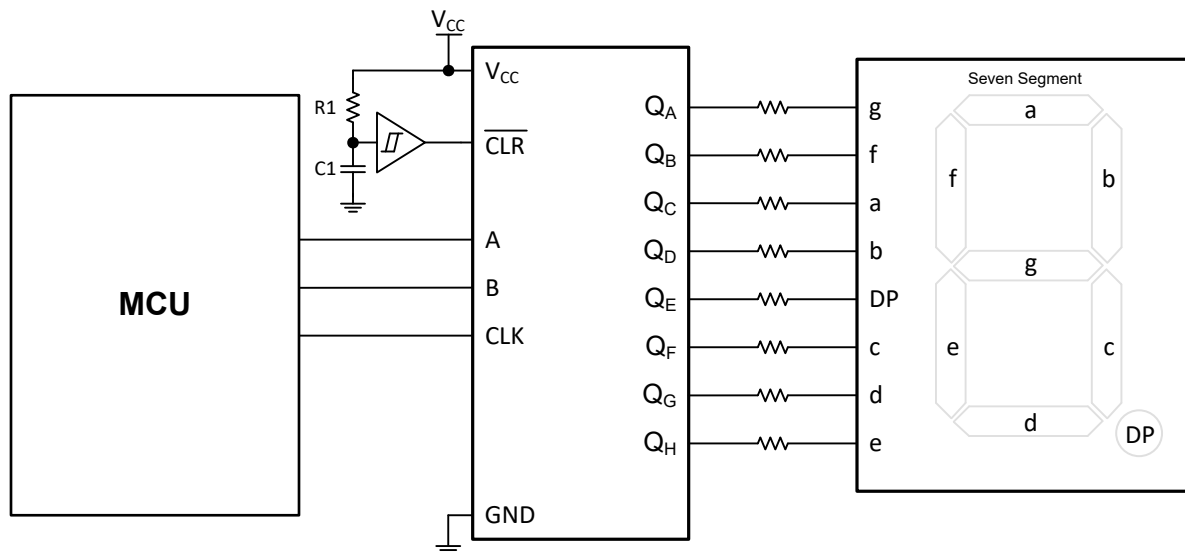


Figure 8-1. Typical Application Block Diagram

8.3 Design Requirements

8.3.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74AHC164-Q1 plus the maximum static supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Ensure the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings* is not exceeded.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74AHC164-Q1 plus the maximum supply current, I_{CC} , listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its

ground connection. Ensure the maximum total current through GND listed in the *Absolute Maximum Ratings* is not exceeded.

The SN74AHC164-Q1 can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74AHC164-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.3.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74AHC164-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10k Ω resistor value is often used due to these factors.

The SN74AHC164-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.3.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.4 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is $\leq 50\text{pF}$. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74AHC164-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)})\Omega$. Doing this will prevent the maximum output current from the *Absolute Maximum Ratings* from being violated. Most CMOS inputs have a resistive load measured in $M\Omega$; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

8.5 Application Curve

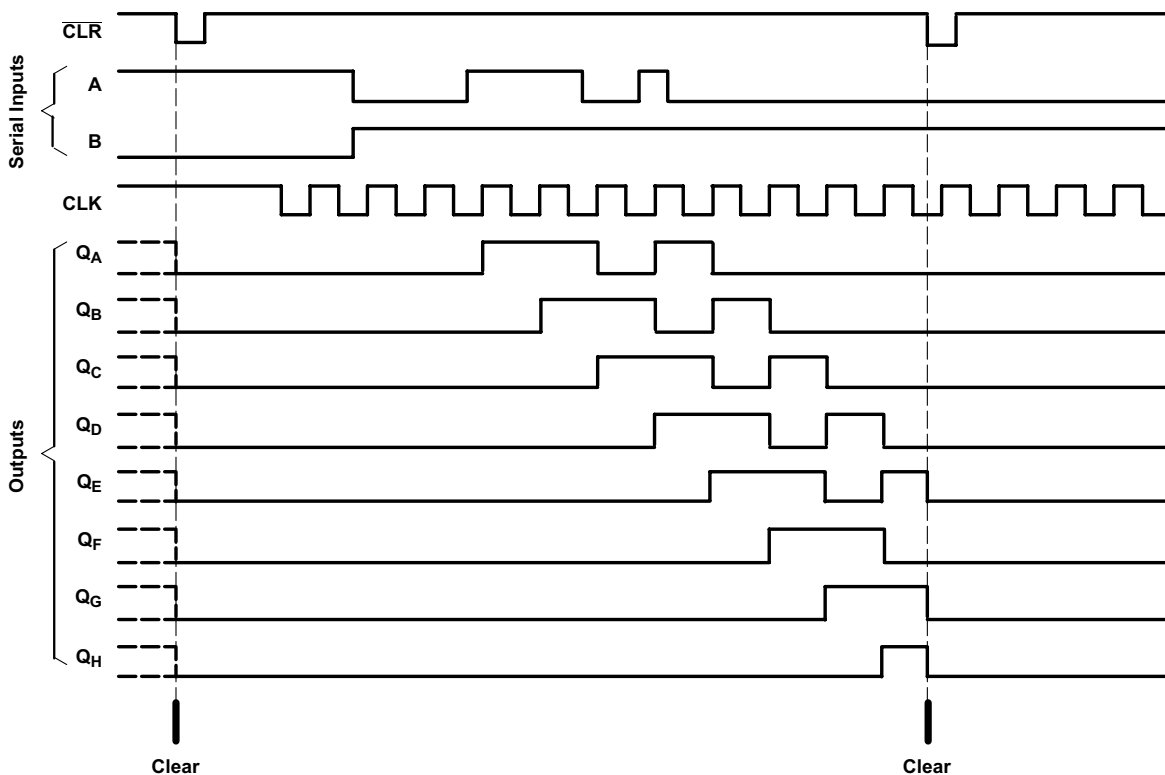


Figure 8-2. Application Timing Diagram

8.6 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A $0.1\mu\text{F}$ capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.7 Layout

8.7.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.7.2 Layout Example

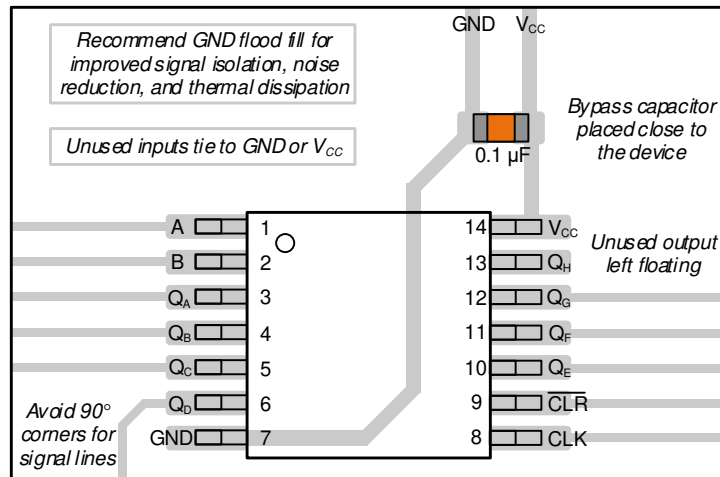


Figure 8-3. Example Layout for the SN74AHC164-Q1

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

DATE	REVISION	NOTES
February 2024	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC164QPWRQ1	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC164Q	Samples
SN74AHC164QWBQARQ1	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AH164Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHC164-Q1 :

- Catalog : [SN74AHC164](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC164QPWRQ1	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC164QWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC164QPWRQ1	TSSOP	PW	14	3000	353.0	353.0	32.0
SN74AHC164QWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

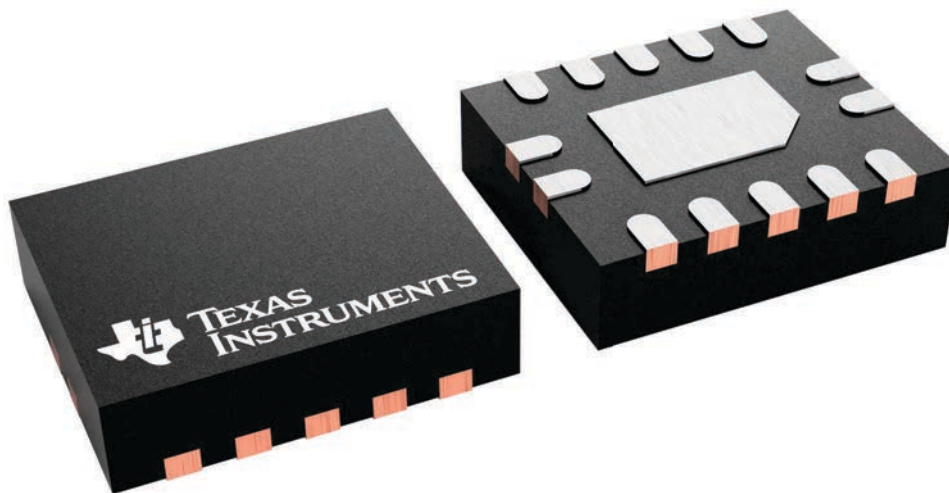
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

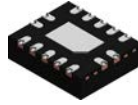
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A

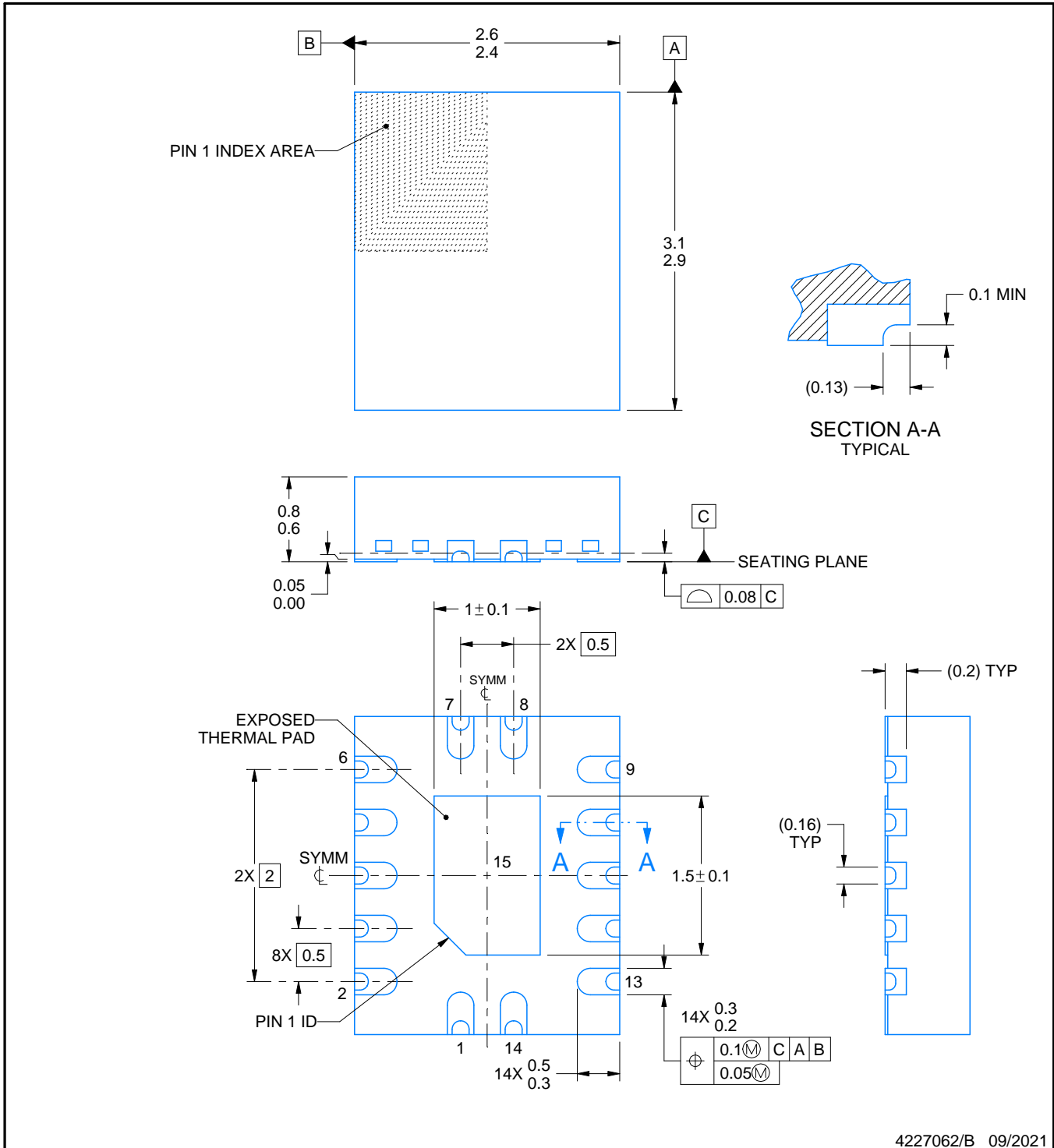
BQA0014B



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

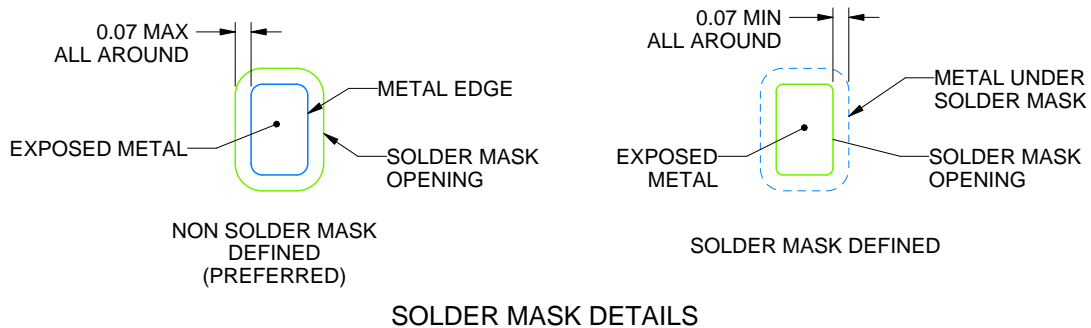
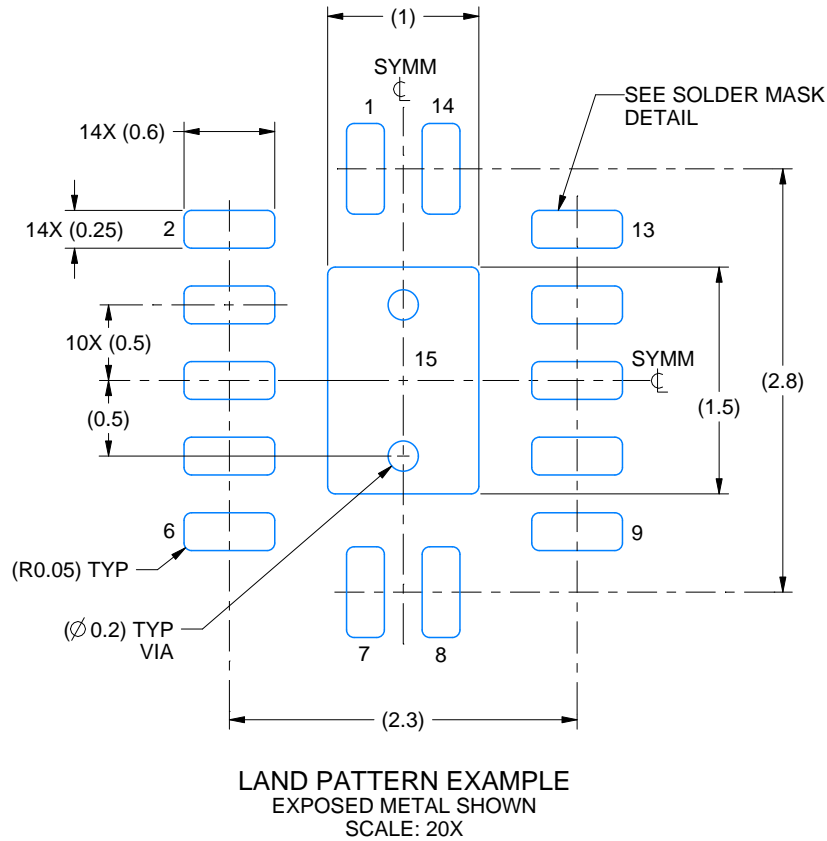
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4227062/B 09/2021

NOTES: (continued)

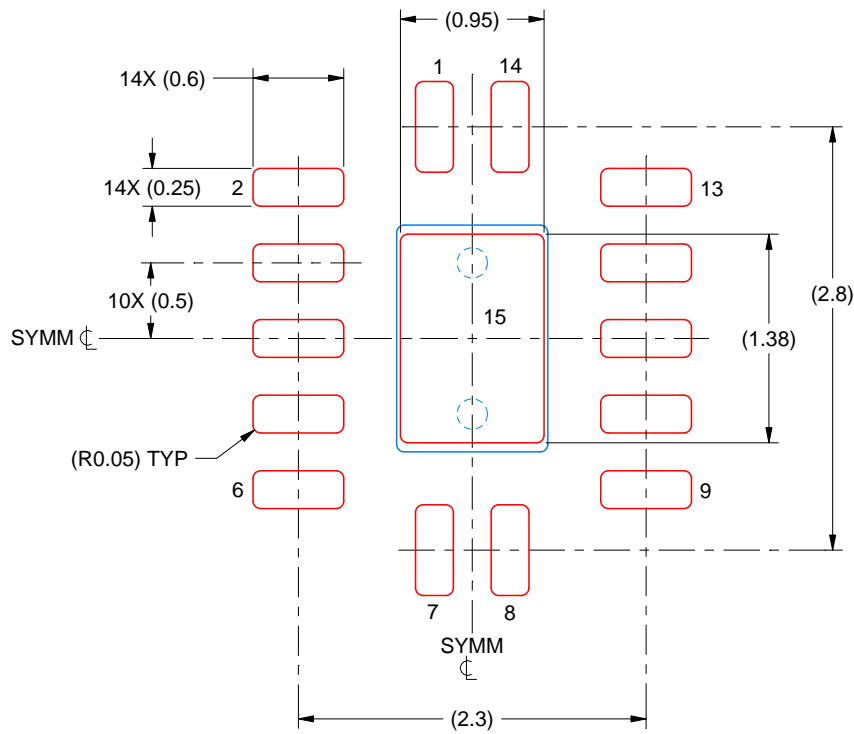
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4227062/B 09/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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